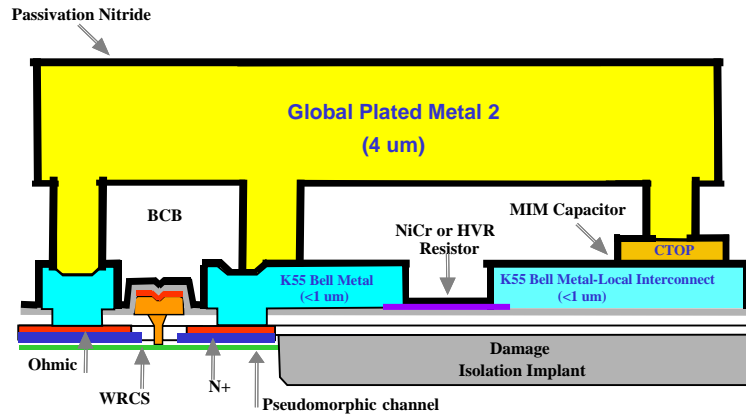


Process Cross Section Diagram

Updated Process Diagram



Features

- D-Mode, -1.0 V Vp
- InGaAs Active Layer pHEMT Process
- 0.15 μm Low Cost Optical Lithography Gates
- High Density Interconnects:
 - 1 Global
 - 1 Local
- High-Q Passives
- Thin Film Resistors
- High Value Capacitors (620 pF/mm²)
- Backside Vias Optional
- Based on Production TQP13 Processes

Process Description

TriQuint's TQP15 process is based on our production-released TQP13 processes. TQP15 is a breakthrough technology offering both high breakdown voltage and high frequency/ gain capability all within an optical process technology that enables commercialization of mmw markets. TQP15 is targeted at the emergent Ka-band segment and is ideal for the VSAT, satellite communications, and point-to-point radio markets. The two metal interconnecting layers are encapsulated in a high performance dielectric that allows wiring flexibility, optimized die size and plastic packaging simplicity. Precision NiCr resistors and high value MIM capacitors are included allowing higher levels of integration, while maintaining smaller, cost-effective die sizes.

Applications

- Medium Power, D-Mode Applications
- Point-to-Point Radio
- Converters
- VSAT
- Ka-band Power Amplifiers

Process Details

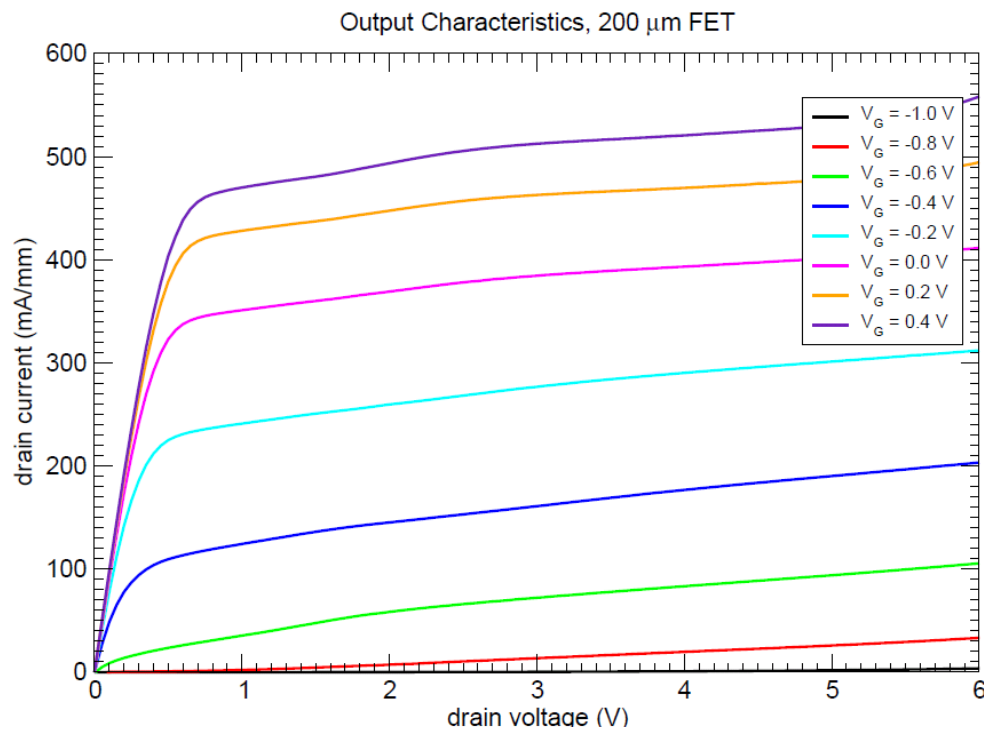
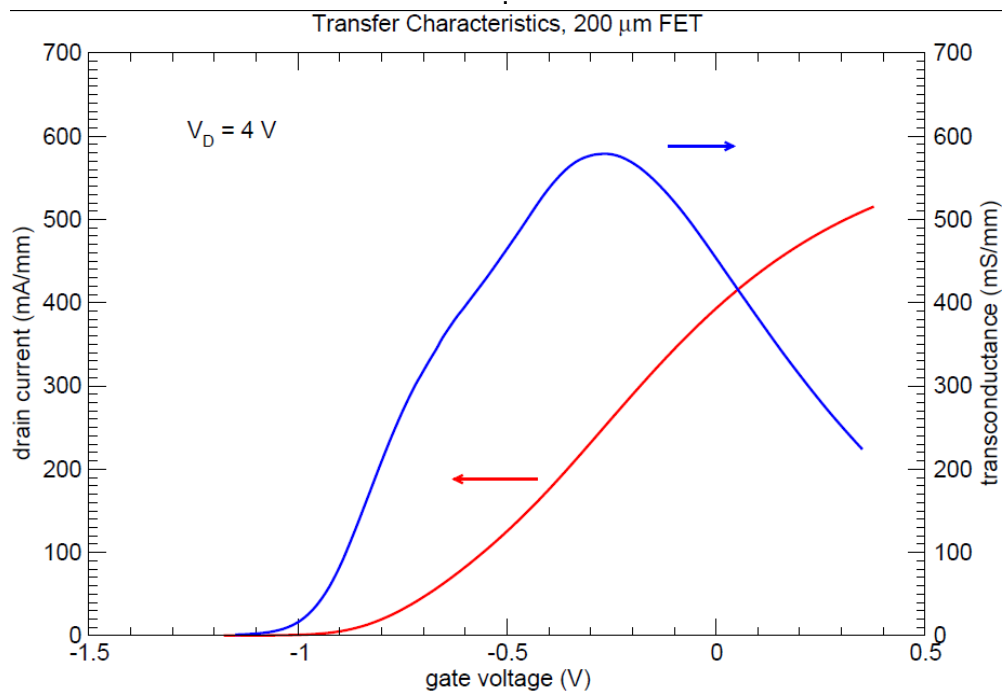
Absolute Maximum Ratings

Storage Temperature Range	-65 to +150	Deg C
Operating Temperature Range	-55 to +150	Deg C
Capacitor	40	V

Process Details

Transistor Details @ Vds = 3.0V			
Element	Parameter	Typical	Units
D-Mode pHEMT	Vp (1uA/ μm)	-1.0	V
	Idss	380	mA/mm
	Imax	580	mA/mm
	Breakdown, Vdg	14	V
	Ft (peak)	80	GHz
	Gm @ Idss	550	mS/mm
Common Process Element Details			
Gate Length	D-Mode	0.15	μm
Interconnect		2	Metal Layers
MIM Caps	Value	620	pF/mm ²
Resistors	NiCr	50	Ohms/sq
	Bulk	120	Ohms/sq

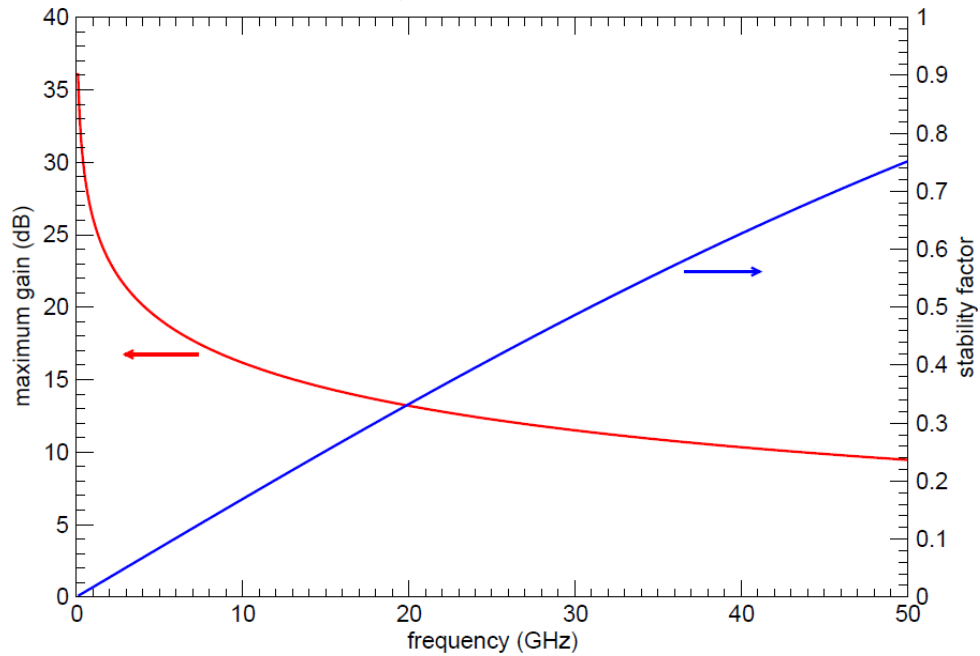
Performance Details



Unless otherwise noted; models and graphs in this process data sheet are for devices on a full thickness substrate.

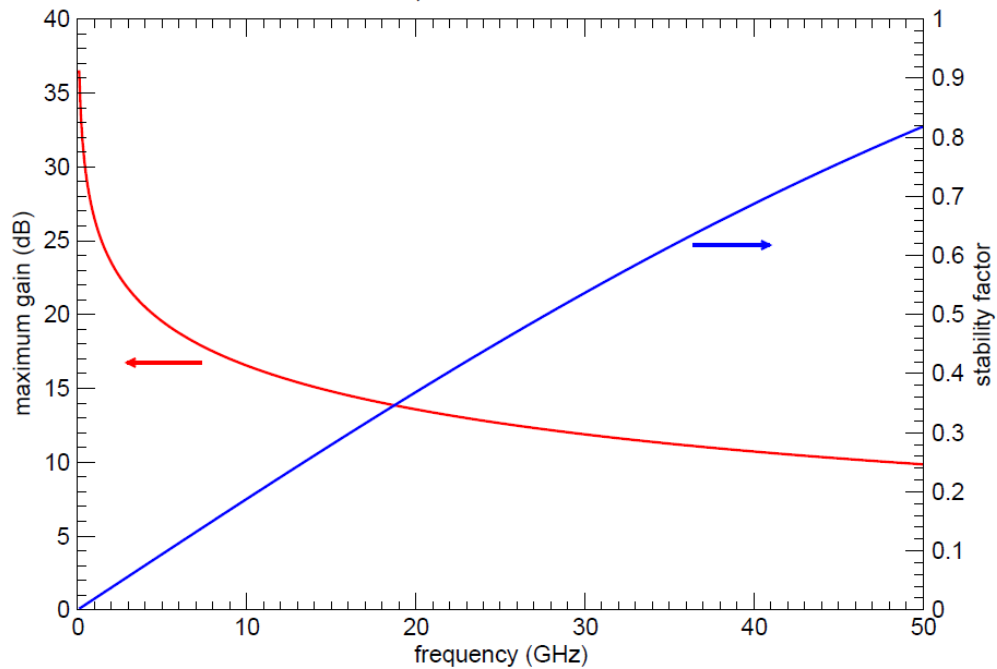
Maximum Available Gain/Stable Gain (MAG/MSG)

200 μm FET: 3 V, 22.8 mA

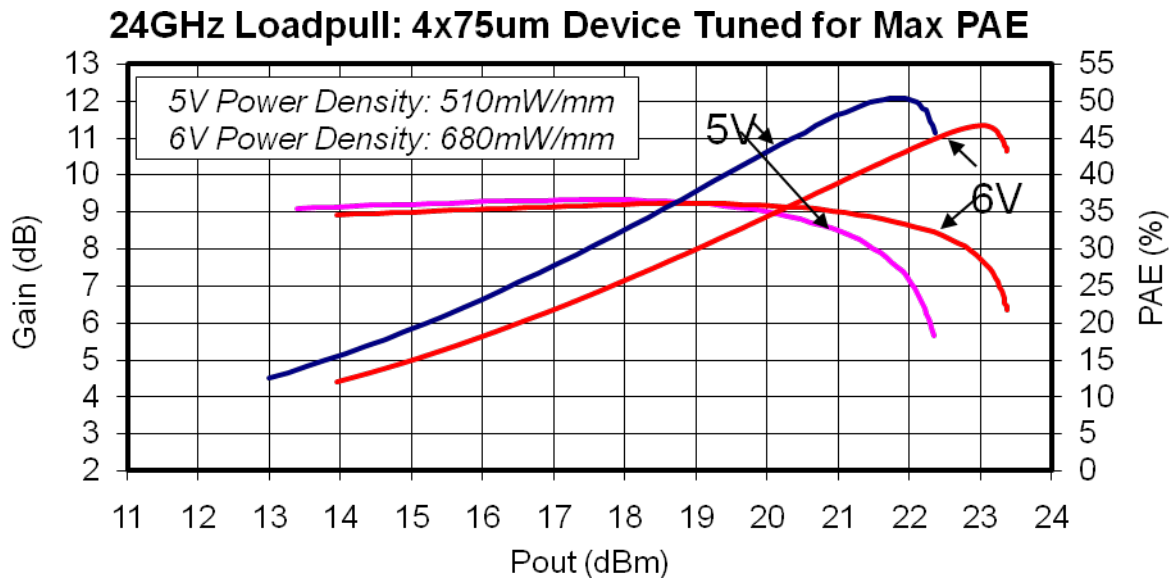


Maximum Available Gain/Stable Gain (MAG/MSG)

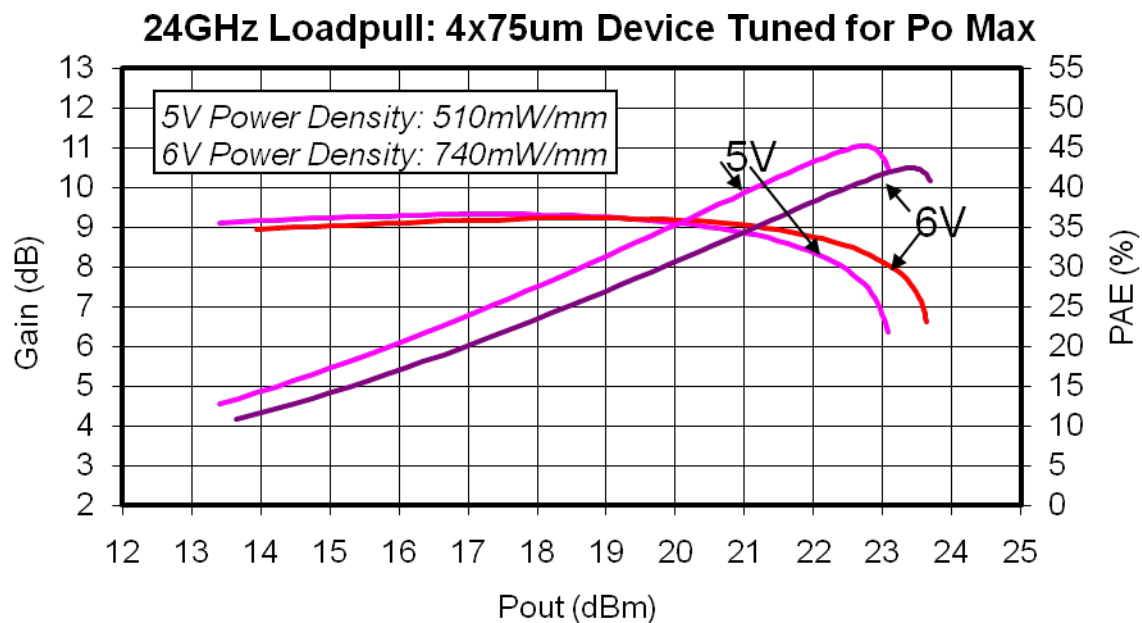
200 μm FET: 6 V, 38 mA



Unless otherwise noted; models and graphs in this process data sheet are for devices on a full thickness substrate.



Devices used on a 100- μ m thick substrate.



Devices used on a 100- μ m thick substrate.

Prototyping and Development

- Prototype Development Quick Turn (PDQ):
 - Shared mask set
 - Hot Lot cycle time
- Prototype Wafer Option (PWO):
 - Customer-specific masks; Customer schedule
 - 2 wafers delivered
 - With thinning and sawing; optional backside vias

Design Tool Status

- Complete Design Manual
- Device Library of circuit elements: FETs, diodes, thin film resistors, capacitors, inductors
- Design Kit for Agilent's ADS design environment
- Design Kit for AWR Microwave Office
- Layout Library in GDS II format
- Cadence Development Kit with PCells
- Layout Rule Sets for Design Rule Check for ICED, Cadence

Process Qualification Status

- Process fully released to production
- Full 150mm wafer Process Qualification complete
- For more information on Quality and Reliability, contact TriQuint or visit:
www.triquint.com/manufacturing/QR/

Applications Support Services

- Tiling of GDSII stream files including PCM
- Design Rule Check services
- Layout Versus Schematic check services
- Test Development Engineering:
 - On-wafer
- Thermal Analysis Engineering
- Yield Enhancement Engineering
- Failure Analysis

Manufacturing Services

- Mask making
- Production 150-mm wafer fab
- Wafer Thinning
- Wafer Sawing
- Substrate Vias
- DC Diesort Testing
- RF On-wafer testing

Training

- For Training & PDQ Schedules, please visit: www.triquint.com/foundry/

Contact Information

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