TQM879006

1.8-2.7GHz Digital Variable Gain Amplifier

Applications

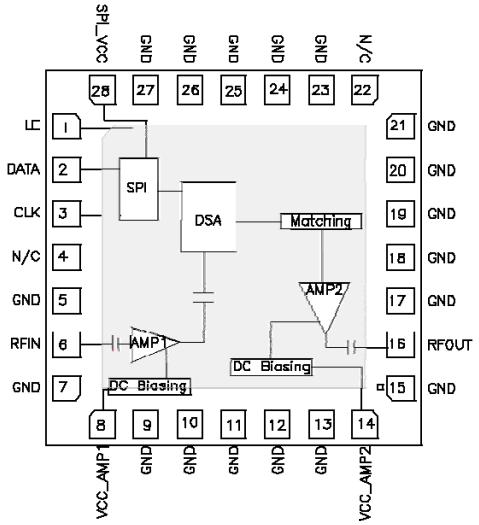
- 3G / 4G Wireless Infrastructure
- CDMA, TD-CDMA, WCDMA, LTE
- Repeaters
- PTP Radio IF Chains

28-pin 6x6mm leadless SMT package

Product Features

- 1.8-2.7 GHz Frequency Range
- 31 dB Maximum Gain at 2 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +41.3 dBm Output IP3
- +25.4 dBm Output P1dB
- 1.5 dB Noise Figure
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- 3-wire SPI Control Programming

Functional Block Diagram



General Description

The TQM879006 is a digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator (DSA), along with a high linearity ¼W amplifier. The module has the added features of integrating all matching components with bias chokes and blocking capacitors. The internal DSA offers 0.5 dB step, 6-bit, and 31.5 dB range and is controlled with a serial periphery interface (SPI™).

The TQM879006 features variable gain from -0.5 to 31dB at 2 GHz, has +41.3 dBm Output IP3, and +25.4 dBm P1dB. The amplifier also has a very low 1.5 dB Noise Figure (at maximum gain) allowing it to be an ideal DVGA for both receiver and transmitter applications. The amplifier operates from a single +5V supply and is available in a compact 28-pin 6x6 mm leadless SMT package.

Pin Configuration

Pin #	Symbol
1	LE
2	DATA
3	CLK
4, 22	NC
6	RFIN
8	VCC_AMP1
14	VCC_AMP2
16	RFOUT
28	VCC_SPI
All Other Pins	GND

Ordering Information

Part No.	Description
TQM879006	1.8-2.7GHz Digital Variable Gain Amp
TQM879006-PCB	Fully Assembled Evaluation Board Includes USB control board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power, CW, 50Ω,T = 25ºC	+23 dBm
Vcc (pins 8, 14, 28)	+5.5 V
Junction Temperature, T_J	+170 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vcc (pins 8, 14, 28)	4.75	5	5.25	V
Case Temperature	-40		85	°C

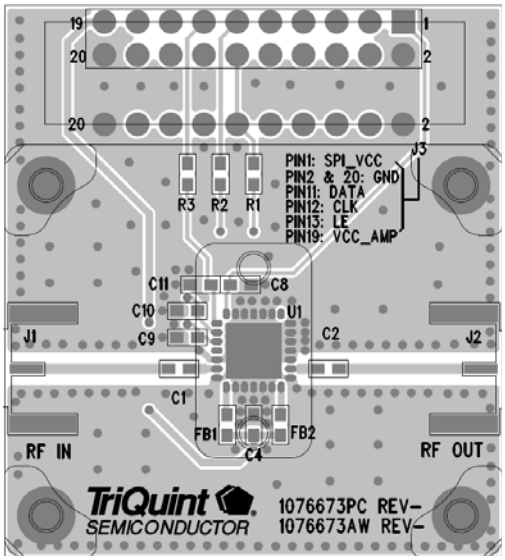
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

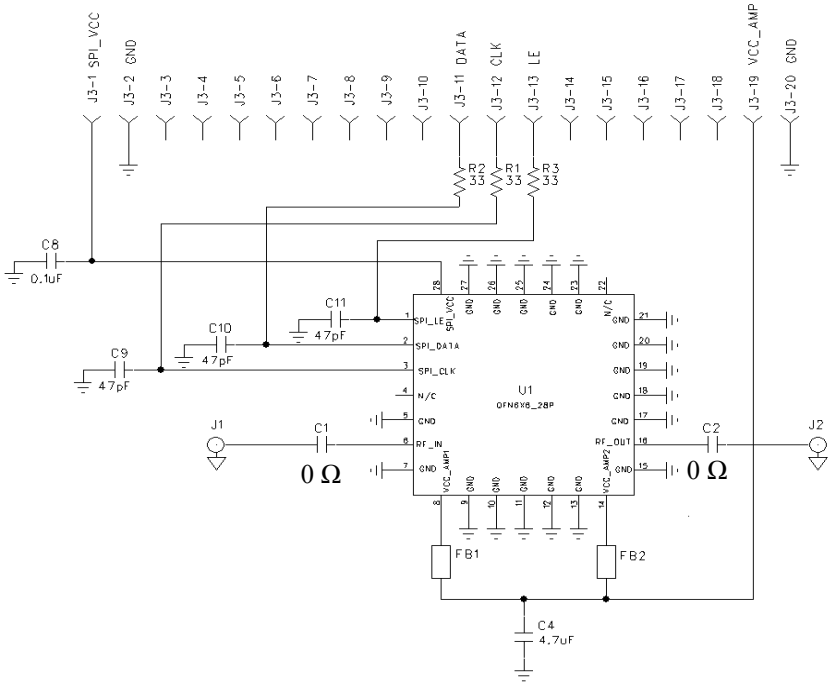
Electrical Specifications

Test conditions unless otherwise noted: 25ºC, +5Vcc, Maximum Gain State.

Parameter	Conditions	Min	Typ	Max	Units
Operational Freq Range		1800		2700	MHz
Test Frequency			2000		MHz
Gain		27.5	31		dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Accuracy Error	All States, 3 wire SPI, 6 states	±(0.3+5% of Attenuation setting) Max			dB
Control Interface	3-wire serial interface		6		Bit
Input Return Loss			24		dB
Output Return Loss			11		dB
Output P1dB			+25.4		dBm
Output IP3	Pout = +11 dBm/tone, Δf = 1MHz Spacing	+38	+41.3		dBm
Noise Figure			1.5		dB
I/O Impedance			50		Ohm
Supply Voltage			+5		V
Supply Current			200	240	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			45	°C/W

Application Circuit (TQM879006-PCB)





Notes:
1. For PCB Board Layout, see page 6 for more information.
2. All Components are of 0603 size unless stated otherwise.
3. For SPI Timing Diagram, see page 5.
4. Input and Output DC blocks (C1, C2) may be replaced by 0 Ω jumpers since module is DC blocked internally.
5. 0 Ω jumpers may be replaced with copper traces in the target application layout.
6. R1, R2 and R3 are used as termination for digital noise or any noise reflection.
7. Different ground pins are used for SPI (digital) and analog supply voltages.
8. The primary RF microstrip characteristic line impedance is 50 Ω.
9. The single power supply is used to provide supply voltage to AMP1 and AMP2.
10. Ferrite Bead FB1 eliminates bypass line resonances between internal bypass capacitor and C4. Steward MI0603K300R-10.

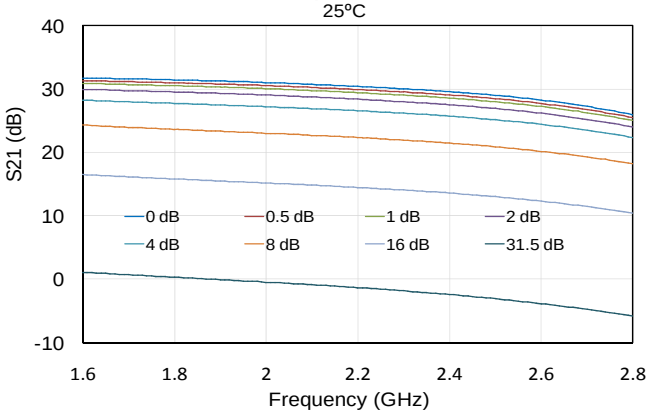
Typical Performance, Maximum Gain State

Frequency	GHz	1.8	2.0	2.14	2.35	2.6
Gain	dB	31.4	31	30.6	30	28
Input Return Loss	dB	16	24.5	26	23.5	21
Output Return Loss	dB	10.5	11	12	15	22.4
Output P1dB	dBm	+24.8	+25.4	+25.5	+25.7	+24.8
Output IP3 @ Pout = 11 dBm/tone, Δf = 1 MHz	dBm	+44	+41.3	+40	+38.6	+38.4
Noise Figure	dB	1.4	1.5	1.5	1.7	1.9
Supply Voltage	V	+5				
Supply Current	mA	200				

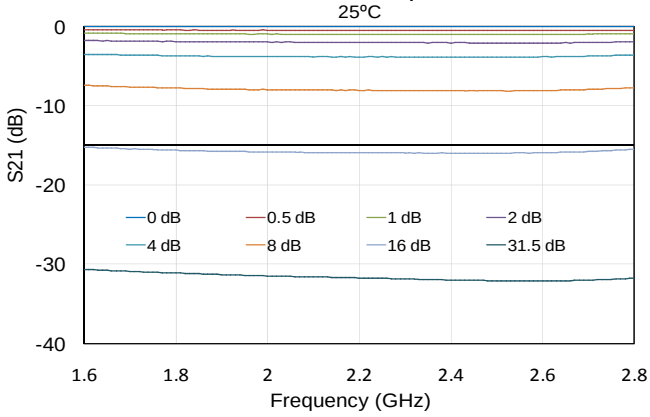
Note:
1. The evaluation board can be used with TriQuint's USB interface board. Refer to TriQuint's website for more information.

Typical Performance Plots

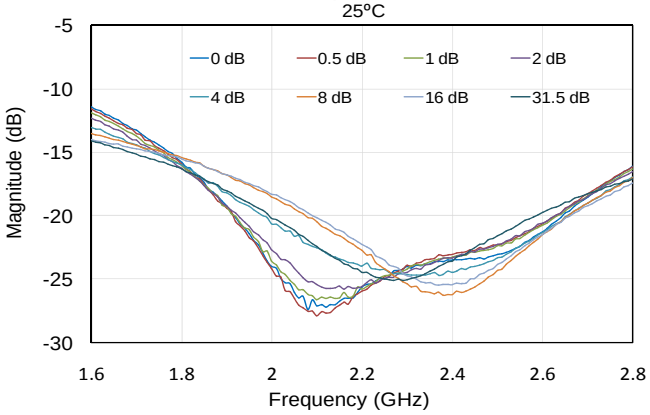
S21 vs. Freq over Attenuation
25°C



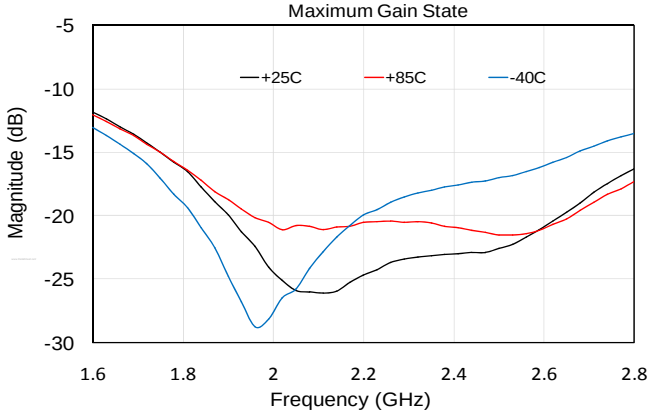
Normalized Gain vs. Freq over Attenuation
25°C



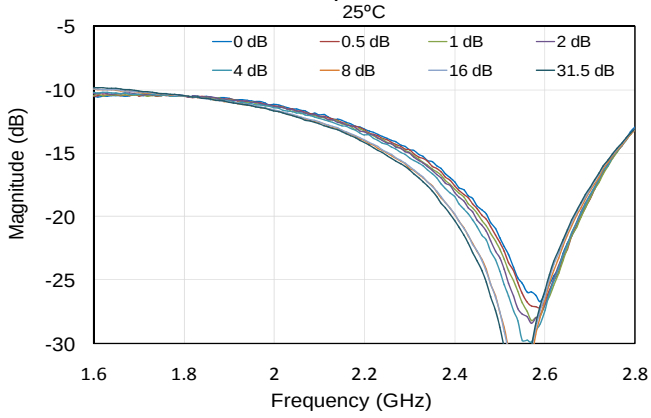
S11 vs. Freq over Attenuation
25°C



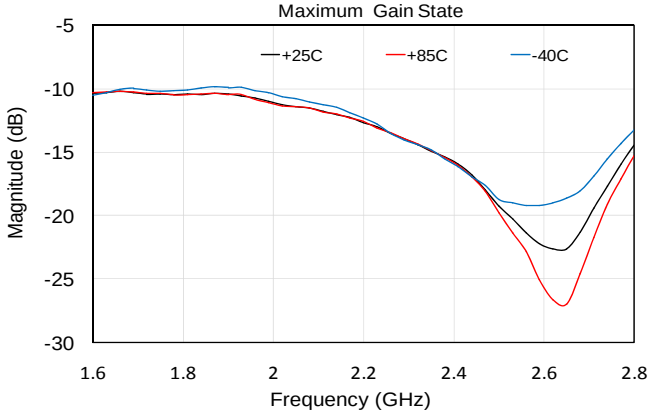
S11 vs. Freq over Temperature
Maximum Gain State



S22 vs. Freq over Attenuation
25°C

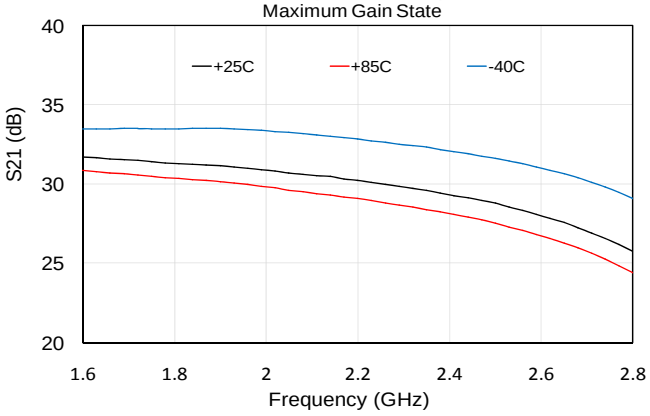


S22 vs. Freq over Temperature
Maximum Gain State

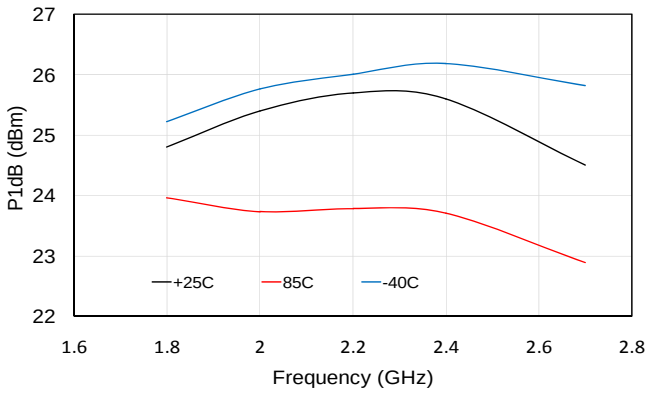


Typical Performance Plots

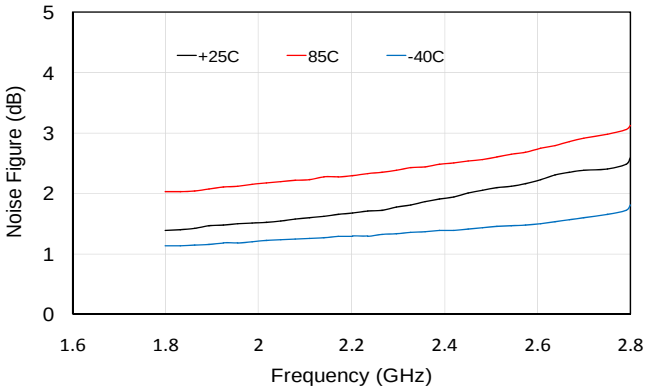
S21 vs. Freq over Temperature
Maximum Gain State



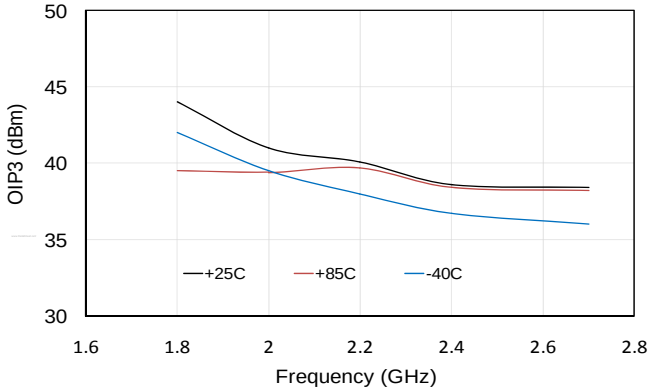
P1dB vs. Freq over Temperature
Maximum Gain State



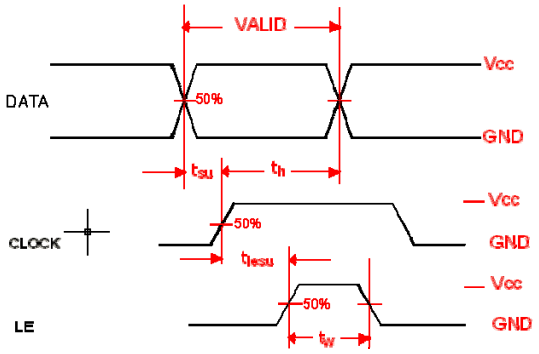
Noise Figure vs. Freq over Temperature
Maximum Gain State



OIP3 vs. Freq over Temperature
11 dBm/tone, 1 MHz Spacing, Maximum Gain State



Serial Interface Timing Diagram



Symbol	Parameter	Conditions	Limits	Units
fmax	Maximum Operating frequency, Clock	C_L=45pF	30	MHz
$V_{IH, min}$	Minimum HIGH Level Input Voltage	R_L=1kΩ, C_L=45pF	3.3	V
$V_{IL, max}$	Maximum LOW Level Input Voltage		0.8	
t_{su}	Minimum Set-up time from Data to Clock		20	ns
t_h	Minimum Hold time from Clock to Data		20	
t_{lesu}	Minimum Set-up time from Clock to LE		5	
t_w	Minimum LE Pulse Width		20	
t_R, t_F	Maximum Input Rise and Fall Time, Clock		15	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time (Parallel Data Outputs)		15	
	Maximum Output Rise and Fall Time (Serial Data Outputs)		19	

6-bit Attenuator Serial Programming Register Map

6-Bit Attenuator Serial Programming Register Map					
B5	B4	B3	B2	B1	B0
A5	A4	A3	A2	A1	A0

MSB (first in)

LSB (last in)

Truth Table

Attenuation State	A5	A4	A3	A2	A1	A0
Reference Loss	H	H	H	H	H	H
0.5 dB	H	H	H	H	H	L
1 dB	H	H	H	H	L	H
2 dB	H	H	H	L	H	H
4 dB	H	H	L	H	H	H
8 dB	H	L	H	H	H	H
16 dB	L	H	H	H	H	H
31.5 dB	L	L	L	L	L	L

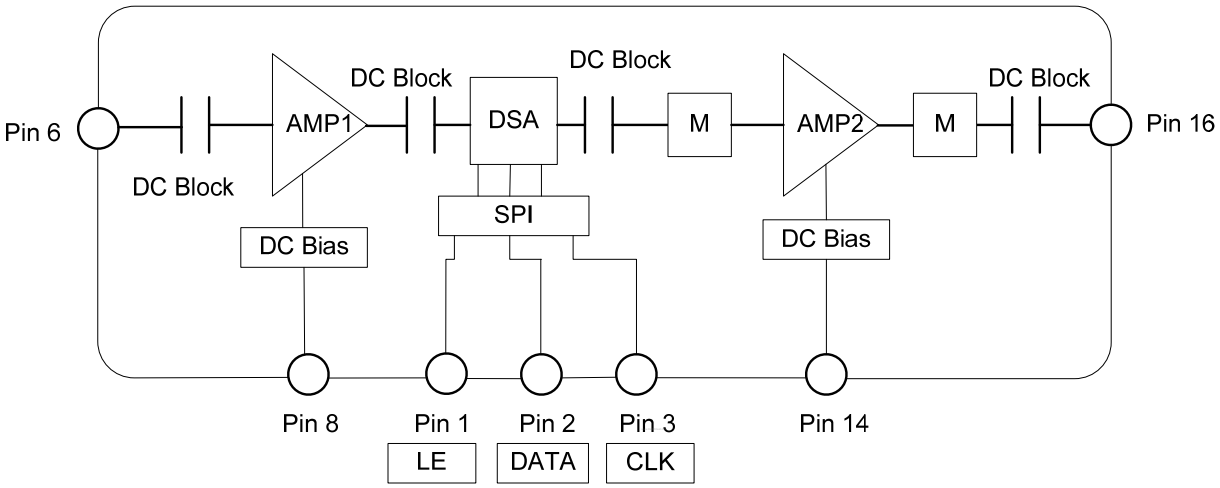
Note : Not all 64 possible combinations of A0-A5 are shown in this table.

Detailed Device Description

The TQM879006 is a 50 Ω internally matched digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator (DSA), along with a high linearity ¼W amplifier as shown in the functional diagram below. The module is unconditionally stable. Internal blocking capacitors and bias structures keep external parts count to a minimum. The DVGA has an operational frequency range from 1800-2700 MHz.

For any further technical questions, please email to **sjcapplications.engineering@tqs.com**.

Functional Schematic Diagram



Where M = Matching Network.

Chain Analysis Table

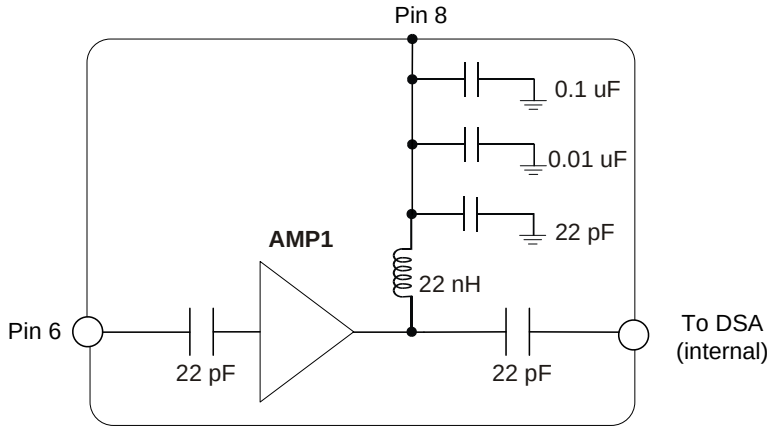
The chain analysis of DVGA module is shown below in the table. This table provides the typical performance of individual stages in the module as well as overall module performance.

	Individual Stage Performance			Overall Performance
Function	**AMP1**	**DSA**	**AMP2**	
Gain (dB)	19	-1.8	14	31
NF (dB)	1.3	1.8	4.5	1.5
OIP3 (dBm)	37	55	41	41
P1dB (dBm)	19.5	26	25.4	25.4
Icc (mA)	85	0	115	200

Detailed Device Description

AMP1

AMP1 is a wide band low noise amplifier gain block in DVGA module. The amplifier provides 19 dB gain, 1.3 dB noise figure, +37 dBm OIP3 at 1.9 GHz while only drawing 85 mA current. External DC blocks and biasing is not required. AMP1 is DC blocked internally and is connected internally to three bypass capacitors (22 pF, 0.01 uF, 0.1 uF) followed by 22 nH inductor inside the module as shown in the figure below.

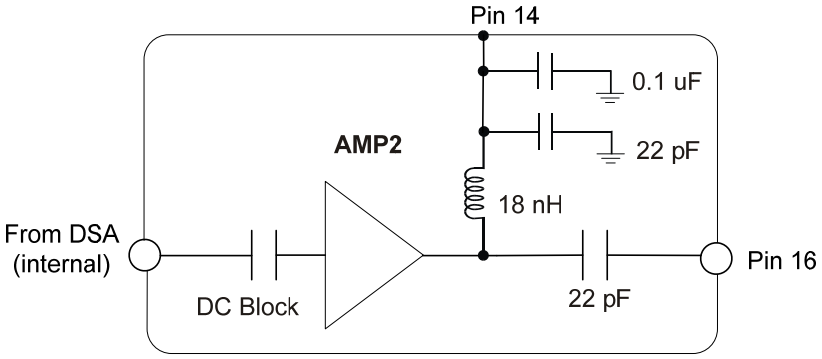


DSA (Digital Step Attenuator)

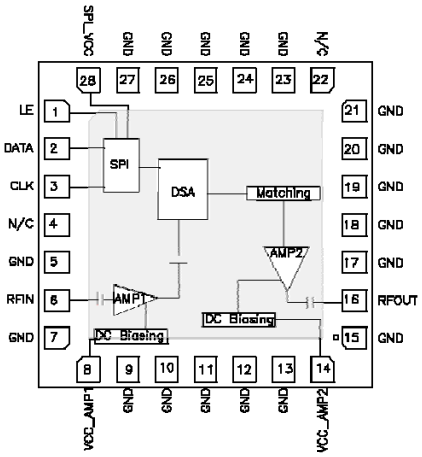
DVGA has a serial digital step attenuator that is controlled with 6-bit serial periphery interface (SPI™) and has 0.5 dB step size with 31.5 dB attenuation range. This 50-ohm RF DSA maintains high attenuation accuracy over frequency and temperature. "000000" represents maximum attenuation state. External bypass capacitors are needed to compensate the inductance effect associated with long transmission lines on the evaluation board.

AMP2

AMP2 is high linearity ¼-W amplifier in DVGA module. The amplifier provides 14 dB gain, +25.4 dBm P1dB, +41 dBm OIP3 at 2.14 GHz while only drawing 115 mA current. The amplifier is tuned over 1800 -2700 MHz bandwidth using internal matching components. AMP2 is DC blocked internally and is connected internally to two bypass capacitors (22 pF, 0.1 uF) followed by an 18 nH inductor inside the module as shown in the figure below. External DC blocks and biasing is not required.



Pin Configuration and Description



Pin	Symbol	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial clock input.
4, 22	N/C	No connect or open. This pin is not connected in this module
6	RFIN	Input, matched to 50 ohms between 1800 and 2700 MHz. Internally DC blocked.
8	VCC_AMP1	Supply Voltage to AMP1. This pin is connected internally to 3 bypass capacitors (22pF, 0.01uF, 0.1uF) followed by a 22 nH inductor inside the module.
14	VCC_AMP2	Supply Voltage to AMP2. This pin is connected internally to 2 bypass capacitors (22pF, 0.1uF) followed by an 18 nH inductor inside the module.
16	RFOUT	Output, matched to 50 ohms between 1800 and 2700 MHz. Internally DC blocked.
28	VCC_SPI	Supply voltage for SPI and DSA chip. This pin is connected to 1000 pF bypass capacitor internally.
All other Pins	GND	RF/DC Ground Connection

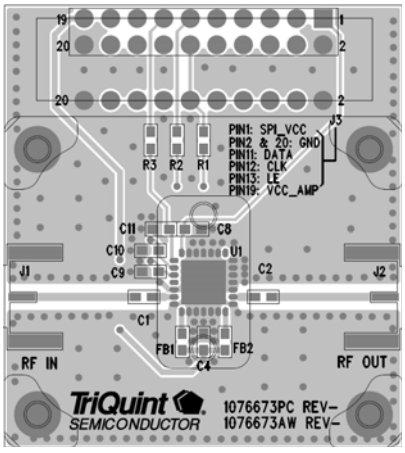
Applications Information

PC Board Layout

Top RF layer is .014" NELCO N4000-13 material, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .030", spacing = .036".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

For further technical information, Refer to www.TriQuint.com

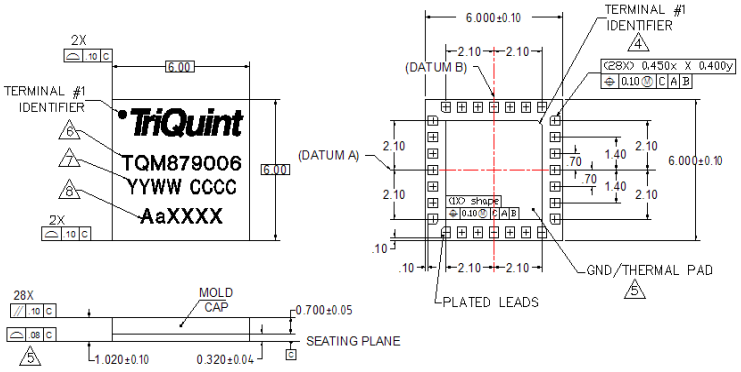


Mechanical Information

Package Information and Dimensions

This package is RoHS-compliant. The package bottom finish is electrolytic plated Au over Ni. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes. Also recommend adding active fluxes of 2% during solder reflow.

The component will be laser marked with "TQM879006" product label with an alphanumeric lot code on the top surface of the package.

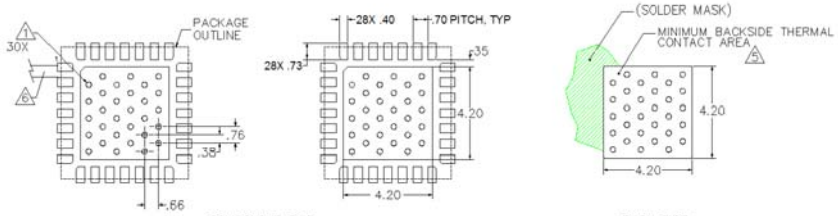


NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINEPITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PRODUCT CODE.
7. ALPHA-NUMERIC LOT CODE.
8. VENDOR CODE AND TRIQUINT LOT NUMBER

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIA LAND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1B
Value:	Passes ≥ 500 V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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