TQM829007

0.6-1.0GHz ¼W Digital Variable Gain Amplifier

Applications

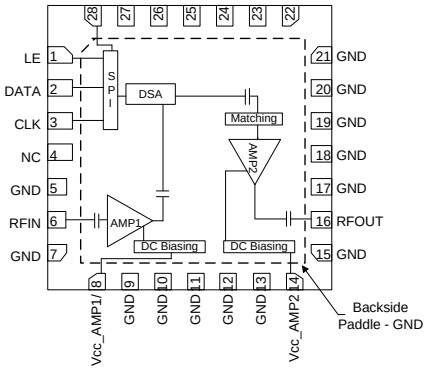
- 3G / 4G Wireless Infrastructure
- CDMA, WCDMA, LTE
- Repeaters
- ISM Infrastructure

28-pin 6x6mm leadless SMT package

Product Features

- 0.6-1.0 GHz Frequency Range
- 31.5 dB Maximum Gain at 0.9 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +40 dBm Output IP3
- +24.3 dBm Output P1dB
- 2.1 dB Noise Figure at Max. Gain State
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- 3-wire SPI Control Programming

Functional Block Diagram



General Description

The TQM829007 is a digital variable gain amplifier (DVGA) featuring high linearity performance in a fully integrated module. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator (DSA), along with a high linearity ¼W amplifier. The module has the added features of integrating all matching components with bias chokes and blocking capacitors. The internal DSA offers 0.5 dB step, 6-bit, and 31.5 dB range and is controlled with a serial periphery interface (SPI™).

The TQM829007 features variable gain from 0 to 31.5 dB at 0.9 GHz, has +40 dBm Output IP3, and +24.3 dBm P1dB. The amplifier also has a very low 2.1 dB Noise Figure (at maximum gain) allowing it to be an ideal DVGA for both receiver and transmitter applications. The amplifier operates from a single +5V supply and is available in a compact 28-pin 6x6 mm leadless SMT package.

The TQM829007 is pin compatible with the TQM879006 (1.4-2.7GHz, 0.25W DVGA) and TQM879008 (1.5-2.7 GHz, 0.5W DVGA). This allows one to size the right type of device for specific system level requirements as well as making the DVGA family ideal for applications where a common PCB layout is used for different frequency bands.

Pin Configuration

Pin #	Symbol
1	LE
2	DATA
3	CLK
4, 22	NC
6	RFIN
8	VCC_AMP1
14	VCC_AMP2
16	RFOUT
28	VCC_SPI
All Other Pins	GND

Ordering Information

Part No.	Description
TQM829007	0.6-1.0 GHz Digital Variable Gain Amp
TQM829007-PCB	Fully Assembled Evaluation Board Includes USB control board (EVH)

Standard T/R size = 2500 pieces on a 13” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power, CW, 50Ω,T = 25ºC	+12 dBm
Vcc (pins 8, 14, 28)	+5.5 V
Junction Temperature, T_J	160 °C
Digital Input Voltage	V_{cc}+ 0.5V

T_J specified for >10^6 hours MTTF
Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vcc (pins 8, 14, 28)	4.75	5	5.25	V
Case Temperature	-40		85	°C

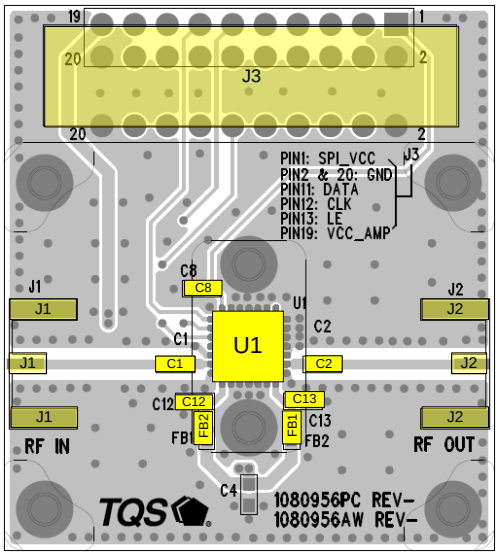
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

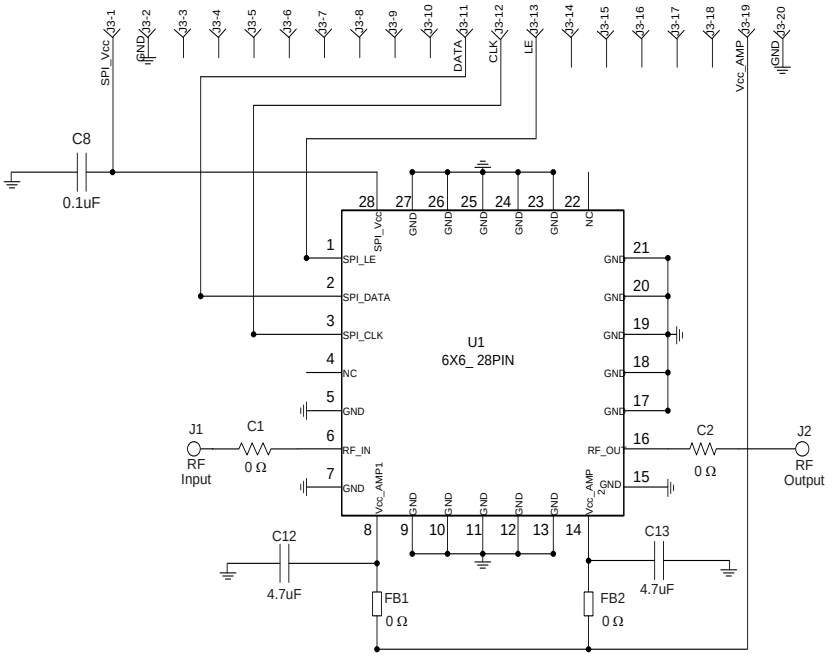
Electrical Specifications

Test conditions unless otherwise noted: 25ºC, Vcc = +5V, Maximum Gain State.

Parameter	Conditions	Min	Typ	Max	Units
Operational Freq Range		600		1000	MHz
Test Frequency			900		MHz
Gain		28.5	31.7		dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Accuracy Error	All States, 3 wire SPI, 6 states	±(0.5+5% of Attenuation setting) Max			dB
Control Interface	3-wire serial interface		6		Bit
Input Return Loss			16		dB
Output Return Loss			22		dB
Output P1dB			+24.3		dBm
Output IP3	Pout = +11 dBm/tone, Δf = 1MHz Spacing	+36.5	+40		dBm
Noise Figure			2.1		dB
I/O Impedance			50		Ω
Supply Voltage			+5		V
Supply Current		130	174	215	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			36.7	°C/W

Application Circuit (TQM829007-PCB)





Notes:
1. For PCB Board Layout, see page 9 for more information.
2. All Components are of 0603 size unless stated otherwise.
3. For SPI Timing Diagram, see page 6.
4. 0 Ω jumpers may be replaced with copper traces in the target application layout.
5. Different ground pins are used for SPI (digital) and analog supply voltages.
6. The primary RF microstrip characteristic line impedance is 50 Ω.
7. The single power supply is used to provide supply voltage to AMP1 and AMP2.

Bill of Material: TQM829007-PCB

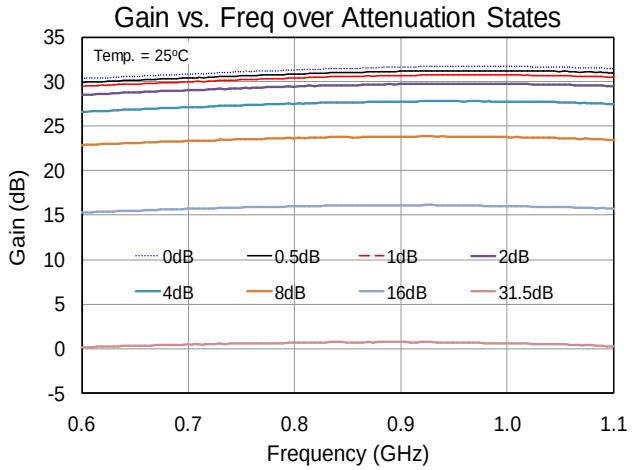
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		0.6 – 1.0 GHz ¼ W DVGA	TriQuint	TQM829007
C8	0.1 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C12, C13	4.7 uF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
C1, C2, FB1, FB2	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	
C4	Do Not Place			

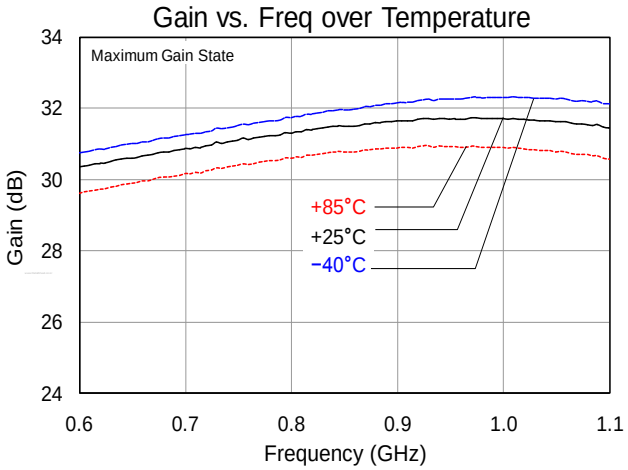
Typical Performance, Maximum Gain State

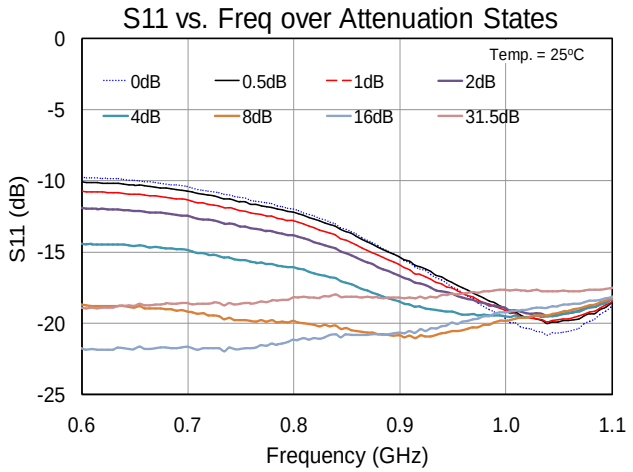
Frequency	GHz	0.6	0.7	0.8	0.9	1.0
Gain	dB	30.5	31	31.5	31.7	31.6
Input Return Loss	dB	10	10.5	12	16	20
Output Return Loss	dB	8	10	14	22	18
Output P1dB	dBm	+24.6	+24.5	+24.3	+24.3	+24.4
Output IP3 @ Pout = 11 dBm/tone, Δf = 1 MHz	dBm	+40	+39.5	+39.3	+39.5	+38.7
Noise Figure	dB	2.2	2.2	2.0	2.1	2.1
Supply Voltage	V			+5		
Supply Current	mA			174		

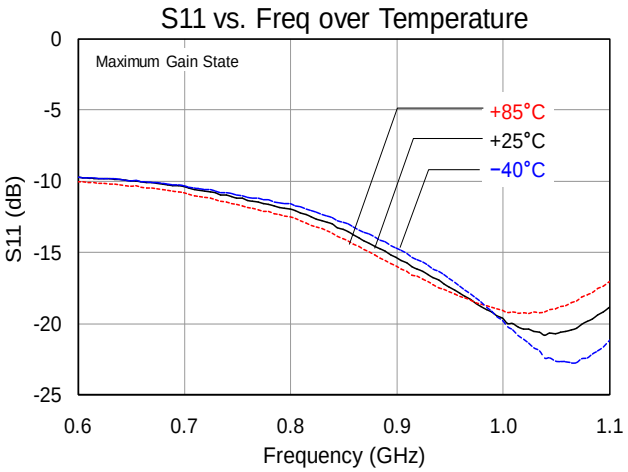
Note:
1. The evaluation board can be used with TriQuint's USB interface board. Refer to TriQuint's website for more information.

Typical Performance Plots

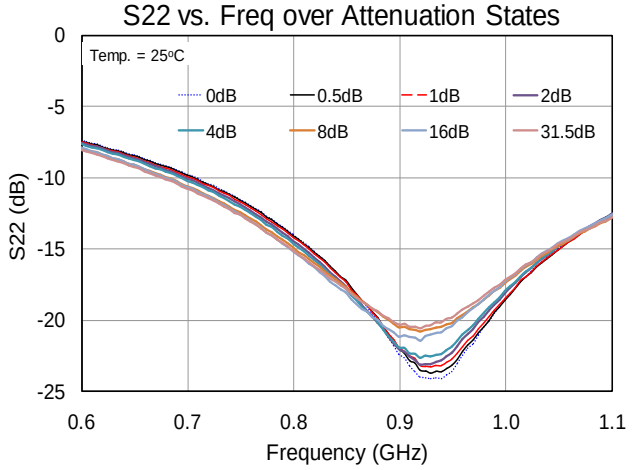




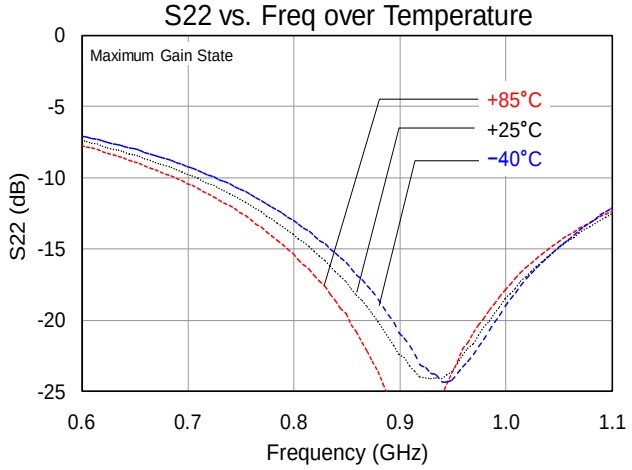




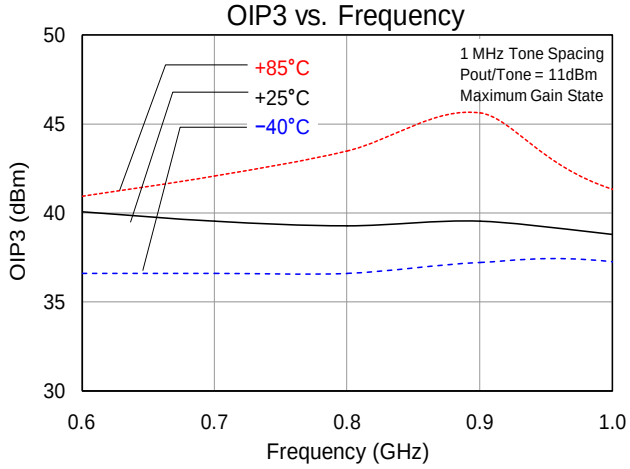
S22 vs. Freq over Attenuation States



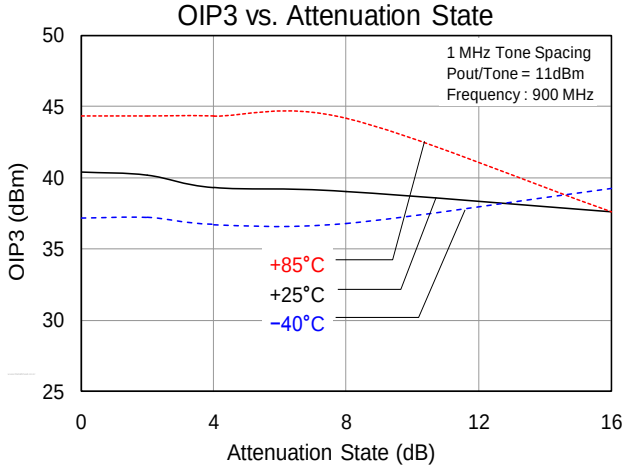
S22 vs. Freq over Temperature



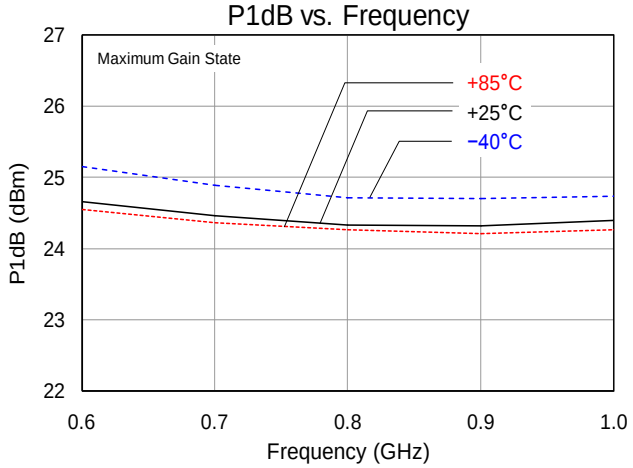
OIP3 vs. Frequency



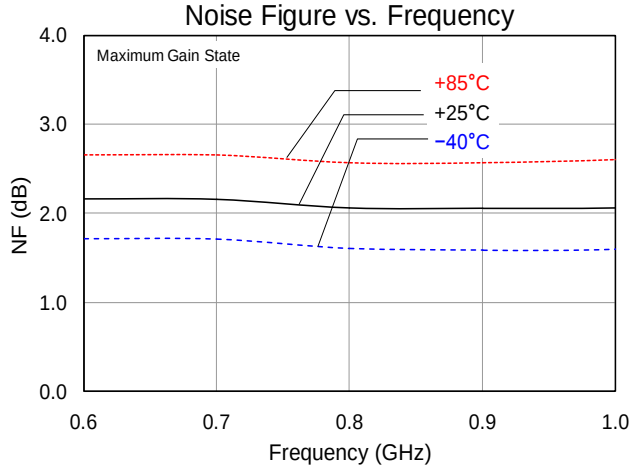
OIP3 vs. Attenuation State



P1dB vs. Frequency



Noise Figure vs. Frequency



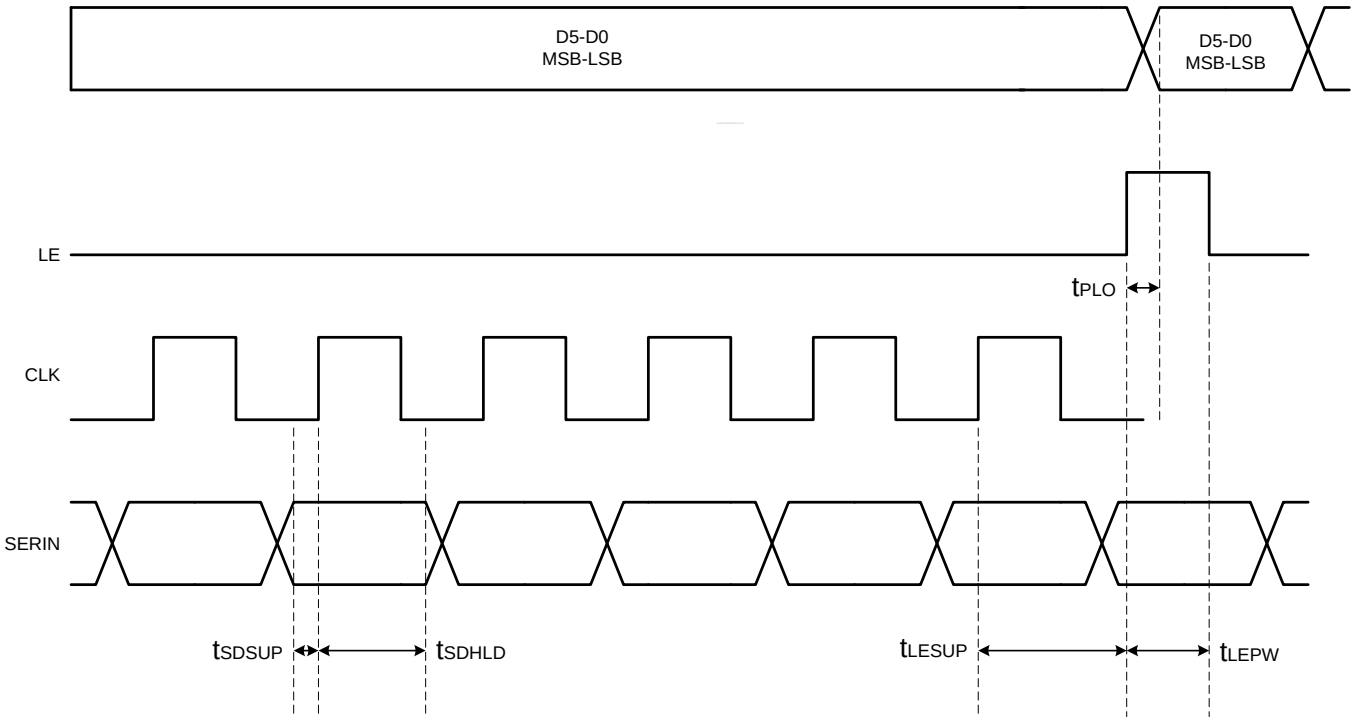
Serial Control Interface

SERIN (MSB in First 6-Bit Word) Control Logic Truth Table

6-Bit Control Word to DSA MSB					LSB	Attenuation State
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB
Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected						

Serial Control Interface Timing Diagram

CLK is disabled when LE is high



Serial Control Timing Characteristics

Test conditions: 25ºC

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

Serial Control DC Logic Characteristics

Test conditions: 25ºC

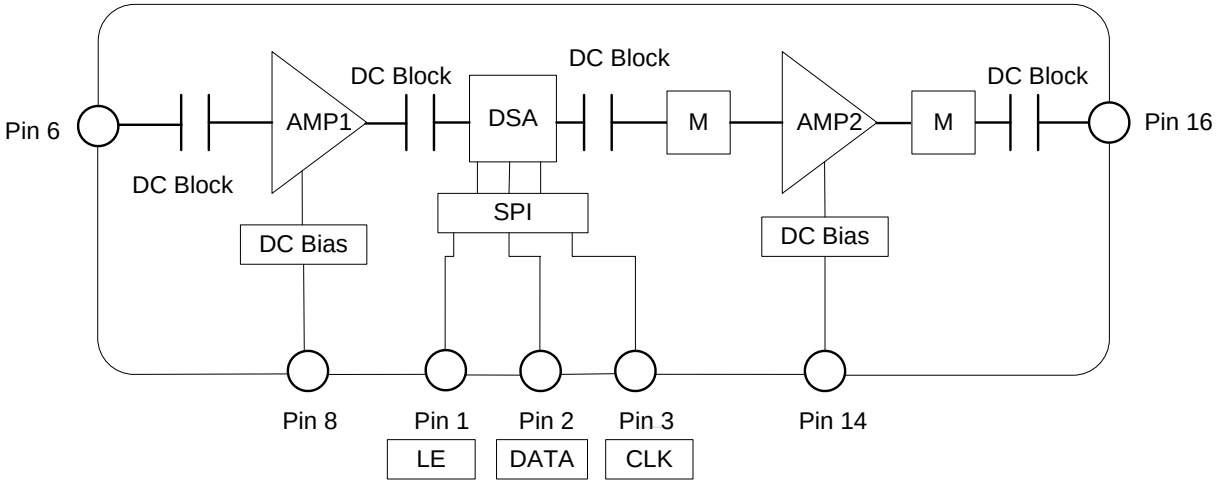
Parameter	Condition	Min	Max	Units
Input Low Voltage, V_{IL}		0	0.8	V
Input High Voltage, V_{IH}		2.4	Vcc	V
Input Current, I_{IH} / I_{IL}	On SERIN, LE and CLK	-10	+10	µA

Detailed Device Description

The TQM829007 is a 50 Ω internally matched digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator, along with a high linearity ¼W amplifier as shown in the functional diagram below. The module is unconditionally stable. Internal blocking capacitors and bias structures keep external parts count to a minimum. The DVGA has an operational frequency range from 0.6 – 1.0 GHz.

For any further technical questions, please email to **sjcapplications.engineering@tqs.com**.

Functional Schematic Diagram



Where M = Matching Network.

Chain Analysis Table

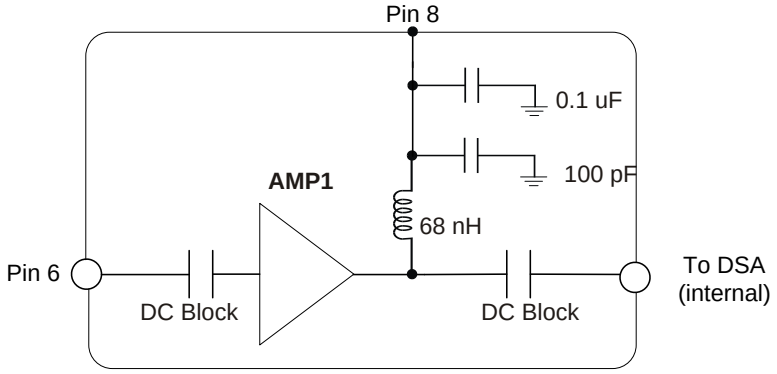
The chain analysis of DVGA module is shown below in the table. This table provides the typical performance of individual stages in the module as well as overall module performance.

	Individual Stage Performance			Overall Performance
Function	**AMP1**	**DSA**	**AMP2**	
Gain (dB)	14.5	-1.2	18.4	31.7
NF (dB)	2.0	1.2	2.1	2.1
OIP3 (dBm)	40.6	56	39.5	39.5
P1dB (dBm)	21.4	28.8	24.3	24.3
Icc (mA)	85	2.0	87	174

Detailed Device Description

AMP1

AMP1 is a wide band low noise amplifier gain block in DVGA module. The amplifier provides 14.5 dB gain, 2.0 dB noise figure, +40.6 dBm OIP3 at 0.9 GHz while only drawing 85 mA current. External DC blocks and biasing is not required. AMP1 is DC blocked internally and is connected internally to two bypass capacitors (100 pF, 0.1 uF) followed by 68 nH inductor inside the module as shown in the figure below.

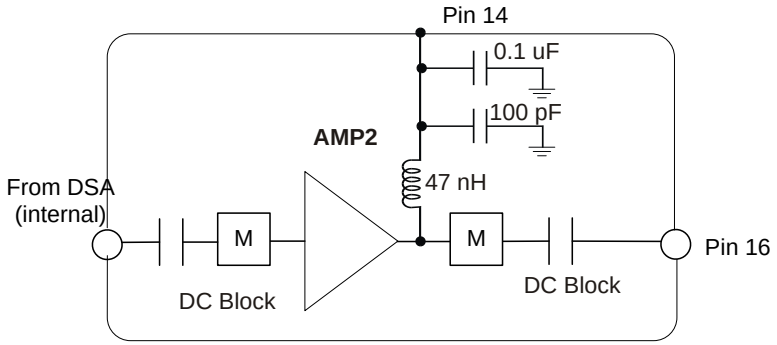


DSA (Digital Step Attenuator)

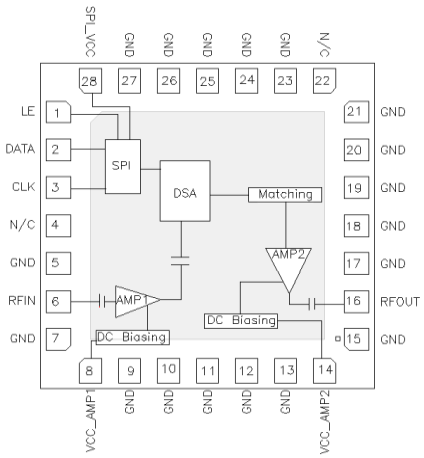
DVGA has a serial digital step attenuator that is controlled with 6-bit serial periphery interface (SPI™) and has 0.5 dB step size with 31.5 dB attenuation range. This 50-ohm RF DSA maintains high attenuation accuracy over frequency and temperature. "000000" represents maximum attenuation state. External bypass capacitors are needed to compensate the inductance effect associated with long transmission lines on the evaluation board.

AMP2

AMP2 is high linearity ¼-W amplifier in DVGA module. The amplifier provides 18.4 dB gain, +24.3 dBm P1dB, +39.5 dBm OIP3 at 0.9 GHz while only drawing 87 mA current. The amplifier is tuned over 0.6 – 1.0 GHz bandwidth using internal matching components. AMP2 is DC blocked internally and is connected internally to two bypass capacitors (100 pF, 0.1 uF) followed by a 47 nH inductor inside the module as shown in the figure below. External DC blocks and biasing is not required.



Pin Configuration and Description



Pin	Symbol	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial clock input.
4, 22	N/C	No connect or open. This pin is not connected in this module
6	RFIN	Input, matched to 50 ohms. Internally DC blocked.
8	VCC_AMP1	Supply Voltage to AMP1. This pin is connected internally to 2 bypass capacitors (100 pF, 0.1 uF) followed by a 68 nH inductor inside the module.
14	VCC_AMP2	Supply Voltage to AMP2. This pin is connected internally to 2 bypass capacitors (100 pF, 0.1 uF) followed by a 47 nH inductor inside the module.
16	RFOUT	Output matched to 50 ohms. Internally DC blocked.
28	VCC_SPI	Supply voltage for SPI and DSA chip. This pin is connected to 0.1 uF bypass capacitor internally.
All other Pins	GND	RF/DC Ground Connection

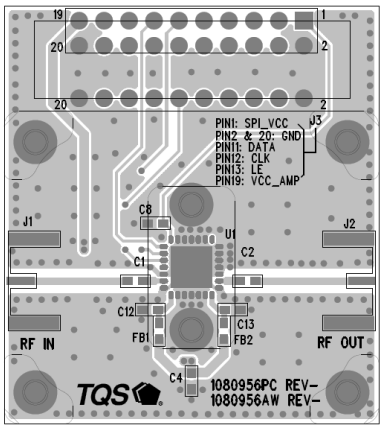
Applications Information

PC Board Layout

Top RF layer is .014" NELCO N4000-13 material, ϵ_r (typical) = 3.7, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .030", spacing = .036".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

For further technical information, Refer to www.TriQuint.com

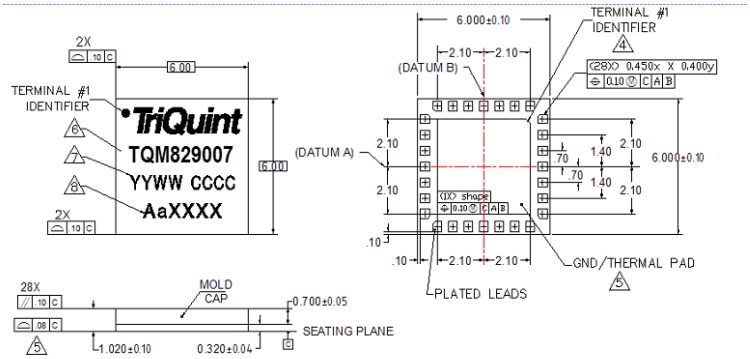


Mechanical Information

Package Information and Dimensions

This package is RoHS-compliant. The package bottom finish is electrolytic plated Au over Ni. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes. Also recommend adding active fluxes of 2% during solder reflow.

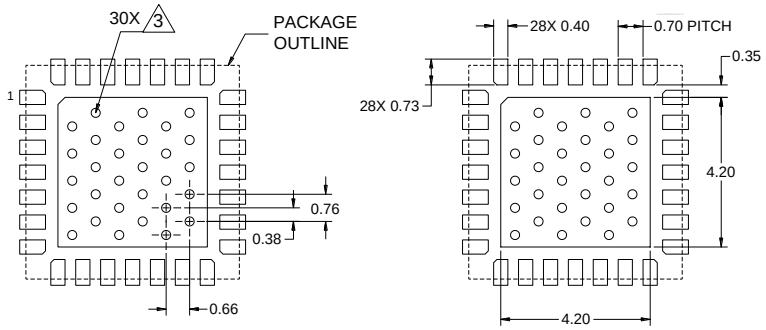
The component will be laser marked with "TQM829007" product label with an alphanumeric lot code on the top surface of the package.



NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINEPITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PRODUCT CODE.
7. ALPHA-NUMERIC LOT CODE.
8. VENDOR CODE AND TRIQUINT LOT NUMBER

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000 V to < 2000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with both lead-free (maximum 260 °C reflow temperature) and tin/lead (maximum 245 °C reflow temperature) soldering processes.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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