



TQ8101C

622/155 Mb/s SONET/SDH MDFP

Features

- Byte-wide Multiplexing, Demultiplexing, Framing, and PLL (MDFP) in one device
- Choice of STS-12/STM-4 or STS-3/STM-1 transmission rates
- Configurable master or slave reference clock generation and PLL bypass for external clocking
- 77.76 MHz or 19.44 MHz output for the multiplexer; 77.76 MHz or 19.44 MHz and 51.84 MHz output for the demultiplexer
- External RC loop filter
- Pass-through mode and three loopback modes for enhanced field diagnostics
- Frame-synchronous and byte-aligned demultiplexer output, compliant with SONET and SDH
- Search, detect, and recovery of framing on out-of-frame input
- Standard TTL and differential or single-ended ECL I/O (except TXCK)
- Tristate TTL output for factory circuit-board testability
- 68-pin TriQuint MLC controlled-Z surface-mount package with integral heat spreader
- Dual-supply operation (+5V, -5.2V)
- Low power dissipation (2.3W nom.)

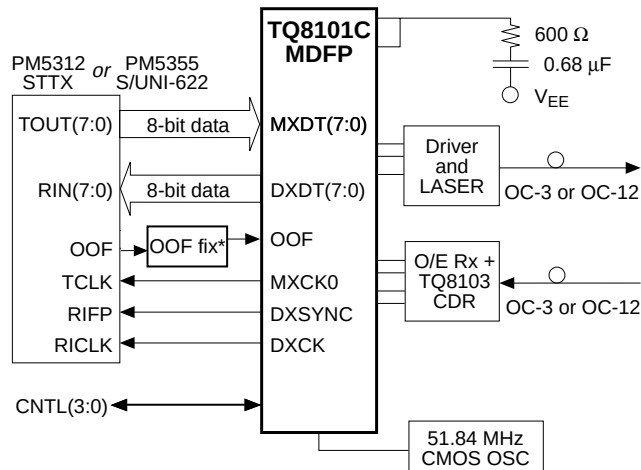
The TQ8101C is a SONET/SDH transceiver that integrates Multiplexing, Demultiplexing, SONET/SDH Framing, clock synthesis PLL (MDFP), and loopback functions in a single monolithic integrated circuit. Implementation with the TQ8101C requires only a simple external RC loop filter and standard TTL and ECL power supplies. For optimal performance, the TQ8101C MDFP is packaged in a 68-pin multilayer ceramic (MLC) surface-mount package with an integral CuW heat spreader. The TQ8101C provides an integrated solution for physical interfaces intended for use in STS-12/STM-4 (622.08-Mb/s) and STS-3/STM-1 (155.52-Mb/s) SONET/SDH systems.

The TQ8101C meets ANSI, Bellcore, and ITU requirements for a SONET/SDH device. With a 51.84-MHz reference clock, the phase-locked loop (PLL) provides 77.76-MHz or 19.44-MHz output for the multiplexer and 77.76-MHz or 19.44-MHz and 51.84-MHz output for the demultiplexer.

Typical SONET/SDH system applications for the TQ8101C include:

- Transmission system transport cards
- Switch and cross-connect line cards
- Repeaters
- ATM physical layer interfaces
- Test equipment
- Add/drop multiplexers

Figure 1. Logical Application



*Contact PMC-Sierra for application note.

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Figure 2. TQ8101C Block Diagram

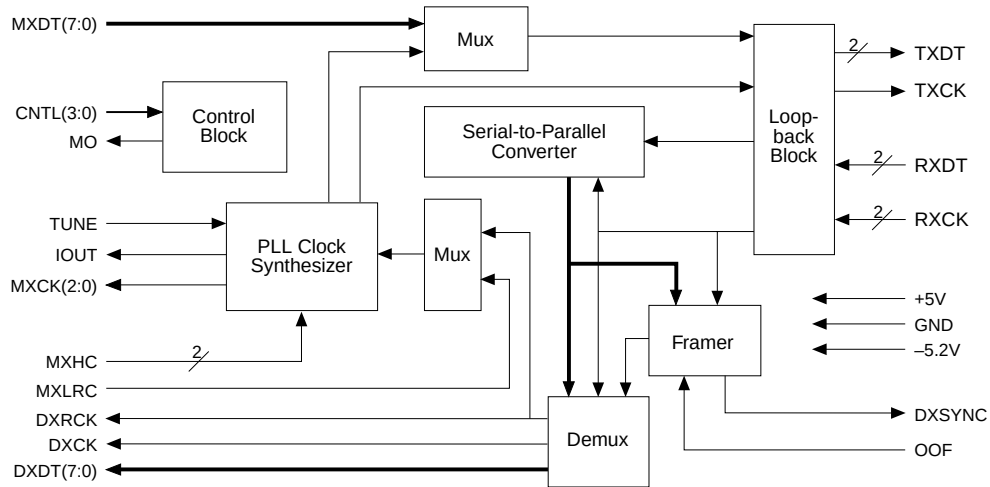
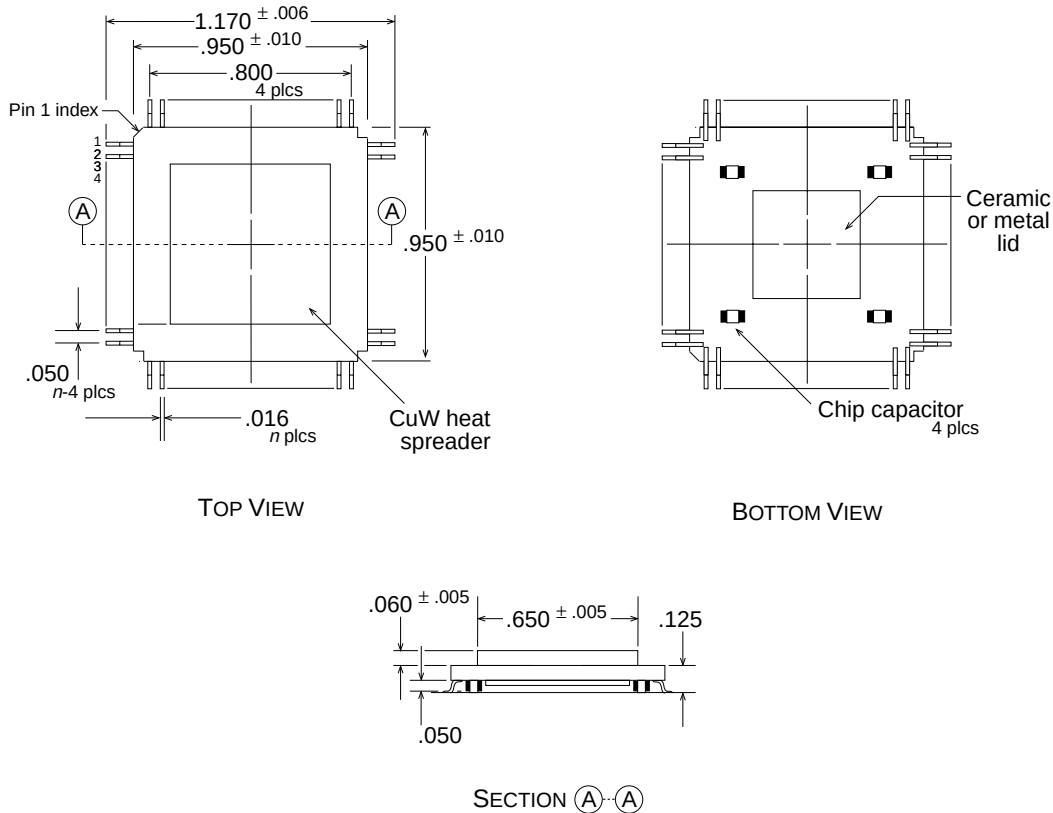


Figure 3. TQ8101C Package—68-pin MLC



Functional Description

Figure 2 shows a block diagram of the TQ8101C multiplexer, demultiplexer, framer, and PLL clock synthesizer (MDFP). The primary purpose of TQ8101C is to integrate the conversion of serial and parallel SONET/SDH data with bit alignment and clock synthesis in a single device.

Multiplexing

Byte-wide input data on MXDT(7:0)¹ is continuously strobed into the multiplexer on the rising edge of the multiplexer clock output, MXCK(2:0).² Any of these three MXCK pins may be used as a reference point for relative timing. (See Table 8 for setup, hold, and skew times. See Table 1 for clock selection options.)

Either an on-chip synthesized clock (see “PLL Clock Synthesis”) or an external high-speed multiplexer

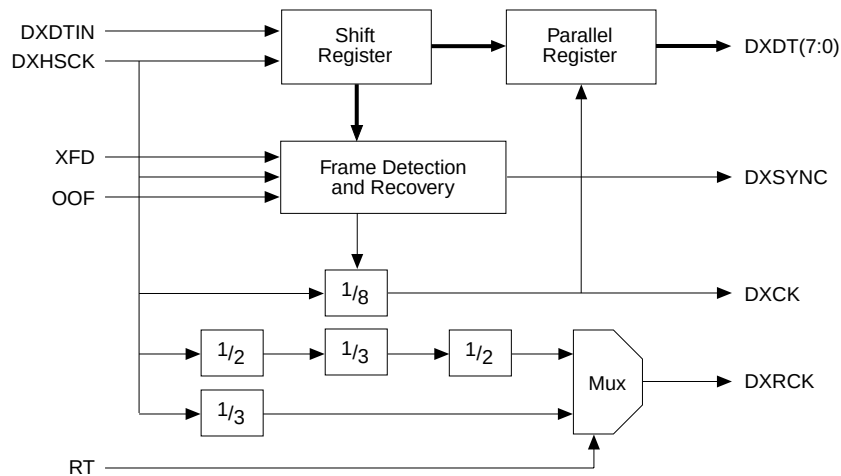
clock, MXHC, serializes the input data bytes. In the normal mode of operation, the serial data is then buffered as ECL-compatible output on TXDT. An ECL output is provided for the transmit clock, TXCK.

Demultiplexing

As shown in Figure 4, The demultiplexer block converts incoming serial data on DXDTIN³. Byte-wide output data is presented on DXDT(7:0)⁴ slightly after the falling edge of the output demultiplexer clock, DXCK. (See Table 8 for setup, hold, and skew times.)

The demultiplexer block also includes clock divider circuitry, which is used by the demultiplexer to control divide-by-8 output on DXCK. The MDFP provides a divide-by-3 or divide-by-12 output, DXRCK. (See Table 1 for mode selection options.)

Figure 4. Demultiplexer Functional Block



- Notes:
1. MXDT(0) is defined as the least significant bit.
 2. MXCK(2:0) nominally runs at 77.76 MHz in STS-12/STM-4 mode, and at 19.44 MHz in STS-3/STM-1 mode.
 3. Internal signal. See Figure 5, "TQ8101C Loopback Modes."
 4. DXDT (0) is defined as the least significant bit.

Framing

The demultiplexer block (see Figure 2) includes a frame-detection and recovery block. Regardless of the state of the OOF input signal, this block takes DXSYNC high for one period of DXCK whenever it detects a pattern of three “A1” bytes followed by three “A2” bytes.

Frame recovery is initiated by the rising edge of the OOF input signal. The recovery process involves a search for a bit rotation that satisfies the three-“A1”–three-“A2” byte pattern specified for SONET/SDH. Once the pattern is found, DXSYNC goes high and the bit rotation is synchronized to the correct byte boundaries. No further byte boundary adjustments are made, regardless of “A1”-“A2” indication, unless they have been preceded by an OOF rising edge.

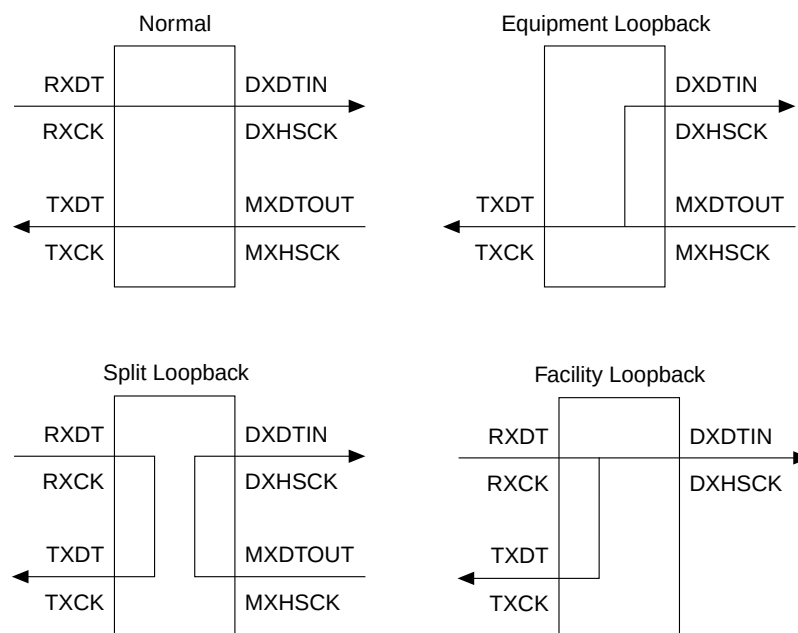
PLL Clock Synthesis

The PLL utilizes a monolithic voltage-controlled oscillator with a typical tuning constant of 50 to 100 MHz per volt on the TUNE input. This configuration provides jitter performance superior to other technologies. In a typical SONET/SDH application the TUNE input and charge pump output IOU are connected and tied to V_{EE} through a 600-ohm resistor and 0.68- μ F capacitor.

Loopback

The TQ8101C features four loopback modes: normal (pass-through), equipment loopback, split loopback, and facility loopback. Loopback modes are controlled by pins CNTL(3:0). Note that the loopback mode does not affect the latched selection of clock modes and rates. Note that the RXCK input is directly connected to the TXCK output in most loopback modes (see below).

Figure 5. TQ8101C Loopback Modes



Control

The signals on pins CNTL(3:0) can be used to control the clock rate, clock mode, loopback scheme, and tristate pins. Also, the internal PLL high-speed clock may be disabled, allowing an external clock source to be used on the MXHCN and MXHCP pins.

At power-up or during initialization, CNTL(3) should be set to logic 1. During reset, all internal counters, dividers, and loopback states, and the phase-frequency detector, are reset or deactivated. Note that frame search is initiated only by a rising edge on OOF.

Note that the NAND tree enable normally is used only for device testing of the V_{IH} and V_{IL} parameters.

Table 1. Modes of Operation

CNTL(3:0)	Modes of operation
0h	Reset
1h	Tristate all TTL outputs except DXRCK and MO
2h	NAND-tree test all TTL inputs except CNTL(3:0)
3h	DXRCK tristate
4h	Frame recovery disable
5h	Equipment loopback
6h	Facility loopback
7h	Split loopback
8h	Bypass, slave, internal VCO disabled, STS-3 rate
9h	Bypass, master, internal VCO disabled, STS-3 rate
Ah	Bypass, slave, internal VCO disabled, STS-12 rate
Bh	Bypass, master, internal VCO disabled, STS-12 rate
Ch	Normal, slave, internal VCO enabled, STS-3 rate
Dh	Normal, master, internal VCO enabled, STS-3 rate
Eh	Normal, slave, internal VCO enabled, STS-12 rate
Fh	Normal, master, internal VCO enabled, STS-12 rate

Notes: • "Bypass" indicates the use of the external high-speed clock in lieu of the internal transmit PLL.
 • "Normal" indicates use of the internal transmit PLL.
 • "Master" derives PLL timing from the reference 51.84-MHz oscillator input, MXLRC
 • "Slave" derives PLL timing from the demultiplexer clock input, RXCK.

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Table 2. Absolute Maximum Ratings

<i>Parameter</i>	<i>Symbol</i>	<i>Level</i>	<i>Minimum</i>	<i>Maximum</i>	<i>Unit</i>
Positive supply	V_{CC}	—	0	7	V
Negative supply	V_{EE}	—	−7	0	V
Output voltage	V_O	ECL	$V_{EE} - 0.5$	+0.5	V
Output current	I_O	ECL	—	40	mA
Input voltage	V_I	ECL	$V_{EE} - 0.5$	+0.5	V
Input current	I_I	ECL	−1	1	mA
Output voltage	V_O	TTL	−0.5	$V_{CC} + 0.5$	V
Output current	I_O	TTL	—	20	mA
Input voltage	V_I	TTL	−0.5	$V_{CC} + 0.5$	V
Input current	I_I	TTL	−1	1	mA
Junction temperature	T_J	—	−55	+150	°C
Storage temperature	T_S	—	−65	+175	°C

Table 3. Recommended Operating Conditions

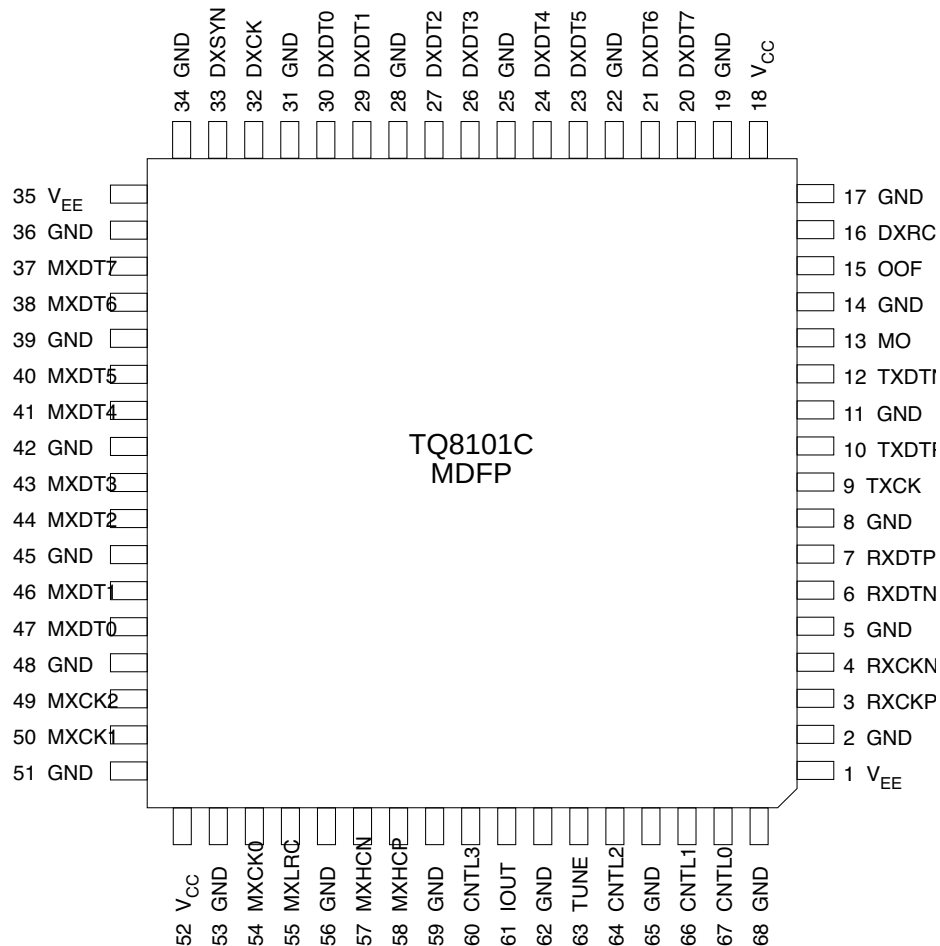
<i>Parameter</i>	<i>Symbol</i>	<i>Minimum</i>	<i>Nominal</i>	<i>Maximum</i>	<i>Unit</i>
Positive supply	V_{CC}	4.75	5	5.25	V
Negative supply	V_{EE}	−5.5	−5.2	−4.75	V
Operating ambient temperature	T_O	0		70	°C

Table 4. Power Consumption

<i>Function</i>	<i>+5 V supply</i>	<i>−5.2 V supply</i>	<i>Unit</i>
Nominal	40	320	mA
Max	55	420	mA

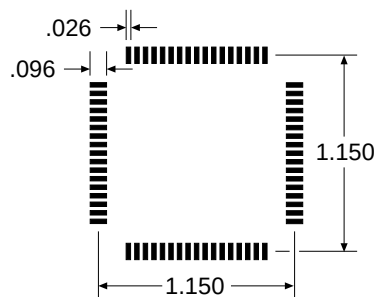
<i>Parameter</i>	<i>Symbol</i>	<i>Level</i>	<i>Minimum</i>	<i>Maximum</i>	<i>Unit</i>
Thermal resistance, junction-case	θ_{JC}			4	°C / W

Figure 6. Pinout Diagram
(heat spreader side—top view)



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Figure 7. Recommended Package Footprint



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Table 5. Signal Descriptions

<i>Pin</i>	<i>Signal</i>	<i>Type</i>	<i>Description</i>
1	V _{EE}		Negative power supply input (–5.2V)
2	GND		Ground
3	RXCKP	In	Receive bit-serial clock; differential ECL, positive
4	RXCKN	In	Receive bit-serial clock; differential ECL, negative
5	GND		Ground
6	RXDTN	In	Receive bit-serial data (MSB first); differential ECL, negative
7	RXDTP	In	Receive bit-serial data (MSB first); differential ECL, positive
8	GND		Ground
9	TXCK	Out	Transmit bit-serial clock; single-ended ECL level
10	TXDTP	Out	Transmit bit-serial data (MSB first); differential ECL, positive
11	GND		Ground
12	TXDTN	Out	Transmit bit-serial data (MSB first); differential ECL, negative
13	MO	Out	NAND tree monitor output; TTL level
14	GND		Ground
15	OOF	In	Out of frame; TTL level; rising-edge initiated frame search
16	DXRCK	Tri Out	Demultiplexer reference clock; TTL level; 50-pF backplane driving capacity
17	GND		Ground
18	V _{CC}		Positive power supply input (+5.0V)
19	GND		Ground
20	DXDT7	Tri Out	Demultiplexer byte-serial data (bit 7); TTL level
21	DXDT6	Tri Out	Demultiplexer byte-serial data (bit 6); TTL level
22	GND		Ground
23	DXDT5	Tri Out	Demultiplexer byte-serial data (bit 5); TTL level
24	DXDT4	Tri Out	Demultiplexer byte-serial data (bit 4); TTL level
25	GND		Ground
26	DXDT3	Tri Out	Demultiplexer byte-serial data (bit 3); TTL level
27	DXDT2	Tri Out	Demultiplexer byte-serial data (bit 2); TTL level
28	GND		Ground
29	DXDT1	Tri Out	Demultiplexer byte-serial data (bit 1); TTL level
30	DXDT0	Tri Out	Demultiplexer byte-serial data (bit 0); TTL level
31	GND		Ground
32	DXCK	Tri Out	Demultiplexer byte-serial clock; TTL level
33	DXSYNC	Tri Out	Demultiplexer synchronization; TTL level
34	GND		Ground

(Continues on next page)

Table 5. Signal Descriptions (continued)

Pin	Signal	Type	Description
35	V _{EE}		Negative power supply input (–5.2V)
36	GND		Ground
37	MXDT7	In	Multiplexer byte-serial data (bit 7); TTL level
38	MXDT6	In	Multiplexer byte-serial data (bit 6); TTL level
39	GND		Ground
40	MXDT5	In	Multiplexer byte-serial data (bit 5); TTL level
41	MXDT4	In	Multiplexer byte-serial data (bit 4); TTL level
42	GND		Ground
43	MXDT3	In	Multiplexer byte-serial data (bit 3); TTL level
44	MXDT2	In	Multiplexer byte-serial data (bit 2); TTL level
45	GND		Ground
46	MXDT1	In	Multiplexer byte-serial data (bit 1); TTL level
47	MXDT0	In	Multiplexer byte-serial data (bit 0); TTL level
48	GND		Ground
49	MXCK2	Tri Out	Multiplexer byte-serial clock (bit 2); TTL level. See Table 1 for output rate.
50	MXCK1	Tri Out	Multiplexer byte-serial clock (bit 1); TTL level. See Table 1 for output rate.
51	GND		Ground
52	V _{CC}		Positive power supply input (+5.0V)
53	GND		Ground
54	MXCK0	Tri Out	Multiplexer byte-serial clock (bit 0); TTL level. See Table 1 for output rate.
55	MXLRC	In	Multiplexer low-speed reference clock (51.84 MHz); TTL level
56	GND		Ground
57	MXHCN	In	Multiplexer high-speed reference clock (max. 640 MHz); differential ECL, negative
58	MXHCP	In	Multiplexer high-speed reference clock (max. 640 MHz); differential ECL, positive
59	GND		Ground
60	CNTL3	In	Control (bit 3); TTL level
61	IOUT	Out	Tristate charge pump output (analog); connect to pin 63
62	GND		Ground
63	TUNE	In	VCO tune (analog); connect to external loop filter and pin 61
64	CNTL2	In	Control (bit 2); TTL level
65	GND		Ground
66	CNTL1	In	Control (bit 1); TTL level
67	CNTL0	In	Control (bit 0); TTL level
68	GND		Ground

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Table 6. DC Characteristics—ECL I/O ⁽¹⁾

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Internal ECL reference	(2)	V_{REF}	—	$0.26 V_{EE}$		mV
Common mode voltage	(3)	V_{COM}	–1500	—	–1100	mV
Differential voltage	(3)	V_{DIFF}	200	—	1200	mV
Input HIGH voltage	(4)	V_{IH}	–1100	—	–400	mV
Input LOW voltage		V_{IL}	V_{EE}	—	–1500	mV
Output HIGH voltage	(5)	V_{OH}	–1000	0	–500	mV
Output LOW voltage	(5)	V_{OL}	$V_{TT} - 100$	—	–1600	mV
Input HIGH current	$V_{IH} (MAX)$	I_{IH}	—	—	30	mA
Input LOW current	$V_{IL} (MIN)$	I_{IL}	—	—	–30	mA
Output HIGH current	(6)	I_{OH}	20	23	30	mA
Output LOW current	(6)	I_{OL}	–2	5	8	mA
Input capacitance		C_{IN}	—	3	—	pF
Output capacitance		C_{OUT}	—	3	—	pF
ESD breakdown	(1)	V_{ESD}	500	—	—	V

Table 7. DC Characteristics—TTL I/O ⁽¹⁾

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0	—	V_{CC}	V
Input LOW voltage		V_{IL}	0	—	0.8	V
Input HIGH current	$V_{IH} (MAX)$	I_{IH}	—	—	100	mA
Input LOW current	$V_{IL} (MIN)$	I_{IL}	–100	—	—	mA
Output HIGH voltage	$I_{OH} = 3 \text{ mA}$	V_{OH}	2.4	—	V_{CC}	V
Output LOW voltage	$I_{OL} = -1 \text{ mA}$	V_{OL}	0	—	0.4	V
Tristate current		I_{OZ}	–100	—	100	mA
Input capacitance		C_{IN}	—	8	—	pF
Output capacitance		C_{OUT}	—	10	—	pF
ESD breakdown	(1)	V_{ESD}	1000	—	—	V

Notes (tables 6 and 7):

1. Specifications apply over recommended operating ranges.
2. Single-ended inputs
3. Differential inputs
4. $V_{REF} = -1300 \text{ mV}$
5. $R_{LOAD} = 50 \text{ ohms}$ to $V_{TT} = -2.0V$
6. Not tested; consistent with V_{OH} and V_{OL} tests

Table 8. AC Characteristics

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RXCK clock period	$T_{C(RXCK)}$	1.6	—	—	ns
MXHC clock period	$T_{C(MXHC)}$	1.6	—	—	ns
TXCK clock period	$T_{C(TXCK)}$	1.6	—	—	ns
MXCK clock period	$T_{C(MXCK)}$	12.8	—	—	ns
DXCK clock period	$T_{C(DXCK)}$	12.8	—	—	ns
MXLRC clock period	$T_{C(MXTRC)}$	18.87	19.29	19.61	ns
DXRCK clock period	$T_{C(DXRCK)}$	4.80	19.29	—	ns
RXCK clock duty cycle	$T_{DC(RXCK)}$	30	50	70	%
MXHC clock duty cycle	$T_{DC(MXHC)}$	30	50	70	%
TXCK clock duty cycle	$T_{DC(TXCK)}$	40	50	60	%
MXCK clock duty cycle	$T_{DC(MXCK)}$	40	50	60	%
DXCK clock duty cycle	$T_{DC(DXCK)}$	40	50	60	%
MXLRC clock duty cycle	$T_{DC(MXIRC)}$	30	50	70	%
DXRCK clock duty cycle	$T_{DC(DXRCK)}$	40	50	60	%
High-speed rise/fall time ¹ (more than 79 MHz)	$T_{H(R/F)}$	—	—	320	ps
Low-speed rise/fall time ¹ (less than 79 MHz)	$T_{L(R/F)}$	—	—	2.56	ns
CNTL(2:0) Setup Time to CNTL(3)	$T_{S(CNTL)}$	5500	—	—	ps
CNTL(2:0) Hold Time to CNTL(3)	$T_{H(CNTL)}$	2000	—	—	ps
RXDT setup time to RXCK	$T_{S(RXDT)}$	225	—	—	ps
RXDT hold time to RXCK	$T_{H(RXDT)}$	125	—	—	ps
OOF rising edge before A1 changes to A2	$T_{(OOFH)}$	51.44	—	—	ns
OOF pulse width	$T_{(OOFPW)}$	12.86	—	—	ns
DXSYNC rising edge from parallel data output change from A1 to A2	$T_{(DSYNC)}$	—	25.72	—	ns
DXSYNC pulse width	$T_{(DXSYNCPW)}$	12.86	—	—	ns
DXCK falling edge to valid parallel data output	$T_{P(DXDT)}$	$T_{C(RXCK)}$	$T_{C(RXCK)} + 0.5$	$T_{C(RSCK)} + 1.5$	ns
MXDT(0:7) setup time to MXCK	$T_{S(MXDT)}$	4500	—	—	ps
MXDT(0:7) hold time to MXCK	$T_{H(MXDT)}$	-2000	—	—	ps
TXCK falling edge to TXDT	$T_{P(TXDT)}$	—	—	500	ps

Notes: 1. 20% to 80% of min V_{OH} and max V_{OL} levels.

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Figure 8. Input Timing

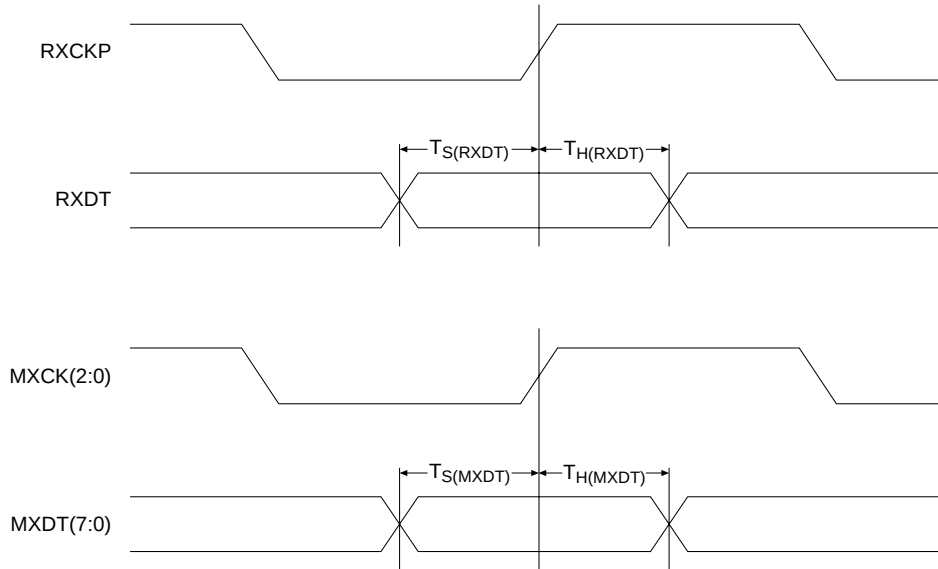


Figure 9. Output Timing

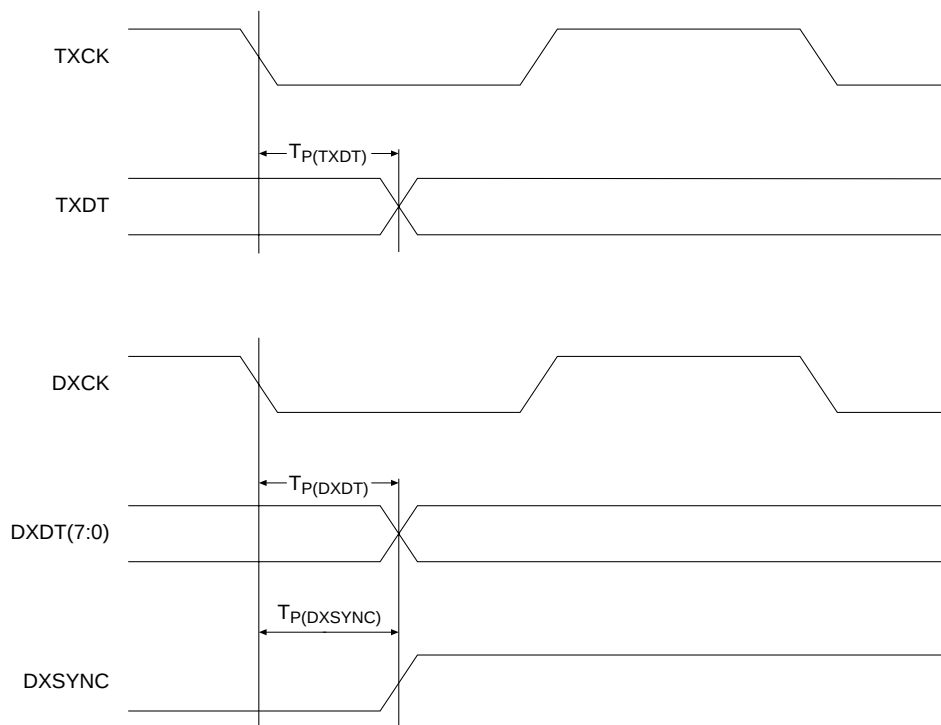


Figure 10. Multiplexer Timing

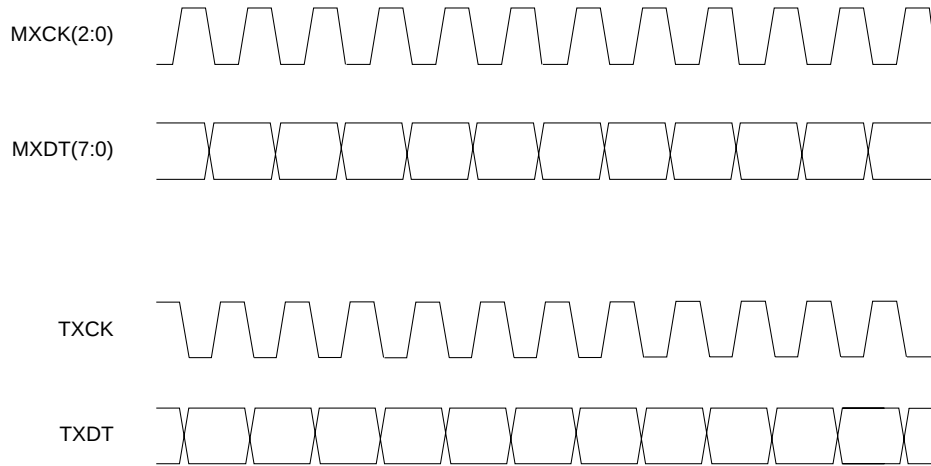
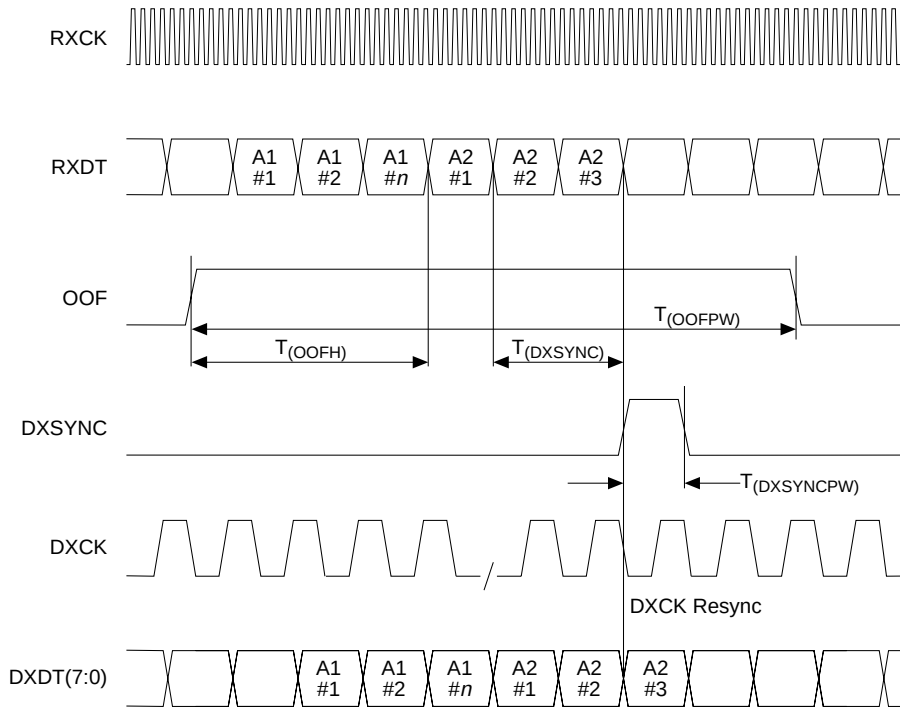


Figure 11. Demultiplexer Timing



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SONET/SDH Considerations

Jitter Tolerance

This measurement does not apply to the TQ8101C, since data is transmitted from the input parallel bus relative to a TQ8101C-generated clock output (MXCK[2:0]). The user must meet setup and hold time requirements in order to ensure that data tracking is maintained.

Jitter Generation

By exploiting material characteristics, fully differential SCFL logic, and on-chip reactive elements, the TQ8101C typically has a jitter generation of 0.008 UI RMS (where 1 UI is 1/622.08E06) using recommended loop filter component values.

Ordering Information

TQ8101-M *SONET/SDH MDFP*

*Evaluation Board Please contact a TriQuint representative or the factory
for availability and pricing.*

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