N- and P-Channel Quad Power MOSFET Arrays

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max) Q1 + Q2 or Q3 + Q4	$V_{GS(th)}$ (max)		Order Number / Package		
		N-Channel	P-Channel	14-Pin P-Dip	14-Pin C-Dip	20 Terminal LCC Quad
40V	3Ω	2.0V	3.0V	VQ3001N6	VQ3001N7	VQ3001NF
40V	3Ω	1.6V	2.4V	TQ3001N6	TQ3001N7	TQ3001NF
20V	3Ω	2.0V	3.0V	VQ7254N6	VQ7254N7	—

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices
- ☐ Low Threshold version available

Applications

- ☐ Bubble/Memory drivers
- ☐ General purpose complementary drivers and switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Thermal Characteristics

Package	I_D (continuous)*		I_D (pulsed)*		Power Dissipation	θ_{ja}	θ_{jc}	I_{DR}		I_{DRM}*	
	N	P	N	P	@ T_C = 25°C	°C/W	°C/W	N	P	N	P
Ceramic Dip	850mA	-600mA	3.0A	3.0A	2.0†	—	62.5	850mA	-600mA	3.0A	-3.0A
Plastic Dip	640mA	-450mA	3.0A	3.0A	1.5†	—	83.3	640mA	-450mA	3.0A	-3.0A
20 Terminal LCC	410mA	-300mA	3.0A	3.0A	1.0†	—	125.0	410mA	-300mA	3.0A	-3.0A

*Total for 4 die. †Each die.

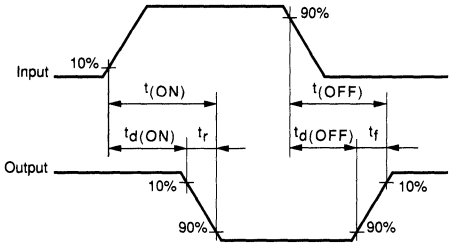
Electrical Characteristics (@ 25°C unless otherwise specified)

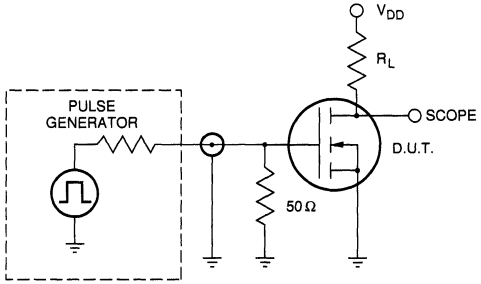
(Notes 1, 2, and 3)

Symbol	Parameter		N-Channel Min	N-Channel Max	P-Channel Min	P-Channel Max	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TQ3001 VQ3001	40		-40		V	V_{GS} = 0, I_D = 10μA
		VQ7254	20		-20			
$V_{GS(th)}$	Gate Threshold Voltage	VQ3001 VQ7254	0.8	2.0	-0.8	-3.0	V	V_{GS} = V_{DS}, I_D = 1mA T_A = 25°C
		TQ3001	0.6	1.6	-1.0	-2.4	V	
		VQ3001 VQ7254	0.5		-0.65		V	V_{GS} = V_{DS}, I_D = 1mA T_A = 85°C
I_{GSS}	Gate Body Leakage			100		-100	nA	V_{GS} =16V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current			0.5		-0.5	μA	V_{GS} = 0, V_{DS} = 0.8 Min Rating
$V_{DS(ON)}$	Total Static Drain-to-Source ON-State Resistance Q_1 + Q_2 or Q_3 + Q_4	VQ3001 TQ3001		3.0		3.0	V	V_{GS} = 11.4V, I_D = 1A
		VQ7254	2.0	3.0	2.0	3.0		
$R_{DS(ON)}$	Total Static Drain-to-Source ON-State Resistance Q_1 + Q_2 or Q_3 + Q_4	TQ3001		5.0		5.0	Ω	V_{GS} = 5.0V, I_D = 250mA
		VQ3001 TQ3001		3.0		3.0		V_{GS} = 11.4V, I_D = 1A
		VQ7254	2.0	3.0	2.0	3.0		
G_{FS}	Forward Transconductance		200		200		m℧	V_{DS} ≥ 2$V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance			175		195	pF	V_{GS} = 0, V_{DS} = 12V f = 1Mz
C_{OSS}	Output Capacitance			95		100		
C_{RSS}	Reverse Transfer Capacitance			25		60		
$t_{d(ON)}$	Turn-ON Delay Time			30		30	ns	V_{DD} = 17V, R_S = 50Ω
$t_{d(OFF)}$	Turn-OFF Delay Time			30		30	ns	R_L = 15Ω
V_{SD}	Forward ON Voltage	VQ7254		-0.75		0.75	V	V_{GS} = 0, I_F = 50mA
				-1.20		1.2		V_{GS} = 0, I_F = 1A

Note 1: All D.C. parameters 100% tested (pulse test: 300μs pulse, 2% duty cycle).
Note 2: All A.C. parameters sample tested.
Note 3: Refer to device types TN06L and TP06L for characteristic curves.

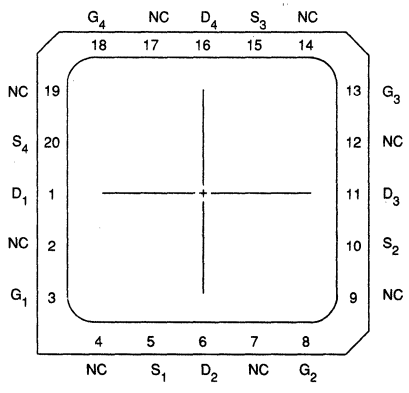
Switching Waveforms and Test Circuit





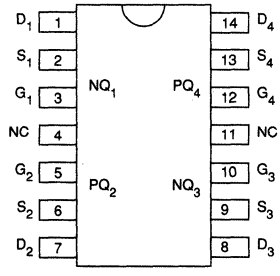
FET polarity in test circuit is N-channel only.

Pin Configuration and Schematic



top view

20-pin Ceramic LCC



top view

14-pin DIP