Automotive Grade 5-V General Purpose Analog Switch

Features

- AEC Q100: Automotive Grade 1
- Analog Switch Voltage: 1.8 V, 2.5 V, 3.3 V, 5 V
- Low ON-State Resistance:
  - typical 75 Ω at Vs = 5 V
  - typical 120Ω at Vs = 3.3 V
  - typical 650 Ω at Vs = 1.8 V
- Bandwidth: 250 MHz
- Fast Switching Times: t_{ON} = 22 ns, t_{OFF} = 8 ns
- Break-Before-Make Switching
- Operation Temperature Range: –40°C to 125°C
- TPW3188Q – P2P with: – Industry version TPW4051

Applications

- Industry Control Systems
- Battery-Powered Systems
- Audio Signal Routing
- Instrumentation

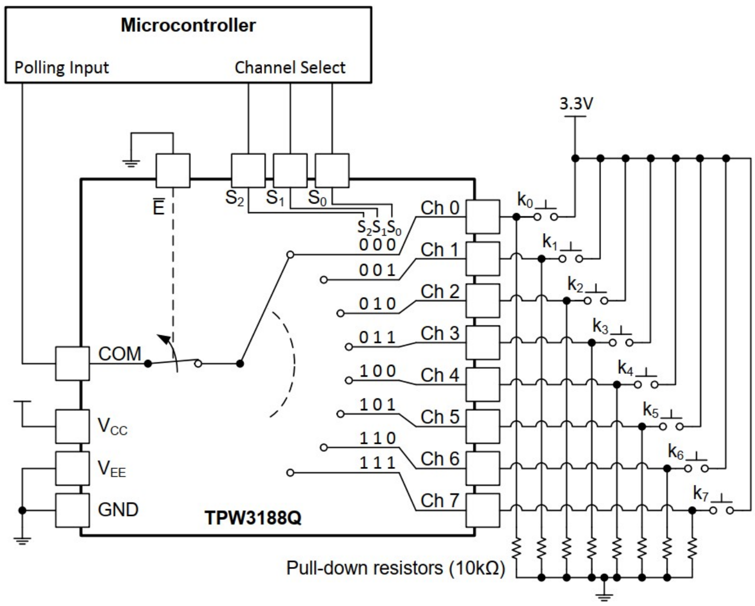
Description

The TPW3188Q is a single-pole octal-throw analog switch (SP8T) suitable for analog or digital 8:1 multiplexer/ demultiplexer applications. The switch features three digital select inputs (S0, S1, and S2), eight independent inputs/outputs (An), a common input/output (A), and a digital enable input (/E). When /E is HIGH, the switches are turned off.

The device is designed on an enhanced process that provides lower power dissipation and gives high switching speeds. These devices can operate equally well as either multiplexers or de-multiplexers and have an input range that extends to the supplies. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels.

The TPW3188Q is available in the TSSOP-16 package and is characterized from −40°C to +125°C.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2022-11-28	Rev. Pre.0	Initial version.
2023-05-28	Rev. A.0	Released version.
2023-07-10	Rev. A.1	• Added I_{GND}, I_{OK}, P_{tot} parameters in the table of Absolute Maximum Ratings. • Added LU parameter in the table of ESD, Electrostatic Discharge Protection.

Pin Configuration and Functions

TPW3188Q
TSSOP16 Package
Top View

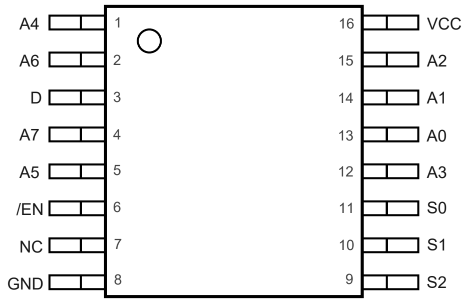


Table 1. Pin Functions: TPW3188Q

Pin No.	Name	I/O	Description
1	A4	I/O	Channel 4 input or output
2	A6	I/O	Channel 6 input or output
3	D	I/O	Common input or output
4	A7	I/O	Channel 7 input or output
5	A5	I/O	Channel 5 input or output
6	/E	I	Enable switches, active low
7	NC		Not Connected
8	GND		Ground
9	S2	I	Control Input
10	S1	I	Control Input
11	S0	I	Control Input
12	A3	I/O	Channel 3 input or output
13	A0	I/O	Channel 0 input or output
14	A1	I/O	Channel 1 input or output
15	A2	I/O	Channel 2 input or output
16	V_{CC}		Positive Power Input

Table 2. Functional Table

/E, Enable	S2	S1	S0	ON Channel
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

(1) X = Don’t care

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	6	V
V_{SD}	Analog Switch Voltage, VS=Voltage of Ax, VD=Voltage of D	–0.5	V_{CC} +0.5	V
I_{CC}	Analog Switch Current	−25	+25	mA
I_{CCI}	Digital Input Current, /E, S2, S1, S0	−30	+30	mA
V_{DI}	Digital Input Voltage, /E, S2, S1, S0	GND	V_{CC} +0.5	V
I_{GND}	Continuous Current through GND	−100	+100	mA
I_{OK}	Current per input into source or drain pins when singal voltage exceeds recommended operating voltage	-50	0	mA
P_{tot}	Total Power Dissipation		500	mW
T_C	Maximum Junction Temperature		150	°C
T_S	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1	kV
LU	Latch up	LU, per JESD78, All Pin (3)	±100	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Test at the temperature of 25℃.

Recommended Operating Conditions (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, V_{CC}	1.65	5.5	V
V_S or V_D	Analog Switch Voltage, VS = Voltage of Ax, VD = Voltage of D	0	V_{CC}	
V_I	Select Input Voltage	0	V_{CC}	V
$T_{R/F}$	Input Transition Rise and Fall Rate		100	ns/V
V_{IO}	Switch I/O Port Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	125	°C

(1) Input select must be held HIGH or LOW and it shouldn' t float.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP16	150	70	°C/W

Electrical Characteristics

All test conditions: T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Test Conditions	VCC	Min	Typ	Max	Units
Analog Switch							
R_{ON}	On-state Switch Resistance	V_S = 0 V to V_{CC} I_{SD} = 0.5 mA	1.8 V		650	2100	Ω
			2.5 V		230 (1)	900 (1)	
			3.3 V		120	370	
			5 V		75 (1)	270 (1)	
ΔR_{ON}	On-state Switch Resistance Matching between Inputs	V_S = V_{CC} / 2 I_{SD} = 0.5 mA	1.8 V		10	45	Ω
			2.5 V		3 (1)	22 (1)	
			3.3 V		2	15	
			5 V		1 (1)	14 (1)	
$I_{S(OFF)}$	Source off State Leakage Current	Switch Off V_D = 0.8 x V_{CC} / 0.2 x V_{CC} V_S = 0.2 x V_{CC} / 0.8 x V_{CC}	1.8 V	−800	±1	800	nA
			2.5 V	−800	±1	800	
			3.3 V	−800	±1	800	
			5 V	−800	±1	800	
$I_{D(OFF)}$	Drain off-State Leakage Current (Common Drain Pin)	Switch Off V_D = 0.8 x V_{CC} / 0.2 x V_{CC} V_S = 0.2 x V_{CC} / 0.8 x V_{CC}	1.8 V	−800	±1	800	nA
			2.5 V	−800	±1	800	
			3.3 V	−800	±1	800	
			5 V	−800	±1	800	
$I_{D(ON)}$	Channel Onstate	Switch On	1.8 V	−800	±1	800	nA
$I_{S(ON)}$	Leakage Current	V_D = V_S = 0.8 x V_{CC} or V_D = V_S = 0.2 x V_{CC}	2.5 V	−800	±1	800	
			3.3 V	−800	±1	800	
			5 V	−800	±1	800	
C_{SOFF} (1)	Source off Capacitance (1)	V_S = V_{CC} / 2 f = 1 MHz	1.8 V		4.5	14	pF
			2.5 V		4.5	14	
			3.3 V		4	14	
			5 V		5	14	
C_{DOFF} (1)	Drain off Capacitance (1)	V_S = V_{CC} / 2 f = 1 MHz	1.8 V		15	37	pF
			2.5 V		15	37	
			3.3 V		14	37	
			5 V		14	37	
C_{SON} (1)	On Capacitance (1)	V_S = V_{CC} / 2 f = 1 MHz	1.8 V		20	40	pF
C_{DON} (1)			2.5 V		20	40	
			3.3 V		20	40	
			5 V		20	40	

(1) The data is based on bench test and design simulation.

Electrical Characteristics (Continued)

All test conditions: T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Test Conditions	VCC	Min	Typ	Max	Units
Power Supply							
I_{CC}	VCC Supply Current	Logic inputs = 0 V or V_{CC}	1.8 V			1.2	uA
			2.5 V			1.5	
			3.3 V			2	
			5 V			3	
Logic Inputs							
V_{IH}	Input Logic High		1.8 V	1.05		5.5	V
			2.5 V	1.12		5.5	
			3.3 V	1.18		5.5	
			5V	1.25		5.5	
V_{IL}	Input Logic Low		1.8V	0		0.6	V
			2.5 V	0		0.65	
			3.3 V	0		0.7	
			5 V	0		0.75	
I_{IH}	Logic High Input Leakage Current	V_{LOGIC} = 1.8 V or V_{CC}	all			1	uA
I_{IL}	Logic Low Input Leakage Current	V_{LOGIC} = 0 V	all	−1			uA
C_{IN} (1)	Logic Input Capacitance (1)	V_{LOGIC} = 0 V, 1.8 V, V_{CC} f = 1 MHz	all		2		pF

(1) Typ data is based on bench test and design simulation.

Electrical Characteristics (Continued)

All test conditions: T_A = −40°C to 125°C, unless otherwise noted.

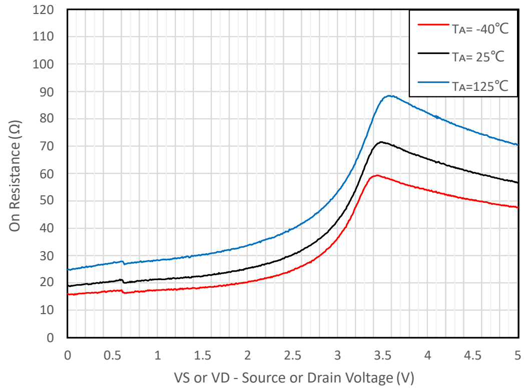
Parameter		Test Conditions	VCC	Min	Typ	Max	Units
Dynamic Characteristics							
Q_{INJ} (1)	Charge Injection (1)	$V_S = V_{CC}$ / 2 RS = 0 Ω, C_L = 100 pF	1.8 V		8		pC
			2.5 V		8		
			3.3 V		10		
			5 V		15		
O_{ISO} (1)	OFF-Isolation (1)	$V_{BIAS} = V_{CC}$ / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 100 kHz	1.8 V		-110		dB
			2.5 V		-110		
			3.3 V		-110		
			5 V		-110		
O_{ISO} (1)	OFF-Isolation (1)	$V_{BIAS} = V_{CC}$ / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	1.8 V		-90		dB
			2.5 V		-90		
			3.3 V		-90		
			5 V		-90		
X_{TALK} (1)	Crosstalk (1)	$V_{BIAS} = V_{CC}$ / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 100 kHz	1.8 V		-110		dB
			2.5 V		-110		
			3.3 V		-110		
			5 V		-110		
X_{TALK} (1)	Crosstalk (1)	$V_{BIAS} = V_{CC}$ / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF f = 1 MHz	1.8 V		-90		dB
			2.5 V		-90		
			3.3 V		-90		
			5 V		-90		
BW (1)	Bandwidth (1)	$V_{BIAS} = V_{CC}$ / 2 V_S = 200 mVpp R_L = 50 Ω, C_L = 5 pF	1.8 V		250		MHZ
			2.5V		250		
			3.3 V		250		
			5 V		250		
Switching Characteristics (Timing Characteristics)							
t_{PD}	Propagation Delay	C_L = 50 pF Sx to D, D to Sx	1.8 V		15	30	ns
			2.5 V		8	20	
			3.3 V		5	15	
			5 V		4	10	
		C_L = 15 pF (1)	5 V		1.5	5	
t_{TRAN}	Transition-time between Inputs	R_L = 10 kΩ, C_L = 50 pF Ax to D, Ax to Sx	1.8 V		44	103	ns
			2.5 V		30	67	
		R_L = 10 kΩ, C_L = 50 pF	3.3 V		23	54	

Parameter		Test Conditions	VCC	Min	Typ	Max	Units
	Transition-time between Inputs	Ax to D, Ax to Sx	5 V		18	46	
		R_L = 10 kΩ, C_L = 15 pF (1)	5 V		15	43	
$t_{ON(EN)}$	Turnon-time from Enable	R_L = 10 kΩ, C_L = 50 pF EN to D, EN to Sx	1.8 V		39	75	ns
			2.5 V		30	50	
			3.3 V		26	42	
			5 V		24	37	
		R_L = 10 kΩ, C_L = 15 pF (1)	5 V		22	35	
$t_{OFF(EN)}$	Turnoff Time from Enable	R_L = 10 kΩ, C_L = 50 pF EN to D, EN to Sx	1.8 V		58	85	ns
			2.5 V		21	72	
			3.3 V		15	70	
			5 V		11	45	
		R_L = 10 kΩ, C_L = 15 pF (1)	5		8	20	
t_{BBM} (1)	Break before make time (1)	R_L = 10 kΩ, C_L = 15 pF Sx to D, D to Sx	1.8 V	1	16		ns
			2.5 V	1	22		
			3.3 V	1	24		
			5 V	1	33		

(1) The data is based on bench test and design simulation.

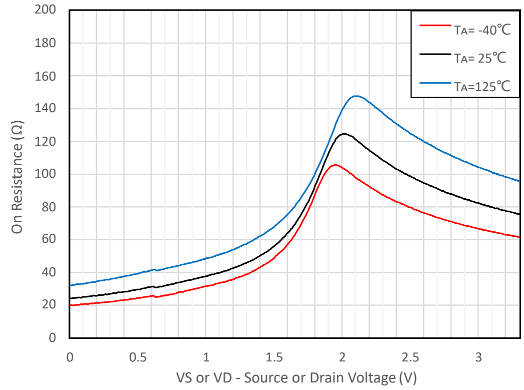
Typical Performance Characteristics

All test conditions: T_A= 25°C, VCC = 5 V, unless otherwise noted.



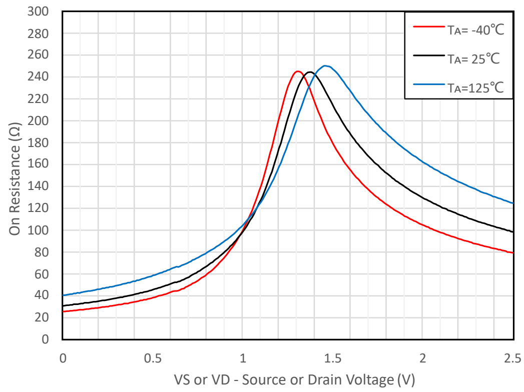
V_{CC} = 5 V

Figure 1. On-Resistance vs Temperature



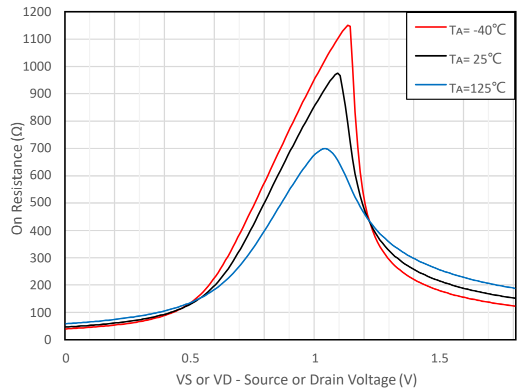
V_{CC} = 3.3 V

Figure 2. On-Resistance vs Temperature



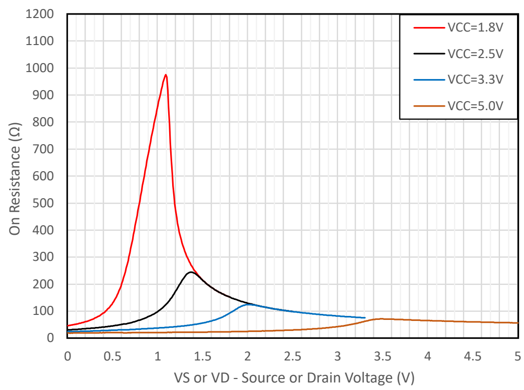
V_{CC} = 2.5 V

Figure 3. On-Resistance vs Temperature



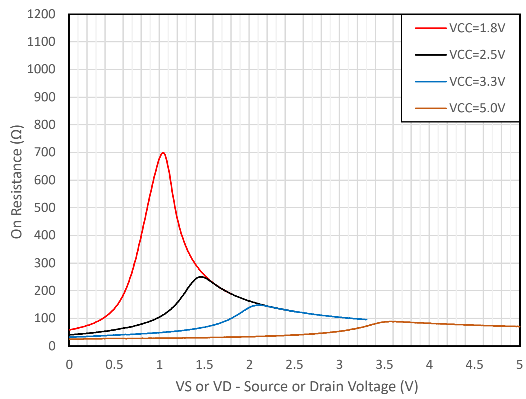
V_{CC} = 1.8 V

Figure 4. On-Resistance vs Temperature



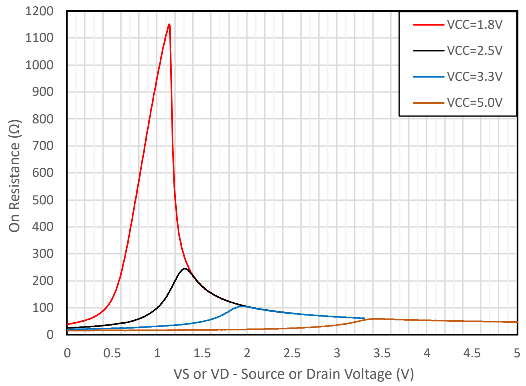
T_A = 25°C

Figure 5. On-Resistance vs Source or Drain Voltage



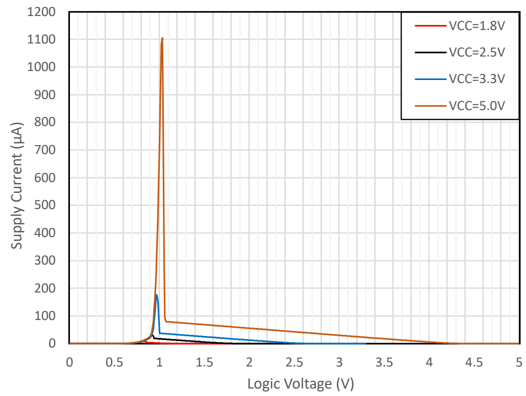
T_A = 125°C

Figure 6. On-Resistance vs Source or Drain Voltage



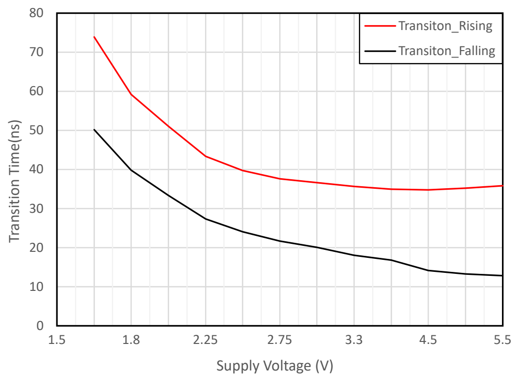
T_A = −45°C

Figure 7. On-Resistance vs Source or Drain Voltage



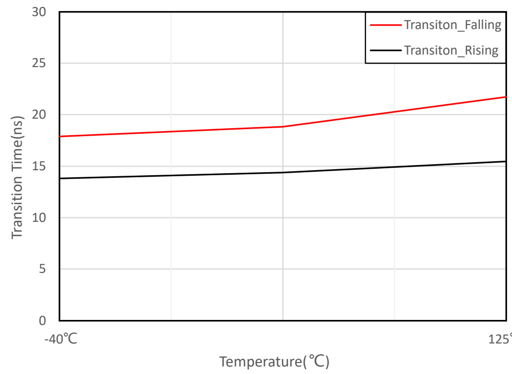
T_A = 25°C

Figure 8. Supply Current vs Logic Voltage



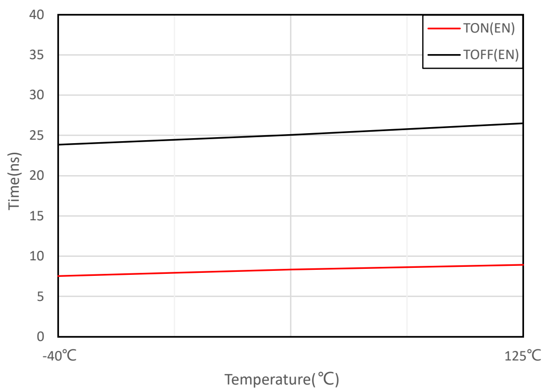
T_A = 25°C

Figure 9. $T_{TRANSITION}$ vs Supply Voltage



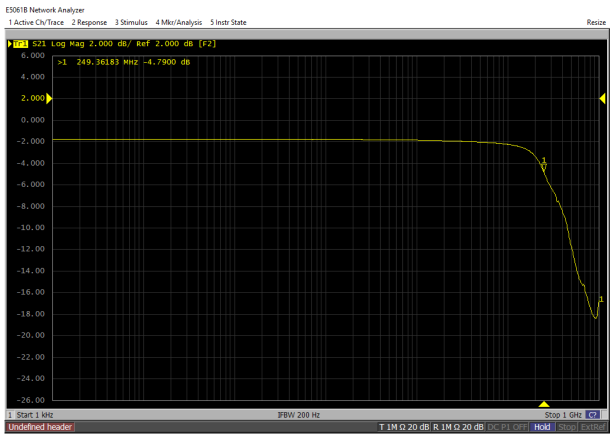
VCC = 5 V

Figure 10. $T_{TRANSITION}$ vs Temperature



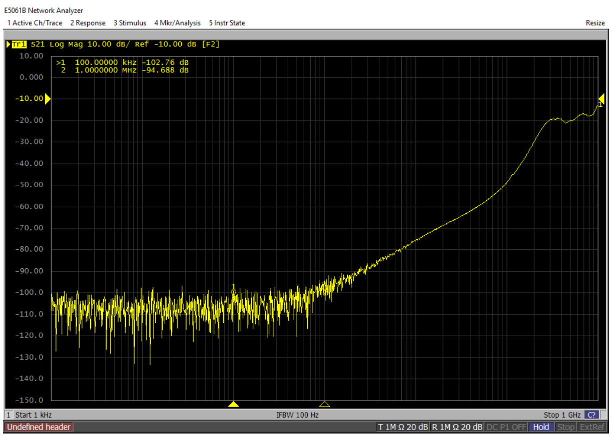
VCC = 5 V

Figure 11. $T_{ON(EN)}$ and $T_{OFF(EN)}$ vs Temperature



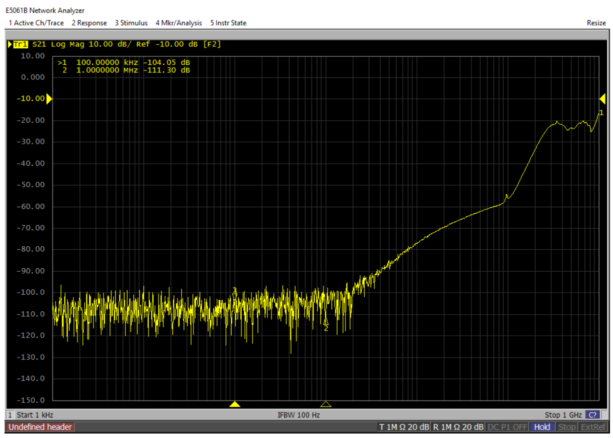
T_A = 25°C; VCC = 5 V

Figure 12. On Response vs Frequency



T_A = 25°C; VCC = 5 V

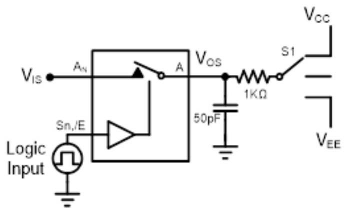
Figure 13. Xtalks vs Frequency



T_A = 25°C; VCC = 5 V

Figure 14. Off-Isolation vs Frequency

Test Circuits and Waveforms



Parameter	Vis	S1 Position
t_{PHL} ,t_{PLH}	Pulse	Open
t_{PZH} ,t_{PHZ}	V_{CC}	V_{EE}
t_{PZL} ,t_{PLZ}	V_{EE}	V_{CC}

t_{ON}: t_{PZH} or t_{PZL}

t_{OFF}: t_{PHZ} or t_{PLZ}

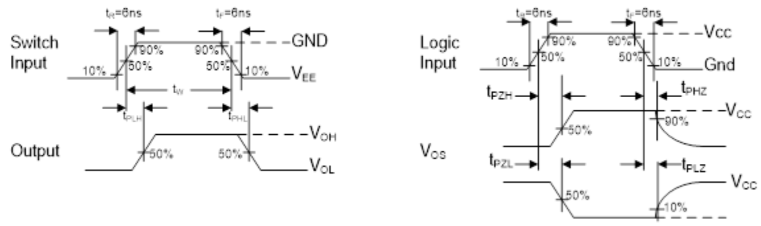


Figure 15. AC Test Circuit and Test Waveforms

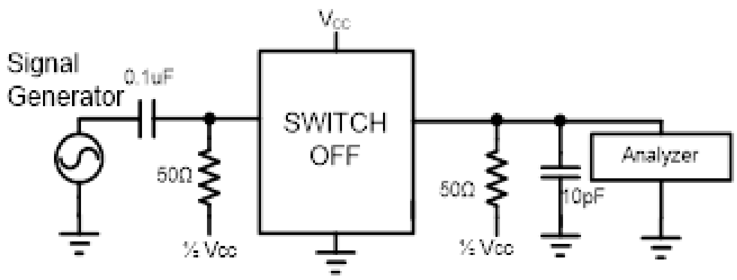


Figure 16. Off Isolation

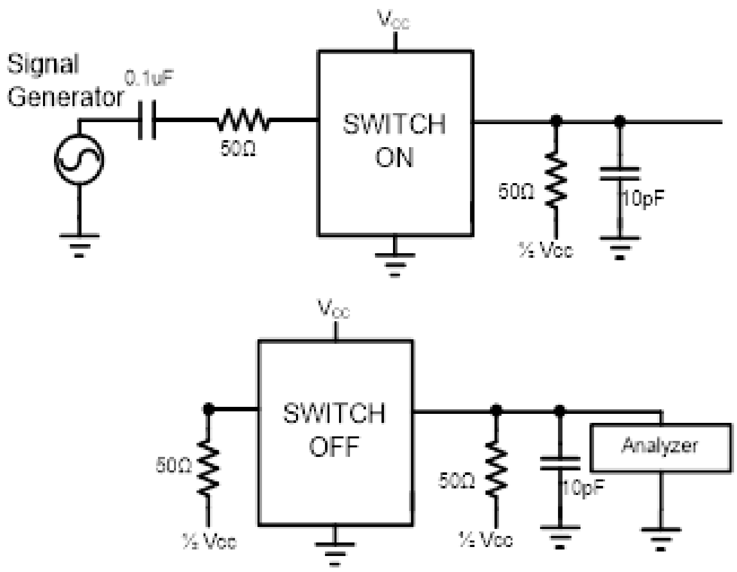


Figure 17. Crosstalk

Detailed Description

Overview

The TPW3188Q is a single-pole octal-throw analog switch (SP8T) suitable for analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S0, S1, and S2), eight independent inputs/outputs (An), a common input/output (A), and a digital enable input (/E). When /E is HIGH, the switches are turned off.

Functional Block Diagram

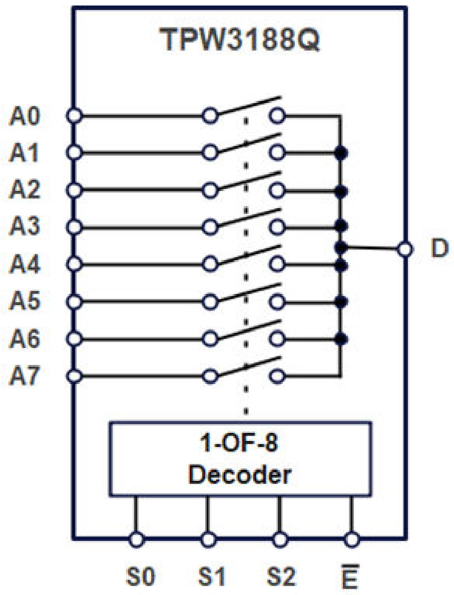


Figure 18. Functional Block Diagram

Feature Description

The TPW3188Q is the automotive analog switch qualified as AEC Q100 - automotive grade 1. The VCC voltage range is 1.8 V, 2.5 V, 3.3 V, and 5 V. The Ron resistance is very low, such as typical 75 Ω at Vs = 5 V, typical 120 Ω at Vs = 3.3 V, typical 650 Ω at Vs = 1.8 V. The TPW3188Q bandwidth is 250 MHz, it will be in break state before the switch operation. The switching time is very fast, which is 22 ns in the ON state, and 8 ns in the OFF time. The TPW3188Q is available in the TSSOP16 package and is characterized from −40°C to +125°C.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPW3188Q line of multiplexers and demultiplexers can be used for a wide variety of applications.

A 0.1-μF bypass capacitor on V_{CC} is recommended to prevent power disturbance.

The current per input into source or drain pin when input signal voltage exceeds V_{CC}

As the input signal voltage is higher than the V_{CC} voltage, the current per input into source or drain will be very large and close to 50 mA, which may damage the device. Therefore, the input signal is not recommended to exceed V_{CC}.

Input signal voltage should be less than V_{CC} + 0.5 V

The TPW3188Q has an internal ESD diode to the GND pin, which will be around 20 mA as the diode is turned on. The input signal voltage should NOT be lower than GND-0.5V. A series of resistor is suggested to be added to limit the current. The device requires the input signal voltage be less than V_{CC}+ 0.5 V. Otherwise, the current will increase in exponential magnitude as the input signal voltage raises higher than V_{CC}+ 0.5 V. Thus, the function cannot be guaranteed in the application and the device may be damaged.

In some special cases, if the input signal voltage is over than VCC as the channel is in OFF status, the voltage will be clamped to VCC+0.7V approximately. The input current may be as large as tens of mA and will introduce coupling to other channels, so the device is not recommended in this case.

Typical Application

One application of the TPT3188Q device is used in conjunction with a microcontroller to poll a keypad. Figure 19 shows the basic schematic for such a polling system.

The microcontroller uses channel-select pins to cycle through different channels while reading the input to see if a user is pressing any of the keys. This is a very robust setup that allows for simultaneous key presses with very little power consumption. It also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must frequently scan the keys for a press.

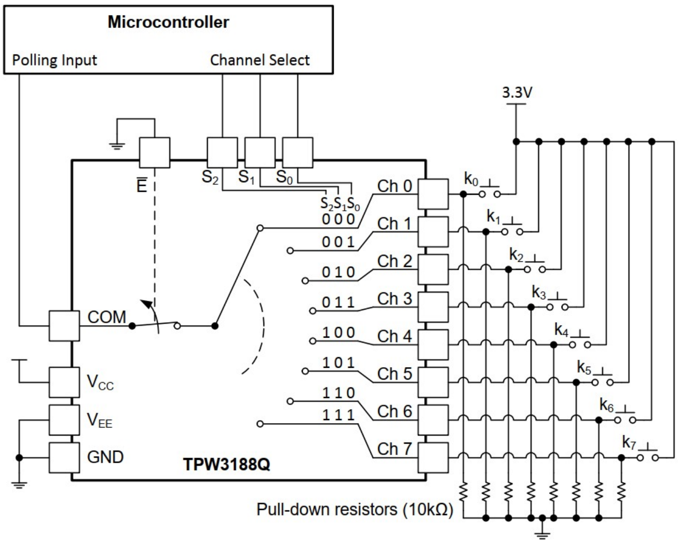


Figure 19. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 20 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

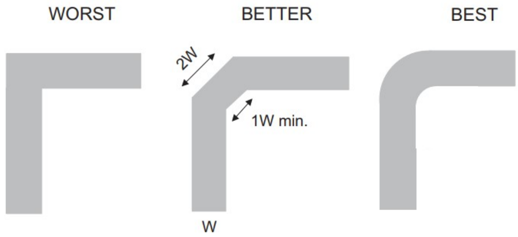


Figure 20. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 21 illustrates an example of a PCB layout with the TPW3188Q. Some key considerations are:

- Decouple the VDD pin with a 0.1-μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the VDD supply.
- Decouple the VDD pin with a 0.1-μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the VDD supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

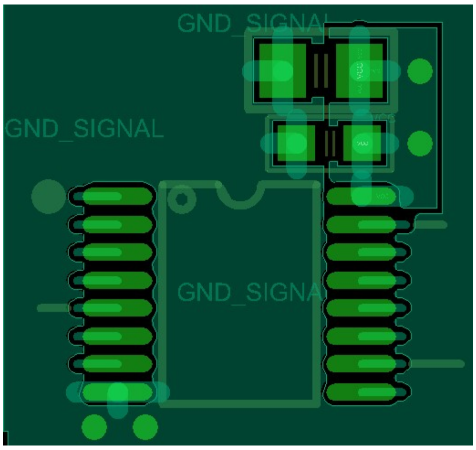
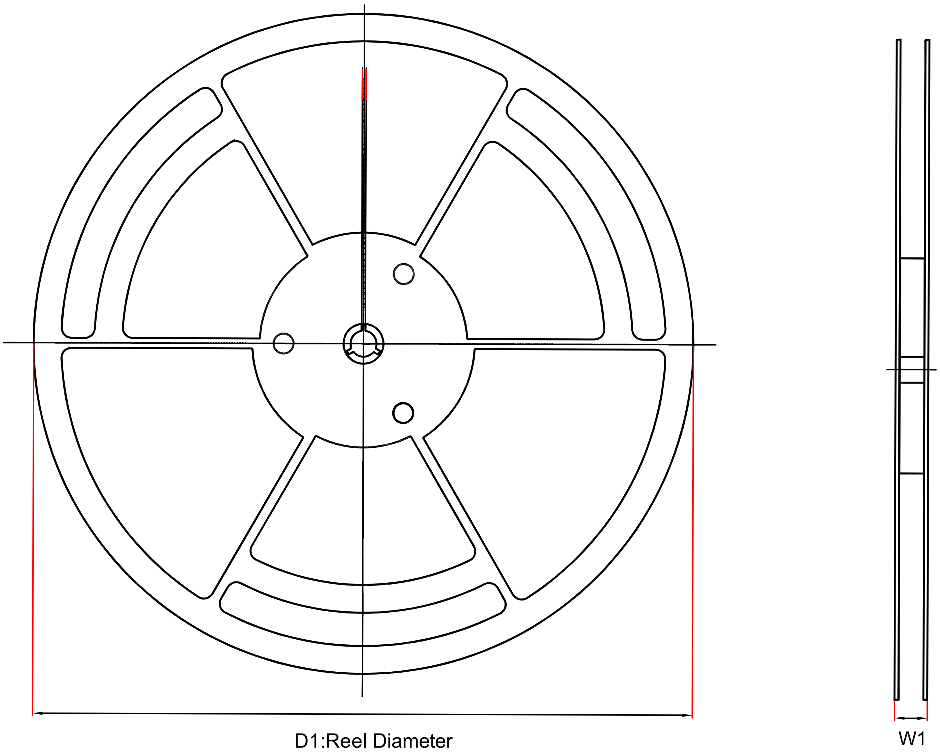
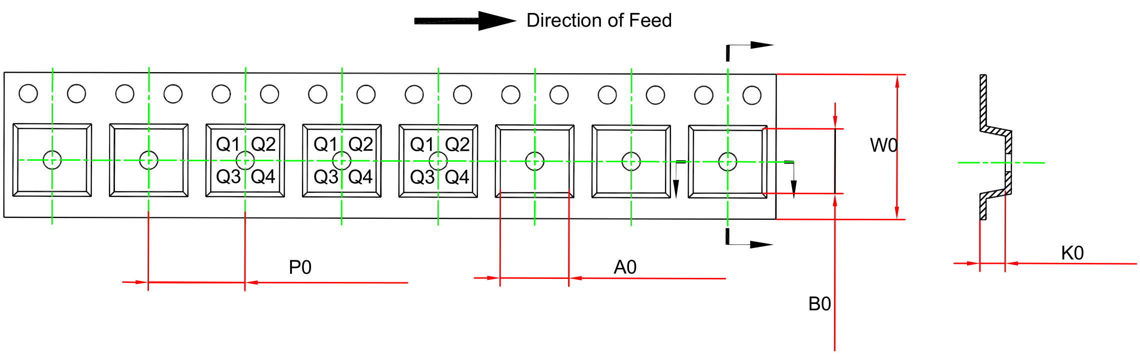


Figure 21. TPW3188Q Layout Example

Tape and Reel Information



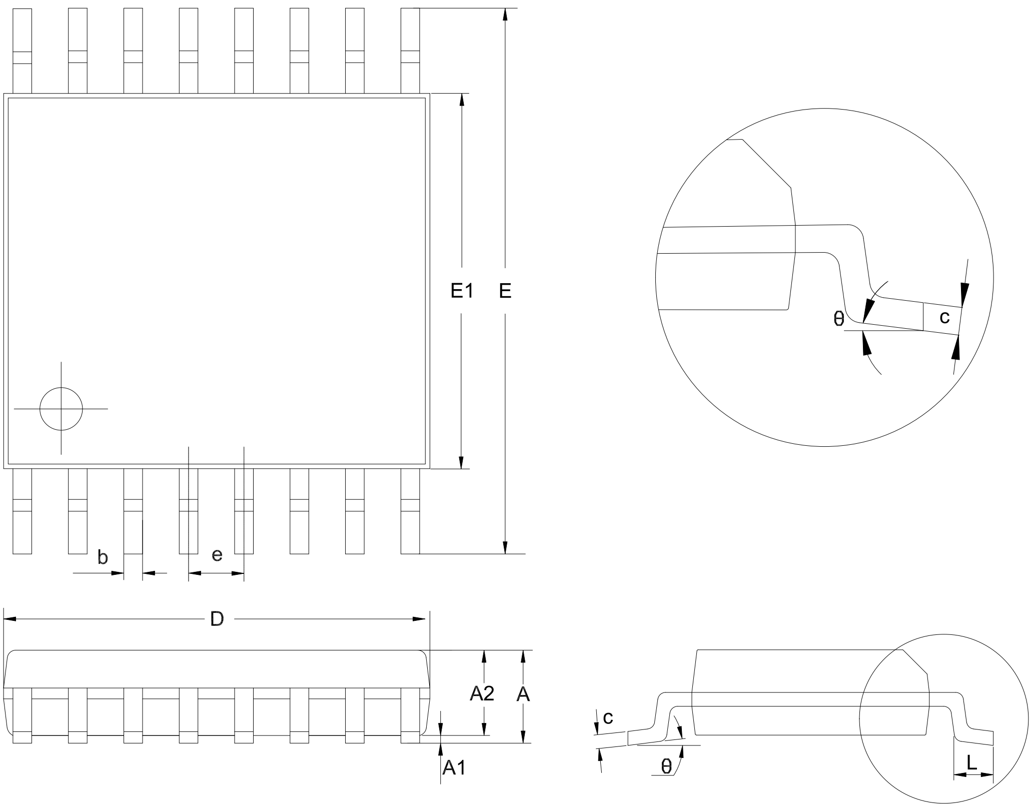


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPW3188Q-TS3R-S	TSSOP-16	330.0	6.8	1.2	12.0	17.6	5.4	8.0	Q1

Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPW3188Q-TS3R-S	−40 to 125°C	TSSOP16	3188Q	MSL1	Tape and Reel, 3000	Green

(1) MSL will be updated depending on the qualification report.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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