Features

- **Precision low voltage monitoring**
- **200 ms (typical) reset timeout**
- **Manual reset input**
- **Reset output stage**
- **Open Drain Active-low output (TPV821)**
- **Low power consumption: 2.2 μA**
- **Guaranteed reset output valid to VCC = 1 V**
- **Power supply glitch immunity**
- **Specified from −40°C to +125°C**
- **5-lead SOT-23-5 package and 4-lead SOT-143 package**

Applications

- **Microprocessor systems**
- **Computers**
- **Controllers**
- **Intelligent instruments**
- **Portable equipment**

Description

The TPV821 is a supervisory circuit that monitors power supply voltage levels and provides a power-on reset signal.

A reset signal can also be asserted by an external manual reset input.

The reset periods are fixed at 200 ms (typical).

The TPV821 is available in a 5-lead SOT-23-5 package and 4-lead SOT-143 package. And typically consumes only 2.2 μA, suitable for use in low power, portable applications.

Function block diagram

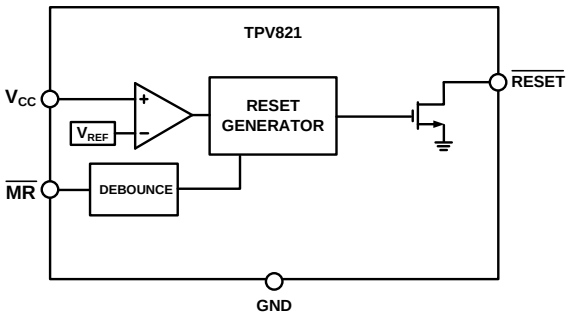

Figure 1.

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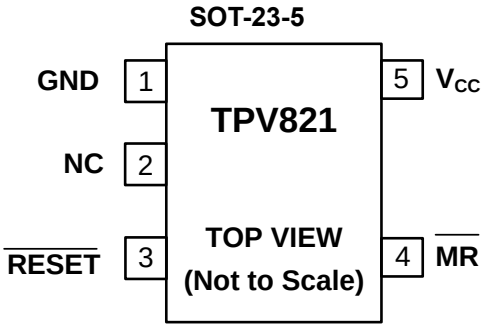
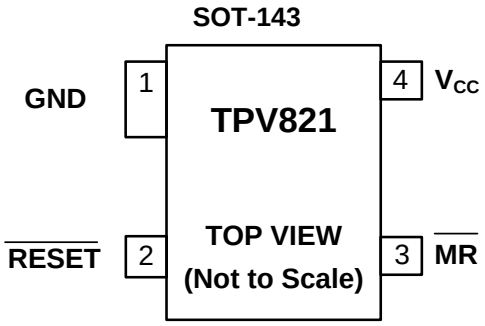
Revision History

Table 1.

Date	Revision	Notes
2019/7/7	1.0	Version 1.0

Pin Configuration and Functions





Name	PIN NO (SOT-23-5)	PIN NO (SOT-143)	Description
GND	1	1	Ground.
NC	2	NA	Not connected.
$\overline{\text{RESET}}$	3	2	TPV821: Active-Low Reset Open Drain Output Stage. Asserted whenever VCC is below the reset threshold, VTH.
$\overline{\text{MR}}$	4	3	Manual Reset Input. This is an active-low input, which, when forced low for at least 1 μs, generates a reset. It features a 50 kΩ internal pull-up.
VCC	5	5	Power Supply Voltage Being Monitored.

Order Information

Table 2.

Model Name	Order Number	Package	Transport Media, Quantity	Package Marking
TPV821	TPV821V-5TR	SOT-23-5	Tape and Reel, 3,000	V4V
TPV821	TPV821W-5TR	SOT-23-5	Tape and Reel, 3,000	V4W

TPV821	TPV821Y-5TR	SOT-23-5	Tape and Reel, 3,000	V4Y
TPV821	TPV821Z-5TR	SOT-23-5	Tape and Reel, 3,000	V4Z
TPV821	TPV821R-5TR	SOT-23-5	Tape and Reel, 3,000	V4R
TPV821	TPV821S-5TR	SOT-23-5	Tape and Reel, 3,000	V4S
TPV821	TPV821T-5TR	SOT-23-5	Tape and Reel, 3,000	V4T
TPV821	TPV821M-5TR	SOT-23-5	Tape and Reel, 3,000	V4M
TPV821	TPV821L-5TR	SOT-23-5	Tape and Reel, 3,000	V4L
TPV821	TPV821V-4LTR	SOT-143	Tape and Reel, 3,000	V4V
TPV821	TPV821W-4LTR	SOT-143	Tape and Reel, 3,000	V4W
TPV821	TPV821Y-4LTR	SOT-143	Tape and Reel, 3,000	V4Y
TPV821	TPV821Z-4LTR	SOT-143	Tape and Reel, 3,000	V4Z
TPV821	TPV821R-4LTR	SOT-143	Tape and Reel, 3,000	V4R
TPV821	TPV821S-4LTR	SOT-143	Tape and Reel, 3,000	V4S
TPV821	TPV821T-4LTR	SOT-143	Tape and Reel, 3,000	V4T
TPV821	TPV821M-4LTR	SOT-143	Tape and Reel, 3,000	V4M
TPV821	TPV821L-4LTR	SOT-143	Tape and Reel, 3,000	V4L

Absolute Maximum Ratings

Table 3

Parameter	Rating
VCC	−0.3 V to 6 V
Output Current	20 mA
Operating Temperature Range	−40°C to 125°C
Storage Temperature Range	−65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Table 4

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2000	V

Electrical Characteristics

VCC = 1.53 V to 5.5V; TA = –40°C to +125°C, unless otherwise noted.

Table 5

TPV821			SPEC		
Parameter	Test conditions	Unit	Min	Typ	Max
VCC Operating Voltage Range		V	1		5.5
Supply Current	VCC=1.8V	μA		2.2	10
	VCC=5V	μA		6	15
RESET THRESHOLD VOLTAGE					
TPV8xxV	Vth	V	1.51	1.58	1.63
TPV8xxW	Vth	V	1.62	1.67	1.71
TPV8xxY	Vth	V	2.12	2.19	2.25
TPV8xxZ	Vth	V	2.25	2.32	2.38
TPV8xxR	Vth	V	2.55	2.63	2.70
TPV8xxS	Vth	V	2.85	2.93	3.00
TPV8xxT	Vth	V	3.00	3.08	3.15
TPV8xxM	Vth	V	4.25	4.38	4.5
TPV8xxL	Vth	V	4.5	4.63	4.75
RESET THRESHOLD TEMPERATURE COEFFICIENT		ppm/°C		60	
RESET THRESHOLD HYSTERESIS		mV		2 × VTH	
VCC TO RESET DELAY	VTH − VCC = 100 mV	μs		20	
RESET TIMEOUT PERIOD		ms	140	200	280
RESET OUTPUT VOLTAGE VOL (Push-Pull)	VCC ≥ 1 V, ISINK = 50 μA	V			0.3
RESET OUTPUT VOLTAGE VOL (Push-Pull)	Vcc=Vth, Isink=1.2mA Vth≥2.63V	V			0.3
RESET OUTPUT VOLTAGE VOL (Push-Pull)	Vcc=Vth, Isink=3.2mA Vth≥4V	V			0.4
RESET OUTPUT VOLTAGE VOH (Push-Pull)	VCC ≥ 1.8 V, ISOURCE = 200 μA	V	0.8 × VCC		
RESET OUTPUT VOLTAGE VOH (Push-Pull)	VCC=Vth, ISOURCE = 500 μA Vth≥2.63V	V	0.8 × VCC		
RESET OUTPUT VOLTAGE VOH (Push-Pull)	VCC=Vth, ISOURCE = 800 μA Vth≥4V	V	VCC-1.5V		
MR Input Threshold VIL		V			0.3 × VCC
MR Input Threshold VIH		V	0.7 × VCC		
MR Input Pulse Width 1 μs		μS	1		
MR Glitch Rejection		nS		100	
MR to Reset Delay		nS		200	
MR Pull-Up Resistance		kΩ		50	

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

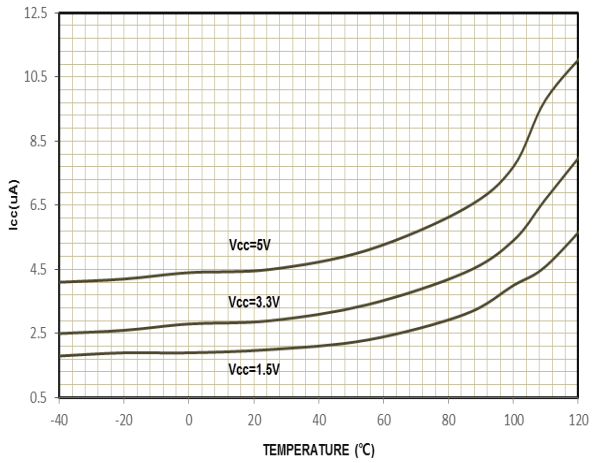


Figure 2. Supply Current vs. Temperature

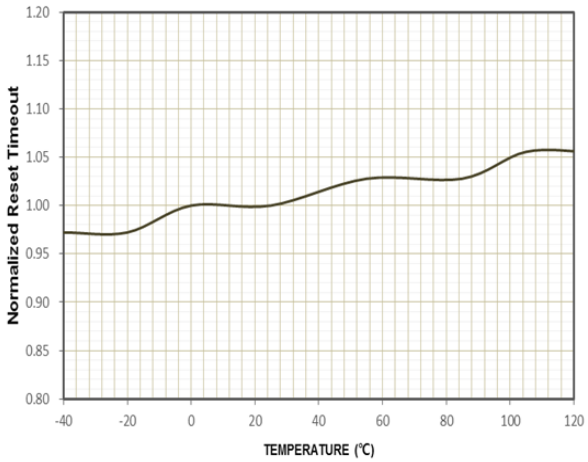


Figure 3. Normalized RESET Timeout Period vs. Temperature

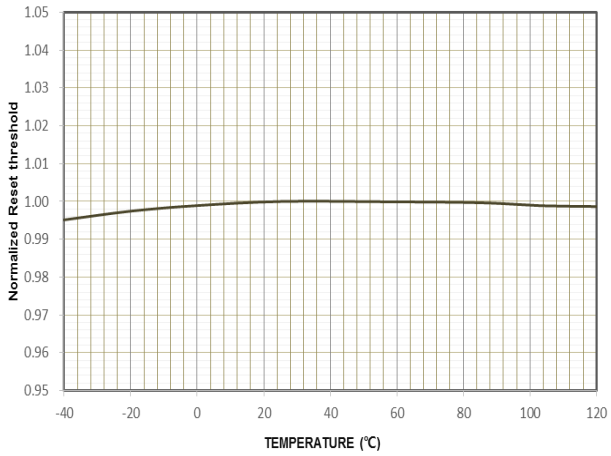


Figure 4. Normalized RESET Threshold vs. Temperature

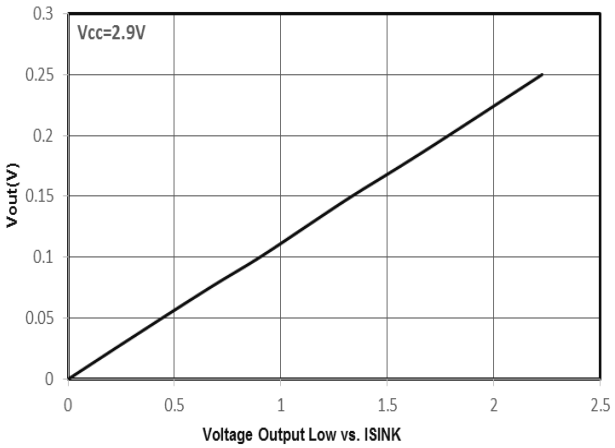


Figure 5. Voltage Output Low vs. ISINK

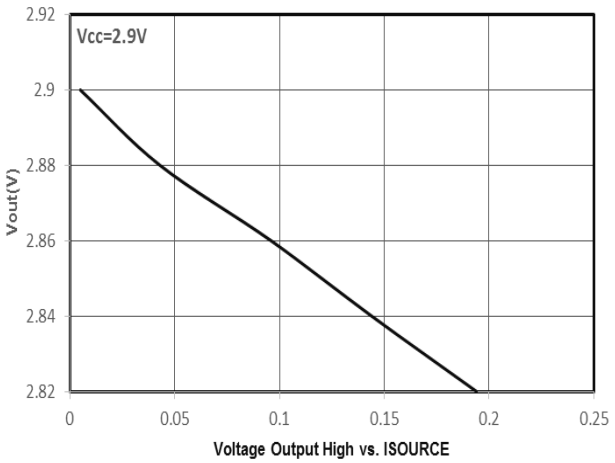


Figure 6. Voltage Output Low vs. ISOURCE

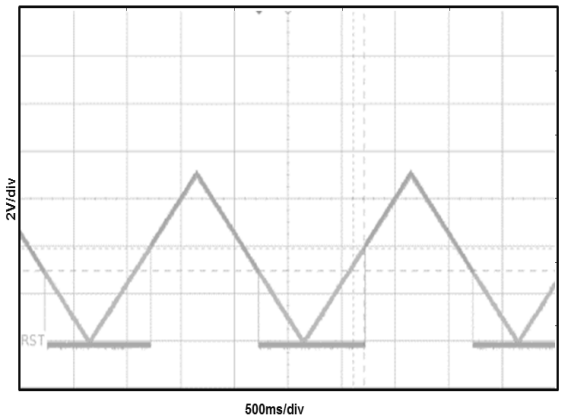


Figure 7. RESET Output Voltage vs. Supply Voltage

Theory of Operation

The TPV821 provides supply voltage supervision as well as manual reset function.

A reset signal is asserted when the supply voltage is below a preset threshold. In addition, the TPV821 allows supply voltage stabilization with a fixed timeout before the reset de-asserts after the supply voltage rises above the threshold.

A manual reset input is available to reset the microprocessor, for example, by using an external push-button.

RESET OUTPUT

The TPV821 features an active-low or active-high push-pull output. For active-low output, the reset signal is guaranteed to be logic low for VCC down to 1 V. The reset output is asserted when VCC is below the reset threshold (VTH), when MR is driven low. Reset remains asserted for the duration of the reset active timeout period (tRP) after VCC rises above the reset threshold, after MR transitions from low to high. Figure 10 shows the reset (active low) outputs.

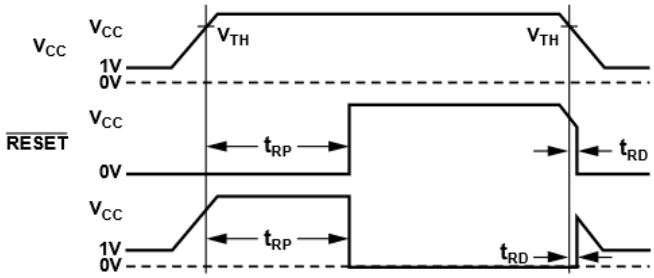


Figure 10. Reset Timing Diagram

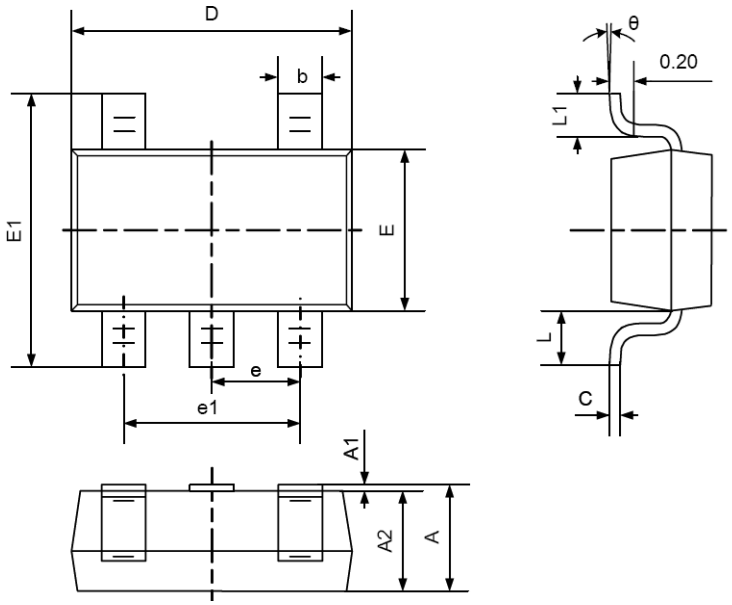
MANUAL RESET INPUT

The TPV821 features a manual reset input (MR), which, when driven low, asserts the reset output. When MR transitions from low to high, reset remains asserted for the duration of the reset active timeout period before de-asserting.

The MR input has an internal pull-up resistor so that the input is always high when unconnected. Noise immunity is provided on the MR input, and fast, negative-going transients are ignored. A 0.1 μF capacitor between MR and ground provides additional noise immunity.

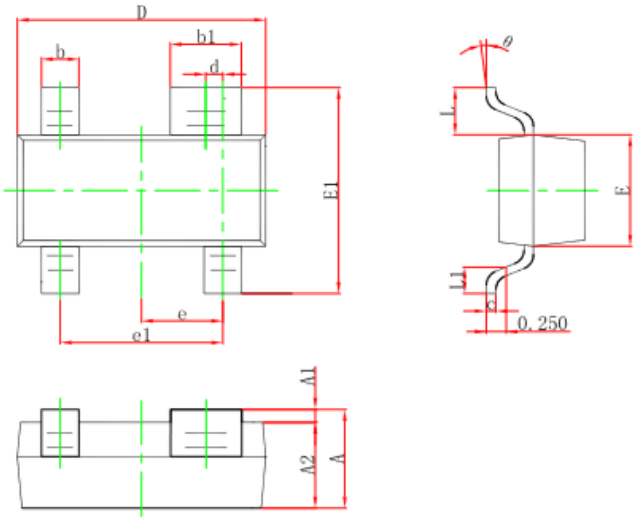
Package Outline Dimensions

SOT-23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
A2	1.000	1.150
b	0.300	0.500
C	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.600	3.000
e	0.950TYP	
e1	1.800	2.000
L	0.600REF	
L1	0.300	0.600
θ	0°	8°

SOT-143



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
b1	0.750	0.900	0.030	0.035
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
d	0.200 TYP.		0.008 TYP.	
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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