Features

- **Precision low voltage monitoring**
- **200 ms (typical) reset timeout**
- **Watchdog timer with 1.6 sec timeout**
- **Manual reset input**
- **Reset output stage**
- **Push-pull active-low**
- **Low power consumption: 2.2 μA**
- **Guaranteed reset output valid to VCC = 1 V**
- **Power supply glitch immunity**
- **Specified from −40°C to +125°C**
- **5-lead SOT-23 package**

Applications

- **Microprocessor systems**
- **Computers**
- **Controllers**
- **Intelligent instruments**
- **Portable equipment**

Description

The TPV6823 is a supervisory circuit that monitors power supply voltage levels and provides a power-on reset signal.

It also has on-chip watchdog timer, which can give out a reset signal if the microprocessor fails to strobe watchdog timer within a preset timeout period.

A reset signal can also be asserted by an external manual reset input.

The reset and watchdog timeout periods are fixed at 200 ms (typical) and 1.6 sec (typical), respectively.

The TPV6823 is available in a 5-lead SOT-23 package and typically consumes only 2.2 μA, suitable for use in low power, portable applications.

Function block diagram

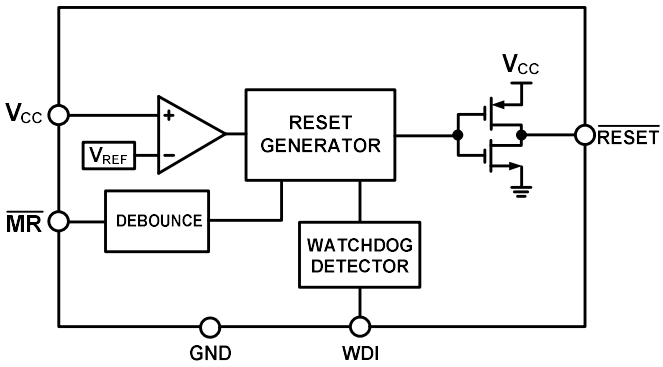

Figure 1.

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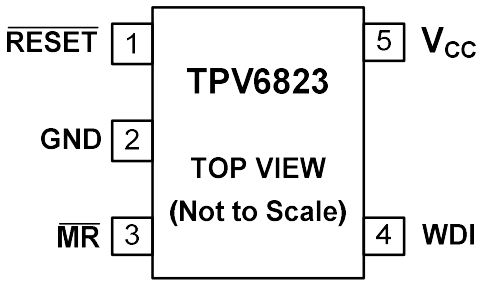
Pin Configuration and Functions

Pin Description



PIN NO	Name	Description
1	RESET	Active-Low Reset Push-Pull Output Stage. Asserted whenever VCC is below the reset threshold, VTH.
2	GND	Ground.
3	MR	Manual Reset Input. This is an active-low input, which, when forced low for at least 1 μs, generates a reset. It features a 50 kΩ internal pull-up.
4	WDI	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated.
5	VCC	Power Supply Voltage Being Monitored.

Order Information

Table 1.

Model Name	Order Number	Package	MSL Level	Transport Media, Quantity	Package Marking
TPV6823V-TR	TPV6823V-TR	SOT23-5	1	Tape and Reel, 3,000	V1V
TPV6823W-TR	TPV6823W-TR	SOT23-5	1	Tape and Reel, 3,000	V1W
TPV6823Y-TR	TPV6823Y-TR	SOT23-5	1	Tape and Reel, 3,000	V1Y
TPV6823Z-TR	TPV6823Z-TR	SOT23-5	1	Tape and Reel, 3,000	V1Z
TPV6823R-TR	TPV6823R-TR	SOT23-5	1	Tape and Reel, 3,000	V1R
TPV6823S-TR	TPV6823S-TR	SOT23-5	1	Tape and Reel, 3,000	V1S
TPV6823T-TR	TPV6823T-TR	SOT23-5	1	Tape and Reel, 3,000	V1T
TPV6823M-TR	TPV6823M-TR	SOT23-5	1	Tape and Reel, 3,000	V1M
TPV6823L-TR	TPV6823L-TR	SOT23-5	1	Tape and Reel, 3,000	V1L

Absolute Maximum Ratings

Table 3

Parameter	Rating
VCC	−0.3 V to 6 V
Output Current (RESET)	20 mA
Operating Temperature Range	−40°C to 125°C
Storage Temperature Range	−65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Table 4

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	2000	V

Electrical Characteristics

VCC = 1.53 V to 5.5V; TA = –40°C to +125°C, unless otherwise noted.

Table 5

TPV6823			SPEC		
Parameter	Test conditions	Unit	Min	Typ	Max
VCC Operating Voltage Range		V	1		5.5
Supply Current	WDI and MR unconnected (VCC=1.8V)	μA		2.2	10
	WDI and MR unconnected (VCC=5V)	μA		6	15
RESET THRESHOLD VOLTAGE					
TPV6823V	Vth	V	1.51	1.58	1.63
TPV6823W	Vth	V	1.62	1.67	1.71
TPV6823Y	Vth	V	2.12	2.19	2.25
TPV6823Z	Vth	V	2.25	2.32	2.38
TPV6823R	Vth	V	2.55	2.63	2.70
TPV6823S	Vth	V	2.85	2.93	3.00
TPV6823T	Vth	V	3.00	3.08	3.15
TPV6823M	Vth	V	4.25	4.38	4.5
TPV6823L	Vth	V	4.5	4.63	4.75
RESET THRESHOLD TEMPERATURE COEFFICIENT		ppm/°C		60	
RESET THRESHOLD HYSTERESIS		mV		2 × VTH	
VCC TO RESET DELAY	VTH − VCC = 100 mV	μs		20	
RESET TIMEOUT PERIOD		ms	140	200	280
RESET OUTPUT VOLTAGE VOL (Push-Pull)	VCC ≥ 1 V, ISINK = 50 μA	V			0.3
RESET OUTPUT VOLTAGE VOH (Push-Pull Only)	VCC ≥ 1.8 V, ISOURCE = 200 μA	V	0.8 × VCC		
MR Input Threshold VIL		V			0.3 × VCC
MR Input Threshold VIH		V	0.7 × VCC		
MR Input Pulse Width 1 μs		μS	1		
MR Glitch Rejection		nS		100	
MR to Reset Delay		nS		200	
MR Pull-Up Resistance		kΩ		50	
Watchdog Timeout Period		sec	1.12	1.6	2.4
WDI Pulse Width 50 ns		nS	50		
WDI Pulse Interval		mS	12		
WDI Input Threshold VIL		V			0.3 × VCC
WDI Input Threshold VIH		V	0.7 × VCC		
WDI Input Current	VWDI = VCC	μA		20	
	VWDI = 0	μA		-15	

Typical Performance Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND, unless otherwise noted.

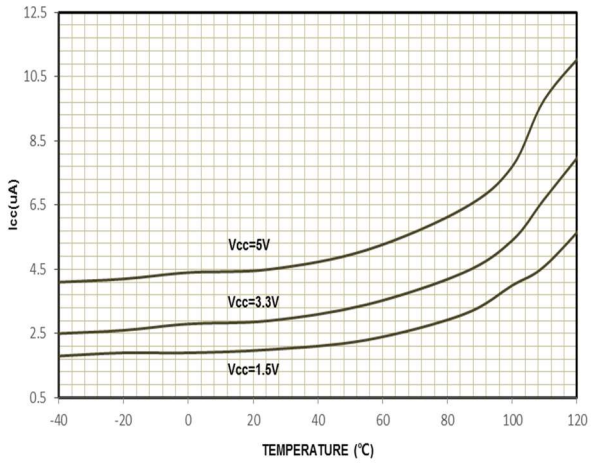


Figure 2. Supply Current vs. Temperature

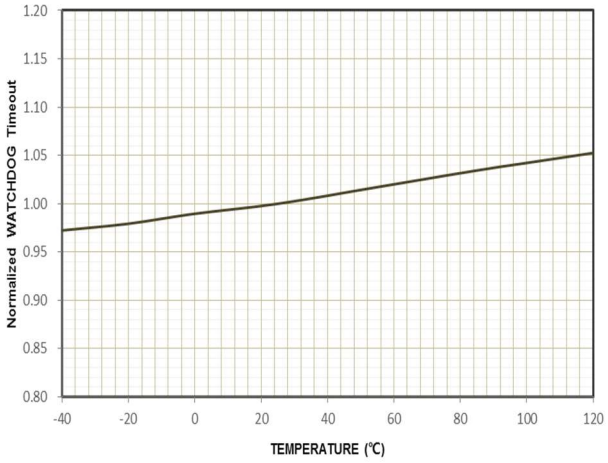


Figure 3. Normalized Watchdog Timeout Period vs. Temperature

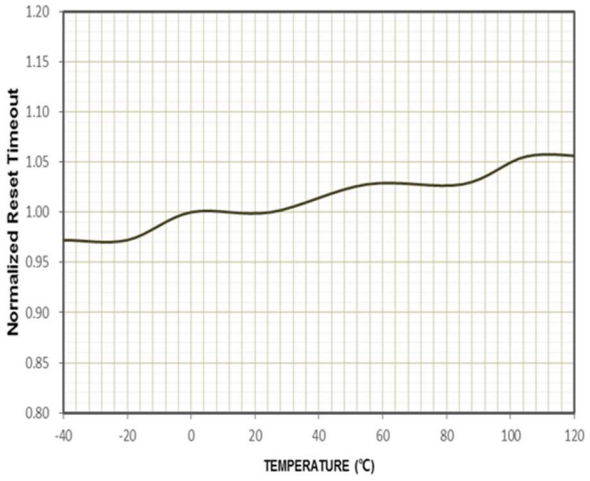


Figure 4. Normalized RESET Timeout Period vs. Temperature

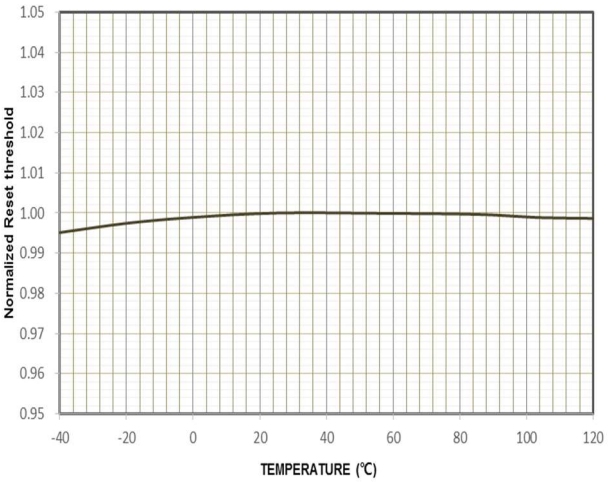


Figure 5. Normalized RESET Threshold vs. Temperature

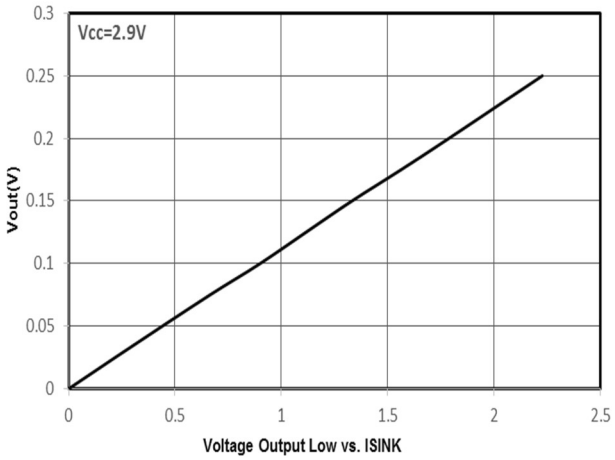


Figure 6. Voltage Output Low vs. ISINK

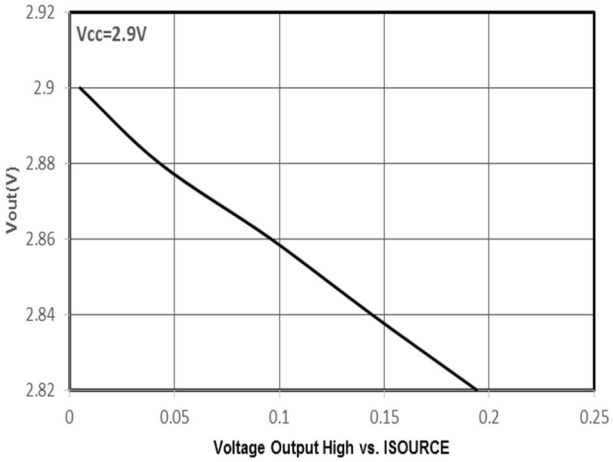


Figure 7. Voltage Output Low vs. ISOURCE

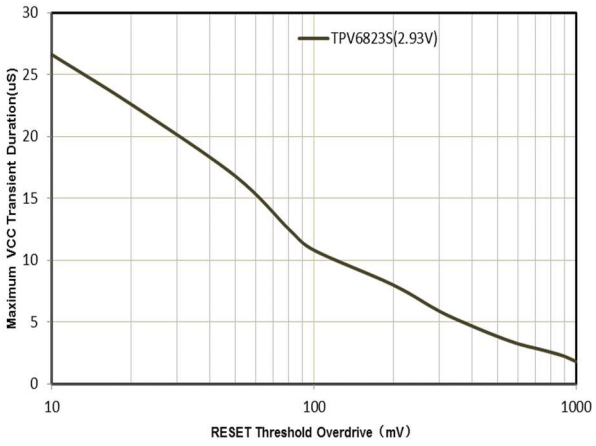


Figure 8. Maximum VCC Transient Duration vs. RESET Threshold Overdrive

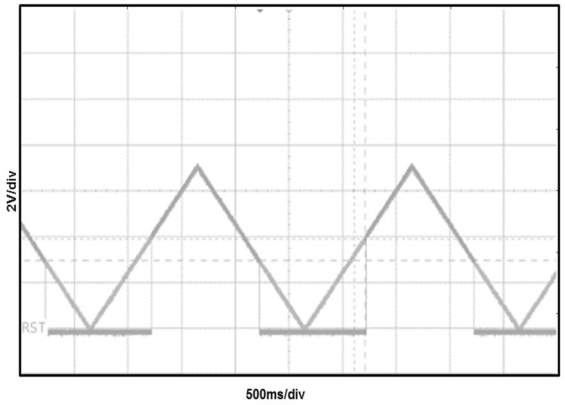


Figure 9. RESET Output Voltage vs. Supply Voltage

Theory of Operation

The TPV6823 provides supply voltage supervision as well as manual reset and watchdog functions.

A reset signal is asserted when the supply voltage is below a preset threshold. In addition, the TPV6823 allows supply voltage stabilization with a fixed timeout before the reset de-asserts after the supply voltage rises above the threshold.

A watchdog timer detects if the microprocessor code breaks down or becomes stuck in an infinite loop. If this happens, the watchdog timer asserts a reset pulse, which restarts the microprocessor in a known state.

A manual reset input is available to reset the microprocessor, for example, by using an external push-button.

RESET OUTPUT

The TPV6823 features an active-low push-pull output. For active-low output, the reset signal is guaranteed to be logic low for VCC down to 1 V. The reset output is asserted when VCC is below the reset threshold (VTH), when MR is driven low, or when WDI is not serviced within the watchdog timeout period (tWD). Reset remains asserted for the duration of the reset active timeout period (tRP) after VCC rises above the reset threshold, after MR transitions from low to high, or after the watchdog timer times out. Figure 10 shows the reset outputs.

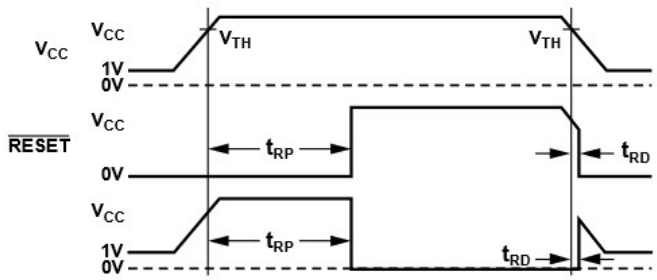


Figure 10. Reset Timing Diagram

MANUAL RESET INPUT

The TPV6823 features a manual reset input (MR), which, when driven low, asserts the reset output. When MR transitions from low to high, reset remains asserted for the duration of the reset active timeout period before de-asserting.

The MR input has an internal pull-up resistor so that the input is always high when unconnected. Noise immunity is provided on the MR input, and fast, negative-going transients are ignored. A 0.1 µF capacitor between MR and ground provides additional noise immunity.

WATCHDOG INPUT

The TPV6823 features a watchdog timer, which monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI). If the timer counts through the preset watchdog timeout period (tWD), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an under-voltage condition on VCC or MR being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset de-asserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

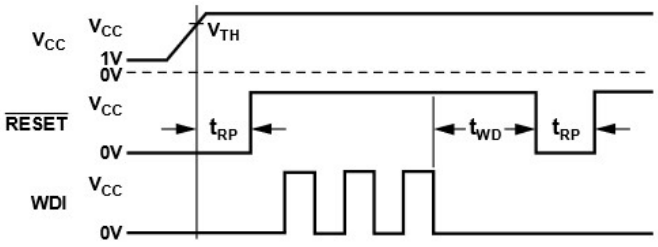
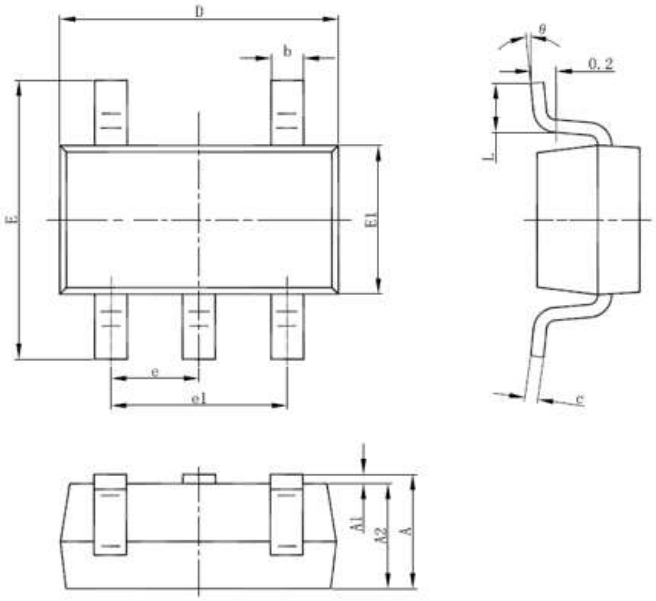


Figure 11. Reset Timing Diagram

Package Outline Dimensions

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Revision History

Table 2.

Date	Revision	Notes
2018/12/10	1.0	Version 1.0
2019/4/15	1.1	Update package POD information
2019/5/28	1.2	Add WDI pulse interval spec