TPS99110-Q1 System-Basis Chip for Automotive Applications

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Operating Case Temperature: –40°C to 150°C
- Ambient Temperature: –40°C to 125°C
- Absolute Maximum Junction Temperature: –40°C to 175°C
- Absolute Maximum VBAT: –0.3 to 40 V
- Multi-Rail Power Supply
  - Two Pre-regulating LDO Controllers: 6-V and 10-V Outputs
  - Linear Regulator Controller With External FET: Adjustable Output From 0.8 to 2.6 V (VDD1)
  - 5-V Output Linear Regulator With Internal FET: 400 mA Maximum (VDD5)
  - 3.3-V Output Linear Regulator With Internal FET: 400 mA Maximum (VDD3), Generated From VDD5
  - Voltage Monitoring on VDD1, VDD3, and VDD5
  - 5-V Sensor Supply Output Tracking to VDD5, 100-mA Maximum, Protection Against Short to Battery and GND
  - Two Adjustable Sensor Supplies, 200-mA Maximum With Protection Against Short to Battery and GND
  - Switched Battery Output Provides VBAT Input With Low Drop
- Analog Features:
  - Two Operational Amplifiers for Signal Conditioning
  - Thee Independent Current Loop Interfaces With Current Sense Input and Digital Output
- Microcontroller Interface
  - 3.3-V and 5-V Compatible 32-Bit, 2-Mbps SPI
  - MCU Monitoring With SPI Q&A Watchdog
- Dual Polarity Enable-Drive Outputs for Disabling Safing-Path or External Power Stages on Any Detected System Failure
- One HS-CAN Transceiver With Bus Wakeup
- One KLINE/LIN Transceiver

2 Applications

- Transmission Control Unit
- Engine Control Unit

3 Description

The TPS99110-Q1 device is a system-basis chip (SBC) offering a highly integrated solution for the typical requirements of transmission and engine electrical control units (ECU) in the automotive space. The integrated multi-rail power supply is designed to power microcontroller units (MCUs) and other circuits in ECUs. The device is designed to support rugged, high-temperature conditions and incorporates three low-dropout (LDO) regulators along with three sensor supplies. The integrated HS-CAN with bus wakeup and KLINE/LIN transceivers help reduce the component count on the board. The TPS99110-Q1 functional architecture features undervoltage and overvoltage monitoring, current limits, temperature warning flags, and overtemperature shutdown on all regulator outputs. Additional features include a window watchdog and SPI Q&A watchdog for MCU-monitoring.

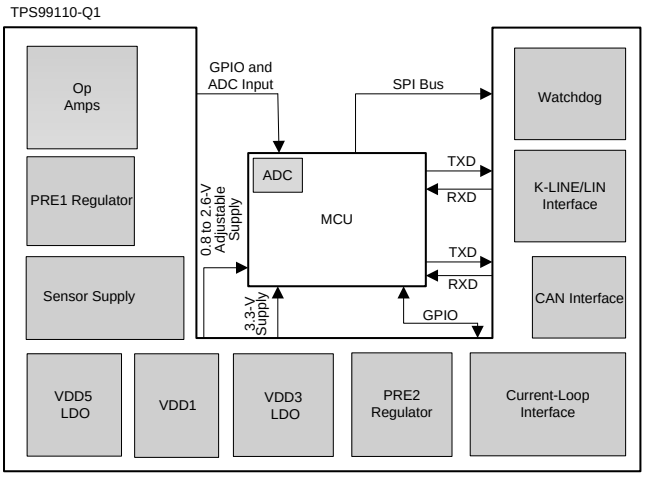
The device is available in a 64-pin HTQFP (PAP) PowerPAD™ integrated circuit package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS99110-Q1	HTQFP (64)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic of Typical Application



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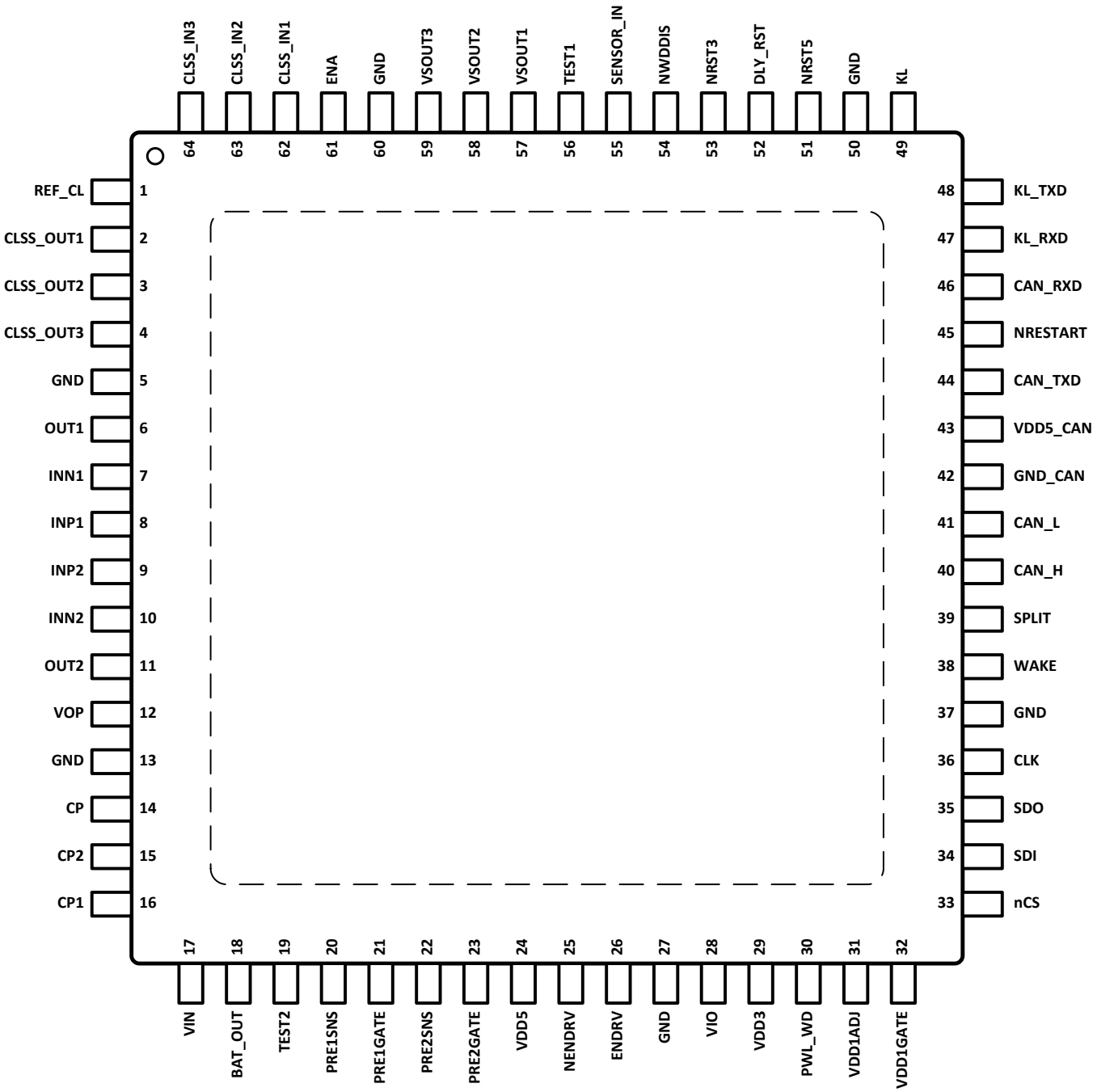
4 Revision History

Changes from Original (October 2014) to Revision A **Page**

- Released the full version of the data sheet ... 1

5 Pin Configuration and Functions

PAP Package
64-Pin HTQFP With PowerPAD™
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BAT_OUT	18	O	Switched battery output
CAN_H	40	I/O	CAN high input and output
CAN_L	41	I/O	CAN low input and output

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
CAN_RXD	46	O	Asynchronous receive data line of the CAN interface
CAN_TXD	44	I	Asynchronous transmission data line of the CAN interface
CLK	36	I	SPI clock
CLSS_IN1	62	I	Input of the current-loop speed-sensor interface 1
CLSS_IN2	63	I	Input of the current-loop speed-sensor interface 2
CLSS_IN3	64	I	Input of the current-loop speed-sensor interface 3
CLSS_OUT1	2	O	Output of the current-loop speed-sensor interface 1
CLSS_OUT2	3	O	Output of the current-loop speed-sensor interface 2
CLSS_OUT3	4	O	Output of the current-loop speed-sensor interface 3
CP	14	O	Pin to the external charge-pump tank capacitor
CP1	16	O	Pin to the external charge-pump fly capacitor
CP2	15	O	
DLY_RST	52	I	This pin adjusts the reset delay with an external resistor.
ENA	61	I	Ignition enable input
ENDRV	26	O	Enable output to switch on external drivers
GND	5	GND	Ground
	13		
	27		
	37		
	50		
	60		
GND_CAN	42	GND	GND supply input for the CAN driver
INN1	7	I	Comparator 1 negative input
INN2	10	I	Comparator 2 negative input
INP1	8	I	Comparator 1 positive input
INP2	9	I	Comparator 2 positive input
KL	49	I/O	K-line/LIN driver input and output
KL_RXD	47	O	Asynchronous receive-data line of K-line (LIN)
KL_TXD	48	I	Asynchronous transmission-data line of K-line (LIN)
nCS	33	I	SPI chip select
NENDRV	25	O	Enable output to switch on the external drivers
NRESTART	45	I	Restart internal logic. A static-low disables the ENDRV and NENDRV pins.
NRST3	53	O	Reset output for the VDD3 and VDD1 supplies
NRST5	51	O	Reset output for the VDD5 supply
NWDDIS	54	I	Disable watchdog for debug purposes
OUT1	6	O	Comparator 1 digital output
OUT2	11	O	Comparator 2 digital output
PRE1GATE	21	O	External linear power-device control for presupply 1
PRE1SNS	20	I	Voltage feedback input for presupply 1 regulation
PRE2GATE	23	O	External linear power device control for presupply 2
PRE2SNS	22	I	Voltage feedback input for presupply 2 regulation
PWL_WD	30	I	Logic-level enable and watchdog trigger
REF_CL	1	O	Reference resistor for current loop interfaces
SDI	34	I	SPI data in
SDO	35	O	SPI data out
SENSOR_IN	55	P	Supply input for sensor and tracker control 1 and 2. Connect this pin externally with PRE1SNS or PRE2SNS.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SPLIT	39	O	2.5-V split output
TEST1	56	O	For internal TI testing purposes. Connect this pin to ground in an application.
TEST2	19	O	For internal TI testing purposes. Connect this pin to ground in an application.
VDD1ADJ	31	I	Voltage feedback input for VDD1 regulation
VDD1GATE	32	O	External linear power device control for VDD1
VDD3	29	O	3.3-V output
VDD5	24	O	5-V output
VDD5_CAN	43	P	5-V supply input for CAN driver
VIN	17	P	Power supply input and battery voltage
VIO	28	P	Supply input for digital outputs
VOP	12	P	Supply voltage for the operation amplifiers (op amps)
VSOUT1	57	O	Sensor-supply output 1
VSOUT2	58	O	Sensor-supply output 2
VSOUT3	59	O	Sensor-supply output 3
WAKE	38	I	Wake input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	PWL_WD, DLY_RST, NWDDIS, VIO, SDI, CLK, NCS, NRESTART, CAN_TXD, VDD5_CAN, KL_TXD, and VDD1ADJ	–0.3	7	V
	PRE2SNS	–0.3	12	
	VOP	–0.3	13.2	
	VIN, SENSOR_IN, ENA, PRE1SNS, and WAKE	–0.3	40	
	INPx/INNx	–0.3	V_{VOP} + 0.3	
	CLSS_INx	–2	40	
Output voltage	VDD5, VDD3, NRSTx, SDO, NENDRV, ENDRV, CAN_RXD, CLSS_OUTx, REF_CL, and KL_RXD	–0.3	7	V
	VDD1GATE	–0.3	8	
	PRE2GATE	–0.3	19	
	VSOUTx, PRE1GATE, CP2, and BAT_OUT	–0.3	40	
	CP and CP1	–0.3	50	
	OUTx	–0.3	V_{VOP} + 0.3	
	CAN_H, CAN_L, and KL_TXD	–27	40	
Source current	NRSTx, ENDRV/NENDRV, CLSS_OUTx, and OUTx	–20	20	mA
	BAT_OUT	–50	20	
	VDD5 and VDD3		400	
	VSOUTx		700	
Sink current	SENSOR_IN and VIN	–10		mA
	ENA, PWL_WD, DLY_RST, NWDDIS, WAKE, INP/Nx, KL_TXD, and KL_RXD	–20	20	
	VDD1ADJ		20	
Ground current, I_{GND}			100	mA
Power-supply power dissipation, P_D			3.5	W
Operating junction temperature, T_J		–40	175	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100–002(1)	All pins except CANH, CANL, SPLIT, and global pins	±2000	V
		CANH(2), CANL, and SPLIT pins(3)	±8000	
		Global pins(3)(4)	±4000	
	Charged device model (CDM), per AEC Q100–011	All pins	±500	
		Corner pins (1, 16, 17, 32, 33, 48, 49, and 64)	±750	

(1) AEC Q100–002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS–001 specification.
(2) The CANH pin has 2kV HBM capability, verified to pass up to 8kV with IEC HV ESD testing conditions.
(3) CANH, CANL, SPLIT, and all Global pins rating is met with respect to GND.
(4) Global pins are VIN, ENA, WAKE, VSOUTx, PRE1SNS, KL, CLSS_INx

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VIN}	Input supply voltage	Full functionality, wakeup from standby mode requires 5.5-V V_{VIN} minimum	5.2		38.5	V
V_{VIO}	VIO pin Input voltage		3		5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		PAP (HTQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	7.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Range of Functionality

Functionality remains the same for all functional blocks including the block affected by a short- circuit or test pulse event. These affected blocks can be: K/LIN and CAN transceivers, current-loop interface, operational amplifier, sensor supplies. T_C = –40°C to 150°C, T_J = –40°C to 175°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIN}	Input voltage, VIN	All functions are operational in this voltage range. Wakeup from standby mode requires VIN minimum of 5.5 V	5.2		38.5	V
		NRST5 might output a low level, but NRST3 outputs a high level, VDD5 must be above 3.3 V, ENDRV or NENDRV must be inactive Wakeup from standby mode requires VIN minimum of 5.5 V	4		5.2	
$I_{Q(STBY)}$	Quiescent current in standby modes, ENA, PWL_WD = Low(1)	V_{IN} = 16 V and T_J < 70°C			50	µA
		V_{IN} = 28 V and T_J < 175°C			400	µA
I_{IN_IDLE}	Input current in enabled mode	No external current consumption			15	mA
V_{VIO}	VIO voltage range		3		5.5	V
V_{DIGIN_HIGH}	Digital input high threshold,KL_TXD, CAN_TXD, SDI, CLK, NCS, PWL_WD, NRESTART, NWDDIS		2			V
V_{DIGIN_LOW}	Digital input low threshold, KL_TXD, CAN_TXD, SDI, CLK, NCS, PWL_WD, NRESTART, NWDDIS				0.8	V
V_{DIGIN_HYST}	Digital input Hysteresis, KL_TXD, CAN_TXD, SDI, CLK, NCS, PWL_WD, NRESTART, NWDDIS		0.1			V
I_{DIG_LEAK}	Digital input leakage current, CAN_TXD, SDI, CLK, NCS, PWL_WD, NRESTART, NWDDIS	0 V < V_{LEAK} ≤ 5.5 V	–60		60	µA
$I_{KL\_TXD\_LEAK}$	KL_TXD leakage current	0 V < V_{LEAK} ≤ 5.5 V	–300		300	µA
V_{DIGOUT_HIGH}	Digital output high level, KL_RXD, CAN_RXD, SDO, CLSS_OUTx	I_{OUT} = –2 mA	V_{VIO} – 0.2			V
V_{DIGOUT_LOW}	Digital output low level, KL_RXD, CAN_RXD, SDO, CLSS_OUTx	I_{OUT} = 2 mA			0.2	V
V_{SENSOR_IN}	Forced voltage at SENSOR_IN pin				40	V
I_{WAKE_LEAK}	Leakage current, WAKE pin	V_{VIN} = 16 V and T_J < 70°C			1.5	µA
		V_{VIN} = 28 V and T_J < 175°C			15	
I_{REV_ENA}	Digital output high level, KL_RXD, CAN_RXD, SDO, CLSS_OUTx	Functionality remains the same for all functional blocks:	–5		5	mA

(1) Sum of current into VIN and WAKE.

6.6 Enable Operation Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ENA_HIGH}	Enable input threshold high	ENA is connected to ignition line through a minimum of 1 kΩ			3.8	V
V_{ENA_LOW}	Enable input threshold low	ENA is connected to ignition line through a minimum of 1 kΩ	2			V
V_{ENA_HYST}	Enable input hysteresis	If no connection to ENA pin, the default state must be OFF	440			mV
R_{ENA}	ENA resistor to ground	V_{ENA} = 2 V	0.4		2	MΩ
$V_{VIN\_TH\_L}$	VIN undervoltage switch-off		3.7		3.9	V
$V_{VIN\_TH\_H}$	VIN undervoltage switch-on		5		5.4	V
$V_{VIN\_TH\_HYS}$	VIN undervoltage hysteresis		1		1.5	V
V_{WAKE_HIGH}	WAKE input threshold high	WAKE pin is connected to VIN through a minimum of 1 kΩ			3.8	V
V_{WAKE_LOW}	WAKE input threshold low	WAKE pin is connected to VIN through a minimum of 1 kΩ	2			V
V_{WAKE_HYST}	WAKE input hysteresis	If no connection to WAKE pin, the default state must be OFF.	0.1			V
I_{WAKE}	WAKE sink current to GND	V_{WAKE} > 2 V			1	µA

6.7 Preregulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{GS(th)}$	Gate threshold voltage	I_D = 1 mA and T_J = –40°C to 175°C	0.3		3	V
C_{ISS}	Maximum input capacitance	V_{GS} = 0 V			5000	pF
Q_{GATE}	Maximum gate charge	V_{GS} = 0 V to 10 V			190	nC
g_{FS}	Minimum forward transconductance	I_D = 50 mA	0.4			S
$C_{PREXSNS}$	Value of the output ceramic capacitor	0 mΩ ≤ ESR ≤ 250 mΩ, see Figure 37	0.5	1	15	µF
$V_{PRE1SNS}$	Regulated voltage to PRE1SNS pin	10 V ≤ V_{IN} ≤ 38.5 V	9	10	11	V
$V_{PRE1GATE}$	External device voltage at PRE1GATE pin	I_{Load} = –20 µA at the PRE1GATE pin	14			V
V_{PRE1_GS}	External PRE1 FET Gate to Source voltage	4 V ≤ V_{VIN} ≤ 6 V	2.5		4.5	V
		V_{VIN} > 6 V	4.5			
$V_{PRE1GATE\_OFF}$	External device voltage at PRE1GATE pin	Off condition, I_{Load} = 20 µA at PRE1GATE pin			1	V
V_{CLAMP1}	External FET V_{GS} clamp	$V_{PRE1GATE}$ – $V_{PRE1SNS}$, internal Zener diode	10		15	V
		$V_{PRE1SNS}$ – $V_{PRE1GATE}$, internal Zener diode	10		15	
$V_{PRE2SNS}$	Regulated voltage to PRE2SNS pin		5.5	6	6.5	V
$V_{PRE2GATE}$	External device voltage at PRE2GATE pin	Load = –20 µA at PRE2GATE pin	11			V
V_{PRE2_GS}	External PRE2 FET Gate to Source voltage	4 V ≤ V_{IN} ≤ 4.5 V	2.5		3	V
		4.5 V < V_{IN}	3.5			
$V_{PRE2GATE\_OFF}$	External device voltage at PRE2GATE pin	Off condition, load = 20 µA at PRE2GATE pin			0.3	V
V_{CLAMP2}	External device V_{GS} clamp	$V_{PRE2GATE}$ – $V_{PRE2SNS}$, internal Zener diode	10		15	V
		$V_{PRE2SNS}$ – $V_{PRE2GATE}$, internal Zener diode	10		15	

6.8 VDD5 Voltage Regulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{VDD5}	Value of output ceramic capacitor	0 mΩ ≤ ESR ≤ 250 mΩ		5	10	40	µF
P_{VDD5}	Maximum power dissipation					2	W
I_{VDD5}	VDD5 output current			0		400	mA
V_{VDD5}	VDD5 output voltage	0 ≤ I_{VDD5} ≤ 400 mA (1)		4.9	5	5.1	V
V_{VDD5_dyn}	VDD5 output voltage dynamic Go-no-go test for RESET behavior	Square wave on VDD5 f = 50 kHz to 50 Hz Duty cycle = 50% I_{VDD5} = 10% to 90% I_{max}		4.8	5	5.151	V
V_{VDD5_max}	Maximum VDD5 output voltage during VIN step from 5.1 V to 13.5 V within 10 µs	C_{VDD5} = 6 µF I_{VDD5} < 400 mA				5.5	V
V_{Vdr5}	VDD5 output dropout voltage Vdr5 = (VPRE2 – VDD5)	0 mA ≤ I_{VDD5} ≤ 400 mA	T_J = –40°C			0.25	V
			T_J = 25°C			0.29	
			T_J = 175°C			0.32	
$PSRR_{VDD5}$	Power supply rejection ratio VIN	50 Hz ≤ f ≤ 20 kHz U = 4 V_{PP} V_{IN} > 9 V mean value 0 ≤ I_{VDD5} ≤ 400mA		40			dB
LiR_{VDD5}	Line regulation (I_{VDD5} is constant during test)	0 ≤ I_{VDD5} ≤ 400 mA, 8 V ≤ V_{IN} ≤ 19 V		–25	0	25	mV
LoR_{VDD5}	Load regulation (VPRE2 is constant during test)	0 ≤ I_{VDD5} ≤ 400 mA, 8 V ≤ V_{IN} ≤ 19 V		–25	0	25	mV
Tmp_{VDD5}	Temperature drift	Compared to 25°C value		–100	0	100	ppm/K
D_{VDD5}	Long-term drift			–0.8%	0	0.8%	
C_{VDD5}	Regulator output with ripple on VIN input	Square wave on VIN, 8 V to 16 V; F0 = 10 kHz; dV/dt = 5 V/µs		4.8		5.2	V
dVDD5/dt	dV/dt at VDD5	For MCU supply C_{VDD5} = 10 µF I_{VDD5} = 0 mA Slope from 0.5 V to 1 V and slope from 1 V to 90% of VDD5 (2) C_{VDD5} = 10 µF 0 ≤ I_{VDD5} ≤ 400 mA PRE1 and PRE2 used SENSORIN connected to PRE1		5		50	V/ms

(1) Including line regulation, loads regulation, temperature drift and long-term drift.
(2) if current limitation is reached, the slope will be controlled by the current limitation and output capacitor

6.9 VDD3 Voltage Regulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{VDD3}	Value of output ceramic capacitor	0 mΩ ≤ ESR ≤ 250 mΩ		5	10	40	µF
P_{VDD3}	Maximum power dissipation					1.75	W
I_{VDD3}	VDD3 output current			0		400	mA
V_{VDD3}	VDD3 output voltage	$0 \le I_{VDD3} \le 400$ mA (1)		3.234	3.3	3.366	V
V_{VDD3_dyn}	VDD3 output voltage dynamic	Square wave on VDD3 f = 50 kHz to 50 Hz Duty cycle = 50% I_{VDD3} = 10% to 90% I_{max}		3.17	3.3	3.43	V
V_{VDD5_max}	Maximum VDD3 output voltage during VIN step from 5.1 V to 13.5 V within 10 µs	C_{VDD3} = 6 µF I_{VDD3} < 400 mA PRE1 and PRE2 used				3.6	V
V_{Vdr3}	VDD5 output dropout voltage Vdr5 = (VDD5 – VDD3)	0 mA ≤ I_{VDD3} ≤ 400 mA	T_J = –40°C			0.25	V
			T_J = 25°C			0.29	
			T_J = 175°C			0.32	
$PSRR_{VDD3}$	Power supply rejection ratio VIN	50 Hz ≤ f ≤ 20 kHz U = 4 V_{PP} V_{IN} > 9 V mean value C_{VDD3} = 10 µF $0 \le I_{VDD3} \le 400$ mA PRE1 and PRE2 used SENSORIN connected to PRE1		40			dB
LiR_{VDD3}	Line regulation (I_{VDD3} is constant during test)	$0 \le I_{VDD3} \le 400$ mA, 8 V ≤ V_{IN} ≤ 19 V		–25	0	25	mV
LoR_{VDD3}	Load regulation (VPRE2 is constant during test)	$0 \le I_{VDD3} \le 400$ mA, 8 V ≤ V_{IN} ≤ 19 V		–25	0	25	mV
Tmp_{VDD3}	Temperature drift	Compared to 25°C value		–100	0	100	ppm/K
D_{VDD3}	Long-term drift			–0.8%	0	0.8%	
C_{VDD3}	Regulator output with ripple on VIN input	Square wave on VIN, 8 V to 16 V; F0 = 10 kHz; dV/dt = 5 V/µs		3.2		3.4	V
dVDD3/dt	dV/dt at VDD3	For MCU supply: C_{VDD3} = 10 µF I_{VDD3} = 0 mA Slope from 0.5 V to 1 V and slope from 1 V to 90% of VDD3 (2)		5		50	V/ms

(1) Including line regulation, load regulation, temperature drift, and long-term drift.
(2) if current limitation is reached, the slope will be controlled by the current limitation and output capacitor

6.10 VDD1 Voltage Regulator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{GS(th)}$	Gate threshold voltage	I_D = 1 mA	0.3		3	V
C_{ISS}	Maximum input capacitance	V_{GS} = 0 V			3200	pF
Q_{GATE}	Maximum gate charge	V_{GS} = 0 V to 10 V			70	nC
g_{FS}	Minimum forward transconductance	I_D = 50 mA	0.4			S
C_{VDD1}	Value of the output ceramic capacitor	0 mΩ ≤ ESR ≤ 250 mΩ, see Figure 37	5	10	40	µF
V_{VDD1}	VDD1 programmable output	Dependent on external resistive divider	0.8		2.6	V
I_{VDD1}	VDD1 output current		10		700	mA
$V_{ref(VDD1ADJ)}$	VDD1ADJ reference voltage	10 mA ≤ I_{VDD1} ≤ 700 mA (1)	0.784	0.8	0.816	V

(1) Including line regulation, loads regulation, temperature drift and long-term drift.

VDD1 Voltage Regulator Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{dref(VDD1ADJ)}$	VDD1ADJ reference voltage dynamic, go-no-go test for RESET behavior	10 mA ≤ I_{VDD1} ≤ 700 mA Square wave on VDD1 I_{VDD1} = 10% to 90% I_{max} f = 50 kHz to 50 Hz Duty cycle = 50% C_{VDD1} > 30 µF ESR < 50 mΩ No reset allowed	0.753	0.8	0.835	V
V_{VDD1_GATE}	VDD1_GATE output voltage		7		15	V
		4 V ≤ V_{IN} ≤ 4.5 V T_J > 70°C	6.55		15	
$V_{VDD1ADJmax}$	Maximum VDD1ADJ voltage at switch-on	C_{VDD1} > 6 µF I_{VDD1} < 700 mA Internal soft-start function			$V_{VDD1ADJ}$ × 1.03	V
$C_{VDD1ADJ}$	Regulator output with ripple on VIN input	Square wave on VIN 8 V to 16 V F0 = 10 kHz dV/dt = 5 V/µs	0.773	0.8	0.827	V
$V_{O(VDD1ADJmax)}$	Maximum VDD1ADJ output voltage during VIN step from 5.1 V to 13.5 V within 10 µs	C_{VDD1} = 6 µF I_{VDD1} < 700 mA			0.88	V
dVDD1ADJ/dt	Rate at which VDD1 powers up	C_{VDD1} = 10 µF I_{VDD1} = 10 mA	0.8		8	V/ms
$LiR_{VDD1ADJ}$	Line regulation (IVDD1 is constant during test)	0 ≤ I_{VDD1} ≤ 700 mA 8.0 V ≤ VIN ≤ 19 V	–7	0	7	mV
$LoR_{VDD1ADJ}$	Load regulation (VIN is constant during test)	0 ≤ I_{VDD1} ≤ 700 mA 8 V ≤ VIN ≤ 19 V	–7	0	7	mV
$PSRR_{VDD1}$	Power supply rejection ratio VIN	50 Hz ≤ f ≤ 20 kHz C_{VDD1} > 10 µF 10 mA ≤ I_{VDD1} ≤ 700 mA PRE1 and PRE2 used SENSORIN connected to PRE1	40			dB
$Tmp_{VDD1ADJ}$	Temperature drift		–100	0	100	ppm/K
D_{VDD1}	Long-term drift		–0.8%	0	0.8%	

6.11 VSOUT1, VSOUT2, and VSOUT3 Sensor-Supply Output Characteristics

Other functions must not be interfered by VSOUTx an output shorted to GND or battery voltage or other VSOUT outputs.
Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{VSOUT}	Value of output capacitor	ESR range 0 mΩ to 250 mΩ		0.5	1	15	µF
$P_{VSOUT1/2}$	Maximum power dissipation, VSOUT1 and VSOUT2	Single use power dissipation or sum dissipation VSOUT1 + VSOUT2				1	W
P_{VSOUT3}	Maximum power dissipation, SOUT3					0.1	W
$I_{VSOUT1/2}$	Output current	VSOUT1 and VSOUT2 only		0		200	mA
I_{VSOUT3}	Output current	VSOUT3 only		0		100	mA
V_{VSOUTx_UV}	Under voltage detection threshold, VSOUTx			0.9 × V_{VSOUT}		0.96 × V_{VSOUT}	V
V_{VSOUTx_OV}	Overvoltage detection threshold, VSOUTx			1.04 × V_{VSOUT}		1.1 × V_{VSOUT}	V
Vdrtx	VSOUT dropout voltage, Vdrtx = (SENSOR_IN-VVSOUT)	SENSOR_IN < VDD5 0 mA ≤ I_{VSOUT} ≤ I_{VSOUT_Max}	T_J = –40°C			0.24	V
			T_J = 25°C			0.275	
			T_J = 175°C			0.44	
$-I_{VSOUTx\_REV}$	Output reverse current (limited by the regulator)	VVSOUT = 38.5 V Only one Sensor supply tested at a time, others disabled				15	mA
I_{VSOUT_LIM}	Output current limit	–2 V ≤ V_{VSOUT} ≤ VDD5		200		700	mA

VSOUT1, VSOUT2, and VSOUT3 Sensor-Supply Output Characteristics (continued)

Other functions must not be interfered by VSOUTx an output shorted to GND or battery voltage or other VSOUT outputs. Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSOUT_SH}	Output short circuit voltage range	No effect on other functions. $-0.3\ V \le V_{VIN} \le 38.5\ V$	–2		38.5	V
BitSPI_UV_OV	Load step behavior	Square wave on VSOUTx I_{VSOUTx} = 10% to 90% I_{max}; f = 50 Hz to 50 kHz; duty cycle = 50% No undervoltage or overvoltage detection allowed	pass or fail			
TRACKING MODE (SPI REGISTER FOR VSOUT1/2 = 0000) AND VSOUT3						
MV_{VSOUTx}	Matching output error MV_{VSOUT} = (VDD5 – V_{VSOUT})	Within I_{VSOUT} limits(1) $-40°C < T_J < 140°C$	–15	0	15	mV
		$140°C < T_J < 150°C$	–20		20	
		$150°C < T_J < 160°C$	–25		25	
		$160°C < T_J$	–30		30	
V_{VSOUTx}	Output voltage	SPI register VSOUTx = 0001	–3%	5.25	3%	V
		SPI register VSOUTx = 0010	–3%	5.5	3%	
		SPI register VSOUTx = 0011	–3%	5.75	3%	
		SPI register VSOUTx = 0100	–3%	6	3%	
		SPI register VSOUTx = 0101	–3%	6.25	3%	
		SPI register VSOUTx = 0110	–3%	6.5	3%	
		SPI register VSOUTx = 0111	–3%	6.75	3%	
		SPI register VSOUTx = 1000	–3%	7	3%	
		SPI register VSOUTx = 1001	–3%	7.25	3%	
		SPI register VSOUTx = 1010	–3%	7.5	3%	
		SPI register VSOUTx = 1011	–3%	7.75	3%	
		SPI register VSOUTx = 1100	–3%	8	3%	
		SPI register VSOUTx = 1101	–3%	8.25	3%	
		SPI register VSOUTx = 1110	–3%	8.5	3%	
		SPI register VSOUTx = 1111	–3%	8.75	3%	

(1) Referenced to VDD5 output, including long-term drift and temperature drift

6.12 NRST5 Electrical Characteristics

Reset function remains operational for voltages as low as VDD5 = 1 V. Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DLY_RST}	Voltage capability of external resistor at pin DLY_RST(1)		2			V
V_{VDD5_UV}	VDD5 under voltage threshold		4.5	4.65	4.8	V
V_{VDD5_HEAD}	VDD5 headroom		200			mV
V_{RST_l}	Reset output low level (on)	1 V = V_{VDD5}(2)			0.4	V
V_{RST_h}	Reset output high level (off)		V_{VDD5} – 50		V_{VDD5} + 50	mV
R_{DLY_RST}	Value of reset delay resistor	Nominal value is 22 kΩ; Can be open or short	0	22	∞	kΩ

(1) The external resistors to GND must be selected according these limits.
(2) An external pullup of 2 kΩ to VDD5 output is added.

6.13 NRST3 Electrical Characteristics

Reset function remains operational for voltages as low as VDD3 = 0 V. Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DLY_RST}	Voltage capability of external resistor at pin DLY_RST	The external resistor to GND must be selected according these limits.	2			V
V_{VDD3_UV}	VDD3 reset threshold		2.97	3.07	3.17	V
V_{VDD3_HEAD}	VDD3 headroom		130			mV
V_{VDD1_UV}	VDD1 reset threshold	Voltage at pin VDD1ADJ	0.726	0.745	0.764	V
V_{VDD1_HEAD}	VDD1 headroom	Voltage at pin VDD1ADJ	30			mV
V_{RST3_LOW}	Reset output low level by external pull-down resistor	0 V≤ V_{VIO} ≤ 7 V			0.1	V
V_{RST3_HIGH}	Reset output high level		V_{VIO} – 200		V_{VIO} + 50	mV
R_PD3	External pulldown resistor		1		47	kΩ
V_{BIAS_RESET}	Biasing voltage at pin DLY_RST	R_{RST_DLY} = 22 kΩ	0.935		1.16	V
R_{RST_DLY}	Value of reset delay resistor	Nominal value is 22 kΩ Can be open or short	0	22	∞	kΩ

6.14 SPI Characteristics

C_{LOAD} at SDO = 150 pF, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PUC_SPI}	Internal pullup current source between NCS and VIO		–120		–40	µA
I_{PDC_SPI}	Internal pulldown current sink SDI, CLK to GND		40		120	µA
C_{IntSPI}	Internal capacitance at SDI, SDO, CLK, and NCS(1)			5	10	pF

(1) For information only, ensured by design.

6.15 NENDRV and ENDRV Output Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{NENDRVL}$	NENDRV low output level	I_{NENDRV} = 5mA open drain current			0.2	V
I_{NENDRV_LEAK}	NENDRV off state leakage current	V_{NENDRV} = 0 to 5 V	–2		2	µA
V_{NENDRV_th}	NENDRV input threshold	Feedback for internal logic	2		3	V
V_{ENDRVH}	ENDRV high output level	I_{ENDRV} = 5 mA to GND	V_{VDD5} – 0.2		V_{VDD5}	V
		I_{ENDRV} = 5 mA to GND T_J > 150°C	V_{VDD5} – 0.3			
I_{ENDRV_LEAK}	ENDRV off state leakage current	V_{ENDRV} = 0 to VDD5	–2		2	µA
		V_{ENDRV} = 0 to VDD5 T_J > 150°C	–6		6	
V_{ENDRV_th}	ENDRV input threshold	Feedback for internal logic	2		3	V

6.16 K-Line and LIN Driver Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{KL_TXD}	Internal KL_TxD pull-up resistor to VIO	$0\ V \le V_{KL\_TXD} \le V_{VIO}$	5		40	kΩ
V_{OL_KL1}	Output low level pin KL	I_{KL} = 20 mA	0.4		1.2	V
V_{OL_KL2}	Output low level pin KL	I_{KL} = 40 mA T_J = 150°C	0.4		1.7	V
		I_{KL} = 40 mA T_J = 175°C	0.4		2	V
I_{LIM_KL}	Output current limitation pin KL	$0\ V \le V_{KL} \le V_{VIN}$	40		200	mA
I_{LEAK_KL}	Input leakage current pin KL	$0\ V \le V_{KL} \le 40\ V$	$-V_{KL}$ / 20 kΩ		V_{KL} / 20 kΩ	A
		$-28\ V \le V_{KL} \le 0\ V$	$-V_{KL}$ / 16.4 kΩ		VV_{KL} / 16.4 kΩ	A
		V_{VIN} = 0 V $0\ V \le V_{KL} \le 18\ V$		20	30	µA
V_{IL_KL}	Input low voltage KL input threshold		0.4 × V_{VIN}			V
V_{IH_KL}	Input high voltage KL input threshold				0.6 × V_{VIN}	V
V_{HYST_KL}	Hysteresis voltage KL input		0.05 × V_{VIN}		0.175 × V_{VIN}	V
f_{BAUD}	Transmission speed on KL in LIN mode	C_L = 1 nF, R_L = 1 kΩ	2.4		20	kb/s
		C_L = 6.8 nF, R_L = 660 Ω	2.4		20	
		C_L = 10 nF; R_L = 500 Ω	2.4		20	

6.17 CAN Transceiver Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CANH and CANL PINS						
V_{COMM}	CANH/CANL common mode voltage range		–12		20	V
V_{DIFF_THR}	Differential receiver threshold voltage	Normal mode	500	700	900	mV
		Standby mode	400	700	1150	mV
$V_{DIFF\_THR\_HYS}$	Differential receiver threshold voltage hysteresis		50		400	mV
V_{DIFF_REC}	Differential recessive output voltage	No bus termination	–50		50	mV
V_{REC}	Recessive output voltage (VCANH + VCANL) / 2	No bus termination	2	2.5	3	V
V_{REC_PD}	Recessive output voltage	Standby mode, no bus connected V_{VDD5_CAN} < 200 mV	–0.1		0.1	V
V_{CANH_DOM}	CANH dominant output voltage	R_L = 45 Ω to 65 Ω	2.75	3.6	4.5	V
V_{CANL_DOM}	CANL dominant output voltage	R_L = 45 Ω to 65 Ω	0.5	1.4	2.25	V
V_{CAN_MATCH}	Matching of dominant output voltage	R_L = 45 Ω to 65 Ω $(V_{CANH} + V_{CANL}) – 5$ V 4.7 nF connected to SPLIT line.	–250		200	mV
		R_L = 120 Ω f_{CAN_TXD} = 250 kHz 4.7 nF connected to SPLIT line	0.9	1	1.1	VDD5_CAN

CAN Transceiver Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIFF_DOM}	Differential dominant output voltage	R_L = 45 Ω to 65 Ω	1.5		3	V
I_{CANH_SH}	CANH short-circuit output current	Normal mode VDD5_CAN = 5 V V_{CANH} = 0 V V_{CAN_TxD} = 0 V After short circuit occurs, up to 170 mA for 2 µs is allowed	–100			mA
I_{CANL_SH}	CANL short-circuit output current	Normal mode VDD5_CAN = 5 V V_{CANL} = 40 V V_{CAN_TxD} = 0 V After short circuit occurs, up to 152 mA for 2 µs is allowed			100	mA
R_{COM_IN}	Common-mode input resistance	Normal mode CANx to GND	25	32	42	kΩ
$R_{COM\_IN\_MATCH}$		Input resistance matching	–3		3	%
R_{DIFF_IN}	Differential input resistance	Normal mode	40	65	90	kΩ
I_{CAN_LEAK}	CANH and CANL input leakage current	Standby mode V_{CANH} = V_{CANL} = 5 V	100		250	µA
		Power down mode V_{CANH} = V_{CANL} = 5 V VIN connected to GND with 0 Ω	0		10	
		Power down mode V_{CANH} = V_{CANL} = 5 V VIN connected to GND with 47 kΩ	0		10	
I_{SPLIT_LEAK}	SPLIT leakage current	Standby mode –27 V ≤ V_{SPLIT} ≤ 40 V T_J = 150°C	–5		5	µA
		T_J = 175°C	–15		15	µA
V_{SPLIT}	SPLIT output voltage	$\lvert I_{SPLIT} \rvert$ = 0 mA	0.475 × V_{VDD5_CAN}	2.5	0.525 × V_{VDD5_CAN}	V
		$\lvert I_{SPLIT} \rvert$ = 500 µA	0.3 × V_{VDD5_CAN}	2.5	0.7 × V_{VDD5_CAN}	V

6.18 Current-Loop Interface Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Voltage capability of external resistor at pin DLY_RST bias voltage at pin REF_CL	The external resistor to GND must chosen according these limits.	2			V
		During normal operation (5 to 15K)		1	2	
$I_{CLSS\_THRESHx}$	CLSS_Inx input average threshold with RREF_CL = 10kΩ (excluding the tolerance of RREF_CL)	SPI register THRESHx = 0000	–4%	5.5	4%	mA
		SPI register THRESHx = 0001	–4%	5.9	4%	
		SPI register THRESHx = 0010	–4%	6.3	4%	
		SPI register THRESHx = 0011	–4%	6.7	4%	
		SPI register THRESHx = 0100	–3%	7.1	3%	
		SPI register THRESHx = 0101	–3%	7.5	3%	
		SPI register THRESHx = 0110	–3%	7.9	3%	
		SPI register THRESHx = 0111	–3%	8.3	3%	
		SPI register THRESHx = 1000	–3%	8.7	3%	
		SPI register THRESHx = 1001	–3%	9.1	3%	
		SPI register THRESHx = 1010	–3%	9.5	3%	
		SPI register THRESHx = 1011	–3%	9.9	3%	
		SPI register THRESHx = 1100	–3%	10.3	3%	
		SPI register THRESHx = 1101	–3%	10.7	3%	
		SPI register THRESHx = 1110	–3%	11.1	3%	
		SPI register THRESHx = 1111	–3%	11.5	3%	
I_{CLSS_HYSTx}	CLSS_Inx input hysteresis with R_{REF_CL} = 10 kΩ (excluding the tolerance of R_{REF_CL})	SPI register HYSTx = 00	–20%	0.6	20%	mA
		SPI register HYSTx = 01	–20%	1.2	20%	
		SPI register HYSTx = 10	–20%	1.8	20%	
		SPI register HYSTx = 11	–20%	2.4	20%	
R_{REF_CL}	Current loop reference resistor	connected between pin REF_CL and GND	5	10	15	kΩ
R_{CLSS_Inx}	Resistance between CLSS_Inx and ground	I_{clss} = 25 mA	20	32	40	Ω
$I_{CLSS\_Inx\_MAX}$	Current limitation	With overcurrent diagnosis send to digital part	–100		75	mA
$t_{CLSS\_Inx\_MAX}$	Filter time overcurrent limit detection	Realized in digital core	100	128	140	µs
$I_{CLSS\_Inx\_OC}$	Open circuit or short to ground diagnosis	With undercurrent diagnosis send to digital part	0		1	mA
$t_{CLSS\_Inx\_OC}$	Filter time open circuit detection	Realized in digital core	100	128	140	µs

6.19 Operational Amplifier Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VOP}	Operating supply voltage		3		12	V
V_{ICM}	Input common mode range		–0.1		V_{VOP}	V
$V_{o\_high\_1mA}$	Output voltage high	I_{OUTPUT} = ±1 mA	V_{VOP} – 0.3		V_{VOP}	V
$V_{o\_low\_1mA}$	Output voltage low		0		0.1	
$V_{o\_high\_5mA}$	Output voltage high	I_{OUTPUT} = ±5 mA	V_{VOP} – 1		V_{VOP}	V
$V_{o\_low\_5mA}$	Output voltage low		0		0.32	
I_b	Input bias current	T_J = 150°C	–250		250	nA
		T_J = 175°C	–500		500	nA

Operational Amplifier Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_o	Input offset current		–100		100	nA
VIO	Input offset voltage		–12		12	mV
GBP	Unity Gain bandwidth	At 0-dB amplification LOAD = 100 pF // 1 kΩ	1			MHz
SR	Slew rate	At 0-dB amplification, LOAD = 100 pF // 1 kΩ.	1			V/µs
PHMΩP	Phase margin	At 0-dB amplification, LOAD = 100 pF // 1 kΩ	45			°
I_{force_INNx}	Forced current INNx inputs	no impact on other function, output must not change state	–1		1	mA
I_{force_INPx}	Forced current INPx inputs	no impact on other function, output must not change state	–1		1	mA
AVD	Large signal voltage gain	Test set-up: output voltage 2 V_{PP} LOAD = 100 pF // 1 kΩ	70			dB
INCLPP	Positive input clamp	1-mA forced; V_{VOP} < 11 V	V_{VOP} + 0.1		VOP1	V
		1-mA forced; V_{VOP} > 11 V	V_{VOP} – 0.1			
INCLPN	Negative input clamp	–1-mA forced current.	–1		–0.3	V

6.20 Switched Battery Characteristics

over operating free-air temperature range (unless otherwise noted)

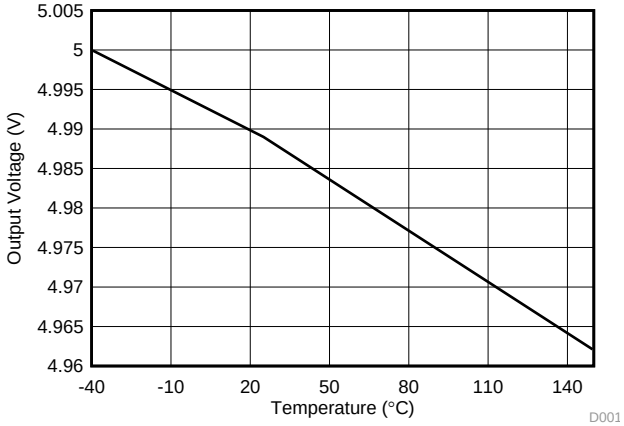
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{batout}	BAT_OUT output voltage	Normal mode; I_{BATT_OUT} = 50 mA	V_{VIN} – 0.45		V_{VIN}	V
		Normal mode; I_{BATT_OUT} = 10 mA, V_{VIN} < 28 V	V_{VIN} – 0.1		V_{VIN}	V
$I_{leakbatout}$	BAT_OUT leakage current	Standby mode			5	µA
		STANDBY mode, V_{VIN} > 28 V			10	µA
C_{batout}	Maximum external capacitance		0	100	200	nF

6.21 Charge Pump Characteristics

over operating free-air temperature range (unless otherwise noted)

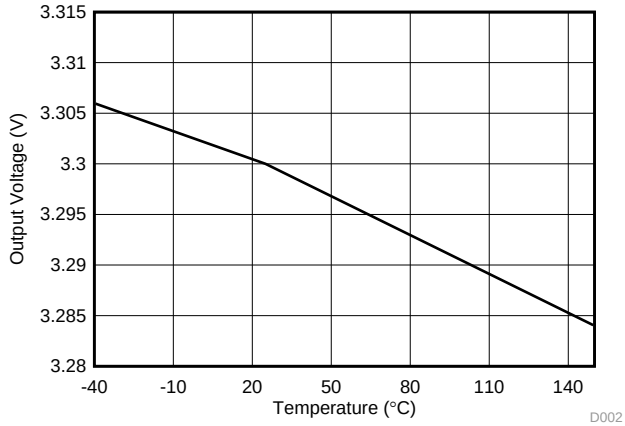
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{buck}	Bucket capacitor		10	47		nF
C_{CP}	Storage capacitor			100		nF
	Voltage capability of external capacitor at pin CP, CP1, CP2	The external capacitor to GND must chosen according these limits	55			V
VCP-ON	CP output voltage in ON state	6.2 V < V_{VIN} < 38.5 V; I_{CP} = 100 µA (external load at CP)	V_{VIN} + 5		V_{VIN} + 15	V
		4 V < V_{VIN} < 6.2 V; I_{CP} = 100 µA (external load at CP)	V_{VIN} + 2.6			
I_{CP}	External current capability	Static load	100			µA

6.22 Typical Characteristics



No load

Figure 1. VDD5 Output Voltage



No load

Figure 2. VDD3 Output Voltage

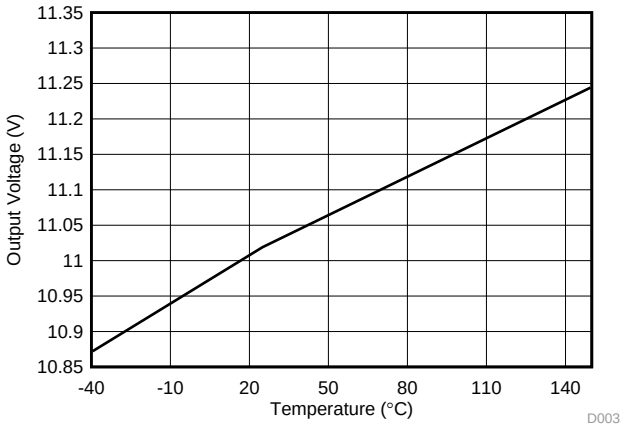
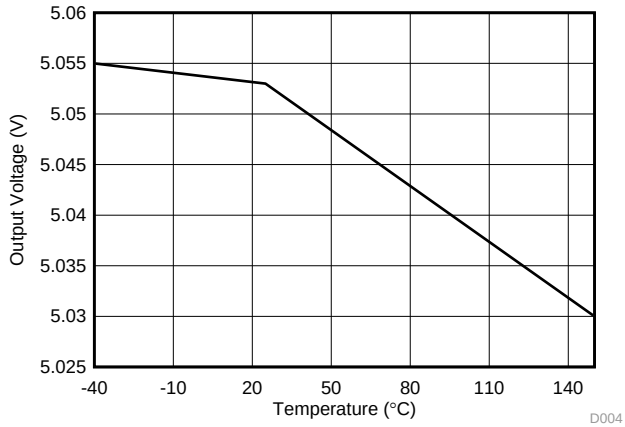
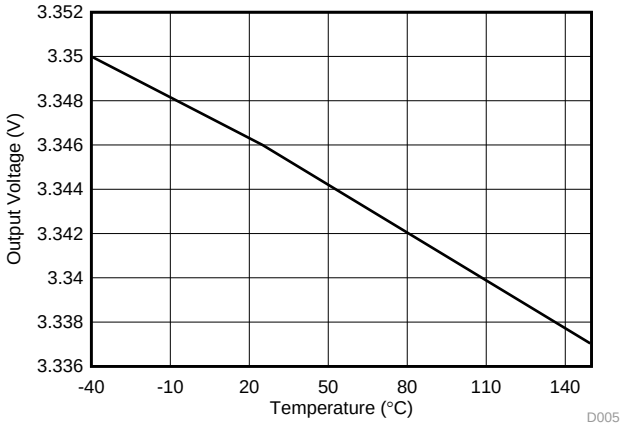


Figure 3. VDD1GATE Voltage at V_{VIN} = 12 V



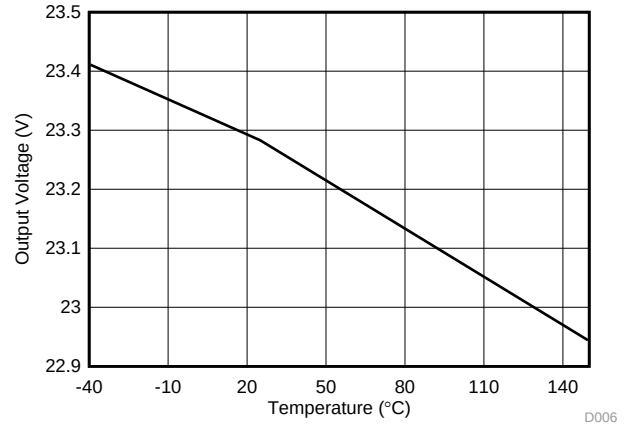
Maximum step, no load

Figure 4. VDD5 Output Voltage During VIN Step from 5.1 V to 13.5 V Within 10 µs



Maximum step, no load

Figure 5. VDD3 Output Voltage During VIN Step from 5.1 V to 13.5 V Within 10 µs



V_{VIN} = 12 V

Figure 6. CP Output Voltage

7 Detailed Description

7.1 Overview

The TPS99110-Q1 device is a system-basis chip that integrates the features required for the basis of an ECU for automotive applications. The device receives power from the 12-V vehicle battery and integrates the complete power supply for such a system, consisting of two LDO controllers (PRE1 and PRE2), an adjustable LDO regulator ranging from 0.8 to 2.6 V (VDD1), an LDO regulator with a fixed 3.3-V output (VDD3), and an LDO regulator with a fixed 5-V output (VDD5). The PRE1, PRE2, and VDD1 pins drive external NMOS transistors.

The device integrates three sensor-supply outputs to provide the supply voltage for peripheral sensors in the automotive system. Two of the outputs are configurable as adjustable through serial peripheral interface (SPI) or in VDD5 tracking mode. The third output is only available in VDD5 tracking mode. Each sensor output has voltage and current monitoring and can be turned on or off by the internal logic as required by the specific application.

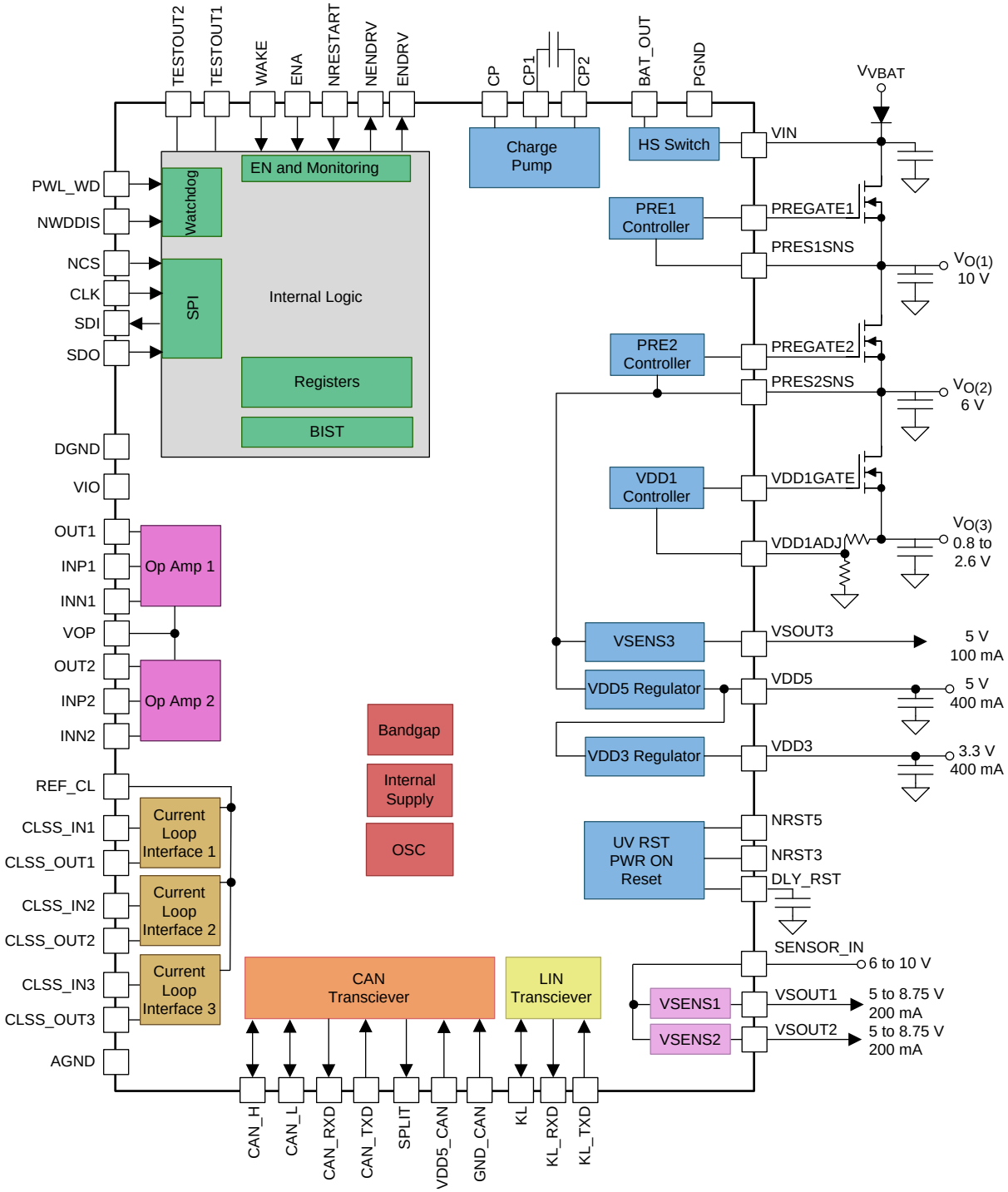
The device includes voltage monitoring on power up and throughout operation. For the internal linear regulators, a specific sequence must be met and all voltages must meet a certain threshold, otherwise the device faults and outputs reset signals. The device also includes thermal protection and current monitoring on the internal regulators along with the communication and sensor interfaces.

Two operational amplifiers, which are independent of each other, are integrated into the TPS99110-Q1 device. The inputs are not connected to the internal logic which gives the user complete control over how the inputs are used within their own application.

Three independent current-loop interfaces are featured on the device with current sense input and digital output and are typically used for speed sensors. This interface has open and short protection, along with diagnosis of these conditions that can be checked through device registers.

High-speed CAN (with wakeup) and K-Line (LIN) transceivers are included in the device. Other integrated functions include an SPI communication interface with the MCU, programmable wakeup event timer, enable logic, and restart input. MCU monitoring functions include a pin-input window watchdog or dual Q&A watchdog units over SPI.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supply

The power supply of the TPS99110-Q1 device consists of several blocks that provide several different output voltages for different parts of an automotive system. The power supply has two linear preregulators using external NMOS FETs, with the option to bridge either of the external transistors. Three additional linear regulators are also included. The VDD1 regulator (external MOS pass transistor) has an adjustable output ranging from 0.8 to 2.6 V, with an external voltage divider as feedback. The VDD3 and VDD5 supplies have 3.3-V and 5-V outputs, respectively. The VDD3 supply is supplied internally from the 5-V output. Both VDD5 and VDD3 use internal pass-transistor FETs. The power-up and power-down sequencing is as follows: VDD5 → VDD3 → VDD1.

The power supply has three sensor-supply outputs: VSOUT1, VSOUT2, and VSOUT3. The VSOUT1 and VSOUT2 outputs are configurable through SPI and can be connected by the SENSOR_IN pin to the PRE1 or PRE2 pins to optimize power dissipation. The VSOUT1, VSOUT2, and VSOUT3 outputs can all be set to track the VDD5 output. These outputs have thermal overload protections as well as short-circuit-to-battery and ground protection. Each of these outputs is designed to operate in a stable condition without an external load. Figure 7 shows the block diagram of the power supply concept.

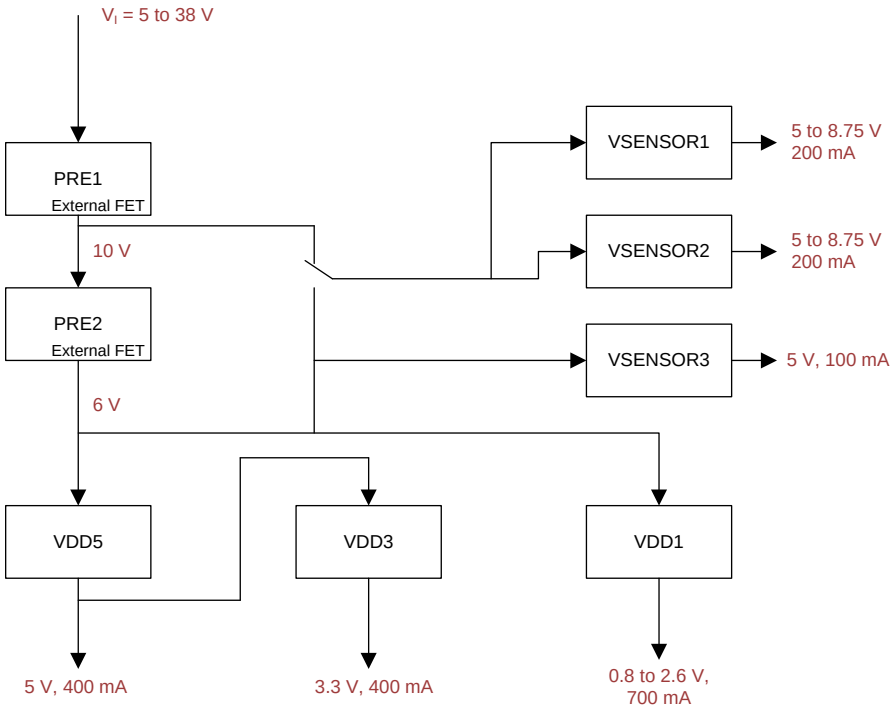


Figure 7. Block Diagram Showing the Power Supply Concept

The power supply block in total is regulating the battery voltage to several outputs: 5 V, 3.3 V, the adjustable output (0.8 to 2.6 V), and sensor supplies. To optimize power consumption, two linear regulators in series with external power devices are used. One in-series regulator is connected between the battery (after reverse battery protection) and the PRE1SNS pin is regulated at 10 V. The other in-series regulator is connected between the PRE1SNS and PRE2SNS pins and is regulated at 6 V. As the power dissipation is mainly proportional to the voltage difference between input and outputs, the two external power NMOS are controlled like a ballast transistor to reduce the PRE1SNS and PRE2SNS voltages of TPS99110-Q1 device. Therefore, the total power dissipation is shared between the TPS99110-Q1 device and the external power devices.

Feature Description (continued)

The PRE1GATE and PRE2GATE pins are used to drive the gate of the power devices. To fully switch-on these regulators at a low battery voltage, the PRExGATE-pin drivers receive additional DC current from the charge pump output, CP. The battery voltage inputs pins, PRE1SNS and PRE2SNS, should be protected against negative voltage levels by an external reverse protection diode keeping the negative voltage at the PRE1SNS and PRE2SNS pins above
–0.3 V. In the off condition the leakage current at all pins connected to battery is low enough to not drain the battery in a car. The linear regulators, VDD5, VSOUT3, and VDD1, are connected to the PRE2SNS pins.

7.3.2 VDD5

The 5-V supply output, VDD5, typically supplies all peripherals and the microcontroller inside the ECU. The tight accuracy of ±2% at the VDD5 supply output (including temperature and long-term drift as well as line and load regulation) allows the output to also be used as a reference voltage inside an ECU. The VDD5 supply output limits the output-voltage overshoot during power up or during line or load transients. This limiting prevents the connected devices from being destroyed or damaged by exceeding the supply-voltage maximum ratings.

7.3.3 VDD3

The 3.3-V supply output, VDD3, typically supplies the microcontroller inside the ECU. The tight accuracy of ±2% at the VDD3 supply output (including temperature and long-term drift as well as line and load regulation) allows the output to also be used as a reference voltage inside an ECU. The VDD3 supply output limits the output-voltage overshoot during power up or during line or load transients. This limiting prevents the connected devices from being destroyed or damaged by exceeding the supply-voltage maximum ratings.

7.3.4 VDD1

The adjustable, 0.8- to 2.6-V supply output, VDD1, supplies the microcontroller core or auxiliary devices inside the ECU. To reduce the power consumption, an external power NMOS is used. The regulation loop and the command gate drive are integrated. For this reason an accuracy of ±2% is provided by the VDD1 supply output. This tolerance includes temperature and long-term drift as well as line and load regulation but does not include tolerance of the external resistor divider. The supply output, VDD1, limits output-voltage overshoot during power up or during line or load transients. This limiting prevents the connected devices from being destroyed or damaged by exceeding the supply-voltage maximum ratings. In applications that do not require the VDD1 output, the VDD1ADJ pin must be connected to the VDD3 output. Otherwise the internal undervoltage comparator test fails. The VDD1GATE pin should be left open. The remaining VDD1 components can be omitted.

7.3.5 VSOUTx

The VSOUT1, VSOUT2, and VSOUT3 supplies are sensor-supply outputs. All sensor supplies can be individually turned on or off by the internal logic via SPI registers. The inputs of the VSOUT1 and VSOUT2 regulators can be connected through the SENSOR_IN pin to either the PRE1SNS or PRE2SNS pins, depending on the desired sensor output voltage. The VSOUT3 regulator input is internally connected to the PRE2SNS pins.

The sensor-supply outputs provide short-to-ground protection by limiting the output. Because the short-to-ground outside the ECU can result in a short to –2 V with respect to the ground line inside the ECU, the TPS99110-Q1 device is designed in a way that all other functional blocks inside the component operate according to the specified characteristics. The sensor-supply outputs also provide a short circuit protection to maximum battery voltage. In case of failure at a sensor supply all other functional blocks inside the component operate according to the specified characteristics.

Each sensor-supply output provides two independent fault detection flags to the internal logic of the TPS99110-Q1 device indicating overvoltage (the output voltage is above V_{VSOUTx_OV}) or undervoltage (the output voltage is below VVSOUTx_UV). Each sensor supply has a temperature sensor that provides an independent fault-detection flag to the internal logic of the TPS99110-Q1 device indicating overtemperature if the sensor supply temperature is above T_{max}. The outputs, VSOUT2 and VSOUT3, switch off when the VDD5 supply output is below the VDD5_UV reset threshold. These outputs turn on again when the VDD5 supply output is above VDD5_UV.

Feature Description (continued)

7.3.5.1 Tracking Mode

The VSOUTx outputs typically supply sensors that are external to the ECU. These outputs can be configured to follow the VDD5 voltage with an accuracy of MV_{VSOUTx}. This accuracy includes temperature and long-term drift as well as line and load regulation. The VSOUT1 output follows the VDD5 output supply in all cases (below or above the VDD5_UV reset threshold), even if the VDD5 output supply goes below the reset threshold.

7.3.5.2 Adjustable Mode

In this mode the level of the VSOUT1 and VSOUT2 outputs are selectable by SPI. These outputs typically supply sensors which are external to the ECU with an accuracy of ±3%. This tolerance includes temperature and long-term drift as well as line and load regulation. Table 1 lists the 16 possible values of the output voltage.

Table 1. Output Voltage Values

NUMBER	MDOE	CONFIGURATION BITS	VSOUTx VOLTAGE (V)	CONNECTION OF SENSOR_IN	ACCURACY (mV)
0	Tracking	0000	VDD5	PRE1SNS and PRE2SNS	±15
1	Adjustable	0001	5.25	PRE1SNS and PRE2SNS	±157
2		0010	5.5		±165
3		0011	5.75		±172
4		0100	6	PRE1SNS	±180
5		0101	6.25		±187
6		0110	6.5		±195
7		0111	6.75		±202
8		1000	7		±210
9		1001	7.25		±217
10		1010	7.5		±225
11		1011	7.75		±232
12		1100	8		±240
13		1101	8.25		±247
14		1110	8.5		±255
15		1111	8.75		±262

7.3.5.3 VSOUT3

This tracking output (VSOUT3) follows the VDD5 voltage. The accuracy specifications given in the *Specifications* section includes temperature and long-term drift as well as line and load regulation.

7.3.6 Undervoltage RESET and Power-on Sequencing

During power up of any supply, the TPS99110-Q1 device ensures that the NRST3 or NRST5 pin is held low, high-level on ENDRV, and low-level on NENDRV. As stated in the *Power Supply* section, the power-up and power-down sequencing is as follows: VDD5 → VDD3 → VDD1.

The device has two reset outputs, NRST5 and NRST3. The NRST5 output triggers an undervoltage reset if the VDD5 supply output is below the threshold and is active down to V_{VDD5} = 1 V. The NRST3 output triggers if the VDD3 or VDD1 output supplies are below the respective thresholds. The NRST3 output is active down to V_{VDD3} or V_{VDD1} = 0 V, and a reset assertion on the NRST3 output immediately asserts a reset on the NRST5 output. When the device begins to switch-off, both NRST3 and NRST5 outputs immediately output a low level independent of the VDD5, VDD3, or VDD1 output supplies while still being above the threshold. A configurable mode for the bidirectional NRESTART pin allows the assertion of internal resets without generating microcontroller reset through the NRST3 or NRST5 output. The VDD5, VDD3, and VDD1 output supplies are all supervised in case the output supplies fall below the respective thresholds.

For an initially powered device, the reset delay is defined by an internal constant value. In active mode, the reset delay can be enabled for digital control and programmed through SPI for different reset-off delay times depending on the reset source. These programmed conditions are stored as long as the VIN is supplied and kept above minimum threshold during reset event.

7.3.6.1 Supply Voltage Supervisor

The VDD5 supply line is monitored and, if the VDD5 supply-output voltage drops below the low reset threshold, the reset output, NRST5, outputs a low level.

The VDD3 and VDD1 supply lines are monitored. If the VDD3 or VDD1 (respective to VDD1ADJ) supply-output voltage drops below the low reset threshold, both reset outputs, NRST3 and consequently NRST5, output a low level.

Table 2. NRSTx Response to Undervoltage Condition

SUPPLY	UNDERVOLTAGE CONDITION
VDD1	NRST3 and NRST5
VDD3	NRST3 and NRST5
VDD5	NRST5

7.3.6.2 Reset Delay

For an initially powered device the reset delay is defined by the external resistor at the DLY_RST pin. After all reset conditions have disappeared the reset outputs continues to assert low levels for a duration programmed at the corresponding delay resistor pin. A resistor (R_{DLY_RST}) at the DLY_RST pin to ground causes a delay, $t_{r(off)}$, for the reset outputs, NRST5 and NRST3, to change the output level from a low level to a high level. The reset delay is retriggered by an undervoltage condition at the corresponding supply output. Each NRSTx pin requires a timer to create a reset delay corresponding to the supply line.

In active mode the reset delay can be enabled for the internal logic control and programmed through SPI for different $t_{r(off)}$ depending on the reset source. These programmed conditions are stored as long VIN is supplied and kept during reset event.

To calculate the resistance value for DLY_RST, see the *DLY_RST Resistance Calculation* section.

7.3.7 Current-Loop Interface

The three independent current-loop interfaces each have two pins for current-sense input and digital output. The current detector has a high and low threshold, $I_{(HIGH)}$ and $I_{(LOW)}$. The output voltage is low when the input current is less than $I_{(LOW)}$, and high when the input current is higher than $I_{(HIGH)}$. The interface displays Schmitt-Trigger behavior with individual SPI-programmable values for average threshold (4 bit) and hysteresis (2 bit). The output is push-pull with the high level being V_{IO}. A separate overtemperature sensor for each channel signals if the local die temperature is greater than or equal to T_{max} through SPI registers. Independent current limitation is also available with individual diagnosis through SPI.

To calculate the resistance value for REF_CL, see the *REF_CL Resistance Calculation* section.

7.3.8 CAN Transceiver

The SBC integrates a high-speed CAN transceiver (1 MBaud) with wakeup capability and several other general features including:

- Full compatibility with the ISO 11898 standard Rev.2.0b wakeup functionality
  - Supported data rate of 37 kbps to 1000 kbps
  - 8-kV ESD with respect to ground capability (HBM 100 pF, 1500, air-discharge) at CAN-H and CAN-L
  - TXD-dominant time-out detection
  - Internal pullup on CAN_TXD to V_{IO}.
- Wakeup behavior selectable through SPI
  - Three CAN wakeup modes selectable through SPI:
    - CAN wakeup by single dominant pulse for > $t_{(WAKE)}$
    - CAN wakeup by two dominant states for > $t_{(WAKE)}$ when each dominant pulse is followed by a recessive state for > $t_{(WAKE)}$
    - CAN wakeup is disabled when the CAN block is disabled
  - SPI error flag if the CAN bus dominant time out
- Separate internal supply of the CAN output stages (VDD_CAN)

7.3.8.1 CAN_TXD-Dominant Clamping Detection

A permanent low level on the CAN_TXD pin (because of a hardware or software application failure) drives the CAN bus into a permanent dominant state, thus blocking all network communication. The CAN_TXD dominant time-out function prevents such a network lockup by disabling the transmitter of the transceiver if the CAN_TXD pin remains at a low level for longer than the CAN_TXD dominant time-out.

7.3.8.2 Recessive Bus-Voltage Stabilization

When the CAN is enabled, the SPLIT pin provides a stabilized 0.5 × VDD5_CAN DC voltage. A *split* supply is high impedance in the power-down mode.

7.3.9 K-LINE/LIN Transceiver

The SBC integrates a LIN transceiver with the following general features:

- The LIN is in accordance to the LIN specification Rev.2.1 (slave without wakeup), K-Line according to ISO9141 specification.
  - The transmission speed at the K-line can go as high as 250 kbps.
  - The LIN_RxD and LIN_TxD pins are noninverting control signals with respect to the LIN pin.
- The LIN is disabled when the VDD5 pin is below the VDD5_UV reset threshold and is enabled when the VDD5 pin is above the VDD5_UV reset threshold (configurable by SPI).

The transceiver functionality can be chosen to be either KLINE or LIN through a configuration bit within TPS99110-Q1 SPI configuration register. K-Line mode is configured as the default mode for start-up and the initial programming purpose. LIN mode must be configured actively by an SPI command.

Table 3. Driver Modes

VDD5_UV (UNDERVOLTAGE)	ENDRV	SPI (KLIN_TXD_EN)	MODE
1	X	X	Disabled
0	0 (off)	0	Listen only
0	X	1	Normal
0	1 (on)	X	Normal

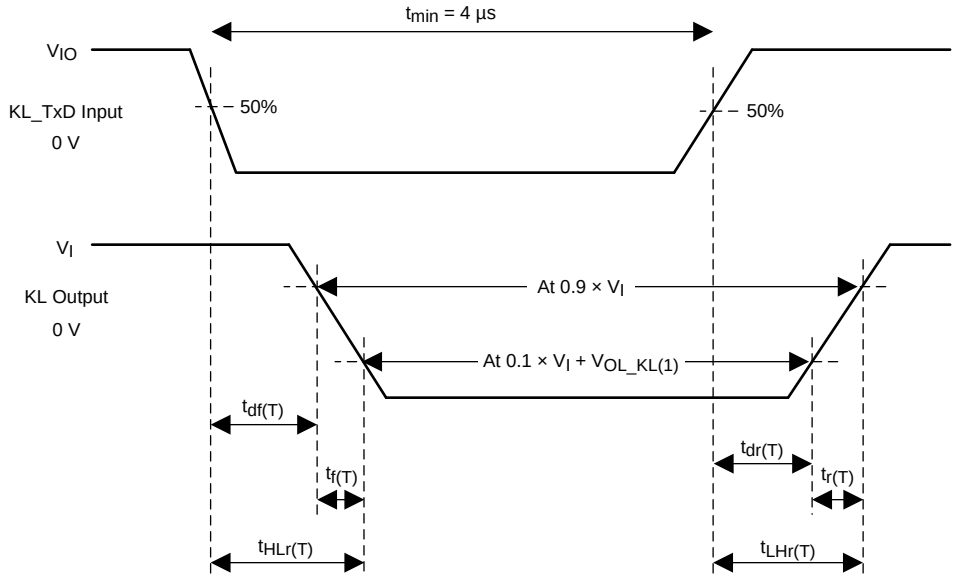


Figure 8. KL Transmitter
Turn-On and Turn-Off Transmitter Timing KL_TxD Pin to KL Pin

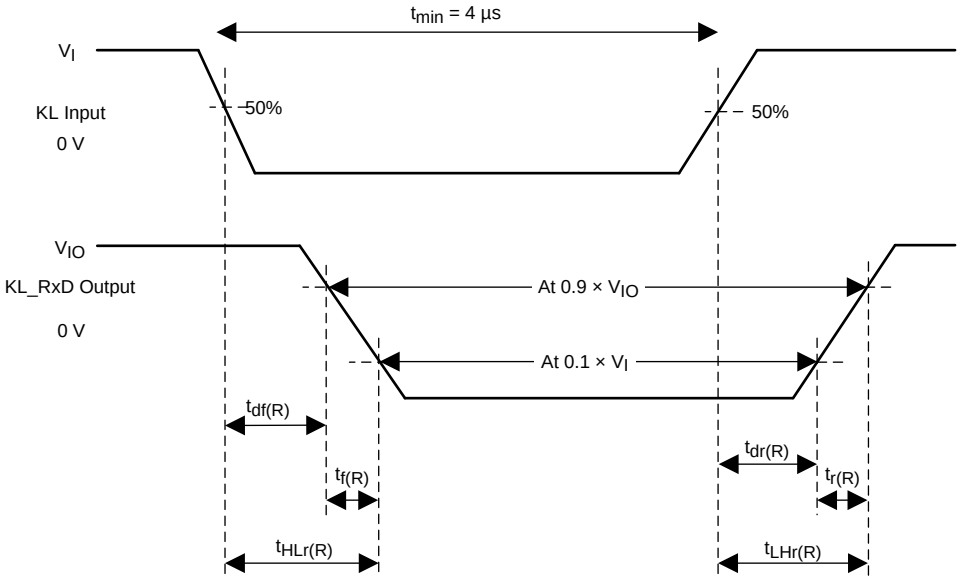


Figure 9. KL Receiver
Turn-On and Turn-Off Receiver Timing KL Pin to KL_RxD Pin

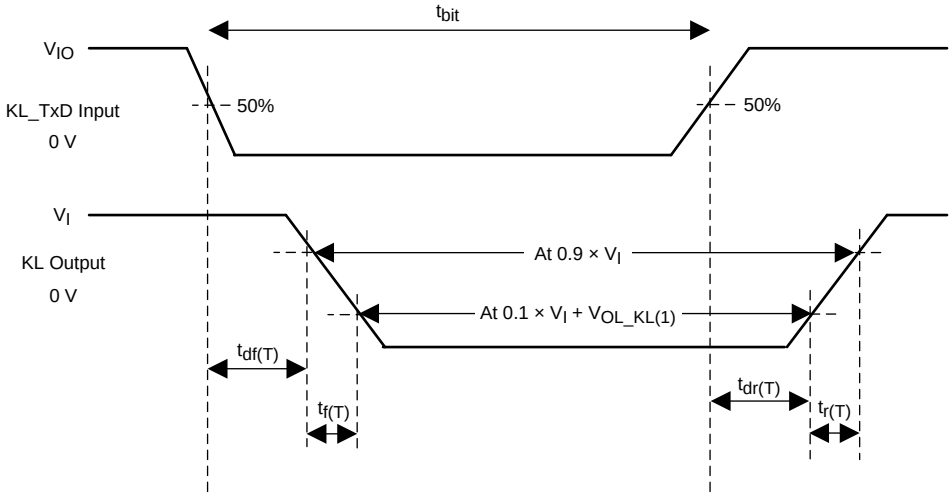


Figure 10. LIN Transmitter
Turn-On and Turn-Off Transmitter Timing KL_TxD Pin to KL Pin

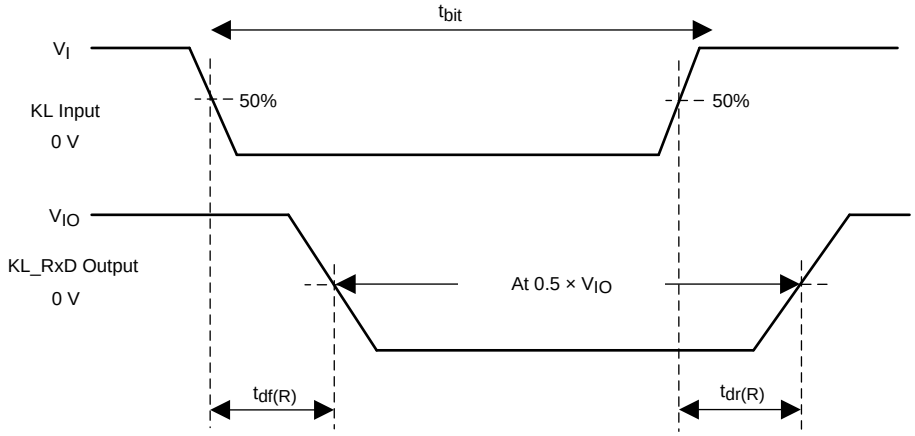


Figure 11. LIN Receiver
Turn-On and Turn-Off Receiver Timing KL Pin to KL_RxD Pin

7.3.10 Operational Amplifiers

The SBC integrates two operational amplifiers (op amps) that are independent of each other. The supply to these op amps is through the VOP pin. Both op amps are fully functional with injection current into inputs, rail-to-rail input and output, and push-pull output. The op amps dissipate minimal power within the device with low input bias and offset currents and low input-offset voltage. The op amps also have a wide operational range with a high gain-bandwidth product. If unused, the operational amplifier pins require no special connection because the circuit block is not connected to the internal logic. The op amps are disabled when the VDD5 pin is below the VDD5_UV reset threshold and is enabled when the VDD5 pin is above the VDD5_UV reset threshold.

7.3.11 Wakeup Timer

The SBC features a wakeup threshold that is loaded through SPI. The timer begins at zero when standby is reached, and wakes up the TPS99110-Q1 device if the threshold is met and a wakeup by timer is enabled through SPI. After the device is awakened by the wakeup by timer function, the wakeup functionality is disabled. The bit width of the timer is 24 bits, the resolution is 100 ms, and the threshold is SPI programmable.

7.3.12 Device State Controller

The device state controller controls initialization, wakeup, and sleep sequences to and from the STANDBY and ACTIVE primary operating states. An error detected during a wakeup sequence aborts the sequence and initiates a transition to the STANDBY state. An error-free wakeup sequence ends in a transition to the ACTIVE state. A sleep sequence is launched from the ACTIVE state upon standby request. A sleep sequence always ends in a transition to the STANDBY state.

Figure 12 shows a device-state transition diagram. The system clock is enabled following the release of the power-on reset (nPOR = 1). The device configuration data is downloaded from nonvolatile memory. Upon completion, the device enters the STANDBY state. The system clock is disabled in this state.

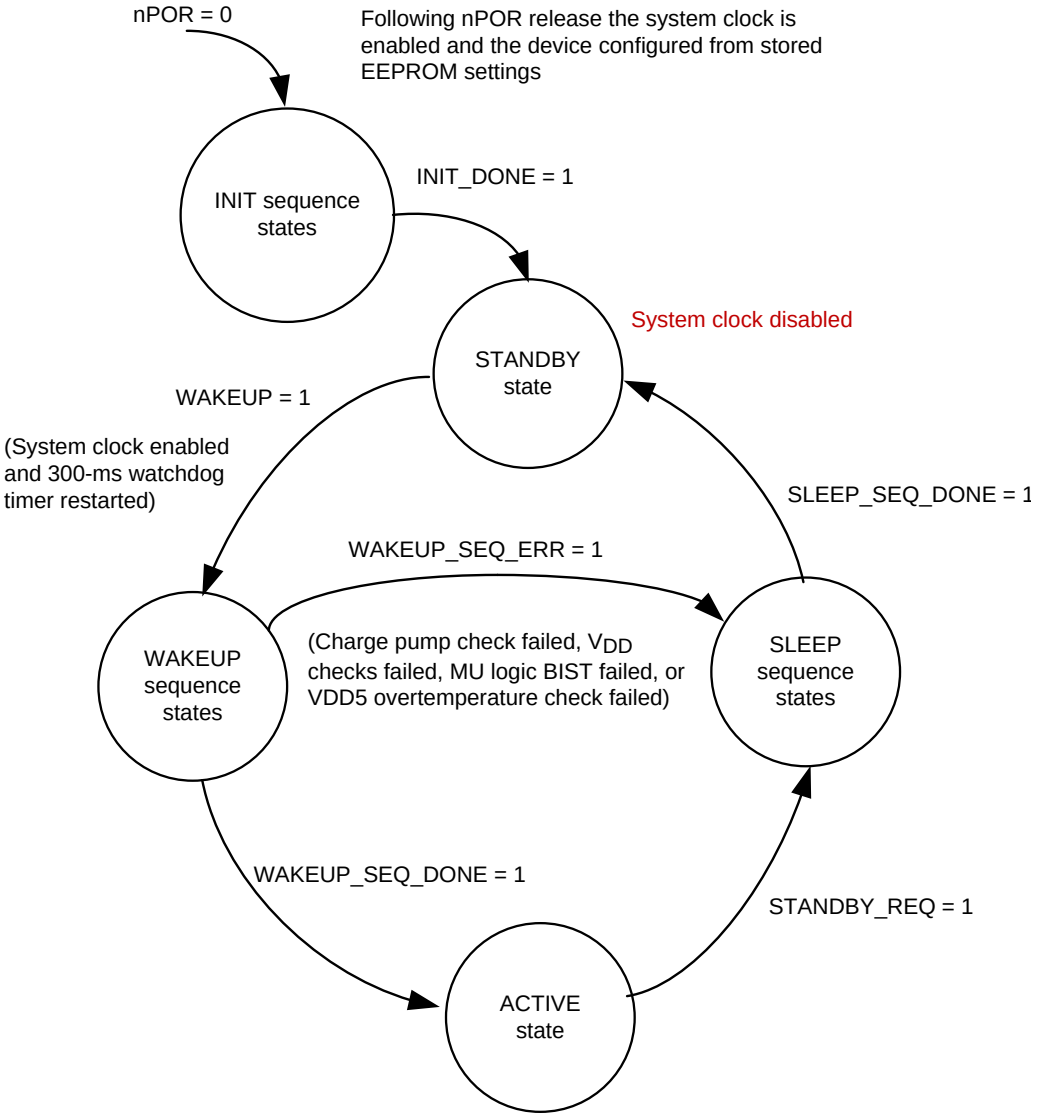


Figure 12. Device State Control Diagram

7.3.12.1 Wakeup

A wakeup event is required to transition out of the STANDBY state. The event can be triggered from any of the four following sources: CAN wakeup module, ENA pin, WAKE pin, or wakeup timer. Each wakeup event is latched in a SPI register for source identification. Table 4 lists a summary of the wakeup sources.

Table 4. Wakeup Sources Summary

WAKEUP SOURCE	TRIGGER OPTIONS	SOURCE ENABLE
CAN wakeup module	Defaults to wakeup upon a double received data transition. SPI register bit CANSINGLE can be set to 1 to switch to wakeup upon a single received data transition.	Enabled, unless explicitly disabled through SPI registers bits CANWKEN1 and CANWKEN2. These bits must be set to 0 and 1, respectively, to disable CAN wakeup option.
ENA pin	A logic high level	Always enabled
WAKE pin	A rising or falling edge or if at a high logic level after the power-on reset is released	Always enabled
Wakeup timer	The time-out period is configurable thru SPI in the range of 0 s to approximately 466 hr in increment of 0.1 s.	Disabled by default. SPI can enable by setting the TIMERWKEN bit to 1.

A wakeup event restarts a 300-ms time-out watchdog timer. A wakeup sequence error (WAKEUP_SEQ_ERR = 1) is generated if this timer expires before the ACTIVE state is reached. Wait-for-condition checks are performed throughout the wakeup sequence. These conditions include VDD undervoltage, charge pump undervoltage, VDD5 overtemperature, and MU logic BIST run-time. The accumulated time for these checks to complete must fall under the 300-ms watchdog time-out threshold to prevent a transition back to the STANDBY state.

7.3.12.1.1 Standby

A standby request is automatically generated upon a VDD5 overtemperature indication or, while the ENA pin is in a low logic state, upon a watchdog time-out or SPI-triggered event. The later is achieved through writing the standby mode request 24-bit code (0xA2FD02) to the CHANGE_STATE register.

If the ENA pin is in a logic high state when a VDD5 overtemperature condition triggers a transition to STANDBY, a wakeup event is generated upon entering the state because a logic high level at the ENA pin is a wakeup source (see Table 5). If the VDD5 overtemperature persists longer than 300 ms, a wakeup sequence error is generated. The device does not return to the ACTIVE state until the VDD5 overtemperature condition is removed.

Table 5. Standy Request Source Summary

STANDBY REQUEST SOURCE	ENA PIN LOGIC STATE	TRIGGER EVENT
Watchdog	0	Active state 1-s watchdog time-out
SPI	0	SPI writes 0xA2FD02 into the CHANGE_STATE register
VDD5 OT	X	VDD5 overtemperature indication

7.3.12.2 Monitor Unit (Question-Answer Watchdog)

The control of critical external power stages or drivers is the responsibility of the monitoring unit. This module contains two identical microcontroller monitoring units used to check that the microcontroller is functioning normally. The module also monitors internal critical fault indicators and the current device state. The external output enable is asserted only if the device is in the ACTIVE state, the microcomputer is functioning properly, and no internal faults or active resets are present.

Use of two microcomputer monitoring units allows defining of up to 32 unique microcomputer check sequences, 16 per microcomputer monitoring unit. The second unit can be disabled if not required.

To check that the monitoring unit remains logically correct, a scan vector-based BIST is automatically executed during device standby to active mode transitions. A BIST error prohibits the enabling of the external power stages and drivers. The BIST status, pass or fail indication, and final signature value, is available in a read-only SPI register.

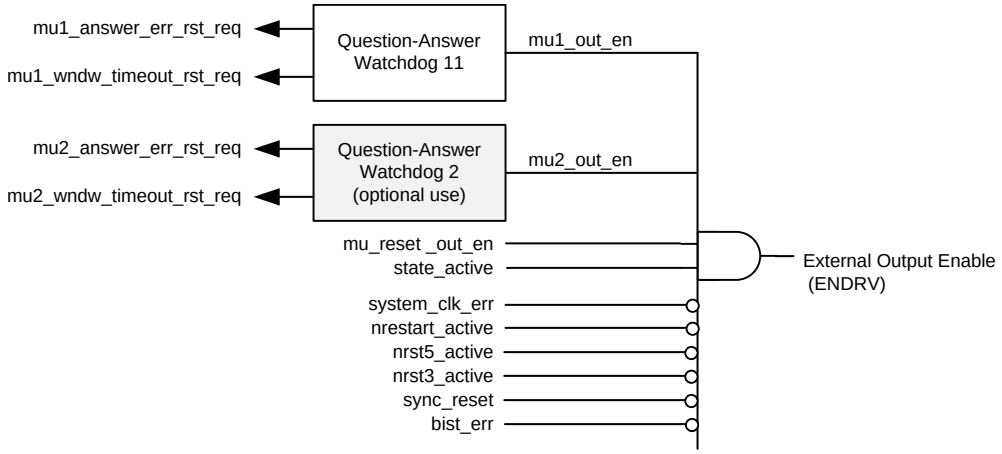


Figure 13. Monitoring Unit External Output Enable Activation

7.3.12.2.1 Microcomputer Monitoring Unit (Question-Answer Watchdog)

The microcomputer monitoring unit employs a question-and-answer scheme to the microcomputer. The monitoring unit provides the questions, then checks the answers of the microcomputer. Each question requires the microcomputer to run a specific task to come up with the correct answer. Each task should include program flow and instruction-set type checks. Each sequence of checks must pass to yield the correct answer.

The microcomputer monitoring unit checks that answers are received within a valid answer time-window and uses a look-up table to check answer values. An error counter is incremented or decremented depending on whether a valid response was received or not. A new question is not generated until the current question is responded to successfully. Both the valid answer time-window and error count thresholds are configurable.

The module generates two reset requests. One is generated whenever an error threshold value is reached because of an accumulation of wrong answers or because answers are not provided within the valid answer time-window. The other reset request is generated if the monitoring-unit state machine times out after receiving the SPI command to lock-in the monitoring unit configuration and does not receive the next SPI command to transition to the normal operating state within 50 ms. These requests are monitored and contribute to forming the mu_reset_out_en shown in Figure 13. The SPI register enables for the reset-request generation of the reset request generation is enabled by default.

The microcomputer monitoring unit generates a sequence of 16 questions in a pseudorandom order. A 4-bit linear-feedback shift register is used to maintain the questions generator after each 16 question sequence. This maintenance ensures every microcomputer check sequence is performed once for every 16 questions generated. Table 6 lists all possible question sequences.

Table 6. Question Code Sequences

	QUESTION NUMBER															
LSFR	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	3	2	5	4	7	6	9	8	11	10	13	12	15	14
2	2	3	0	1	6	7	4	5	10	11	8	9	14	15	12	13
3	3	2	1	0	7	6	5	4	11	10	9	8	15	14	13	12
4	4	5	6	7	0	1	2	3	12	13	14	15	8	9	10	11
5	5	4	7	6	1	0	3	2	13	12	15	14	9	8	11	10
6	6	7	4	5	2	3	0	1	14	15	12	13	10	11	8	9
7	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
8	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
9	9	8	11	10	13	12	15	14	1	0	3	2	5	4	7	6
10	10	11	8	9	14	15	12	13	2	3	0	1	6	7	4	5
11	11	10	9	8	15	14	13	12	3	2	1	0	7	6	5	4
12	12	13	14	15	8	9	10	11	4	5	6	7	0	1	2	3
13	13	12	15	14	9	8	11	10	5	4	7	6	1	0	3	2
14	14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1
15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Each 4-bit question code has a unique 4-bit answer code. The answer codes are stored in a look-up table. These codes are not configurable. Table 7 lists the answer code for each possible question code.

Table 7. Answers Look-Up Table

QUESTION CODE	ANSWER CODE
0	14
1	10
2	6
3	2
4	15
5	11
6	7
7	3
8	12
9	8
10	4
11	0
12	13
13	9
14	5
15	1

Figure 14 shows a typical start-up sequence. The MCU initiates a Q&A session by writing the end-of-initialization (EOI) command after it has completed configuring the microcomputer monitoring unit. The monitoring unit runs in switched off program-timing checks (SOPC) mode at this time. During this mode, timed responses to questions are not monitored. The MCU has 50 ms from the time it sends the EOI command to the time it sends the end-of-SOPC (EOSOPC) command to transition the monitoring unit to the normal valid-answer window mode.

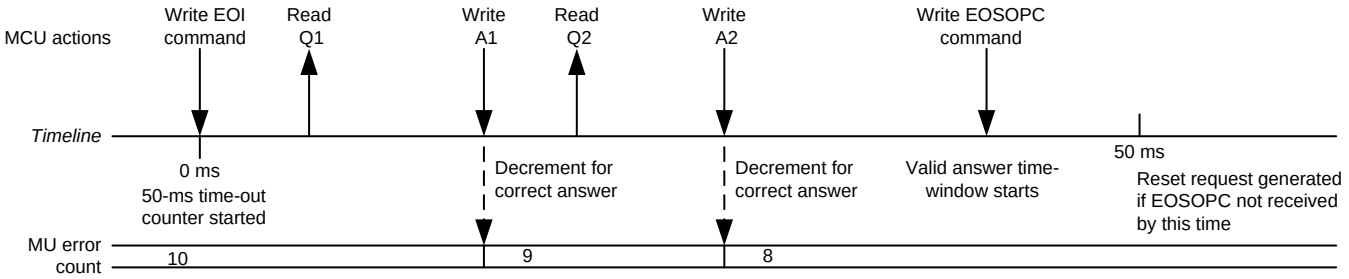


Figure 14. Q&A Open Window Sequence Example

Figure 15 shows a typical Q&A sequence following a transition to the valid answer window mode. After writing the EOSOPC command, the valid answer time-window is generated using SPI programmed values TWIND and TRESP. Each window can programmed from 0 to 255 ms in 1-ms increments. Each correct response, such as a correct answer received within the valid answer time-window, decrements the error counter by 1. Each incorrect response increments the error count by two. The valid answer time-out window-generation function restarts for each correct answer received.

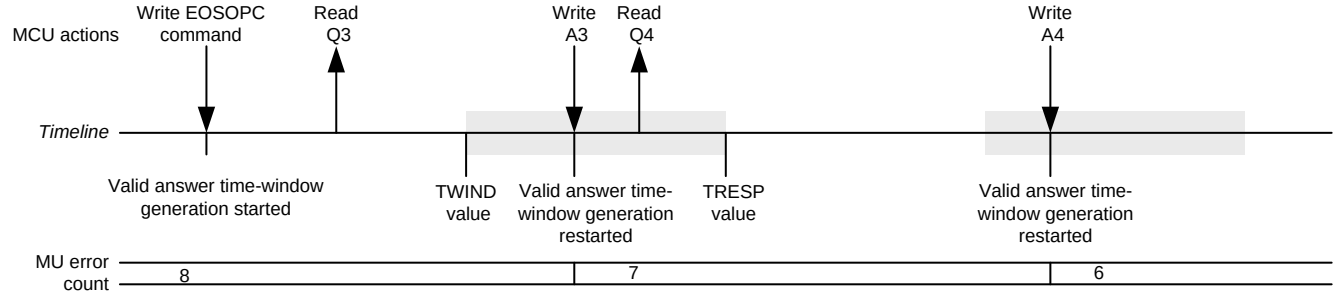


Figure 15. Q&A Valid Answer Window Sequence Example

7.3.12.3 Open-Close Window Watchdog

The ACTIVE-state watchdog function is enabled when a logic high is applied to the NWDDIS pin. Up to six triggers can each restart the 1-s timer of the watchdog. These include a rising edge on device pin PWL_WD, a device state transition to the ACTIVE state, a valid SPI-frame reception, a VDD3 undervoltage condition, a VDD1 undervoltage condition, or a synchronous reset not because of a VDD3 or VDD1 undervoltage condition.

The valid SPI-frame received trigger is disabled by default. The SPIWDTRG bit must be set to 1 to enable this trigger source.

If the timer is allowed to time-out, either a reset request or standby request is generated. Which gets generated depends on the state of the ENA pin. If this input is at a logic-high state, the reset request is generated and the device remains in the ACTIVE state. If the ENA pin is in a logic-low state, the standby request is generated which transitions the device to the STANDBY state.

In the case of a VDD3 or VDD1 undervoltage condition, the watchdog timer restarts at the time the condition is detected. The synchronous reset, asserted for as long as a VDD3 or VDD1 undervoltage condition is present, is not used in this situation which allows the timer to count down. If the condition is resolved within the 1-s time-out period, the device remains in the ACTIVE state. However, if the ENA pin is at a logic-low state the device transitions to the STANDBY state.

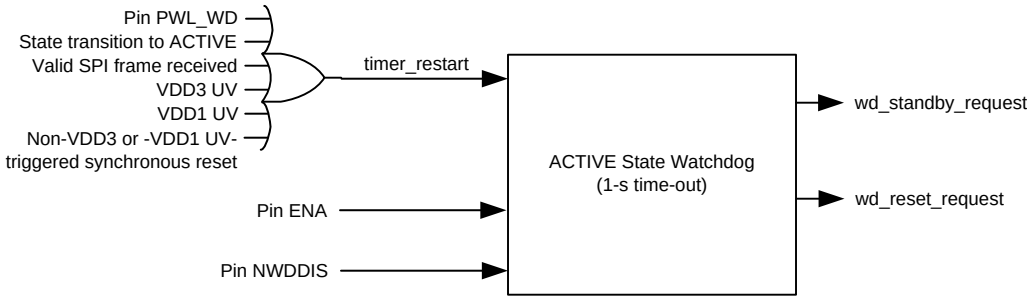


Figure 16. ACTIVE Watchdog Control Inputs and Outputs

7.3.12.4 Device Configuration Register Protection

The data from the device configuration register is monitored by a function designed to detect all single-bit and most 2-bit unexpected state changes to each 24-bit data word of the register. This monitoring occurs using a cyclic redundancy check (CRC) algorithm to periodically compute a 3-bit check-sum for each device configuration register and compare the result with the saved checksum calculated the last time the register was updated using the SPI.

If a check-sum mismatch occurs, a CRC error flag is set in the DIAG2 register, an internal synchronous reset is generated, and external resets, NRST3 and NRST5, are generated. The device configuration registers are restored to the default values.

CRC checking is enabled when there are no ongoing SPI write transaction. Each protected device configuration register is checked in sequence. The sequence repeats after the last register in the group is checked. The list of protected device configuration registers is listed in the SPI registers, CRC1 and CRC2. These read-only registers provide the 3-bit CRC check-sums associated with the protected device configuration registers.

CRC checking stops for three system clock cycles whenever an ongoing SPI write transaction occurs. If the write operation targets one of the protected device configuration registers, a new 3-bit CRC is calculated and saved to SPI register CRC1 or CRC2 during this period. This function ensures only SPI updates to device configuration registers are expected and taken into account through new CRC check-sum calculations.

7.3.12.5 Synchronous Reset

The synchronous reset is asserted upon a wakeup event and is maintained in this state until there are no VDD5, VDD3, and VDD1 undervoltage indications, signaling all supplies are stable, and the monitoring unit logic BIST has completed without an error. After deassertion, just before entering the ACTIVE state and while in the ACTIVE state, the synchronous reset can be triggered either by a watchdog time-out event, through the SPI, by a supply undervoltage condition, by the monitoring unit, through the NRESTART pin, or internal error conditions. All of the synchronous reset triggers are listed as follows:

- One-second WDT time-out while the ENA pin = 1 (when the WDT is enabled)
- SPI write to the CHANGE_STATE register requesting an internal sync reset (0xA3F04), a software reset (0xA1FE01), or transition to STANDBY (0xA2FD02). The standby request is executed only if the ENA pin is in the logic-high state.
- VDD3 or VDD1 undervoltage indication
- Device configuration registers protection CRC error
- System clock error
- The NRESTART pin assertion when NRST3 is not active
- Microcomputer monitoring unit time-out or answer error reset

The sync reset is used to reset the SPI-to-registers interface and SPI clock error detection logic, the enable output of the monitoring unit and microcomputer monitoring units, the low-power clock monitor, the device configuration register protection function and the associated DIAG1 and DIAG2 register bits, and the CRC1 and CRC2 registers.

Table 8. Synchronous Reset Affected Logic

FUNCTION	AFFECTED LOGIC
Monitoring Unit	Enable output (to ENDRV pin)
	Microcomputer monitoring unit 1
	Microcomputer monitoring unit 2
SPI Slave	SPI clock error logic
Registers	SPI-registers interface
	Device configuration registers: CHANGE_STATE, TIMER_THRESH, POR_CONFIG, SYNC_CONFIG, CLSS, VSOU, MU1_CONFIG, MU2_CONFIG, and MU_RSTEN
	Device configuration CRC registers: CRC1 and CRC2
	Device configuration register protection function
	Diagnostics registers: DIAG1[23:12] and DIAG2[2]
Low-power clock monitor	Entire function

Reset events are logged in the DIAG1 SPI register. The bits remain set until cleared through SPI. The last reset that is logged is saved to the SOURCE[22:10] SPI register. Only 1 bit in this bit field is asserted at any time. The SPI can write 1 to any bit in DIAG1 to clear it.

7.4 Device Functional Modes

7.4.1 Standby Mode

Standby mode is the mode in which all external regulators are turned off and there is no communication possible on the CAN interface. To enter into Standby mode, simply power up the device with no signal applied to ENA or a transition pulse to WAKE, the device will go into Active mode to download the EEPROM settings, then transition into Standby. In a typical application, the ignition of an automobile acts as the wake up source. See the *Standby* section within the state descriptions for more information.

7.4.2 Active Mode

Active mode is entered if a signal applied to ENA on battery power up, or if a transition pulse from high-to-low or low-to-high is applied to the WAKE pin in Standby mode. In Active mode, all functions are available for use, including all external regulators, and communication interfaces. If Active mode has some functional limitation, a fault is occurring somewhere which can be deduced through the SPI registers.

7.5 Programming

7.5.1 SPI Communications

The serial peripheral interface is a 4-signal, full-duplex communications port used for device configuration and control plus reporting diagnostics. The serial output, SDO, is maintained in a high impedance state when the SPI chip select, nCS, is deasserted. These features support slave-mode operation in a multi-bus system.

7.5.1.1 SPI Protocol

SPI frames are 32 bits. The serial input data is sampled at the falling edges of the SPI clock while the serial output data is updated at the rising edges of the SPI clock. The bit order in each direction is from the least significant bit (LSB) to the most significant bit (MSB). Communication is enabled upon assertion of the SPI chip select.

Each input, or command, frame contains four bit fields: a 2-bit reserved field, 24-bit data, 5-bit address, and 1-bit read-write control. Each input frame is decoded as a register read or write command. A response to each command is sent over the next frame following the command. In the case of a read command, the incoming data field is not used.

Programming (continued)

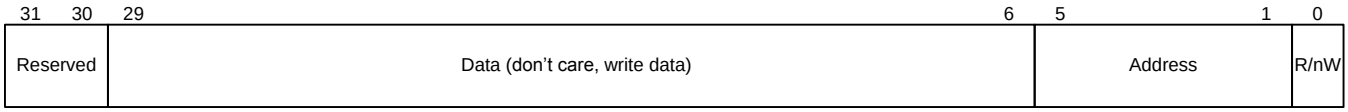


Figure 17. SPI Input Frame Format

Each output, or response, frame contains four bit fields: a 2-bit frame counter, 24-bit data, 5-bit address echo, and 1-bit read/write control echo. The address and read-write (R/W) fields are copies of the address and R/W control fields from the previous input frame. The data field either contains the 24-bit value of the addressed register in response to a read command or a copy of the 24-bit data value written to the addressed register in response to a write command.

The 2-bit frame counter provides status on the internal system clock. The counter is incremented using the system clock at the start of each frame period. If the system clock is not running, the same count value is repeated, otherwise, a pattern is sent as follows: 00b, 01b, 10b, 11b, 00b, 01b, and so on.

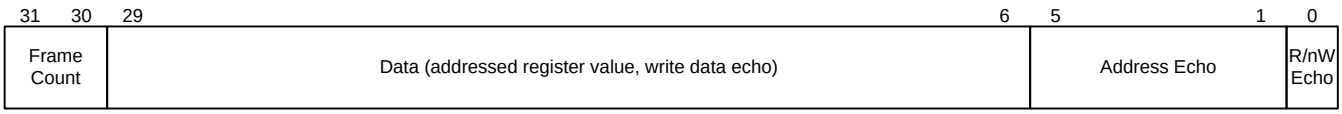


Figure 18. SPI Output Frame Format

The first response frame is the DEVID register value by default. Succeeding responses follow the normal protocol except when a frame error is detected. In these cases, the response to a frame error is a repeat of the last valid frame response. Figure 19 shows an example SPI communication sequence.

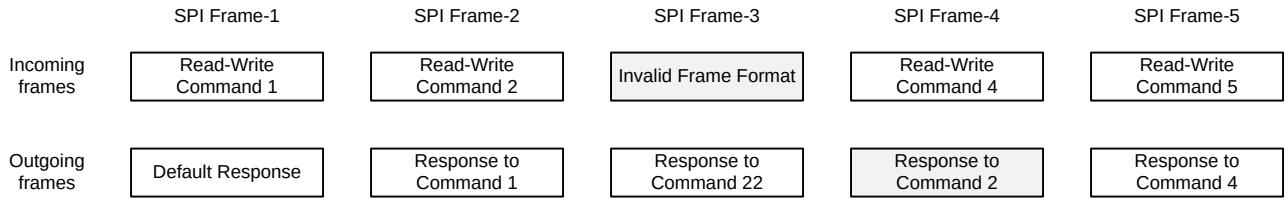


Figure 19. SPI Communication

A valid SPI frame must have the correct number of SCLK rising and falling edges for transmitting and sampling the serial data. In addition, a valid R/W command address must be detected.

7.6 Register Maps

Table 9. Memory Map

Address	Type	Reset	Name
00h	—	—	Reserved
01h	RO	NA	DEVID
02h	R/W	0h	VSOUT
03h	R/W	0h	CLSS
04h	R/W	103h	SYCCFG
05h	R/W	7F8Eb	PORCFG
06h	RWC	7h	DIAG1
07h	RWC	0h	DIAG2
08h	RO	NA	PIN
09h	RO	NA	BIST
0Ah	R	0h	TIMERST
0Bh	R/W	FFFFFFh	TIMERTH
0Ch	R/W	NA	CUST1
0Dh	R/W	NA	CUST2
0Eh	R/W	0h	CHGST
0Fh	R/W	F00000h	MU1CNFG
10h	R/W	3h	MURSTEN
11h	RO	NA	MU1
12h	R/W	0h	MU1ANS
13h	R/W	F00000h	MU2_CONFIG
14h	RO	NA	MU2CFG
15h	R/W	0h	MU2ANS
16h	RO	490852h	CRC1
17h	RO	13Ch	CRC2
18h	RO	0h	SOURCE
19h	RO	0h	DIAGRST
1Ah	—	—	Reserved
1Bh	—	—	Reserved
1Ch	—	0h	TI TEST
1Dh	—	0h	TI TEST
1Eh	—	0h	TI TEST
1Fh	—	—	Reserved

7.6.1 SPI Accessible Registers

7.6.1.1 Reserved Register (offset = 00h) [reset = NA]

Figure 20. Reserved Register

23	22	21	20	19	18	17	16
Reserved							
0h							
15	14	13	12	11	10	9	8
Reserved							
0h							
7	6	5	4	3	2	1	0
Reserved							
0h							

Table 10. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	Reserved	—	0h	Registers not implemented; each bit returns a zero-value when read

7.6.1.2 DEVID Register (offset = 01h) [reset = 00192Ch]

This register will read the same value for the C2 version of the TPS99110-Q1 IC.

Figure 21. DEVID Register

23	22	21	20	19	18	17	16
Reserved				DEVID			
RO-0h				RO-0h			
15	14	13	12	11	10	9	8
DEVID							
RO-19h							
7	6	5	4	3	2	1	0
DEVID							
RO-2Ch							

Table 11. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
23-20	Reserved	RO	0h	Registers not implemented; each bit returns a zero-value when read
19-0	DEVID	RO	0192Ch	Device identification for C2 silicon

7.6.1.3 VSOUT Register (offset = 02h) [reset = 0h]

Figure 22. VSOUT Register

23	22	21	20	19	18	17	16
Reserved							
RO-0h							
15	14	13	12	11	10	9	8
Reserved							
RO-0h							
7	6	5	4	3	2	1	0
VSOUT2				VSOUT1			
RW-0h				RW-0h			

Table 12. VSOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
23-18	Reserved	RO	0h	Registers not implemented; each bit returns a zero-value when read
7-4	VSOUT2	RW	0h	Voltage level select for sensor supply 2
3-0	VSOUT1	RW	0h	Voltage level select for sensor supply 1

7.6.1.4 CLSS Register (offset = 03h) [reset = 0h]

Figure 23. CLSS Register

23	22	21	20	19	18	17	16
Reserved						HYST3	
RO-0h						RW-00b	
15	14	13	12	11	10	9	8
HYST2		HYST1		THRESH3			
RW-00b		RW-00b		RW-0h			
7	6	5	4	3	2	1	0
THRESH2				THRESH1			
RW-0h				RW-0h			

Table 13. CLSS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-18	Reserved	RO	0h	Registers not implemented; each bit returns a zero-value when read
17-16	HYST3	RW	00b	Current-loop speed sensor #3 hysteresis select
15-14	HYST2	RW	00b	Current-loop speed sensor #2 hysteresis select
13-12	HYST1	RW	00b	Current-loop speed sensor #1 hysteresis select
11-8	THRESH3	RW	0h	Current-loop speed sensor #3 threshold select
7-4	THRESH2	RW	0h	Current-loop speed sensor #2 hysteresis select
3-0	THRESH1	RW	0h	Current-loop speed sensor #1 hysteresis select

7.6.1.5 SYCCFG Register (offset = 04h) [reset = 103h]

Figure 24. SYCCFG Register

23	22	21	20	19	18	17	16
Reserved							
RO-0h							
15	14	13	12	11	10	9	8
Reserved							VSOUTEN
RO-NA							RW-100b
7	6	5	4	3	2	1	0
VSOUTEN		CLSSEN			SPIWDTRG	KLINENLIN	KLINTXDEN
RW-100b		RW-000b			RW-0b	RW-1b	RW-1b

Table 14. SYCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
23-9	Reserved	RO	0h	Registers not implemented; each bit returns a zero-value when read
8-6	VSOUTEN	RW	100b	Sensor supply enables
5-3	CLSSEN	RW	000b	Current-loop speed-sensor enables
2	SPIWDTRG	RW	0b	Active watchdog trigger Write this bit to 1 to service the active watchdog function. This bit is self-clearing.
1	KLINENLIN	RW	1b	K-LINE or LIN transceiver select Set this bit to 1 to select the KLINE transceiver otherwise, set this bit to 0 to select the LIN transceiver.
0	KLINTXDEN	RW	1b	K-LINE/LIN transmitter enable Set this bit to 1 the enable the transmitter in the selected transceiver

7.6.1.6 PORCFG Register (offset = 05h) [reset = 7F8Eh]

Figure 25. PORCFG Register

23	22	21	20	19	18	17	16
Reserved							
RO-0h							
15	14	13	12	11	10	9	8
Reserved	VDDRSTTIME						
RO-0h	RW-FFh						
7	6	5	4	3	2	1	0
VDDRSTTIME	RSTCONFEN	CANWKEN2	CANSPLIT	CANWKEN1	CANSINGLE	CANTXDEN	TIMERWKEN
RW-FFh	RW-0b	RW-0b	RW-0b	RW-1b	RW-1b	RW-1b	RW-0b

Table 15. PORCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
23-15	Reserved	RO	0h	Registers not implemented; each bit returns a zero-value when read
14-7	VDDRSTTIME	RW	FFh	Reset extension time
6	RSTCONFEN	RW	0b	Reset extension enable
5	CANWKEN2	RW	0b	Active low CAN wakeup enable
4	CANSPLIT	RW	0b	CAN split enable
3	CANWKEN1	RW	1b	Active high CAN wakeup enable
2	CANSINGLE	RW	1b	CAN single transition wakeup select
1	CANTXDEN	RW	1b	CAN transmitter enable
0	TIMERWKEN	RW	0b	Wakeup timer enable

7.6.1.7 DIAG1 Register (offset = 06h) [reset = 0h]

Figure 26. DIAG1 Register

23	22	21	20	19	18	17	16
CANOTERR	ADDRERR	SCLKERR	LPCLKERR	CANERR	KLINEOTERR	CLSSOTERR	
RWC-0b	RWC-0b	RWC-0b	RWC-0b	RWC-0b	RWC-0b	RWC-0b	
15	14	13	12	11	10	9	8
CLSSOTERR	VSOUTTOERR			CLSSOCURRERR			CLSSOCIRCERR
RWC-0b	RWC-0b			RWC-0b			RWC-0b
7	6	5	4	3	2	1	0
CLSSOCIRCERR		VSOUTOVERR			VSOUTUVERR		
RWC-0b		RWC-0b			RWC-0b		

Table 16. DIAG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	CANOTERR	RWC	0b	CAN over-temperature indicator
22	ADDRERR	RWC	0b	Invalid SPI input frame address received indicator
21	SCLKERR	RWC	0b	Incorrect number of SPI clock edges detected within an active frame period indicator
20	LPCLKERR	RWC	0b	Low power clock error indicator
19	CANERR	RWC	0b	CAN transmit data clamped indicator
18	KLINEOTERR	RWC	0b	K-line over-temperature indicator
17-15	CLSSOTERR	RWC	0b	Current-loop speed-sensor over-temperature indicators
14-12	VSOUTTOERR	RWC	0b	Sensor supply over temperature indicators
11-9	CLSSOCURRERR	RWC	0b	Current-loop speed-sensor overcurrent indicators
8-6	CLSSOCIRCERR	RWC	0b	Current-loop speed-sensor open-circuit indicators
5-3	VSOUTOVERR	RWC	0b	Sensor supply overvoltage indicators
2-0	VSOUTUVERR	RWC	0b	Sensor supply undervoltage indicators

7.6.1.8 DIAG2 Register (offset = 07h) [reset = 0h]

Figure 27. DIAG2 Register

23	22	21	20	19	18	17	16
Reserved							
RO-0h							
15	14	13	12	11	10	9	8
Reserved							
RO-0h							
7	6	5	4	3	2	1	0
Reserved			RSTTIMEOUT	VDD5UV	CRCERR	PWRUPERR	VDD5OTERR
RO-0h			RWC-0b	RWC-0b	RWC-0b	RWC-0b	RWC-0b

Table 17. DIAG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-5	Reserved	RO-0h	0h	Registers not implemented; each bit returns a zero-value when read
4	RSTTIMEOUT	RWC	0b	Reset delay time-out indicator
3	VDD5UV	RWC	0b	VDD5 regulator under voltage indicator
2	CRCERR	RWC	0b	Configuration register CRC error indicator
1	PWRUPERR	RWC	0b	Power-up sequence error indicator
0	VDD5OTERR	RWC	0b	VDD5 over-temperature indicator

7.6.1.9 PIN Register (offset = 08h) [reset = NA]

The PIN register shows the state of the physical pins on the device, so the reset state is completely dependent on the application.

Figure 28. PIN Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved							UCRSTFALL
RO-NA							RO-NA
7	6	5	4	3	2	1	0
UCTRG	UC5V	ENDRV	NENDRV	WAKE	WCHDGEN	IGNITION	TSTMD
RO-NA	RO-NA	RO-NA	RO-NA	RO-NA	RO-NA	RO-NA	RO-NA

Table 18. PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
23-9	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
8	UCRSTFALL	RO	—	
7	UCTRG	RO	—	Logic state of the PWL_WD pin
6	UC5V	RO	—	
5	ENDRV	RO	—	Logic state of the ENDRV pin
4	NENDRV	RO	—	Logic state of the NENDRV pin
3	WAKE	RO	—	Logic state of the WAKE pin
2	WCHDGEN	RO	—	Logic state of the NWDDIS pin
1	IGNITION	RO	—	Logic state of the ENA pin
0	TSTMD	RO	—	Logic state of the ESTMODE pin

7.6.1.10 BIST Register (offset = 09h) [reset = NA]

The BIST register reports any internal logic errors present on the device, the reset state is dependent on the state of the device and thus doesn't have a standard value.

Figure 29. BIST Register

23	22	21	20	19	18	17	16
BISTSTAT							
RO-NA							
15	14	13	12	11	10	9	8
BISTSTAT							
RO-NA							
7	6	5	4	3	2	1	0
BISTSTAT							
RO-NA							

Table 19. BIST Register Field Descriptions

Bit	Field	Type	Reset	Description
23-1	BISTSTAT	RO	—	End-of-BIST signature
0	BISTERR	RO	—	Logic-BIST error indicator

7.6.1.11 TIMERST Register (offset = 0Ah) [reset = 0h]

Figure 30. TIMERST Register

23	22	21	20	19	18	17	16
TIMERST							
RO-0							
15	14	13	12	11	10	9	8
TIMERST							
RO-0							
7	6	5	4	3	2	1	0
TIMERST							
RO-0							

Table 20. TIMERST Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TIMERST	RO	0h	Current state of the wakeup timer

7.6.1.12 TIMERTH Register (offset = 0Bh) [reset = FFFFFFh]

Figure 31. TIMERTH Register

23	22	21	20	19	18	17	16
TIMERTH							
RW-FFh							
15	14	13	12	11	10	9	8
TIMERTH							
RW-FFh							
7	6	5	4	3	2	1	0
TIMERTH							
RW-FFH							

Table 21. TIMERTH Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TIMERTH	RW	FFFFFFh	Threshold count of the wakeup timer

7.6.1.13 CUST1 Register (offset = 0Ch) [reset = NA]

The CUST1 register is for the user of the IC to give their own unique ID, the reset value is totally dependent on the specific application.

Figure 32. CUST1 Register

23	22	21	20	19	18	17	16
CUST1							
RW-MS-ID							
15	14	13	12	11	10	9	8
CUST1							
RW-MS-ID							
7	6	5	4	3	2	1	0
CUST1							
RW-MS-ID							

Table 22. CUST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CUST1	RW	MS-ID	Customer use register 1; defaults to the upper 24 bits of the 48-bit TI-defined Device ID

7.6.1.14 CUST2 Register (offset = 0Dh) [reset = NA]

The CUST2 register is for the user of the IC to give their own unique ID, the reset value is totally dependent on the specific application.

Figure 33. CUST2 Register

23	22	21	20	19	18	17	16
CUST2							
RW-LS-ID							
15	14	13	12	11	10	9	8
CUST2							
RW-LS-ID							
7	6	5	4	3	2	1	0
CUST2							
RW-LS-ID							

Table 23. CUST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CUST2	RW	LS-ID	Customer use register 2; defaults to the lower 24 bits of the 48-bit TI-defined Device ID

7.6.1.15 CHGST Register (offset = 0Eh) [reset = 0h]

Figure 34. CHGST Register

23	22	21	20	19	18	17	16
CHGST							
RW-00h							
15	14	13	12	11	10	9	8
CHGST							
RW-00h							
7	6	5	4	3	2	1	0
CHGST							
RW-00h							

Table 24. CHGST Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CHGST	RW	0h	Device state change request register: Write one of the six 24-bit codes below to request an internal state change. A3_FB_04h = internal sync reset request A1_FE_01h = software reset request A2_FD_02h = transition to STANDBY mode request 6D_75_02h = enable monitor unit 2 request A5_7F_10h = end mux SOPC request A4_F7_08h = end mux initialization request A 6-bit acknowledgment code is returned upon reading this register. The response is defined as follows: 00_00_20h = internal sync reset request acknowledged 00_00_10h = software reset request acknowledged 00_00_08h = transition to STANDBY mode acknowledged 00_00_04h = enable monitor unit 2 request acknowledged 00_00_02h = mux SOPC completed 00_00_01h = mux configured; configuration registers locked

7.6.1.16 MU1CNFG Register (offset = 0Fh) [reset = F00000h]

Figure 35. MU1CNFG Register

23	22	21	20	19	18	17	16
RTHRESH1				DTHRESH1			
RW-Fh				RW-0h			
15	14	13	12	11	10	9	8
TRESP1							
RW-00h							
7	6	5	4	3	2	1	0
TWIND1							
RW-00h							

Table 25. MU1CNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
23-20	RTHRESH1	RW	Fh	Reset threshold for monitor unit 1
19-16	DTHRESH1	RW	0h	Disable threshold for monitor unit 1; value Fh is not valid
15-8	TRESP1	RW	00h	Response time for monitor unit 1
7-0	TWIND1	RW	00h	Window closed time for monitor unit 1

7.6.1.17 MURSTEN Register (offset = 10h) [reset = 3h]

Figure 36. MURSTEN Register

23	22	21	20	19	18	17	16
Reserved							
RO-0h							
15	14	13	12	11	10	9	8
Reserved							
RO-0h							
7	6	5	4	3	2	1	0
Reserved						RSTEN2	RSTEN1
RO-0h						RW-1b	RW-1b

Table 26. MURSTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	Reserved	RO	0h	Registers not implemented; each bit returns a zero-value when read
	RSTEN2	RW	1b	Reset enable for monitor unit 2
	RSTEN1	RW	1b	Reset enable for monitor unit 1

7.6.1.18 MU1 Register (offset = 11h) [reset = 0h]

The MU1 register reports errors observed by the monitoring unit in the device, the reset value is dependent on the error state of the device.

Figure 37. MU1 Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved			FSI	QUEST1			
RO-NA			RO-NA	RO-NA			
7	6	5	4	3	2	1	0
ERRCNT1				STATE1			PSTAGE1
RO-NA				RO-NA			RO-NA

Table 27. MU1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-13	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
12	FSI	RO	Reset state dependent on error state of device	Diagnostic error for monitor unit 1
11-8	QUEST1	RO	Reset state dependent on error state of device	Question code for monitor unit 1
7-4	ERRCNT1	RO	Reset state dependent on error state of device	Error counter status for monitor unit 1
3-1	STATE1	RO	Reset state dependent on error state of device	Monitor unit 1 state
0	PSTAGE1	RO	Reset state dependent on error state of device	POWER-state enable status for monitor unit 1

7.6.1.19 MU1ANS Register (offset = 12h) [reset = 0h]

Figure 38. MU1ANS Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved							
RO-NA							
7	6	5	4	3	2	1	0
Reserved				ANS1			
RO-NA				RW-0h			

Table 28. MU1ANS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
3-0	ANS1	RW	0h	MCU response to monitor unit 1 question

7.6.1.20 MU2_CONFIG Register (offset = 13h) [reset = F00000h]

Figure 39. MU2_CONFIG Register

23	22	21	20	19	18	17	16
RTHRESH2				DTHRESH2			
RW-Fh				RW-0h			
15	14	13	12	11	10	9	8
TRESP2							
RW-00h							
7	6	5	4	3	2	1	0
TWIND2							
RW-00h							

Table 29. MU2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
23-20	RTHRESH2	RW	Fh	Reset threshold for monitor unit 2
19-16	DTHRESH2	RW	0h	Disable threshold for monitor unit 2; value Fh is not valid
15-8	TRESP2	RW	00h	Response time for monitor unit 2
7-0	TWIND2	RW	00h	Window closed time for monitor unit 2

7.6.1.21 MU2 Register (offset = 14h) [reset = NA]

The MU2 register reports errors observed by the monitoring unit in the device, the reset value is dependent on the error state of the device.

Figure 40. MU2 Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved			FSI	QUEST2			
RO-NA			RO-NA	RO-NA			
7	6	5	4	3	2	1	0
ERRCNT2				STATE2			PSTAGE2
RO-NA				RO-NA			RO-NA

Table 30. MU2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-13	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
12	FSI	RO	Reset state dependent on error state of device	Diagnostic error for monitor unit 2
11-8	QUEST2	RO	Reset state dependent on error state of device	Question code for monitor unit 2
7-4	ERRCNT2	RO	Reset state dependent on error state of device	Error counter status for monitor unit 2
3-1	STATE2	RO	Reset state dependent on error state of device	Monitor unit 2 state
0	PSTAGE2	RO	Reset state dependent on error state of device	POWER-state enable status for monitor unit 2

7.6.1.22 MU2ANS Register (offset = 15h) [reset = 0h]

Figure 41. MU2ANS Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved							
RO-NA							
7	6	5	4	3	2	1	0
Reserved				ANS2			
RO-NA				RW-0h			

Table 31. MU2ANS Register Field Descriptions

Bit	Field	Type	Reset	Description
23-4	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
3-0	ANS2	RO	0h	MCU response to monitor unit 2 question

7.6.1.23 CRC1 Register (offset = 16h) [reset = 490852h]

Figure 42. CRC1 Register

23	22	21	20	19	18	17	16
CRC7			CRC6			CRC5	
RO-010b			RO-010b			RO-010b	
15	14	13	12	11	10	9	8
CRC5	CRC4			CRC3			CRC2
RO-010b	RO-000b			RO-100b			RO-001b
7	6	5	4	3	2	1	0
CRC2		CRC1			CRC0		
RO-001b		RO-010b			RO-010b		

Table 32. CRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-21	CRC7	RO	010b	CHANGE_STATE register CRC value
20-18	CRC6	RO	010b	Not used
17-15	CRC5	RO	010b	Not used
14-12	CRC4	RO	000b	TIMER_THRESH register CRC value
11-9	CRC3	RO	100b	POR_CONFIG register CRC value
8-6	CRC2	RO	001b	SYNC_CONFIG register CRC value
5-3	CRC1	RO	010b	CLSS register CRC value
2-0	CRC0	RO	010b	VSOUT register CRC value

7.6.1.24 CRC2 Register (offset = 17h) [reset = 13Ch]

Figure 43. CRC2 Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved							CRC10
RO-NA							RO-100b
7	6	5	4	3	2	1	0
CRC10			CRC9			CRC8	
RO-100b			RO-111b			RO-100b	

Table 33. CRC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-9	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
8-6	CRC10	RO	100b	MU2_CONFIG register CRC value
5-3	CRC9	RO	111b	MU_RSTEN register CRC value
2-0	CRC8	RO	100b	MU1_CONFIG register CRC value

7.6.1.25 SOURCE Register (offset = 18h) [reset = 0h]

Figure 44. SOURCE Register

23	22	21	20	19	18	17	16
Reserved	RSTSRC						
RO-NA	RO-00h						
15	14	13	12	11	10	9	8
RSTSRC						MURSTCNT	
RO-00h						RO-0h	
7	6	5	4	3	2	1	0
MURSTCNT	STDBYOT	STDBYCMD	STDBYWD	WKUPWAKE	WKUPCAN	WKUPTIMER	WKUPIGNITION
RO-0h	RO-0b	RO-0b	RO-0b	RO-0b	RO-0b	RO-0b	RO-0b

Table 34. SOURCE Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Reserved	RO	—	Registers not implemented; bit returns a zero-value when read
22-10	RSTSRC	RO	000h	Copy of register DIAGRST[12:0]
9-7	MURSTCNT	RO	0h	MU mux reset count
6	STDBYOT	RO	0b	VDD5 over-temperature triggered transition to STANDBY
5	STDBYCMD	RO	0b	Software command triggered transition to STANDBY
4	STDBYWD	RO	0b	Watchdog time-out triggered transition to STANDBY
3	WKUPWAKE	RO	0b	WAKE pin triggered transition from STANDBY
2	WKUPCAN	RO	0b	CAN wakeup logic triggered transition from STANDBY
1	WKUPTIMER	RO	0b	Wakeup timer time-out transition from STANDBY
0	WKUPIGNITION	RO	0b	ENA pin triggered transition from STANDBY

7.6.1.26 DIAGRST Register (offset = 19h) [reset = 0h]

Figure 45. DIAGRST Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved			DIAGINTRST	DIAGUCRST	DIAGCLKRST	DIAGWDRST	DIAGSTDBYRST
RO-NA			RO-0b	RO-0b	RO-0b	RO-0b	RO-0b
7	6	5	4	3	2	1	0
DIAGVDD5RST	DIAGVDD3RST	DIAGSOPC2RST	DIAGSOPC1RST	DIAGMU2RST	DIAGMU1RST	DIAGSWRST	
RO-0b	RO-0b	RO-0b	RO-0b	RO-0b	RO-0b	RO-0b	RO-0b

Table 35. DIAGRST Register Field Descriptions

Bit	Field	Type	Reset	Description
23-13	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read
12	DIAGINTRST	RO	0b	Internal synchronous reset-occurred indicator
11	DIAGUCRST	RO	0b	Microcomputer reset-occurred indicator
10	DIAGCLKRST	RO	0b	System-clock error reset-occurred indicator
9	DIAGWDRST	RO	0b	Watchdog time-out reset-occurred indicator
8	DIAGSTDBYRST	RO	0b	Transition-to-STANDBY reset occurred
7	DIAGVDD5RST	RO	0b	VDD5 reset-occurred indicator
6	DIAGVDD3RST	RO	0b	VDD3 reset-occurred indicator
5	DIAGSOPC2RST	RO	0b	SOPC2 time-out reset-occurred indicator
4	DIAGSOPC1RST	RO	0b	SOPC1 time-out reset-occurred indicator
3	DIAGMU2RST	RO	0b	Monitor unit 2 reset-occurred indicator
2	DIAGMU1RST	RO	0b	Monitor unit 1 reset-occurred indicator
1	DIAGSWRST	RO	0b	Software reset-occurred indicator
0	DIAGCRCRST	RO	0b	Configuration register CRC-error reset-occurred indicator

7.6.1.27 Reserved Register (offset = 1Ah to 1Bh) [reset = NA]

Figure 46. Reserved Register

23	22	21	20	19	18	17	16
Reserved							
RO-NA							
15	14	13	12	11	10	9	8
Reserved							
RO-NA							
7	6	5	4	3	2	1	0
Reserved							
RO-NA							

Table 36. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	Reserved	RO	—	Registers not implemented; each bit returns a zero-value when read

7.6.1.28 TI TEST Register (offset = 1Ch to 1Eh) [reset = NA]

Figure 47. TI TEST Register

23	22	21	20	19	18	17	16
TI TEST							
NA							
15	14	13	12	11	10	9	8
TI TEST							
NA							
7	6	5	4	3	2	1	0
TI TEST							
NA							

Table 37. TI TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	TI TEST	NA	NA	For TI TEST use-only

7.6.1.29 Reserved Register (offset = 1Fh) [reset = NA]

Figure 48. Reserved Register

23	22	21	20	19	18	17	16
Reserved							
NA							
15	14	13	12	11	10	9	8
Reserved							
NA							
7	6	5	4	3	2	1	0
Reserved							
NA							

Table 38. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	Reserved	NA	NA	Registers not implemented; each bit returns a zero-value when read

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS99110-Q1 device is a system basis chip used in body and transmission applications. This device is used to take the battery voltage and output several voltage rails for sensor interfaces, current loop interfaces, and microcontroller supplies. The device also integrates the physical interface for LIN and CAN communication used in automotive applications.

8.2 Typical Application

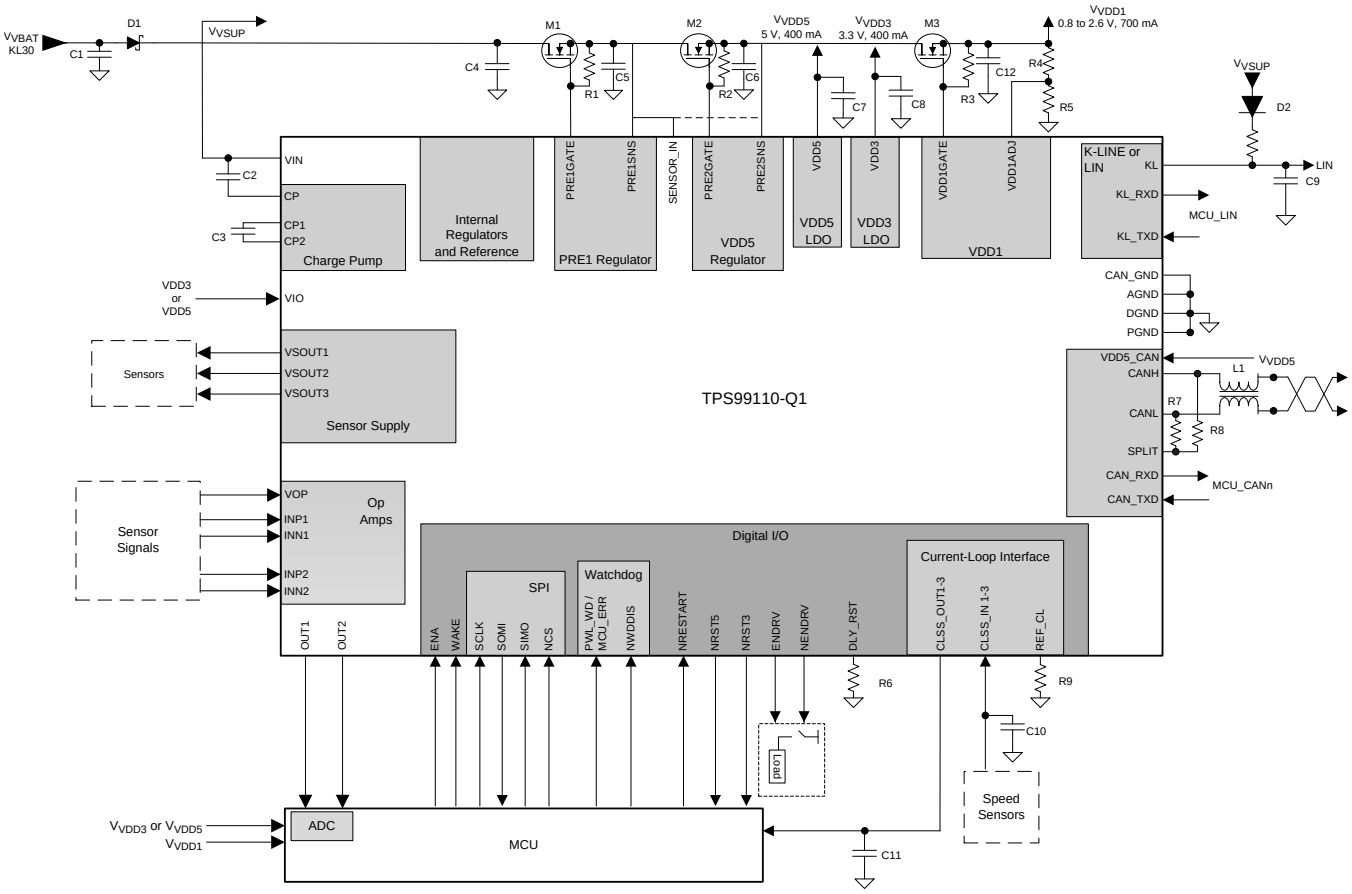


Figure 49. Typical Application Schematic

8.2.1 Design Requirements

The TPS99110-Q1 was designed for use with specific component values, however; some external component values can be selected using formulas for a given application. These external components include the reset delay resistor (see the *Reset Delay* section) and the current-loop reference resistor (see the *Current-Loop Interface* section).

Typical Application (continued)

The TPS99110-Q1 device was designed for specific applications including transmission and engine control units. Therefore the device has specific component values to support the preregulators, regulators, and communication interfaces. These component values are based on the specified device parameters and cannot be calculated through formulas.

Table 39. Design Component Values

COMPONENT REFERENCE	FUNCTION	COMPONENT	RECOMMENDED COMPONENT VALUE
C1	Battery voltage filter	Aluminum electrolytic capacitor	20 µF to 60 µF ≥50-V rated
C2	Coupling capacitor	X7R ceramic capacitor	0.1 µF
C3	Charge-pump fly capacitor	X7R ceramic capacitor	0.01 µF ≥50-V rated
C4	—	X7R ceramic capacitor	2 µF to 10 µF ≥50-V rated
C5	Output capacitor	X7R ceramic capacitor	0.5 µF to 15 µF (typical 1 µF) ≥50-V rated
C6	Output capacitor	X7R ceramic capacitor	0.5 µF to 15 µF (typical 1 µF) ≥50-V rated
C7	Output capacitor	X7R ceramic capacitor	5 µF to 40 µF (typical 10 µF) ≥25-V rated
C8	Output capacitor	X7R ceramic capacitor	5 µF to 40 µF (typical 10 µF) ≥25-V rated
C9	Filter capacitor	X7R ceramic capacitor	1000 pF ≥50-V rated
C10	Smoothing capacitor	X7R ceramic capacitor	Application Specific (1000 pF) ≥25-V rated
C11	Output capacitor	X7R ceramic capacitor	Application Specific (150 pF) ≥25-V rated
C12	Output capacitor	X7R ceramic capacitor	5 µF to 40 µF (typ. 10 µF) ≥25-V rated
D1	Reverse battery protection diode	Schottky diode	≥50-V rated Schottky diode (PDS560-13)
D2	LIN pullup diode	Fast switching diode	≥40-V rated Diode (BAS16W-7-F)
L1	CAN choke inductor	Common mode filter inductor	51 µH -40°C to 150°C operating temperature Rated for ≥ 0.2 A
M1	Preregulator FET	NMOS FET	Gate threshold voltage = 0.3 V to 3 V Maximum Input capacitance = 5000 pF Maximum gate charge = 190 nC Recommended part number: IPD25N06S4L-30
M2	Preregulator FET	NMOS FET	Gate threshold voltage = 0.3 V to 3 V Maximum Input capacitance = 5000 pF Maximum gate charge = 190 nC Recommended part number: IPD25N06S4L-30
M3	Power FET	NMOS FET	Gate threshold voltage = 0.3 V to 3 V Maximum Input capacitance = 3200 pF Maximum gate charge = 70 nC Recommended part number: IPB081N06L3 G
R1	Gate discharge path	SMT resistor	100 kΩ ≥0.125-W rated
R2	Gate discharge path	SMT resistor	100 kΩ ≥0.125-W rated
R3	Gate discharge path	SMT resistor	100 kΩ ≥0.125-W rated
R4	Voltage setting divider	SMT resistor	Application specific, dependent on the desired VDD1 output voltage ≥0.125-W rated
R5	Voltage setting divider	SMT resistor	Application specific, dependent on the desired VDD1 output voltage ≥0.125-W rated
R6	Reset delay adjustment	SMT resistor	See the *Design Requirements* section to determine the correct value ≥0.125-W rated

Typical Application (continued)

Table 39. Design Component Values (continued)

COMPONENT REFERENCE	FUNCTION	COMPONENT	RECOMMENDED COMPONENT VALUE
R7	CAN SPLIT resistor divider	SMT resistor	60 Ω ≥0.125-W rated
R8	CAN SPLIT resistor divider	SMT resistor	60 Ω ≥0.125-W rated
R9	Current-loop reference resistor	SMT resistor	See the *Design Requirements* section to determine the correct value ≥0.125-W rated

8.2.2 Detailed Design Procedure

8.2.2.1 REF_CL Resistance Calculation

The interface has open-circuit and short-to-ground diagnosis through SPI and self-test diagnostics for diagnosis bits through the SPI control bit for activation. The interface includes reference current generation through an external resistor between the REF_CL pin and ground. The status of the CLSS_OUTx signal is readable by SPI. In the following equations, $R_{(CLSSREF)}$ refers to R9 in Figure 49

Use Equation 1 to calculate the average trip of the current-loop interface ($I_{(TRIP-x)}$).

$$I_{(TRIP-x)} = \frac{A + CLSSTHx[3:0] \times B}{R_{(CLSSREF)}}$$

where

- A = 55 V ± 3%
- B = 4 V ± 3%
- x = 1, 2, 3…

(1)

Use Equation 2 to calculate the hysteresis ($I_{(HYST-x)}$) from minimum to maximum.

$$I_{(HYST-x)} = \frac{C + CLSSHYSTx[1:0] \times D}{R_{(CLSSREF)}}$$

where

- C = 6 V ± 3%
- D = 6 V ± 3%
- x = 1, 2, 3…

(2)

The maximum low-to-high trip point is given by the maximum $I_{(TRIP-x)}$ plus half of the maximum $I_{(HYST-x)}$. The minimum low-to-high trip point is given by the minimum $I_{(TRIP-x)}$ plus half of the minimum $I_{(HYST-x)}$. The maximum high-to-low trip point is given by the maximum $I_{(TRIP-x)}$ minus half of the minimum $I_{(HYST-x)}$. The minimum low-to-high trip point is given by the minimum $I_{(TRIP-x)}$ minus half of the maximum $I_{(HYST-x)}$.

8.2.2.2 DLY_RST Resistance Calculation

For more information on the function of this resistance, see the *Reset Delay* section. The resistor described in this section is R6 in Figure 49.

Use to calculate the analog reset delay can be calculated with Equation 3 (minimum value), Equation 4 (typical value), and Equation 5 (maximum value).

$t_{r(off)}$, minimum = 1.14786 ms/kΩ × R6 + 10 ms (3)

$t_{r(off)}$, typical = 1.66262 ms/kΩ × R6 + 15.14 ms (4)

$t_{r(off)}$, maximum = 2.15284 ms/kΩ × R6 + 21.43 ms (5)

8.2.3 Application Curves

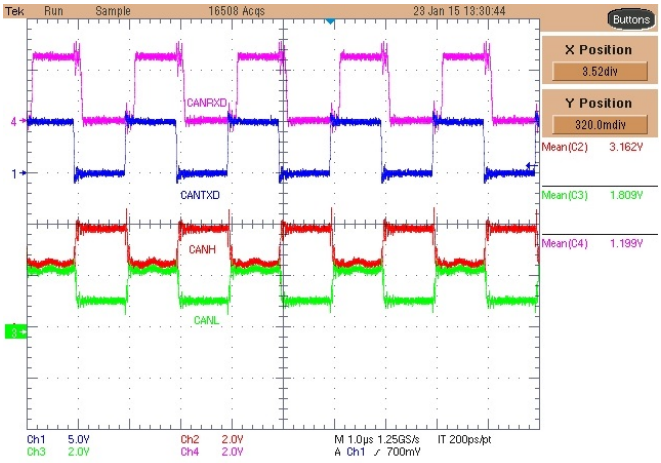


Figure 50. CAN Interface With 500-kHz Square Wave, 50% Duty Cycle, $5V_{PP}$

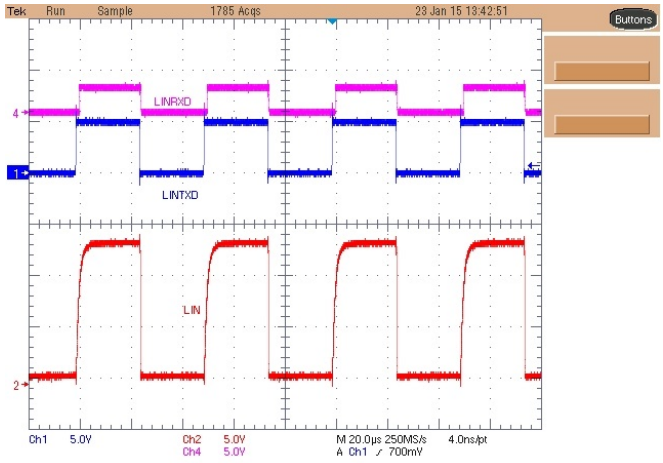


Figure 51. LIN Interface 20-kHz Square Wave, 50% Duty Cycle, 5 V_{PP}

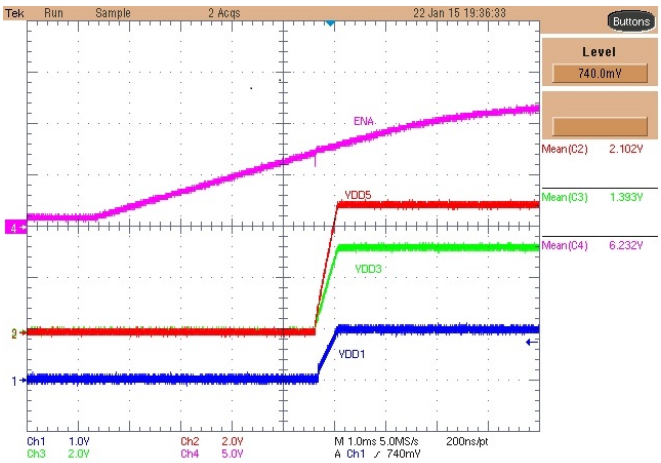


Figure 52. Power-Up Sequence

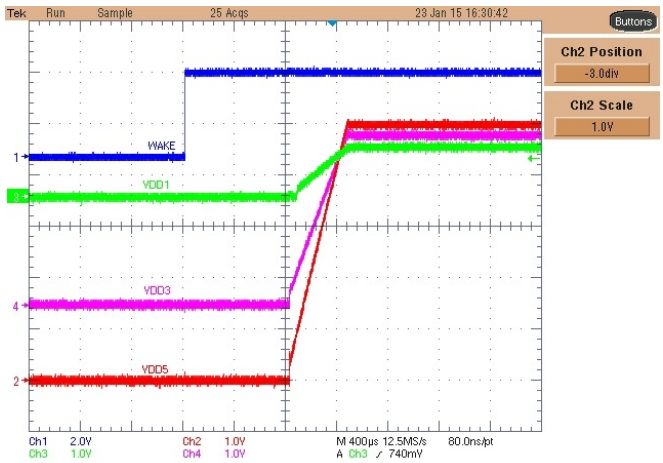


Figure 53. Wake Up Toggling the WAKE Pin

9 Power Supply Recommendations

The TPS99110-Q1 device is a power-supply device relying on the battery voltage within an automotive system. Therefore, no power supply recommendation is provided beyond the automobile battery.

10 Layout

10.1 Layout Guidelines

Use the following guidelines for proper layout design

- IC (refer to Figure 54)
  - Place the CP1 and CP2 capacitor (C22) as close to the CP1 and CP2 pins as possible.
  - Place the charge pump capacitor (C19) as close to the CP pin as possible.
  - The PowerPad must have a solid connection to the landing pad on the board. This connection is critical for optimal heat dissipation when supplying large current loads.
  - Place the output capacitor for VDD5 (C12) as close to the VDD5 pin as possible.
  - Place the CLSS_OUT1, CLSS_OUT2, and CLSS_OUT3 output capacitors (C7, C8, and C9) as close to the respective pins as possible.
  - Place the current-loop reference resistor (R21) as close to the REF_CL pin as possible to avoid any excess trace resistance which could alter the current-limit setting of the current-loop.
  - Place the DLY_RST external resistor (R13) as close to the DLY_RST pin as possible to avoid any excess trace resistance which could alter the delay setting.
  - Place the output capacitors for VSOUT1, VSOUT2, and VSOUT3 (C1, C2, and C3) as close to the VSOUTx pins as possible. Ensure that the traces are thick enough to deliver 200 mA of current.
  - Place the CLSS_IN1, CLSS_IN2, and CLSS_IN3 input capacitors (C4, C5, and C6) as close as possible to the respective pins. Ensure that the thick traces are thick enough to support the current that is driven into the pin.
  - Place the VDD3 output capacitor as close to the pin as possible. On this particular layout, the capacitor is on the underside of the board.
- FETs (refer to Figure 55)
  - Place the VDD1 output capacitor (C16) very close to the source pin of the FET
  - Place the gate-source discharge resistor (R15) close to the FET pins to decrease any trace resistance.
  - The trace for PRE1SNS pin must be very thick and stable because a large amount of current is driven through this FET. In Figure 55, this trace looks like an isolated trace, but it is connected to the power plane at a via to tie the trace to the PRE1SNS pin
  - Place the PRE1 gate-to-source discharge resistor (R5) close to the gate and source pins to eliminate excess trace resistance.
  - Place the PRE2 output capacitor (C13) close to the PRE2SNS pin.
  - Place the PRE2 gate to source discharge resistor (R3) close to the gate and source pins to eliminate excess trace resistance.
  - The output capacitor for PRE1 (C10) needs to be very close to the PRE1SNS pin.
  - The trace for the gate of the VDD1 FET-to-PRE2SNS must be very thick to manage the high amount of current driven to the pin.
  - The trace for the VIN pin must be very thick for sufficient current carrying capability.

10.2 Layout Example

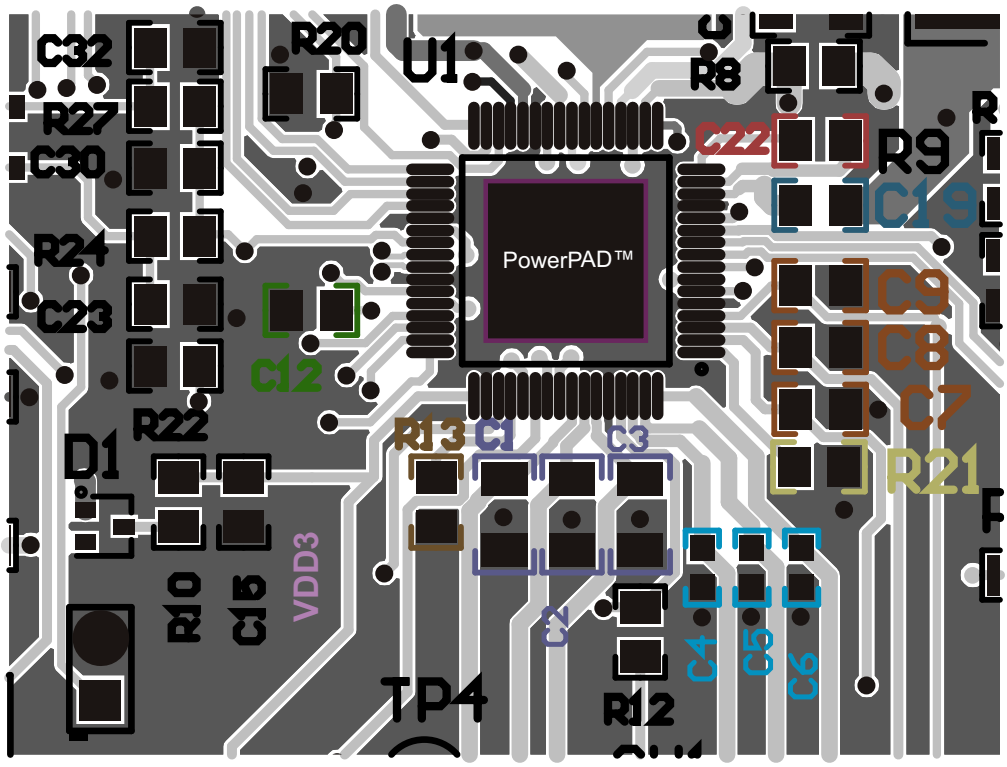


Figure 54. TPS99110-Q1 Layout Example—IC

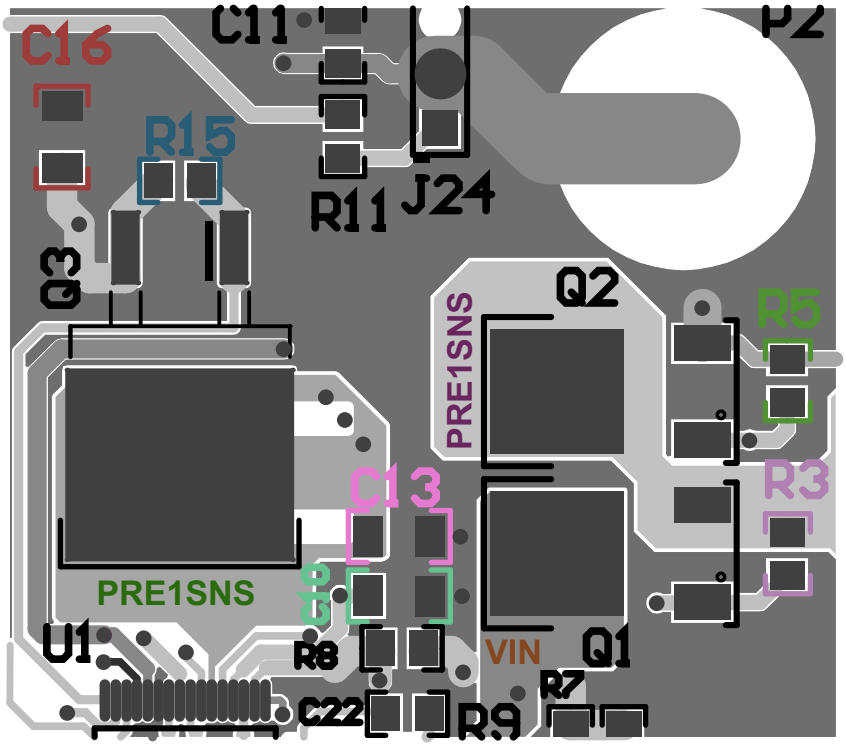


Figure 55. TPS99110-Q1 Layout Example—FETs

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TPS99110EVM and GUI User's Guide, SLIU009

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS99110QPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS99110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

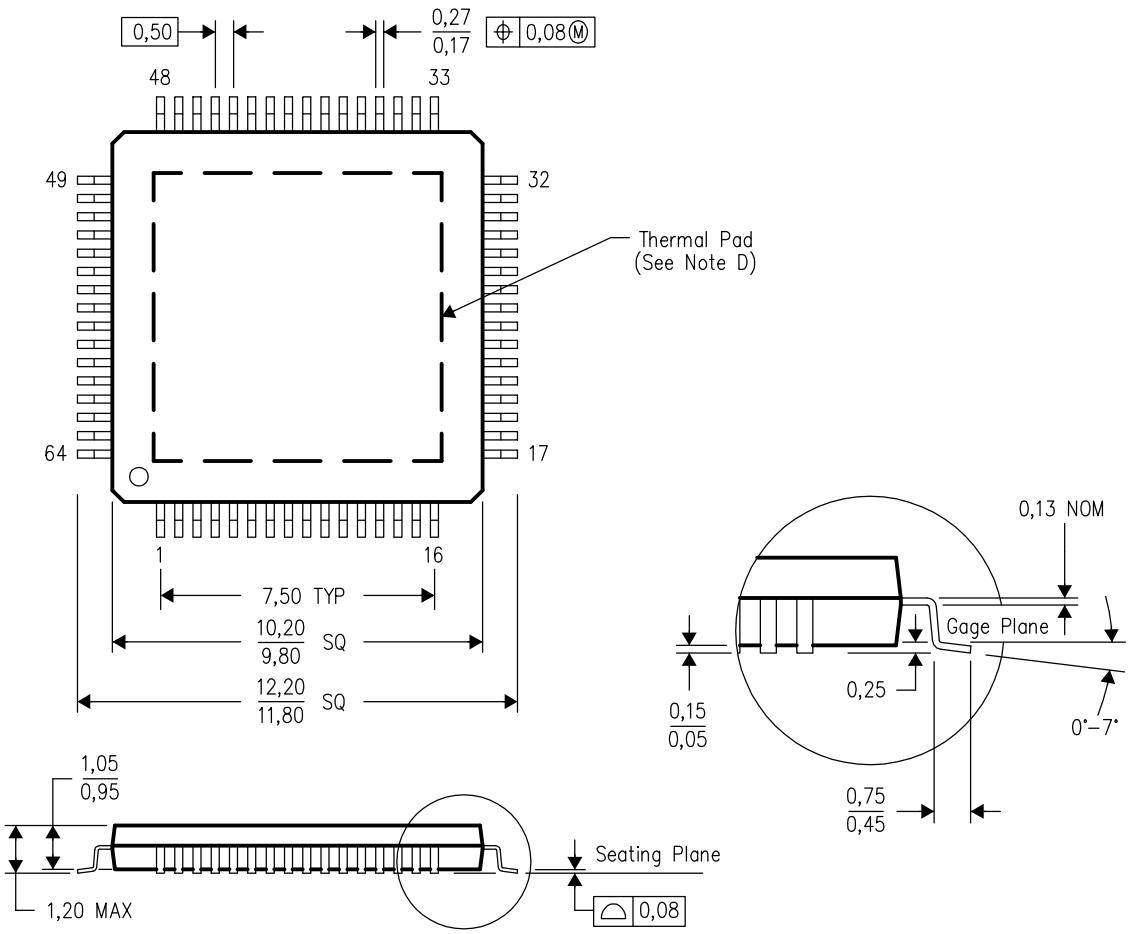
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

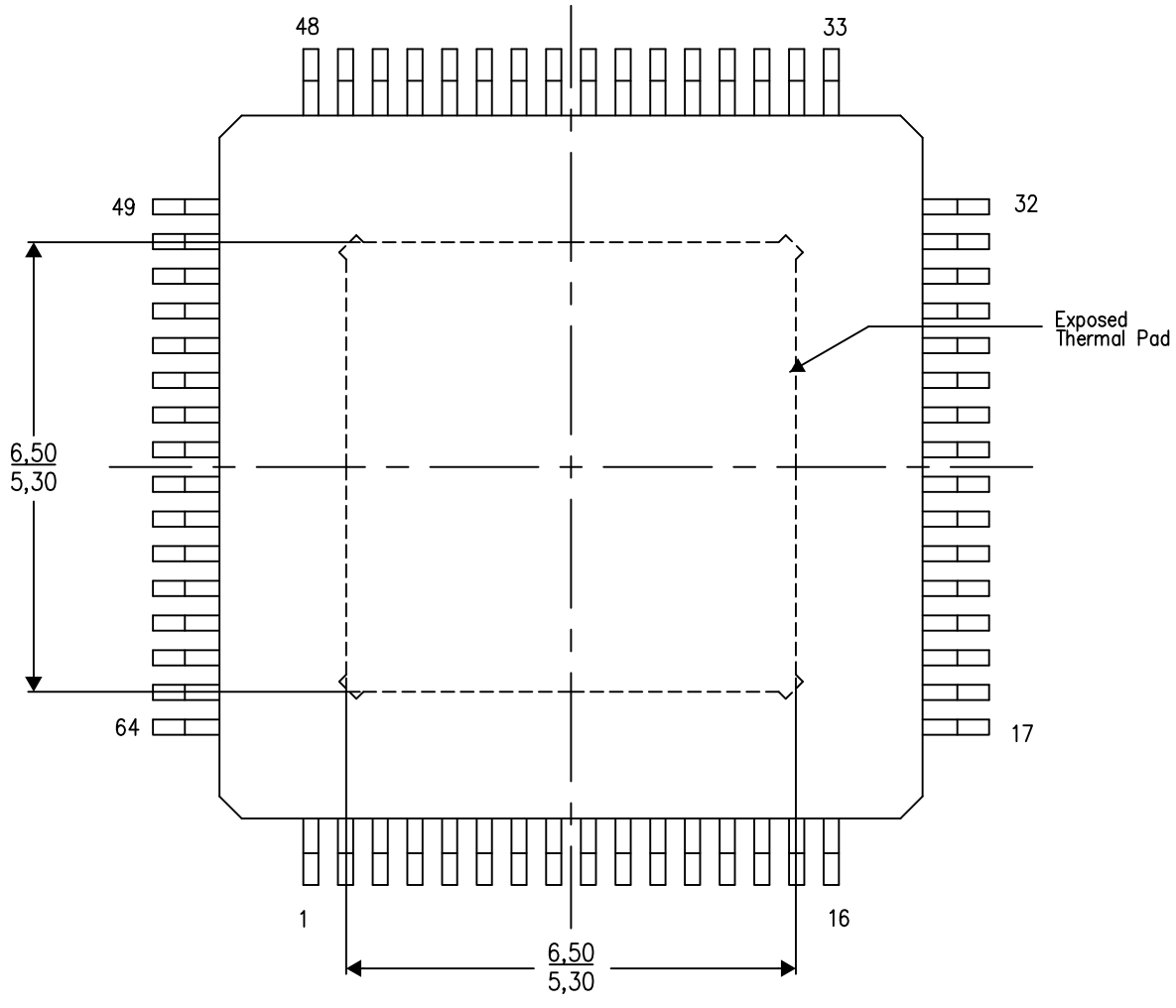
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–4/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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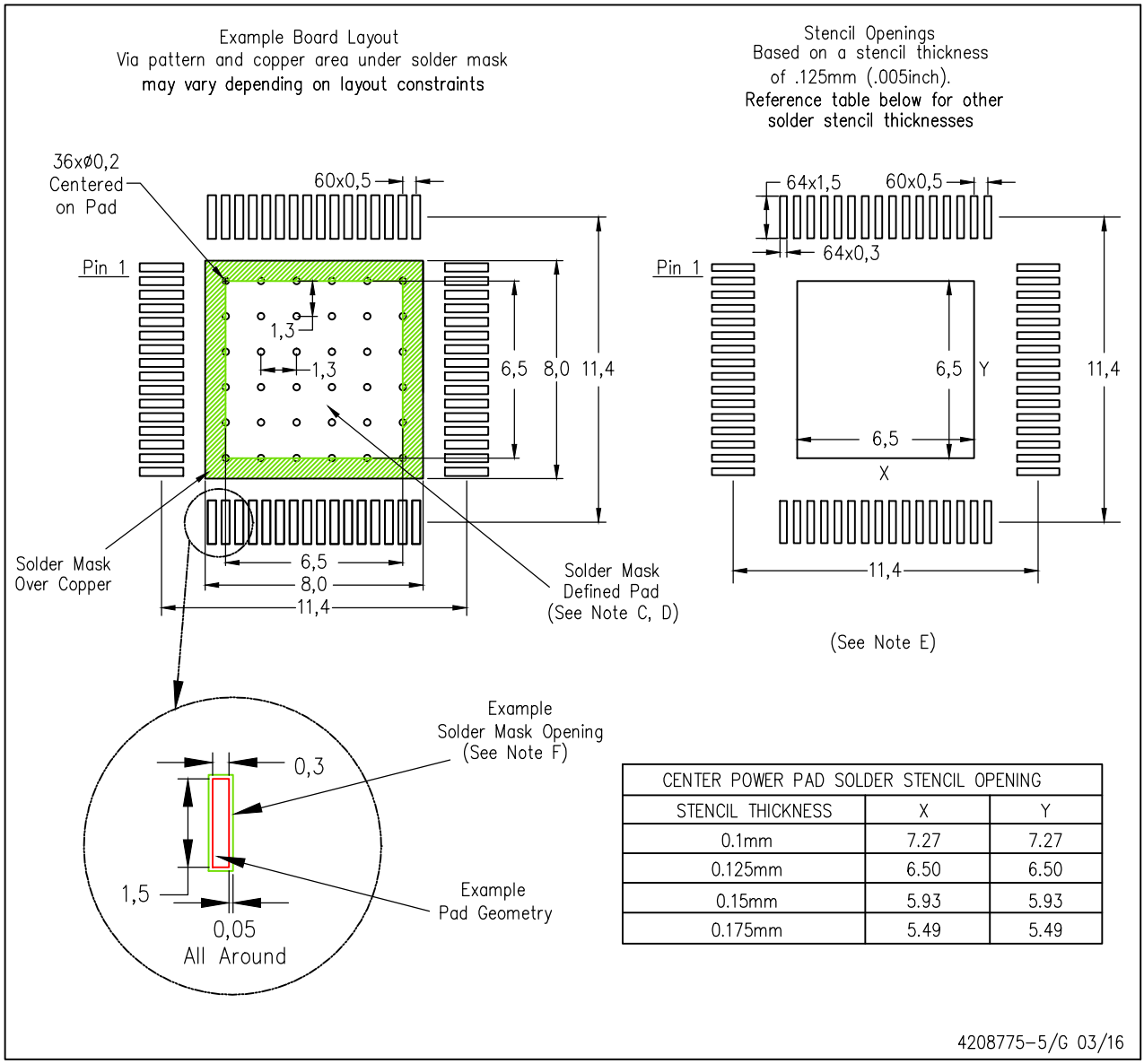
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	7.27	7.27
0.125mm	6.50	6.50
0.15mm	5.93	5.93
0.175mm	5.49	5.49

4208775–5/G 03/16

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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