

## Advanced Power Management Unit

Check for Samples: [TPS658621A](#)

### 1 INTRODUCTION

#### 1.1 MAIN FEATURES

- **BATTERY CHARGER**
  - Complete Charge Management Solution for a Single Cell Li-Ion/Li-Pol Cell With Dynamic Power Management and Thermal Foldback.
  - Maximum 1.0A charge current
  - Programmable Adapter and USB Charge Operation
- **INTEGRATED POWER SUPPLIES**
  - 3 Programmable Step-Down converters
    - Software Controlled Enable/Forced PWM Mode
    - Automatic Power Saving Mode
    - Maximum 1.2A Outputs
  - 11 Programmable General Purpose LDOs
    - 7 With Output Voltages of 1.25V to 3.3V
    - 2 With Output Voltages of 0.725V to 1.5V or 1.25V to 2.586V (factory configurable)
    - 1 “Always On” With Output Voltages of 1.25V to 3.3V
    - 1 With Output Voltage of 1.70V–2.475V
- **DISPLAY SUPPORT FUNCTIONS**
  - 4 PWM Outputs With Programmable Frequency and Duty Cycle
  - Dual RGB LED Drivers
  - Constant Current WLED Driver
    - 26.5V (max) at 25mA
    - Over-Voltage Protection
    - Programmable Current Level and Brightness Control
- **HOST INTERFACE**
  - Interrupt Controller With Maskable Interrupts
  - External ADC Triggering and Step-Down Converter Mode Control
- **SYSTEM MANAGEMENT**
  - Dual Input Power Path
    - USB Current Limiting
  - Max 18V Over-Voltage Protection
  - Power Good Monitoring on all Supply Outputs
  - Software Reset Function
  - Hardware On/Off and Reboot Control
  - 11 Channel ADC With 3 Operating Modes
    - Single Conversion
    - Peak Detection
    - Averaging

#### 1.2 APPLICATIONS

- Smart Phones
- Portable Navigation Devices
- Portable Media Players



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

### 1.3 DESCRIPTION

The TPS658621A provides an easy to use, fully integrated solution for handheld devices, integrating charge management, multiple regulated power supplies, system management and display functions in a small 6x6 package. The I<sup>2</sup>C interface enables control of a wide range of subsystem parameters. Internal registers have a complete set of status information, enabling easy diagnostics and host-controlled handling of fault conditions.

### 1.4 ORDERING INFORMATION<sup>(1)</sup>

| T <sub>A</sub> | PART NUMBER <sup>(2)</sup> <sup>(3)</sup> | PACKAGE <sup>(4)</sup> | PACKAGE DESIGNATOR | ORDERING <sup>(2)</sup> | PACKAGE MARKING |
|----------------|---|------------------------|--------------------|-------------------------|-----------------|
| –40°C to 85°C  | TPS658621A                                | MicroStar BGA          | ZGU                | TPS658621A              | TPS658621A      |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The TPS658621A is only available taped and reeled. Quantities are 2,500 devices per reel.
- (3) Devices with distinct part numbers have unique factory configurations for supply defaults, sequencing and other functions. Consult the factor for configuration information for each part number.
- (4) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

## 2 ELECTRICAL SPECIFICATIONS

### 2.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|   | VALUE / UNITS    |
|---|------------------|
| AC and USB with respect to AGND1  | –0.3 V to 18 V   |
| ANLG1, ANLG2, ANLG3 with respect to AGND2   | –0.3 V to 6.5 V  |
| V(SYS), V(VIN_CHG) with respect to AGND1  | –0.3 V to 6.5 V  |
| VIN_LDO01, VIN_LDO23, VIN_LDO4, VIN_LDO678, VIN_LDO9 with respect to AGND1                    | –0.3 V to 6.5 V  |
| ADC_REF with respect to AGND2   | –0.3 V to 3.6 V  |
| RTC_OUT with respect to V(SYS)  | –5.5 V to 3.6 V  |
| RTC_OUT with respect to AGND1   | –0.3 V to 3.6 V  |
| LDO0, LDO1, LDO2, LDO3, LDO4, LDO5, LDO6, LDO7, LDO8, LDO9, V2V2 and TS with respect to AGND1 | –0.3 V to 3.6 V  |
| V32K with respect to AGND1  | –0.3 V to 3.6 V  |
| TS with respect to V2V2   | –2.3 V to 0.3 V  |
| SM0, L0, VIN_SM0 with respect to PGND0  | –0.3 V to 6.5 V  |
| SM1, L1, VIN_SM1 with respect to PGND1  | –0.3 V to 6.5 V  |
| SM2, L2, VIN_SM2 with respect to PGND2  | –0.3 V to 6.5 V  |
| SM3, L3 with respect to PGND3   | –0.3 V to 29 V   |
| SM3SW with respect to PGND3   | –0.3 V to 29 V   |
| FB3 with respect to PGND3   | –0.3 V to 0.5 V  |
| V(BAT) with respect to AGND1, Battery power only  | –0.3 V to 5.5 V  |
| All other pins (except AGNDn and PGNDn) with respect to AGND1                                 | –0.3 V to 6.5 V  |
| AGND2, AGND3, , DGND1, DGND2DT, PGND0, PGND1, PGND2, PGND3 with respect to AGND1              | –0.3 V to +0.3 V |
| Input Current, AC pin   | Defined by ILIM  |
| Input Current, USB pin  | Defined by ILIM  |
| Output continuous current, SYS, VIN_CHG pins  | 2500 mA          |
| Output continuous current, BAT pin  | –3000 mA         |
| Continuous Current at L0, PGND0, L1, PGND1  | 1500 mA          |
| Continuous Current at L3, PGND3   | 1000 mA          |
| Continuous Current at L2, PGND2   | 2000 mA          |
| Operating free-air temperature, T <sub>A</sub>  | –40°C to 85°C    |
| Maximum junction temperature, T <sub>J</sub>  | 125°C            |
| Storage temperature, T <sub>STG</sub>   | –65°C to 150°C   |
| Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds                                  | 260°C            |
| HBM rating, all pins  | 2 kV             |
| MM rating, all pins   | 100 V            |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 2.2 DISSIPATION RATINGS

| PACKAGE | Psi_Jb | T <sub>A</sub> ≤ 25°C<br>POWER RATING | T <sub>A</sub> = 55°C<br>POWER RATING | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|--------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| ZGU     | 20°C/W | 5000 mW                               | 3500 mW                               | 2750 mW                               | 2000 mW                               |

## 2.3 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|  | MIN   | MAX                 | UNIT |
|--|---|---------------------|------|
| AC and USB with respect to AGND1   | 4.30  | 16.5 <sup>(1)</sup> | V    |
| V(SYS) with respect to AGND1   | 2.9   | 5.5                 | V    |
| V(BAT) with respect to AGND1, battery power only   | 2.9   | 5.25                | V    |
| V(BAT) with respect to AGND1, battery connected, AC or USB power selected, Selected power source >2.9V | 2.15  | 4.6                 | V    |
| ANLG1,ANLG2, ANLG3 with respect to AGND2   | 0   | 2.6                 | V    |
| VIN_LDO01, VIN_LDO23, VIN_LDO678, VIN_LDO4, VIN_LDO9 with respect to AGND1                             | Greater of : 1.7V OR Minimum input voltage required for LDO/Converter operation outside dropout region  | 5.5                 | V    |
| VIN_SM0 with respect to PGND0  | Greater of : 2.3V OR Minimum input voltage required for LDO/Converter operation outside dropout region. 2.9V to meet parametric specifications. | 5.5                 | V    |
| VIN_SM1 with respect to PGND1  |   | 28                  | V    |
| VIN_SM2 with respect to PGND2  |   | 28                  | V    |
| VIN_SM4 with respect to PGND4  |   | 28                  | V    |
| SM3 with respect to PGND3  |   | 28                  | V    |
| GPIOx with respect to AGND1  | 0   | 5.5                 | V    |
| All other pins (except AGNDn and PGNDn) with respect to AGND1  | 0   | 5.5                 | V    |
| Operating free-air temperature, T <sub>A</sub>   | -40   | 85                  | °C   |
| Maximum junction temperature, T <sub>J</sub> , functional operation                                    | -40   | 125                 | °C   |
| Maximum junction temperature, T <sub>J</sub> , electrical characteristics                              | 0   | 125                 | °C   |
| External supply ramp rate, AC or USB pins  | 1 V/mSec  | 1 V/μSec            |      |

(1) Thermal operating restrictions are reduced or avoided if input voltage does not exceed 5V.

## 2.4 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS  | MIN  | TYP | MAX | UNIT |
|--|---|--|------|-----|-----|------|
| QUIESCENT CURRENT – V(BAT) = 4.2V NO EXTERNAL LOADS AT SYS PIN OR SUPPLY OUTPUTS |   |  |      |     |     |      |
| I <sub>Q(ON)</sub>   | Quiescent current, 6586x in normal or sleep mode. All supplies, peripherals and charger off | Power path active, control logic in low power mode <sup>(1)</sup>  |      |     | 375 | μA   |
| I <sub>Q(DIGITAL)</sub>  | Quiescent current, control logic  | Control logic in high power mode <sup>(2)</sup>  | 584  | 716 | 870 | μA   |
| I <sub>Q(SMn)</sub>  | SM0, SM1, SM2 operating quiescent current   | SM0, SM1: enabled, PFM mode, from SYS pin  |      | 14  | 25  | μA   |
|  |   | SM2: enabled, PFM mode, from SYS pin   |      | 19  | 32  | μA   |
|  |   | SM0, SM1, SM2: enabled, PWM mode, from VINSMn pin  |      | 6   |     | mA   |
|  |   | disabled via I <sup>2</sup> C  |      | 1   |     | μA   |
| I <sub>Q(LDOx)</sub>   | LDO quiescent current, All but one LDOx disabled  | I(LDOx) = no external load   |      | 24  | 29  | μA   |
|  |   | I(LDOx) = –1 mA  |      | 24  | 150 | μA   |
|  |   | I(LDOx) = –50 mA   |      | 160 |     | μA   |
|  |   | LDO disabled, T <sub>J</sub> = 85°C  |      | 1   | 3   | μA   |
| I <sub>Q(SM3)</sub>  | SM3 operating quiescent current <sup>(3)</sup>  | SM3 enabled, not switching   |      | 15  | 30  | μA   |
|  |   | Enabled, switching   |      |     | 200 | μA   |
|  |   | Disabled via I <sup>2</sup> C  |      | 1   |     | μA   |
| I <sub>Q(ADC)</sub>  | ADC operating quiescent current   | Conversion active  |      | 1   |     | mA   |
|  |   | Not converting, waiting for trigger  |      | 170 |     | μA   |
|  |   | ADC disabled via I <sup>2</sup> C  |      | 1   |     | μA   |
| I <sub>Q(RTC)</sub>  | RTC_OUT pin quiescent current   | RTC_OUT LDO enabled  |      | 27  | 45  | μA   |
|  |   | RTC_OUT disabled via I <sup>2</sup> C, T <sub>J</sub> = 85°C . Externally applied <sup>(4)</sup><br>V(RTC_OUT) = 2 V supplies real time clock counters and xtal oscillator |      |     | 15  | μA   |
| I <sub>Q(V32K)</sub>   | V32K supply bias current , 32k buffer enabled   | 32k buffer enabled, 100 pF external load   |      |     | 24  | μA   |
|  |   | Disabled via I <sup>2</sup> C  |      |     | 8   | μA   |
| I <sub>Q(CHG)</sub>  | Charger quiescent current   | Charger enabled, termination detected  |      | 40  | 50  | μA   |
|  |   | Charger enabled, termination disabled, charge current=0 <sup>(3)</sup>   |      |     | 2   | mA   |
|  |   | Charger disabled   |      | 10  | 20  | μA   |
| I <sup>2</sup> C INTERFACE TIMING – SDA, PSDA, PSCLK, SCLK <sup>(3)</sup>        |   |  |      |     |     |      |
| T <sub>R</sub>   | SCLK/SDATA rise time  | Pull-up resistors connected to 2.2V  |      |     | 300 | ns   |
| T <sub>F</sub>   | SCLK/SDATA fall time  |  |      |     | 300 | ns   |
| T <sub>W(H)</sub>  | SCLK pulse width high   |  | 600  |     |     | ns   |
| T <sub>W(L)</sub>  | SCLK Pulse Width Low  |  | 1.3  |     |     | μs   |
| T <sub>SU(STA)</sub>   | Setup time for START condition  |  | 600  |     |     | ns   |
| T <sub>H(STA)</sub>  | START condition hold time after which first clock pulse is generated                        |  | 600  |     |     | ns   |
| T <sub>SU(DAT)</sub>   | Data setup time   |  | 100  |     |     | ns   |
| T <sub>H(DAT)</sub>  | Data hold time  |  | 0    |     |     | ns   |
| T <sub>SU(STOP)</sub>  | Setup time for STOP condition   |  | 600  |     |     | ns   |
| T <sub>(BUF)</sub>   | Bus free time between START and STOP condition  |  | 1.3  |     |     | μs   |
| F <sub>SCL</sub>   | Clock Frequency   |  |      |     | 400 | kHz  |
| I <sup>2</sup> C BUFFERS – SDA, PSDA, PSCLK, SCLK                                |   |  |      |     |     |      |
| V <sub>IL(I2C)</sub>   | Low level input voltage   |  |      |     | 0.4 | V    |
| V <sub>IH(I2C)</sub>   | High level input voltage  |  | 1.15 |     |     | V    |
| V <sub>OL(I2C)</sub>   | Low level output voltage  | SDA, PSDA configured as output, I <sub>OL</sub> =3mA   |      |     | 0.4 | V    |
| I <sub>O(I2C)</sub>  | Maximum load current <sup>(3)</sup>   | SDA, PSDA configured as output   |      |     | 8   | mA   |
| I <sub>LKG(I2C)</sub>  | Input current   | V(pin)=5V or 0V  |      |     | 1.0 | μA   |
| C <sub>I2C</sub>   | Input pin capacitance   | SDAT, SCLK, PSDAT, PSCLK pins  |      | 10  |     | pF   |
| C <sub>I2CBUS</sub>  | I <sup>2</sup> C bus capacitance  | SDAT, SCLK, PSDAT, PSCLK   |      | 400 |     | pF   |

- (1) Control logic in low power mode when all functions are off and no I<sup>2</sup>C communication is on going
- (2) Control logic in high power mode when one of the following events happen: 6586x in power-up/rtc/rtc\_on/supplyseq states, any converter in PWM mode, SM3 enabled, PWM driver enabled, ADC conversion on-going, I<sup>2</sup>C communication on-going, voltage transition for DVM supplies on-going, charger on, AC or USB supply detected, initial power-up cycle.
- (3) Not production tested.
- (4) External voltage supplied by supercap or coin cell connected to RTC\_OUT pin, see application diagram for details.

**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS   | MIN        | TYP  | MAX  | UNIT |
|---|---|---|------------|------|------|------|
| DIGITAL INPUT BUFFERS: RESUME, SM0EN, SM1EN, HOTRST, LDO4EN, SYNCEN       |   |   |            |      |      |      |
| V <sub>IL(DIG)</sub>  | Low level input voltage   |   |            |      | 0.4  | V    |
| V <sub>IH(DIG)</sub>  | High level input voltage  |   | 1.15       |      |      | V    |
| I <sub>LKG(DIG)</sub>   | Input current   | V(pin)=5V   |            |      | 0.1  | μA   |
| R <sub>DIG</sub>  | Internal resistor   | RESUME pin , pull-down to AGND  | 55         | 100  | 150  | kΩ   |
|   |   | HOTRST pin, pull-up to V2V2   | 55         | 100  | 150  |      |
| PUSH-PULL OUTPUT BUFFERS, USER SELECTABLE OUTPUT VOLTAGE – NORTC, NOPOWER |   |   |            |      |      |      |
| V <sub>BFRPWR</sub>   | Buffer positive supply  | Internally connected to V32K pin  | 1.1 to 3.3 |      |      | V    |
| V <sub>OL(OBFR)</sub>   | Low level output voltage  | I <sub>OL</sub> = 3 mA, V32K = 1.5 V  |            |      | 0.6  | V    |
|   |   | I <sub>OL</sub> = 10 μA, V32K > 1.1 V   |            |      | 0.1  |      |
| V <sub>OH(OBFR)</sub>   | High level output voltage, referenced to output buffer supply, NORTC            | I <sub>OH</sub> = 1.4 mA, V32K = 1.5 V  | V32K-0.6   |      |      | V    |
|   |   | I <sub>OH</sub> = -10 μA, V32K = 1.1 V  | V32K-0.11  |      |      |      |
| V <sub>OH(OBFR)</sub>   | High level output voltage, referenced to output buffer supply,NOPOWER           | I <sub>OH</sub> = 1.4 mA, V32K = 1.5 V  | V32K-0.6   |      |      | V    |
|   |   | I <sub>OH</sub> = -10 μA, V32K = 1.1 V  | V32K-0.11  |      |      |      |
| I <sub>OL(OBFR)</sub>   | Maximum low level sink current load <sup>(1)</sup>                              | V(pin) = 2.5 V  |            |      | 5    | mA   |
| I <sub>OH(OBFR)</sub>   | Maximum high level source current load <sup>(1)</sup>                           | V(pin) = 0 V  | –5         |      |      | mA   |
| OPEN DRAIN OUTPUT BUFFERS – INT   |   |   |            |      |      |      |
| V <sub>OL(OBFR)</sub>   | Low level output voltage  | I <sub>OL</sub> = 3 mA, V32K = 1.5 V  |            |      | 0.6  | V    |
|   |   | I <sub>OL</sub> = 10 μA, V32K > 1.1 V   |            |      | 0.1  |      |
| I <sub>LKG(OBFR)</sub>  | Output leakage current  | Output buffer, open-drain mode, V(pin)=5.5V                                     |            |      | 0.1  | μA   |
| PUSH-PULL OUTPUT BUFFERS – LDO4PG, SM0PG, SM1PG, CHGSTAT                  |   |   |            |      |      |      |
| V <sub>OL(OBFR)</sub>   | Low level output voltage  | I <sub>OL</sub> = 3 mA  |            |      | 0.6  | V    |
|   |   | I <sub>OL</sub> = 10 μA   |            |      | 0.1  |      |
| V <sub>OH(OBFR)</sub>   | High level output voltage , buffer configured as push-pull via I <sup>2</sup> C | I <sub>OH</sub> = 3 mA  | 1.5        |      |      | V    |
|   |   | I <sub>OH</sub> = –10 μA  | 1.8        |      |      |      |
| I <sub>OL(OBFR)</sub>   | Maximum low level sink current load <sup>(1)</sup>                              | V(pin) = 2.5 V  |            |      | 5    | mA   |
| I <sub>OH(OBFR)</sub>   | Maximum high level source current load <sup>(1)</sup>                           | V(pin) = 0 V  | –5         |      |      | mA   |
| 32kHz OUTPUT BUFFER , V(32K)=1.7V (min), UNLESS OTHERWISE STATED          |   |   |            |      |      |      |
| V <sub>32B</sub>  | Externally applied bias rail for output driver <sup>(1)</sup>                   | Buffer supply voltage   | 1.0        |      |      | V    |
| V <sub>OL</sub>   | Output low level  | V(32K) = 1.1 V, I <sub>OL</sub> = 100 μA  |            |      | 0.05 | V    |
|   |   | V(32K) = 1.1 V, I <sub>OL</sub> = 1 mA  |            |      | 0.2  |      |
|   |   | V(32K) = 1.5 V, I <sub>OL</sub> = 5 mA  |            |      | 0.5  |      |
| V <sub>OH</sub>   | Normal operation  | V(32K) = 1.1 V, I <sub>OH</sub> = -1 μA   | V32K-0.05  |      |      | V    |
|   |   | V(32K) = 1.5 V, I <sub>OH</sub> = 5 mA  | V32K-0.5   |      |      |      |
| T <sub>F</sub> , T <sub>R</sub>   | Rise/fall time  | 32 kHz clock driving 50pF load cap  |            | 15   |      | ns   |
| V <sub>JITTER</sub>   | Output jitter   | Peak to peak  |            | 15   |      | ns   |
|   |   | RMS   |            | 15   |      |      |
| 32kHz CLOCK AND 32K SWITCHING TIMING                                      |   |   |            |      |      |      |
| T <sub>XTAL</sub>   | XTAL oscillator stabilization time <sup>(1)</sup>                               | Frequency within 2% of typical value, frequency defined by XTAL characteristics |            |      | 2    | s    |
| F <sub>32K</sub>  | Internal 32 kHz clock   | Frequency   | 28         | 32   | 36   | kHz  |
| INTERNAL REFERENCES AND POR   |   |   |            |      |      |      |
| V <sub>UVLO</sub>   | Internal UVLO detection threshold   | V(2V2) decreasing   | -3%        | 1.85 | 3%   | V    |
| V <sub>UVLO_HYS</sub>   | UVLO detection hysteresis   | V(2V2) increasing from decreasing trigger point                                 |            | 120  |      | mV   |
| V <sub>O(2V2)</sub>   | Output Voltage  | Always on,  | 2.1        | 2.2  | 2.3  | V    |
| I <sub>SH2V2</sub>  | Short Circuit current limit   | V(2V2)=0v   | 18         |      |      | mA   |

(1) Not production tested.

## 2.5 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                              |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT  |
|--|--|---|--|------|------|-------|
| RTC_OUT LDO                            |  |   |  |      |      |       |
| V <sub>O(RTC_OUT)</sub>                | RTC_OUT output voltage                       | Output Voltage, Selectable via I <sup>2</sup> C <sup>(1)</sup>              | V <sub>O(RTC_OUT)</sub> TYP=1.25, 1.50, 1.8, 2.5, 2.7,2.85,3.1,3.3 |      |      | V     |
|  |  | Dropout voltage, I(RTC_OUT) = –15 mA<br>V(SYS) = 2.8 V                      | 600  |      |      | mV    |
|  |  | Total accuracy, V(AC):2V to 4.7V, –15mA load,<br>V(BAT1)=V(BAT2)=V(USB)=0V  | –5%  |      |      | 5%    |
|  |  | Load regulation, V(AC)=3.5V,<br>load: 1mA → –15mA                           | 1%   |      |      |       |
|  |  | Line regulation, 5mA load,V(AC): 3.5V→18V,<br>V(BAT1) =V(BAT2) =V(USB) =0V  | 1%   |      |      |       |
| I <sub>SHRTC</sub>                     | Short Circuit current limit                  |   | 20   |      |      | mA    |
| V <sub>(RTCGOOD)</sub>                 | RTC_OUT power good fault detection threshold | Falling RTC_OUT pin voltage, set via I <sup>2</sup> C                       | 2.3  | 2.35 | 2.45 | V     |
|  |  |   | 1.8  | 1.90 | 2.0  |       |
| V <sub>HYS(RTC)</sub>                  | Power good fault detection hysteresis        | Rising RTC_OUT pin voltage (Referenced to V <sub>(RTCGOOD)</sub> threshold) | 50   | 75   | 131  | mV    |
| V <sub>UVLO_RTC</sub>                  | Internal RTC UVLO detection threshold        | V <sub>RTC</sub> Decreasing   | –10%   | 1.5  | 10%  | V     |
| V <sub>UVLO_RTC_HYS</sub>              | UVLO detection hysteresis                    | V <sub>RTC</sub> Increasing   | 100  | 150  | 200  | mV    |
| BOOT-UP TIMING                         |  |   |  |      |      |       |
| T <sub>POR</sub>                       | Power-on-reset delay <sup>(2)</sup>          | Fixed time, measured from 2V2>UVLO  | 7.2  | 8    | 8.8  | ms    |
| T <sub>BOOT</sub>                      | Boot-up time                                 | Fixed time  | 500  |      |      | ms    |
|  |  | Accuracy, referenced to T <sub>BOOT(TYP)</sub>                              | –10%   |      |      |       |
| T <sub>HOTPLUG</sub>                   | Hot plug deglitch time                       | Fixed time  | 675  | 750  | 825  | ms    |
| T <sub>WAKEUP</sub>                    | Wakeup pulse width                           | Fixed time  | 225  | 250  | 275  | μs    |
| T <sub>CHECK</sub>                     | RTC check wait time                          | Fixed time  | 2.7  | 3    | 3.3  | ms    |
| T <sub>MAX</sub>                       | RTC_ON watchdog timer                        | Fixed time  | 4×T <sub>NORTC</sub>   |      |      | ms    |
| T <sub>NORTC</sub>                     | NORTC pin pulse width value                  | Fixed time  | 10   |      |      | ms    |
|  |  | Accuracy, relative to T <sub>NORTC (TYP)</sub> <sup>(2)</sup>               | –10%   |      |      |       |
| K <sub>NOPOWER</sub>                   | NOPOWER pin pulse width const.               | T <sub>NOPOWER</sub> = K <sub>NOPOWER</sub> × C <sub>NOPOWER</sub>          | 0.25   |      |      | ms/nF |
|  |  | Pulse width accuracy, C <sub>NOPOWER</sub> < 400nF                          | –25%   |      |      |       |
| T <sub>WAIT</sub>                      | Reboot and sleep request timeout             | Fixed time  | 18   | 20   | 22   | ms    |
| T <sub>WAIT1</sub>                     |  |   | 4.5  | 5    | 5.5  | ms    |
| T <sub>SYNCEND</sub>                   | Synchronization complete delay               | Measured from all supplies synchronized                                     | 4.5  | 5    | 5.5  | ms    |
| T <sub>SYNCDLY</sub>                   | Supply sync delay time                       | Regulator specific. See <a href="#">Table 3-17</a>                          | T <sub>SYNCDLY(TYP)</sub> = 1.25, 2.5, 3.75, 15, 20, 32, 40, 64    |      |      | ms    |
|  |  | Accuracy, relative to T <sub>SYNCDLY(TYP)</sub> <sup>(2)</sup>              | -10  |      |      |       |
| POWER GOOD AND THERMAL FAULT DETECTION |  |   |  |      |      |       |
| T <sub>DGL(PGFLT)</sub>                | Power good deglitch time                     | Applies to all non-masked power good signals, output voltage falling edge.  | 4  | 5    | 6    | ms    |
| T <sub>SHUT</sub>                      | Thermal shutdown                             | Increasing junction temperature   | 150  |      |      | °C    |
| T <sub>HYS(SHUT)</sub>                 | Thermal shutdown hysteresis                  | Decreasing junction temperature   | 30   |      |      | °C    |
| T <sub>DGL(TSHUT)</sub>                | Thermal shutdown detection delay             | Rising temperature  | 15   | 20   | 25   | μs    |

(1) Setting the RTC\_OUT output voltage below the RTC\_OUT power good threshold will result in a NORTC pulse being always generated during reboot cycles or when exiting sleep.

Setting the RTC\_OUT output voltage below V<sub>UVLO\_RTC</sub> disables the use of the internal real time clock counter and xtal oscillator.

(2) Not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                   |  | TEST CONDITIONS  | MIN  | TYP   | MAX  | UNIT |
|---|--|--|------|-------|------|------|
| <b>RESUME CONTROL TIMING</b>                |  |  |      |       |      |      |
| $T_{\text{RESUME(H)}}$                      | RESUME pulse width high <sup>(1)</sup>   |  | 550  |       |      | ms   |
| $T_{\text{RESUME(L)}}$                      | RESUME pulse width low <sup>(1)</sup>  |  | 1500 |       |      | ms   |
| <b>SEQUENCER REBOOT CONTROL</b>             |  |  |      |       |      |      |
| $V_{\text{HOTRST}}$                         | Reboot control threshold   | Reboot started when normal state is set and $V(\text{HOT\_RST}) < V_{\text{REBOOT}}$ for $t > T_{\text{DT(HRST)}}$   |      |       | 0.4  | V    |
| $T_{\text{HRST(H)}}$                        | HOT_RST max pulse width  |  |      |       | 60   | ms   |
| $T_{\text{DT(HRST)}}$                       | HOT_RST min detection pulse width  | HOT_RST deglitch   | 4    |       | 16   | µs   |
| <b>EXTERNAL SUPPLY DETECTION AND STATUS</b> |  |  |      |       |      |      |
| $V_{\text{LOWSYS}}$                         | Minimum system voltage detection threshold   | System voltage V(SYS) decreasing.  |      | 3.0   |      | V    |
|   |  | Total accuracy, referenced to V(LOWSYS)TYP   | -2   |       | 2    | %    |
| $V_{\text{HYS(LOWSYS)}}$                    | Minimum system voltage detection hysteresis  | V(SYS) increasing from decreasing trigger point  |      | 200   |      | mV   |
| $T_{\text{DGL(LOWSYS)}}$                    | Minimum system voltage detection deglitch time   | V(SYS) decreasing  |      | 5     |      | ms   |
| $V_{\text{IN(DT)}}$                         | Input voltage detection threshold. Input voltage increasing, referenced to battery voltage | AC detected when $V(\text{AC}) - V(\text{BAT}) > V_{\text{IN(DT)}}$ AND $V(\text{AC}) > V_{\text{ACMIN}}$<br>USB detected when $V(\text{USB}) - V(\text{BAT}) > V_{\text{IN(DT)}}$ | 180  |       |      | mV   |
| $V_{\text{IN(NDT)}}$                        | Input voltage removal threshold. Input voltage decreasing, referenced to battery voltage   | AC not detected: when $V(\text{AC}) - V(\text{BAT}) < V_{\text{IN(NDT)}}$ USB not detected when $V(\text{USB}) - V(\text{BAT}) < V_{\text{IN(NDT)}}$                               |      |       | 65   | mV   |
| $V_{\text{ACMIN}}$                          | AC detection threshold, relative to GND  | AC voltage decreasing, AC not detected when $V(\text{AC}) < V_{\text{ACMIN}}$  |      | 3.5   |      | V    |
|   |  | Hysteresis, AC voltage increasing  |      | 200   |      | mV   |
| $T_{\text{DGLAC(DT)}}$                      | AC Power detected deglitch   | AC voltage increasing  |      | 22.5  |      | ms   |
| $T_{\text{DGLUSB(DT)}}$                     | USB Power detected deglitch  | USB voltage increasing   |      | 5.5   |      | ms   |
| $V_{\text{IN(OVP)}}$                        | Input over voltage detection   |  | 5.8  | 6.0   | 6.3  | V    |
| $T_{\text{DLY(INOVP)}}$                     | Input over voltage detection delay   | Rising AC or USB voltage   |      | 100   |      | µs   |
| <b>ANALOG COMPARATOR</b>                    |  |  |      |       |      |      |
| $V_{\text{COMPDET}}$                        | Voltage threshold  | Enabled at sleep mode not set  | 1.21 | 1.245 | 1.28 | V    |
| $I_{\text{OCDET}}$                          | Bias current <sup>(1)</sup>  | Always On  |      |       | 5    | µA   |
| $T_{\text{P}}$                              | Propagation time   | V(COMP):0→1.5V→0, measured from input to NOPOWER:HI→LO   |      | 50    |      | µs   |

(1) Not production tested.



## 2.6 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS  |                               | MIN    | TYP   | MAX   | UNIT |
|---|---|--|-------------------------------|--------|-------|-------|------|
| POWER PATH CURRENT LIMIT AND PROTECTION FUNCTIONS |   |  |                               |        |       |       |      |
| I <sub>USB100</sub>                               | Selected input current limit, applies to USB input only         | Selected Input switch not in dropout. I <sup>2</sup> C settings: USBMODE=HI, USBLIMIT=LO   | –40°C < T <sub>A</sub> < 85°C | 90     | 100   | mA    |      |
|   |   |  | –25°C < T <sub>A</sub> < 85°C | 92     | 100   |       |      |
| I <sub>USB500</sub>                               |   | Selected Input switch not in dropout. I <sup>2</sup> C settings: USBMODE=HI, USBLIMIT=HI   |                               | 435    | 500   | mA    |      |
| I <sub>INLIM</sub>                                | Selected input current limit, applies to AC input               | Input current limit range, AC input  |                               | 2.75   |       | A     |      |
|   |   | Total accuracy, relative to I <sub>INLIM(TYP)</sub>  |                               | –20%   | 20%   |       |      |
|   | Selected input current limit, applies to USB input              | Input current limit range, USB input configured with USBMODE=LO  |                               | 2.11   |       | A     |      |
|   |   | Total accuracy, relative to I <sub>INLIM(TYP)</sub>  |                               | –12.5% | 12.5% |       |      |
| T <sub>OVS</sub>                                  | Input current limit transient time                              | Load at SYS pin: 80% of current limit value to 120% of regulation value (I <sub>INLIM</sub> , I <sub>USB100</sub> or I <sub>USB500</sub> ). Time measured from load transient to input current within regulation limits. |                               | 20     |       | μs    |      |
| I <sub>OVSHPKUSB</sub>                            | Input current limit overshoot                                   | Load at SYS pin: 80% of current limit value to 120% of regulation value (I <sub>INLIM</sub> , I <sub>USB100</sub> or I <sub>USB500</sub> ), t < T <sub>OVS</sub>   |                               | 20%    |       |       |      |
| V <sub>SH(SYS)</sub>                              | SYS power path Short Circuit detection threshold                | All power path switches set to OFF if V(SYS) < V <sub>SH(SYS)</sub>  |                               | 1.6    | 1.8   | 2.0   | V    |
| R <sub>FLT(USB)</sub>                             | SYS short circuit recovery pull-up resistor                     | V(SYS) < V <sub>SH(SYS)</sub> , internal resistor connected from USB to SYS  |                               | 550    |       |       | Ω    |
| R <sub>FLT(AC)</sub>                              | SYS short circuit recovery pull-up resistor                     | V(SYS) < V <sub>SH(SYS)</sub> , internal resistor connected from AC to SYS   |                               | 550    |       |       | Ω    |
| I <sub>BATSYS</sub>                               | Battery switch over-current detection                           |  |                               | 2.18   | 2.54  |       | A    |
| T <sub>DGL(BATSYS)</sub>                          | Battery switch over-current detection delay                     | Short circuit detection blanked for TDGL(BATSYS), measured from batt switch: OFF->ON or initial sys power path enable  |                               | 100    | 110   | 120   | ms   |
|   |   | Battery switch already turned on or sys power path enabled   |                               | 1      |       |       | ms   |
| I <sub>FLT(SYS)</sub>                             | Battery switch over-current recovery pull-up current source     | V(BAT) –V(SYS) > V <sub>OC(SYS)</sub> , internal current source connected from BAT to SYS  |                               | 30     |       |       | mA   |
| V <sub>SUP(SYS)</sub>                             | Supplement detection threshold                                  | Battery switch ON at V(BAT)-V(SYS) > V <sub>SUP(SYS)</sub>   |                               | 40     |       |       | mV   |
| V <sub>SUPNDT(SYS)</sub>                          | Supplement mode not detected threshold                          | Battery switch OFF at V(BAT)-V(SYS)<V <sub>SUPNDT(SYS)</sub>   |                               | 7      |       |       | mV   |
| POWER PATH INTEGRATED MOSFETS CHARACTERISTICS     |   |  |                               |        |       |       |      |
| V <sub>ACDO</sub>                                 | AC switch dropout voltage                                       | V <sub>ACDO</sub> = V(AC)-V(SYS); V(AC)=4V AC input current limit set to 2.0A (typ)<br>I <sub>O(SYS)</sub> = 1.0A  |                               |        | 190   |       | mV   |
| V <sub>USBDO</sub>                                | USB switch dropout voltage                                      | V <sub>USBDO</sub> = V(USB)-V(SYS); V(USB)=4.6V  | I(SYS)+I(BAT)= 0.425A         |        | 240   |       | mV   |
|   |   |  | I(SYS)+I(BAT)= 85mA           |        | 240   |       |      |
| V <sub>BATDODCH</sub>                             | Battery Switch dropout voltage, discharge                       | V <sub>BATDODCH</sub> = V(BAT)-V(SYS), V(BAT)=3V, I(BAT)= 1A   |                               | 40     | 155   |       | mV   |
| POWER PATH TIMING CHARACTERISTICS                 |   |  |                               |        |       |       |      |
| T <sub>SW(ACBAT)</sub>                            | Switching from AC to BAT  | No USB, AC power removed   |                               | 150    |       |       | μs   |
| T <sub>SW(USBBAT)</sub>                           | Switching from USB to BAT                                       | No AC, USB power removed   |                               | 150    |       |       | μs   |
| POWER PATH DISCHARGE SWITCHES                     |   |  |                               |        |       |       |      |
| I <sub>DCH(AC)</sub>                              | AC pin discharge current  | Always ON, V(AC) > 1 V   |                               | 100    |       |       | μA   |
| I <sub>DCH(USB)</sub>                             | USB pin discharge current                                       | Always ON, V(USB) > 1 V  |                               | 100    |       |       | μA   |
| SM0, SM1, SM2 DC/DC CONVERTERS                    |   |  |                               |        |       |       |      |
| V <sub>SMUV</sub>                                 | Low input voltage detection threshold, input voltage decreasing | Converter turned OFF at V(VIN_SMN) < V <sub>SMUV</sub>   |                               |        | 2.0   |       | V    |
|   |   | Hysteresis , rising input voltage  |                               | 100    |       |       | mV   |
| R <sub>DS(ON)</sub>                               | High side MOSFET on-resistance                                  | V <sub>IN_SMx</sub> = 3.6V, 100% duty cycle  |                               | 200    |       |       | mΩ   |
|   | Low side MOSFET on-resistance                                   | V <sub>IN_SMx</sub> = 3.6V, 0% duty cycle  |                               | 200    |       |       | mΩ   |
| I <sub>LK_HS</sub>                                | High side leakage current                                       | T <sub>j</sub> = 85°C  |                               |        | 1     |       | μA   |
| I <sub>LK_LS</sub>                                | Low side leakage current  |  |                               |        | 1     |       | μA   |
| I <sub>LIM</sub>                                  | High side and low side current limit                            | 2.9V ≤ V <sub>IN_SMx</sub> ≤ 5.5V  | SM0, SM2                      | 1550   | 1860  |       | mA   |
|   |   |  | SM1                           | 1550   | 1860  |       |      |
| f <sub>SW</sub>                                   | Oscillator frequency  | PWM mode   |                               | 2.025  | 2.25  | 2.475 | MHz  |
| V <sub>SMPG</sub>                                 | Power good threshold  | Power fault detection, Voltage decreasing, referenced to programmed output voltage   |                               | –13.0% | –10%  | –7.0% |      |
|   |   | Hysteresis, voltage increasing, referenced to V <sub>SMPG</sub>  |                               | 5%     |       |       |      |

**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS  |                             | MIN                                     | TYP   | MAX  | UNIT |           |   |
|--|---|--|-----------------------------|---|---|------|------|-----------|---|
| V <sub>O(SMx)</sub>  | Adjustable output voltage range, Selectable via I <sup>2</sup> C              | VIN_SMx = 2.9V to 5.5V   | SM0, low range, 25mV steps  | V <sub>O(SMx)</sub> TYP = 0.725 to 1.50 |   |      | V    |           |   |
|  |   |  | SM1, low range, 25mV steps  | V <sub>O(SMx)</sub> TYP =0.725 to 1.50  |   |      |      |           |   |
|  |   |  | SM2, high range, 50mV steps | V <sub>O(SMx)</sub> TYP =3.0 to 4.55    |   |      |      |           |   |
|  | Output Voltage Accuracy, relative to VO(SMx)TYP                               | V <sub>IN_SMx</sub> = 2.9V to 5.5V, PFM mode   |                             |   | –1%   | 1%   | 3%   |           |   |
|  |   | V <sub>IN_SMx</sub> = 2.9V to 5.5V, PWM mode, 0mA < I <sub>OUT</sub> < 1A  |                             |   | –2%   |      | 2%   |           |   |
|  | DC output voltage load regulation   | PWM mode, VIN_SMn>2.7V, Load<1A  |                             |   |   | 0.25 |      | %/A       |   |
| DC output voltage line regulation                                  | V <sub>IN_SMx</sub> = VOUT + 0.5V (min. 2.5V), PWM mode VIN_SMn>2.7V, Load<1A |  |                             |   | 0.1   |      | %/V  |           |   |
| K <sub>RAMP(SMx)</sub>   | Voltage change ramp constant  | Value set via I <sup>2</sup> C, available options:   |                             |   | SM0, SM1: typical values:Instantaneous, 0.11, 0.22, 0.44, 0.88, 1.76, 3.52, 7.04                                  |      |      | mV/μs     |   |
| t <sub>Start</sub>   | Start-up time   | Time to start switching, measured from end of I <sup>2</sup> C command enabling converter  |                             |   | 210   |      |      | μs        |   |
| t <sub>Ramp</sub>  | V <sub>OUT</sub> Ramp UP time   | Time to ramp from 5% to 95% of V <sub>OUT</sub>  |                             |   | 250   |      |      | μs        |   |
| R <sub>DCH</sub>   | Discharge switch resistance   | SMx disabled   |                             |   | 250   |      |      | Ω         |   |
| I <sub>PFM(ENTER)</sub>  | Load current to enter PFM mode  | V <sub>IN_SMx</sub> = 2.9V to 5.5V, duty cycle > 85%   |                             |   | VIN_SM<br>x/<br>34Ω   |      |      | A         |   |
| C <sub>LC</sub>  | External LC capacitor <sup>(1)</sup>  |  |                             |   | 4.7   |      |      | 22<br>μF  |   |
| L <sub>LC</sub>  | External LC inductor <sup>(1)</sup>   |  |                             |   | 1.5   |      |      | 4.7<br>μH |   |
| C <sub>SMINP</sub>   | External Input capacitor <sup>(1)</sup>                                       |  |                             |   | 10  |      |      | 47<br>μF  |   |
| LDO'S : LDO0, LDO1, LDO2, LDO3, LDO4, LDO5, LDO6, LDO7, LDO8, LDO9 |   |  |                             |   |   |      |      |           |   |
| V <sub>INMIN</sub>   | Input voltage range <sup>(1)</sup>  | Electrical characteristics over the output current range IO(LDOx)  |                             |   | 2.3   |      |      | 5.5       | V |
|  |   | Electrical characteristics specified , max load current = 75mA   |                             |   | 1.7   |      |      | 5.5       |   |
| I <sub>O(LDOx)</sub>   | Output current <sup>(1)</sup>   |  |                             |   | 300   |      |      | mA        |   |
|  |   | Output Voltage, Selectable via I <sup>2</sup> C. LDO6, LDO0, LDO3, LDO5, LDO7,LDO8,LDO9  |                             |   | Available output voltages:<br>V <sub>(LDO6)</sub> TYP = 1.20 (LDO0 only), 1.25, 1.5, 1.8, 2.5, 2.7, 2.85, 3.1,3.3 |      |      | V         |   |
| V <sub>(LDOx)</sub>  | LDOx Output Voltage, Selectable via I <sup>2</sup> C                          | LDO1 Output Voltage, Selectable via I <sup>2</sup> C   | Low range, 25mV steps       | V <sub>(LDO1)</sub> TYP = 0.725 to 1.5  |   |      | V    |           |   |
|  |   | LDO4 Output Voltage, Selectable via I <sup>2</sup> C   | High range, 25mV steps      | V <sub>(LDO4)</sub> TYP = 1.7 to 2.475  |   |      |      |           |   |
|  |   | LDO2 Output Voltage, Selectable via I <sup>2</sup> C   | Low range, 25mV steps       | V <sub>(LDO2)</sub> TYP= 0.725 to 1.5   |   |      |      |           |   |
|  |   | Dropout, V(IN)= V <sub>(LDOx)</sub> TYP - 0.1V , V(IN)=2.3V, 250mA load. 1 LDO active at a time per input pin group <sup>(2)</sup> |                             |   | 415   |      |      | mV        |   |
|  |   | Total accuracy, V(VIN_LDOx)= V <sub>(LDOx)</sub> TYP + 0.5V, 10mA → 250 mA   |                             |   | See <sup>(3)</sup>  |      |      | 3.5%      |   |
|  |   | Line Regulation, 100mA load, V(VIN_LDOx):<br>V <sub>(LDOx)</sub> TYP + 0.5V→ 4.7V  |                             |   | –0.5%   |      |      | 0.5%      |   |
|  |   | Load regulation, load change from 10mA → 250 mA<br>V(VIN_LDOx)> V <sub>(LDOx)</sub> TYP + 0.5V                                     |                             |   | See <sup>(4)</sup>  |      |      | %         |   |
| PSRR <sub>(LDOx)</sub>   | PSRR at 20 kHz  | 250mA load, 1V input to output ,C <sub>L</sub> = 4.7 μF  |                             |   | 40  |      |      | dB        |   |
|  |   | 100mA load, 0.5V input to output, CL = 1 μF  |                             |   | 40  |      |      |           |   |
| I <sub>SCI(LDOx)</sub>   | Short circuit current limit   | Output grounded  | LDO <sub>n</sub> LIM=HI     | 350                                     |   |      | 700  | mA        |   |
| R <sub>DCH(LDOx)</sub>   | Discharge resistor  | LDOx disabled  |                             |   | 415   |      |      | Ω         |   |
| K <sub>RAMP(LDOx)</sub>  | Voltage change ramp constant  | LDO2, LDO4 only. Fixed value, hardwired at top level   |                             |   | 7.04  |      |      | mV/μs     |   |
| C <sub>COMP</sub>  | External output capacitor value <sup>(1)</sup>                                | Stable operation   |                             | load <100 mA                            | 1   |      |      | μF        |   |
|  |   |  |                             | load>100 mA                             | 0.01μF/mA, min cap value = 1μF  |      |      |           |   |
| P <sub>GOOD(LDO)</sub>   | Power good threshold  | LDO output voltage increasing  |                             |   | 95%   |      |      |           |   |
|  | Hysteresis  | Decreasing voltage from increasing trigger   |                             |   | 5%  |      |      |           |   |

(1) Not production tested

(2) Dropout not measured for devices with V(IN) &lt; 2.3V because minimum VIN is 2.3V

(3) MIN = –3.2 – (0.105 × I<sub>LOAD</sub> / V<sub>(LDOx)TYP</sub>), I<sub>LOAD</sub> = load current in mA(4) MIN = –2.5 – (0.105 × I<sub>LOAD</sub>), I<sub>LOAD</sub> = load current in mA

**ELECTRICAL CHARACTERISTICS (continued)**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS  | MIN   | TYP      | MAX      | UNIT  |
|---|---|--|---|----------|----------|-------|
| BATTERY VOLTAGE THRESHOLDS AND CHARGER TIMING                       |   |  |   |          |          |       |
| T <sub>CHGDLY</sub>   | Charger turn-off delay  | Time delay to turn off charger or set suspend mode   | 25  |          |          | ms    |
| V <sub>LOWBAT</sub>   | Precharge to fast-charge transition , selectable via I <sup>2</sup> C | Fast charge at V(BAT) > V <sub>LOWBAT</sub>  | Selectable via I <sup>2</sup> C, 2.9V or 2.5V   |          |          | V     |
|   |   | Total accuracy, relative to selected value   | –3% 3.25%                                       |          |          |       |
| T <sub>DGL(PRE)</sub>   | Deglitch time for fast charge to precharge transition                 | Decreasing battery voltage   | 25  |          |          | ms    |
| V <sub>RCH</sub>  | Recharge threshold voltage  | New charge cycle starts if V(BAT) < V <sub>O(BATREG)</sub> – V <sub>RCH</sub> , after termination was detected | 25  | 100      | 170      | mV    |
| T <sub>DGL(RCH)</sub>   | Deglitch time for battery recharge detection                          |  | 65  |          |          | ms    |
| PACK INSERTION AND PACK TEMPERATURE FAULT DETECTION , V(VTSBIAS)>2V |   |  |   |          |          |       |
| K <sub>THOT</sub>   | Pack hot temperature detection constant                               | Pack hot temp detected and charge suspended at V(TS) < V(2V2) × K <sub>THOT</sub>                              | 0.189   | 0.203    | 0.222    |       |
| K <sub>TCOLD</sub>  | Pack cold temperature detection constant                              | Pack cold temp detected and charge suspended at V(TS) > V(2V2) × K <sub>TCOLD</sub>                            | 0.610   | 0.625    | 0.641    |       |
| K <sub>NOPACK</sub>   | Pack not detected threshold   | V(TS) > V(2V2) × K <sub>NOPACK</sub>   | 0.935   | 0.95     | 0.965    |       |
| T <sub>DGLTEMP</sub>  | Pack temperature fault/no fault detection deglitch                    |  | 15  |          |          | ms    |
| T <sub>DGL(DT)</sub>  | Pack insertion detection deglitch                                     |  | 10  |          |          | ms    |
| T <sub>DLY(NDT)</sub>   | Pack removal detection delay  |  | 100   |          |          | µs    |
| R <sub>DSTSBIAS</sub>   | Integrated switch resistance  | Measured from VTSBIAS to V2V2  |   |          |          | 210 Ω |
| I <sub>TS(DET)</sub>  | TS pin bias current   | VTSBIAS to V2V2 switch open  | –1  |          |          | µA    |
| CHARGER INTEGRATED MOSFET CHARACTERISTICS                           |   |  |   |          |          |       |
| V <sub>BATDOCH</sub>  | Battery Switch dropout voltage, charge                                | V <sub>BATDOCH</sub> = V(VIN_CHG) – V(BAT) , V(BAT) :3V, I(BAT) = –1A  |   | 100      | 200      | mV    |
| I <sub>DCH(BAT)</sub>   | BAT pin discharge current   | ON at battery not detected and discharge switch enabled via I <sup>2</sup> C (BATDCH=HI), V(BAT) > 1 V         | 5   |          | 10       | mA    |
| CHARGER PROTECTION AND RECOVERY FUNCTIONS                           |   |  |   |          |          |       |
| V <sub>SH(VIN_CHG)</sub>  | VIN_CHG Short Circuit detection threshold                             | BATCHG switch set to OFF if V(VIN_CHG) < V <sub>SH(VIN_CHG)</sub>  | 1.0   | 1.2      | 1.4      | V     |
| V <sub>SH(BAT)</sub>  | BAT Short Circuit detection threshold                                 | BATCHG switch set to OFF if V(BAT) < V <sub>SH(BAT)</sub>  | 1.6   | 1.8      | 2.0      | V     |
| R <sub>SH(BAT)</sub>  | BAT short circuit recovery pull-up resistor                           | V(BAT) < V <sub>SH(BAT)</sub> , Internal resistor connected between VIN_CHG and BAT2                           | 1   |          |          | kΩ    |
| T <sub>CHG</sub>  | Charge safety timer   | Safety timer value, thermal and DPPM loops not active or DTC function disabled                                 | Selectable via I <sup>2</sup> C: 4, 5,6,8 hours |          |          | hours |
|   |   | Total accuracy   | –15% 15%  |          |          |       |
| T <sub>PRECHG</sub>   | Precharge timer   | Pre charge timer range, thermal and DPPM loops not active or DTC function disabled                             | TPCH=LO   |          | 25 30 35 | min   |
|   |   | TPCH=HI  |   | 50 60 70 |          |       |
| R <sub>TMR(FLT)</sub>   | Timer fault recovery pull-up resistor                                 | Internal resistor connected from VIN_CHG to BAT when timer fault is detected                                   | 1   |          |          | kΩ    |
| T <sub>STRCHG</sub>   | Charger thermal loop threshold  | Charge current reduced for T <sub>J</sub> > T <sub>STRCHG</sub>  | 125   |          |          | °C    |

## 2.7 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS  |   |            | MIN   | TYP                  | MAX   | UNIT |
|---|--|--|---|------------|-------|----------------------|-------|------|
| FAST CHARGE CURRENT , V(VIN_CHG) > V(BAT) + 0.2V , V(BAT) > V <sub>LOWBAT</sub> , t< T <sub>CHG</sub>                           |  |  |   |            |       |                      |       |      |
| I <sub>O(BAT)</sub>   | Charge current range   | I <sub>O(BAT)</sub> = K <sub>SET</sub> /R <sub>ISET</sub> DPPM/Thermal loops not active  |   |            | 0.1   |                      | 1.03  | A    |
| K <sub>SET</sub>  | Charge current set factor                                      | R <sub>ISET</sub> = 1 kΩ, scalable via I <sup>2</sup> C, (ISET_1, ISET_0) =  | 11, 100% scaling  |            | 703   | 865                  | 1020  | AΩ   |
|   |  |  | 10, 75% scaling   |            | 506   | 648                  | 773   |      |
|   |  |  | 01, 50% scaling   |            | 325   | 432                  | 530   |      |
|   |  |  | 00, 25% scaling   |            | 145   | 215                  | 293   |      |
| PRE CHARGE CURRENT , V(VIN_CHG) > V(BAT) + 0.1V , V <sub>SH(BAT)</sub> < V(BAT) < V <sub>LOWBAT</sub> , t < T <sub>PRECHG</sub> |  |  |   |            |       |                      |       |      |
| I <sub>O(PRECHG)</sub>  | Precharge current range  | I <sub>O(PRECHG)</sub> = K <sub>PRECHG</sub> /R <sub>ISET</sub> DPPM/Thermal loops not active  |   |            | 10    |                      | 170   | mA   |
| K <sub>PRECHG</sub>   | Precharge current set factor                                   | 0C<T <sub>J</sub> <125°C R <sub>ISET</sub> =1 kΩ,scalable via I <sup>2</sup> C, (IPCH_1, IPCH_0)=  | 00  |            | 10    | 43                   | 75    | AΩ   |
|   |  |  | 01  |            | 48    | 85                   | 115   |      |
|   |  |  | 10  |            | 80    | 126                  | 159   |      |
|   |  |  | 11  |            | 85    | 166                  | 205   |      |
| CHARGE CURRENT REDUCTION - THERMAL, DPPM LOOPS ACTIVE (T <sub>J</sub> > T <sub>STRCHG</sub> , V(SYS) < V <sub>SYSDPPM</sub> )   |  |  |   |            |       |                      |       |      |
| K <sub>THERMAL</sub>  | Thermal loop factor  | Charge Current (I <sub>CHG</sub> ) = I <sub>O(BAT)</sub> × (1 – K <sub>THERM</sub> × (T <sub>J</sub> – T <sub>STRCHG</sub> )/100)        |   |            | 10    |                      |       | %/°C |
| K <sub>DPPM</sub>   | DPPM loop factor   | Charge Current (I <sub>CHG</sub> ) = I <sub>O(BAT)</sub> × (1 – K <sub>DPPM</sub> × 10 × (V <sub>SYS(DPPM)</sub> – V <sub>(SYS)</sub> )) |   |            | 0.8   |                      |       | %/mV |
| CHARGE REGULATION VOLTAGE , V(VIN_CHG) > V <sub>O(BATREG)</sub> + 0.3V  |  |  |   |            |       |                      |       |      |
| V <sub>O(BATREG)</sub>  | Battery charge voltage, selectable via I <sup>2</sup> C        | Voltage options, Selection via I <sup>2</sup> C  |   | RSVD4B4=HI |       | 4.3, 4.35, 4.4, 4.45 |       | V    |
|   |  |  |   | RSVD4B4=LO |       | 4.1, 4.15, 4.2, 3.95 |       |      |
|   |  | Accuracy, T <sub>A</sub> = 25°C, relative to selected value  |   | –0.55%     |       | 0.95%                |       | V    |
|   |  | Total Accuracy, relative to selected value   |   | –0.85      |       | 1.2                  |       |      |
|   |  | Total Accuracy range for selected value of 4.2 V   |   | 4.16       |       | 4.25                 |       |      |
| CHARGE TERMINATION, V(BAT) > V <sub>RCH</sub> , t < T <sub>TERM</sub> , VOLTAGE REGULATION MODE SET                             |  |  |   |            |       |                      |       |      |
| I <sub>TERM</sub>   | Charge termination current range                               | I <sub>TERM</sub> = K <sub>TERM</sub> /R <sub>ISET</sub>   |   |            | 10    |                      | 170   | mA   |
| K <sub>TERM</sub>   | Charge termination detection factor                            | 40mA<I <sub>TERM</sub> <170mA, scalable via I <sup>2</sup> C, (ITERM_1, ITERM_0)=  | AC input selected or USBMODE=HI 170mA                         | 00         | 18    | 40                   | 50    | AΩ   |
|   |  |  |   | 01         | 42    | 82                   | 112   |      |
|   |  |  |   | 10         | 70    | 140                  | 188   |      |
|   |  |  |   | 11         | 85    | 165                  | 208   |      |
|   |  |  | USB input selected, (USBMODE=LO and USBLIM=LO) <sup>(2)</sup> |            | 18    |                      | 40    |      |
| T <sub>DGL(TERM)</sub>  | Deglitch time, termination detection                           | I(BAT) < I <sub>TERM</sub>   |   |            | 25    |                      |       | ms   |
| CHARGER DPPM LOOP AND SM2 CONTROL   |  |  |   |            |       |                      |       |      |
| V <sub>SYS(DPPM)</sub>  | SYS DPPM detection threshold , selectable via I <sup>2</sup> C | Charge current reduced for V(SYS)<V <sub>SYS(DPPM)</sub> , V <sub>SYS(DPPM)</sub> set via I <sup>2</sup> C, (SYSDPPM_1, SYSDPPM_0) =     |   | 00         | 3.413 | 3.5                  | 3.588 | V    |
|   |  |  |   | 01         | 3.656 | 3.75                 | 3.844 |      |
|   |  |  |   | 10         | 3.89  | 4.0                  | 4.1   |      |
|   |  |  |   | 11         | 4.144 | 4.25                 | 4.356 |      |
| VSM2TRK   | SM2 output voltage   | Battery tracking enabled – V(BAT)+value  |   |            | 0.17  | 0.265                | 0.37  | V    |

## 2.8 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER  |  | TEST CONDITIONS   | MIN  | TYP  | MAX   | UNIT |
|--|--|---|--|------|-------|------|
| <b>SM3 BOOST CONVERTER – CONTROL CIRCUIT AND POWER STAGE</b> |  |   |  |      |       |      |
| V <sub>VIN(SM3)</sub>  | Input Voltage range <sup>(1)</sup>   | V(VIN)  | 2.5  |      | 6.5   | V    |
| V <sub>O(SM3)</sub>  | Output voltage range <sup>(1)</sup>  | V(SM3)  | V <sub>VIN(SM3)</sub>  |      | 26.5  | V    |
| V <sub>OVP3</sub>  | Output over-voltage trip   | OVP detected at V(SM3) > V <sub>OVP3</sub>  | 26.5   | 28   | 29    | V    |
| V <sub>HYS(OVP3)</sub>                                       | Output over-voltage hysteresis   | OVP not detected at V(SM3) < V <sub>OVP3</sub> – V <sub>HYS(OVP3)</sub>           |  | 1.8  |       | V    |
| V <sub>(SM3REF)</sub>  | FB3 voltage sense threshold <sup>(1)</sup>                                     | V(FB3) below regulation point at V(FB3) < V <sub>(SM3REF)</sub>                   | 238  | 248  | 258   | mV   |
|  |  |   | 1.237  | 1.25 | 1.263 | V    |
| I <sub>O(SM3)</sub>  | LED current <sup>(1)</sup>   | $I_{O(SM3)} = \frac{V_{(SM3REF)}}{R_{FB3}}$<br>Current range,                     | 0  |      | 25    | mA   |
| D <sub>(SM3SW)</sub>   | LED switch duty cycle, selectable via I <sup>2</sup> C                         | Duty cycle range  | D <sub>(SM3SW)</sub> = 0% to 99.96%, set via I <sup>2</sup> C, 2048 steps 0.05% minimum step |      |       | %    |
| F <sub>(REP_SM3)</sub>                                       | LED switch duty cycle pattern repetition rate, selectable via I <sup>2</sup> C | 2048 pulses within repetition rate time, repetition rate set via I <sup>2</sup> C | F <sub>(REP_SM3)TYP</sub> = 550Hz, 366Hz, 275Hz or 220Hz                                     |      |       | Hz   |
|  |  | Total accuracy, relative to F <sub>(REP_SM3)TYP</sub>                             | –12% 12%   |      |       |      |
| R <sub>DS(ON)(SM3SW)</sub>                                   | LED switch FET on-resistance <sup>(1)</sup>                                    | V(VIN)=3.8 V; I(SM3SW)=20 mA  |  | 1    | 2     | Ω    |
| I <sub>LKG(SM3SW)</sub>                                      | LED switch FET leakage   |   |  | 1    | 4     | μA   |
| R <sub>DS(ON)(L3)</sub>                                      | Power stage FET on-resistance  | V(VIN)=3.8 V; I(L3)=200 mA  |  | 300  | 600   | mΩ   |
| I <sub>LKG(L3)</sub>   | Power stage FET leakage  |   |  | 1    | 4     | μA   |
| I <sub>MAX(L3)</sub>   | Power stage FET current limit  | 2.5V < V(IN) < 5.5V   | 400  | 500  | 600   | mA   |
| T <sub>SM3PWR(ON)</sub>                                      | Maximum on time detection threshold  |   | 5  | 6    | 15    | μs   |
| T <sub>SM3PWR(OFF)</sub>                                     | Minimum off time detection threshold   |   | 310  | 400  | 480   | ns   |
| <b>HIGH/LOW BRIGHTNESS CONTROL</b>                           |  |   |  |      |       |      |
| R <sub>DS(ON)(SM3G)</sub>                                    | Output buffer switch on resistance   | V(VIN)=2.5V, I(ISM3G)=25mA  |  | 1    | 2     | Ω    |
| I <sub>LKG(ISM3G)</sub>                                      | Leakage current  | Hi-Z mode, V(ISM3G)=5V  |  |      | 1     | μA   |
| <b>SWITCHING FREQUENCY</b>                                   |  |   |  |      |       |      |
| F <sub>SM3</sub>   | Maximum switching frequency <sup>(1)</sup>                                     | At nominal load   |  |      | 1     | MHz  |
| <b>GPIO1-4 – DIGITAL OUTPUT BUFFER</b>                       |  |   |  |      |       |      |
| V <sub>OL(GPIO)</sub>  | Low level output voltage   | I <sub>OL</sub> = 3 mA  |  |      | 0.6   | V    |
|  |  | I <sub>OL</sub> = 10 μA   |  |      | 0.1   |      |
| V <sub>OH(GPIO)</sub>  | High level output voltage GPIO   | I <sub>OH</sub> = –3 mA   | 1.5  |      |       | V    |
|  |  | I <sub>OH</sub> = –10 μA  | 1.8  |      |       |      |
| I <sub>OL(GPIO)</sub>  | Maximum low level sink current   | V(GPIO <sub>ON</sub> )=2.5V   |  |      | 5     | mA   |
| I <sub>OH(GPIO)</sub>  | Maximum high level source current <sup>(1)</sup>                               | V(GPIO <sub>ON</sub> )=0V   | –5   |      |       | mA   |
| <b>GPIO1-4 – DIGITAL INPUT BUFFER</b>                        |  |   |  |      |       |      |
| V <sub>IL(GPIO)</sub>  | Low level input voltage  |   |  |      | 0.4   | V    |
| V <sub>IH(GPIO)</sub>  | High level input voltage   |   | 1.15   |      |       | V    |
| I <sub>LKG(GPIO)</sub>                                       | Input current  | V(GPIO <sub>ON</sub> )=5V or 0V, GPIO configured, GPIO input current sink OFF     |  |      | 0.5   | μA   |
| <b>GPIO1-4 - INPUT CURRENT SINK</b>                          |  |   |  |      |       |      |
| I <sub>SNK(GPIO)</sub>                                       | Input current sink   | ON if TPS658621A is not in sleep mode and GPIO is not configured.                 |  | 2.5  | 3.5   | μA   |

(1) Not production tested

## 2.9 ELECTRICAL CHARACTERISTICS (Continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                     |  | TEST CONDITIONS  |  | MIN   | TYP | MAX  | UNIT |
|---|--|--|--|---|-----|------|------|
| PWM DRIVER, PWM OPEN DRAIN OUTPUT             |  |  |  |   |     |      |      |
| I <sub>PWM</sub>                              | Maximum operating current <sup>(1)</sup> | PWM driver ON  |  |   |     | 200  | mA   |
| V <sub>OL</sub>                               | Low level output voltage                 | I <sub>OL</sub> = 100mA , V(AVDD6)=3V  |  |   |     | 0.2  | V    |
| F <sub>(PWM)</sub>                            | PWM driver frequency                     | Frequency range  |  | Set via I <sup>2</sup> C F <sub>(PWM)TYP</sub> = 0.75, 1.5, 2.3, 3.0, 4.5, 6.7,11.7,23.4      |     |      | kHz  |
| D <sub>(PWM)</sub>                            | PWM driver duty cycle                    | Duty cycle range   |  | D <sub>(PWM)</sub> = 6.25% to 100%, set via I <sup>2</sup> C, 15 steps, 6.25% minimum step    |     |      | %    |
| I <sub>LKG(PWM)</sub>                         | Output off leakage current               | Output voltage = 5V, driver set to OFF   |  |   | 1   | 5    | µA   |
| LED_PWM DRIVER, LED_PWM OPEN DRAIN OUTPUT     |  |  |  |   |     |      |      |
| I <sub>LEDPWM</sub>                           | Maximum operating current <sup>(1)</sup> | PWM driver ON  |  |   |     | 200  | mA   |
| D <sub>(LEDPWM)</sub>                         | LED_PWM driver duty cycle                | Duty cycle range, 128Hz repetition rate  |  | D <sub>(LEDPWM)</sub> = 0% to 99.6%, set via I <sup>2</sup> C, 255 steps, 0.4% minimum step   |     |      | %    |
|   |  | Total accuracy, relative to selected value   |  | −10% 10%  |     |      |      |
| V <sub>OL(LEDPWM)</sub>                       | Low level output voltage                 | I <sub>OL</sub> = 50mA , V(AVDD6) = 3 V  |  |   |     | 0.2  | V    |
| I <sub>LKG(LEDPWM)</sub>                      | Output off leakage current               | Output voltage = 5 V, driver set to OFF  |  |   | 1   | 5    | µA   |
| RGB DRIVER, RED/GREEN/BLUE OPEN DRAIN OUTPUTS |  |  |  |   |     |      |      |
| T <sub>FLASH(RGB)</sub>                       | RGB1, RGB2 Flashing period               | Flashing period range  |  | T <sub>FLASH(RGB)</sub> = 1 to 8 sec, set via I <sup>2</sup> C, 0.5sec minimum step, 15 steps |     |      | s    |
| T <sub>FLASH(ON)</sub>                        | RGB1, RGB2 Flash On Time                 | Flash on time range, value selectable by I <sup>2</sup> C  |  | Set via I <sup>2</sup> C, T <sub>FLASH(ON)</sub> = 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6   |     |      | s    |
| D <sub>(RGB)</sub>                            | RGB1, RGB2 Duty Cycle                    | Duty cycle range, value selectable via I <sup>2</sup> C  |  | D <sub>(RGB)</sub> = 0% to 96.875%, set via I <sup>2</sup> C, 3.125% minimum step             |     |      | %    |
| I <sub>SINK(RGB1)</sub>                       | RGB1 output sink current                 | V(RED1) = V(GREEN1) = V(BLUE1) = 0.25V   | Sink current, set via I <sup>2</sup> C         | I <sub>SINK(RGB1)TYP</sub> = 0, 3.7, 7.4, 11.1  |     |      | mA   |
|   |  |  | Absolute accuracy relative to selected value   | −35% 35%  |     |      |      |
|   |  |  | Relative accuracy between sink current outputs | −10% 10%  |     |      |      |
| I <sub>SINK(RGB2)</sub>                       | RGB2 output sink current                 | V(RED2) = V(GREEN2) = V(BLUE2) = 0.25V   | Sink current, set via I <sup>2</sup> C         | I <sub>SINK(RGB)</sub> at TYP = 0, 3.7, 7.4, 11.1, 14.9, 18.6, 23.2, 27.3,                    |     |      | mA   |
|   |  |  | Absolute accuracy relative to selected value   | −35% 35%  |     |      |      |
|   |  |  | Relative accuracy between sink current outputs | −10% 10%  |     |      |      |
| V <sub>LO(RGB1)</sub>                         | Low level output voltage                 | Output low voltage, RED1/GREEN1/BLUE1 pins, one current source ON (4 or 8 or 12mA source) ON at a time, V(AVDD6)=3V            |  |   |     | 0.25 | V    |
| V <sub>LO(RGB2)</sub>                         | Low level output voltage                 | Output low voltage, 16mA load, RED2/GREEN2/BLUE2 pins, one current source ON (4 or 8 or 16mA source) ON at a time, V(AVDD6)=3V |  |   |     | 0.25 | V    |
| I <sub>LKG(RGB)</sub>                         | Output off leakage current               | Output voltage = 5V, driver set to OFF   |  |   | 1   | 2    | µA   |
| DIG_PWM , DIG_PWM1 DRIVER , PUSH PULL OUTPUT  |  |  |  |   |     |      |      |
| F <sub>(PWM)</sub>                            | PWM driver frequency                     | Frequency range  |  | 110   | 125 | 140  | Hz   |
|   |  | Total accuracy, relative to selected value   |  | −10% 10%  |     |      |      |
| V <sub>HI(DIGPWM)</sub>                       | Output level, HI                         | V(DIG_PWM) at I(DIG_PWM) = −5 mA   |  | 1.7   |     |      | V    |
|   |  | V(DIG_PWM) at I(DIG_PWM) = −10 µA  |  | 2.0   |     |      |      |
| V <sub>LO(DIGPWM)</sub>                       | Output level, LO                         | V(DIG_PWM) at I(DIG_PWM) = 5 mA  |  | 0.5   |     |      | V    |
|   |  | V(DIG_PWM) at I(DIG_PWM) = −10 µA  |  | 0.1   |     |      |      |

(1) Not production tested

## 2.10 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 |  | TEST CONDITIONS  | MIN            | TYP   | MAX                          | UNIT |
|---|--|--|----------------|-------|------------------------------|------|
| ADC REFERENCE                             |  |  |                |       |                              |      |
| V <sub>REF(ADC)</sub>                     | Internal ADC reference voltage                                       | T <sub>A</sub> = 25°C  | 2.595          | 2.6   | 2.605                        | V    |
|   |  | Over full temp range   | 2.577          | 2.595 | 2.607                        |      |
| I <sub>SHRT(ADCREF)</sub>                 | Internal reference short circuit limit                               | V(ADC_REF)=AGND1   | 3.0            | 4.5   |                              | mA   |
| C <sub>REFADC</sub>                       | Maximum capacitance for internal ADC reference supply <sup>(1)</sup> |  |                |       | 6.8                          | μF   |
| ADC ANALOG INPUTS                         |  |  |                |       |                              |      |
| V <sub>RNG(CH1_6)</sub>                   | Full scale input range Channels 1–6 <sup>(1)</sup>                   | Positive inputs, Full scale ~ 2.60 V   | 0              |       | V <sub>REF(ADC)</sub>        | V    |
| V <sub>RNG(CH7_10)</sub>                  | Full scale input range Channels 7, 10 <sup>(1)</sup>                 | Positive inputs, Full scale ~ 4.622 V  | 0              |       | V <sub>REF(ADC)</sub> × 1.78 | V    |
| V <sub>RNG(CH8_9)</sub>                   | Full scale input range Channels 8, 9 <sup>(1)</sup>                  | Positive inputs , Full scale ~ 5.54 V  | 0              |       | V <sub>REF(ADC)</sub> × 2.13 | V    |
| C <sub>IN(ADC)</sub>                      | Input capacitance (all channels)                                     |  |                | 15    |                              | pF   |
| R <sub>INADC(CH1_6)</sub>                 | Input resistance (all channels)                                      | AVDD6-V(ANLG) >= 500mV   | 1              |       |                              | MΩ   |
| I <sub>LKGADC(CH1_6)</sub>                | Leakage current (all channels)                                       | ADC disabled   |                | 0.1   | 1                            | μA   |
| ADC – DC ACCURACY                         |  |  |                |       |                              |      |
| RES <sub>(ADC)</sub>                      | Resolution   | SAR ADC  |                | 10    |                              | Bits |
| MCD <sub>(ADC)</sub>                      | Missing codes  |  |                | None  |                              |      |
| INL <sub>(ADC)</sub>                      | Integral Linearity Error   |  |                | ±3    |                              | LSB  |
| DNL <sub>(ADC)</sub>                      | Differential non-linearity error                                     |  |                | ±1    |                              | LSB  |
| OFF <sub>ZERO(ADC)</sub>                  | Offset error   | Deviation from the first code transition (00..00) to (00.001) from the ideal AGND + 1LSB         |                | 1     | 5                            | LSB  |
| OFF <sub>CH(ADC)</sub>                    | Offset error match between channels <sup>(1)</sup>                   |  |                | 1     | 5                            | LSB  |
| GAIN <sub>(ADC)</sub>                     | Gain error   | Deviation in code from the ideal full scale code (11...111) for the full scale voltage           |                | ±8    |                              | LSB  |
| GAIN <sub>CH(ADC)</sub>                   | Gain error match   | Any two channels   |                | 2     |                              | LSB  |
| ADC THROUGHPUT SPEED                      |  |  |                |       |                              |      |
| ADC <sub>CLK</sub>                        | Sampling Clock <sup>(1)</sup>  |  | 506            | 562   | 619                          | kHz  |
| ADC <sub>TCONV</sub>                      | Sampling and conversion time   | Sampling time - 9X ADCCLK  |                | 16    |                              | μs   |
|   |  | conversion and settling time -11X ADCCLK   |                | 20    |                              | μs   |
| ANLGx (USER_DEFINED INPUTS) BIAS CURRENTS |  |  |                |       |                              |      |
| I <sub>(ANLGx)</sub>                      | ANLG1, 2, or 3 pin internal pull-up current source                   | ADC channel 1 bias current, set via I <sup>2</sup> C register ADC_WAIT bits (ADICH2_1, ADICH2_2) | 00 =           | 0     |                              | μA   |
|   |  |  | 01 =           | 3     |                              |      |
|   |  |  | 10 =           | 10    |                              |      |
|   |  |  | 11 =           | 50    |                              |      |
|   |  |  | Total Accuracy |       | –20%                         |      |

(1) Not production tested

## 2.11 PIN DESCRIPTION, REQUIRED EXTERNAL COMPONENTS

### 2.11.1 Package Pinout (Top View)

|         |          |          |         |        |          |          |           |           |          |          |          |            |
|---------|----------|----------|---------|--------|----------|----------|-----------|-----------|----------|----------|----------|------------|
| N13     | N12      | N11      | N10     | N9     | N8       | N7       | N6        | N5        | N4       | N3       | N2       | N1         |
| L3      | FB3      | DIG_PWM  | LED_PWM | BLUE1  | VIN_LDO9 | VIN_LDO4 | XTAL2     | VIN_LDO01 | GPIO4    | GPIO2    | HSK      | COMP       |
| M13     | M12      | M11      | M10     | M9     | M8       | M7       | M6        | M5        | M4       | M3       | M2       | M1         |
| L3      | SM3_SW   | nNOPOWER | VTSBIAS | GREEN1 | BLUE2    | LDO9     | XTAL1     | LDO0      | GPIO3    | GPIO1    | ANLG3    | ANLG1      |
| L13     | L12      | L11      | L10     | L9     | L8       | L7       | L6        | L5        | L4       | L3       | L2       | L1         |
| PGND3   | PGND3    | SM3      | nINT    | RED1   | GREEN2   | LDO4     | LDO1      | HSK       | HSK      | ANLG2    | CHG_STAT | LDO4PG     |
| K13     | K12      | K11      | K10     | K9     | K8       | K7       | K6        | K5        | K4       | K3       | K2       | K1         |
| AVDD6   | SM3IG    | ISSET    | HSK     | PWM    | RED2     | HSK      | DGND1     | HSK       | AGND2    | ADC_REF  | LDO7     | LDO8       |
| J13     | J12      | J11      | J10     | J9     | J8       | J7       | J6        | J5        | J4       | J3       | J2       | J1         |
| TS      | VREF1V25 | V2V2     | AGND1   | HSK    | HSK      | HSK      | HSK       | HSK       | PSDAT    | PSCLK    | SDAT     | VIN_LDO678 |
| H13     | H12      | H11      | H10     | H9     | H8       | H7       | H6        | H5        | H4       | H3       | H2       | H1         |
| VIN_CHG | VIN_CHG  | VIN_CHG  | RTC_OUT | HSK    | HSK      | HSK      | HSK       | HSK       | SCLK     | VIN_SM1  | VIN_SM1  | VIN_SM1    |
| G13     | G12      | G11      | G10     | G9     | G8       | G7       | G6        | G5        | G4       | G3       | G2       | G1         |
| BAT     | BAT      | BAT      | BAT     | HSK    | HSK      | HSK      | HSK       | HSK       | LDO6     | VIN_SM1  | L1       | L1         |
| F13     | F12      | F11      | F10     | F9     | F8       | F7       | F6        | F5        | F4       | F3       | F2       | F1         |
| USB     | USB      | USB      | SM0EN   | HSK    | HSK      | HSK      | HSK       | HSK       | DIG_PWM2 | PGND1    | PGND1    | PGND1      |
| E13     | E12      | E11      | E10     | E9     | E8       | E7       | E6        | E5        | E4       | E3       | E2       | E1         |
| USB     | SM2      | SM1EN    | SYNCEN  | HSK    | HSK      | HSK      | HSK       | HSK       | HSK      | PGND0    | PGND0    | PGND0      |
| D13     | D12      | D11      | D10     | D9     | D8       | D7       | D6        | D5        | D4       | D3       | D2       | D1         |
| AC      | AC       | AC       | HSK     | HSK    | HSK      | V32K     | DGND2DT   | HSK       | nNORTC   | VIN_SM0  | L0       | L0         |
| C13     | C12      | C11      | C10     | C9     | C8       | C7       | C6        | C5        | C4       | C3       | C2       | C1         |
| AC      | AC       | SYS      | VIN_SM2 | L2     | PGND2    | OUT32K   | SM1       | AGND3     | SM0      | VIN_SM0  | VIN_SM0  | VIN_SM0    |
| B13     | B12      | B11      | B10     | B9     | B8       | B7       | B6        | B5        | B4       | B3       | B2       | B1         |
| SYS     | SYS      | SYS      | VIN_SM2 | L2     | PGND2    | LDO2     | LDO3      | AGND3     | SM0PG    | LDO4EN   | RESUME   | VIN_SM0    |
| A13     | A12      | A11      | A10     | A9     | A8       | A7       | A6        | A5        | A4       | A3       | A2       | A1         |
| SYS     | SYS      | SYS      | VIN_SM2 | L2     | PGND2    | LDO5     | VIN_LDO23 | SM1PG     | AGND3    | TNOPOWER | nHOT_RST | VIN_SM0    |

### PIN FUNCTIONS

| NAME                     | PIN                                     | I/O | DESCRIPTION  | EXTERNAL REQUIRED COMPONENTS<br>(See Application Diagram)  |
|--------------------------|---|-----|--|--|
| <b>SYSTEM POWER PATH</b> |   |     |  |  |
| AC                       | C12,C13,<br>D11,D12,<br>D13             | I   | Adapter Charge Input Voltage, connect to AC_DC adapter positive output terminal (DC voltage) | 1uF(minimum) capacitor to AGND1 pin to minimize over-voltage transients during AC power hot-plug events.           |
| USB                      | E13,F11,<br>F12,F13                     | I   | USB charge input voltage, connect to USB port positive power output                          | 1uF(minimum) capacitor to AGND1 pin, to minimize over-voltage transients during USB power hot-plug events.         |
| BAT                      | G10,G11,<br>G12,G13                     | I/O | Battery power  | Connect to battery positive terminal. Connect 4.7uF capacitor (minimum) from BAT2 pin to clean analog ground plane |
| SYS                      | A11,A12,<br>A13,B11,<br>B12,B13,<br>C11 | O   | AC/BAT/USB Power path output. Connect to System main power rail (system power bus)           | 10uF capacitor to AGND1 pin  |



### PIN FUNCTIONS (continued)

| NAME                       | PIN                       | I/O | DESCRIPTION   | EXTERNAL REQUIRED COMPONENTS<br>(See Application Diagram)  |
|----------------------------|---------------------------|-----|---|--|
| <b>REFERENCE SYSTEM</b>    |                           |     |   |  |
| TNOPOWER                   | A3                        | I   | NOPOWER pin pulse width   | Capacitor to AGND1. Capacitor value sets pulse width   |
| AVDD6                      | K13                       | O   | Internal supply rail  | Connect 4.7µF capacitor to AGND1   |
| V2V2                       | J11                       | O   | Internal 2.2V supply rail   | 1µF (minimum) decoupling capacitor to AGND1  |
| VREF1V25                   | J12                       | O   | Internal 1.25V reference filter capacitor   | 100nF (minimum) decoupling cap to AGND1  |
| <b>CHARGER</b>             |                           |     |   |  |
| TS                         | J13                       | I/O | Temperature Sense Input, current source output                                    | Connect to battery pack thermistor to sense battery pack temperature   |
| ISET                       | K11                       | I   | Current set point when charging with AC selected.                                 | External resistor from ISET pin to AGND1 pin sets charge current value   |
| VTSBIAS                    | M10                       | O   | Thermistor network bias supply, internally connected to 2V2 via integrated switch | Connect to external thermistor pull-up resistor  |
| VIN_CHG                    | H11,H12,<br>H13           | I/O | Charger supply.   | Connect to SM2 converter output or SYS pin, see charger section  |
| CHG_STAT                   | L2                        | O   | Charger Status  | Push-pull output, 2V2 level  |
| <b>SM3 BOOST CONVERTER</b> |                           |     |   |  |
| L3                         | M13,N13                   | O   | Drain of the integrated boost power stage switch                                  | 4.7µH inductor to SYS pin, external Schottky diode to SM3 pin  |
| FB3                        | N12                       | I   | White LED duty cycle switch output, LED current setting                           | External resistor from FB3 pin to PGND3 pin sets LED peak current. Connect 100pF (minimum) filter capacitor to PGND3 pin.          |
| SM3_SW                     | M12                       | I   | Integrated White LED duty cycle switch input                                      |  |
| SM3IG                      | K12                       | I/O | General purpose input/output  | HI-Z Output, controlled via I <sup>2</sup> C. May be used to set SM3 current gain step, implementing a high/low brightness control |
| SM3                        | L11                       | I   | White LED driver output over-voltage detection                                    | Connect 1µF capacitor to PGND3 pin. Connect SM3 pin to the positive side of white LED ladder.                                      |
| PGND3                      | L12,L13                   | I   | Power ground, SM3 converter   | Connect to the power ground plane  |
| <b>DRIVERS</b>             |                           |     |   |  |
| RED2                       | K8                        | O   | Programmable LED driver, open drain output, current sink output when active.      | Connect to RED input of RGB LED  |
| GREEN2                     | L8                        | O   |   | Connect to GREEN input of RGB LED  |
| BLUE2                      | M8                        | O   |   | Connect to BLUE input of RGB LED   |
| RED1                       | L9                        | O   |   | Connect to RED input of RGB LED  |
| GREEN1                     | M9                        | O   |   | Connect to GREEN input of RGB LED  |
| BLUE1                      | N9                        | O   |   | Connect to BLUE input of RGB LED   |
| LED_PWM                    | N10                       | O   | LED_PWM driver output, open drain, programmable duty cycle.                       | Can be used to drive a keyboard backlight LED or other external functions  |
| PWM                        | K9                        | I   | PWM DRIVER, open drain output   | May be used to control external vibrator motor   |
| DIG_PWM                    | N11                       | O   | PWM, digital push-pull output   | 2V2 output voltage level   |
| DIG_PWM2                   | F4                        | O   | PWM, digital push-pull output   | 2V2 output voltage level   |
| <b>DC/DC CONVERTERS</b>    |                           |     |   |  |
| VIN_SM0                    | A1,B1,C<br>1,C2,C3,<br>D3 | I   | SM0 synchronous buck converter positive supply input                              | 2 x 10µF capacitor to PGND0 pin  |
| SM0                        | C4                        | I   | SM0 synchronous buck converter output voltage sense                               | LC filter: 1.5µH Inductor and 10µF Capacitor. Connect capacitor to PGND0 pin   |
| L0                         | D1,D2                     | O   | SM0 synchronous buck converter power stage output                                 | 1.5µH inductor to SM0 pin  |
| PGND0                      | E1,E2,E3                  | I   | Power ground, SM0 converter   | Connect to the power ground plane  |
| VIN_SM1                    | G3,H1,H<br>2,H3           | I   | SM1 synchronous buck converter positive supply input                              | 2 x 10µF capacitor to PGND1 pin  |
| SM1                        | C6                        | I   | SM1 synchronous buck converter output voltage sense                               | LC filter: 1.5µH Inductor and 10µF Capacitor. Connect capacitor to PGND1 pin   |
| L1                         | G1,G2                     | O   | SM1 synchronous buck converter power stage output                                 | 1.5µH inductor to SM1 pin  |
| PGND1                      | F1,F2,F3                  | I   | Power ground, SM1 converter   | Connect to the power ground plane  |
| VIN_SM2                    | A10,B10,<br>C10           | I   | SM2 synchronous buck converter positive supply input                              | 2 x 10µF capacitor to PGND2 pin  |
| SM2                        | E12                       | I   | SM2 synchronous buck converter output voltage sense                               | LC filter: 1.5µH Inductor, 10µF Capacitor. Connect capacitor to PGND2 pin  |

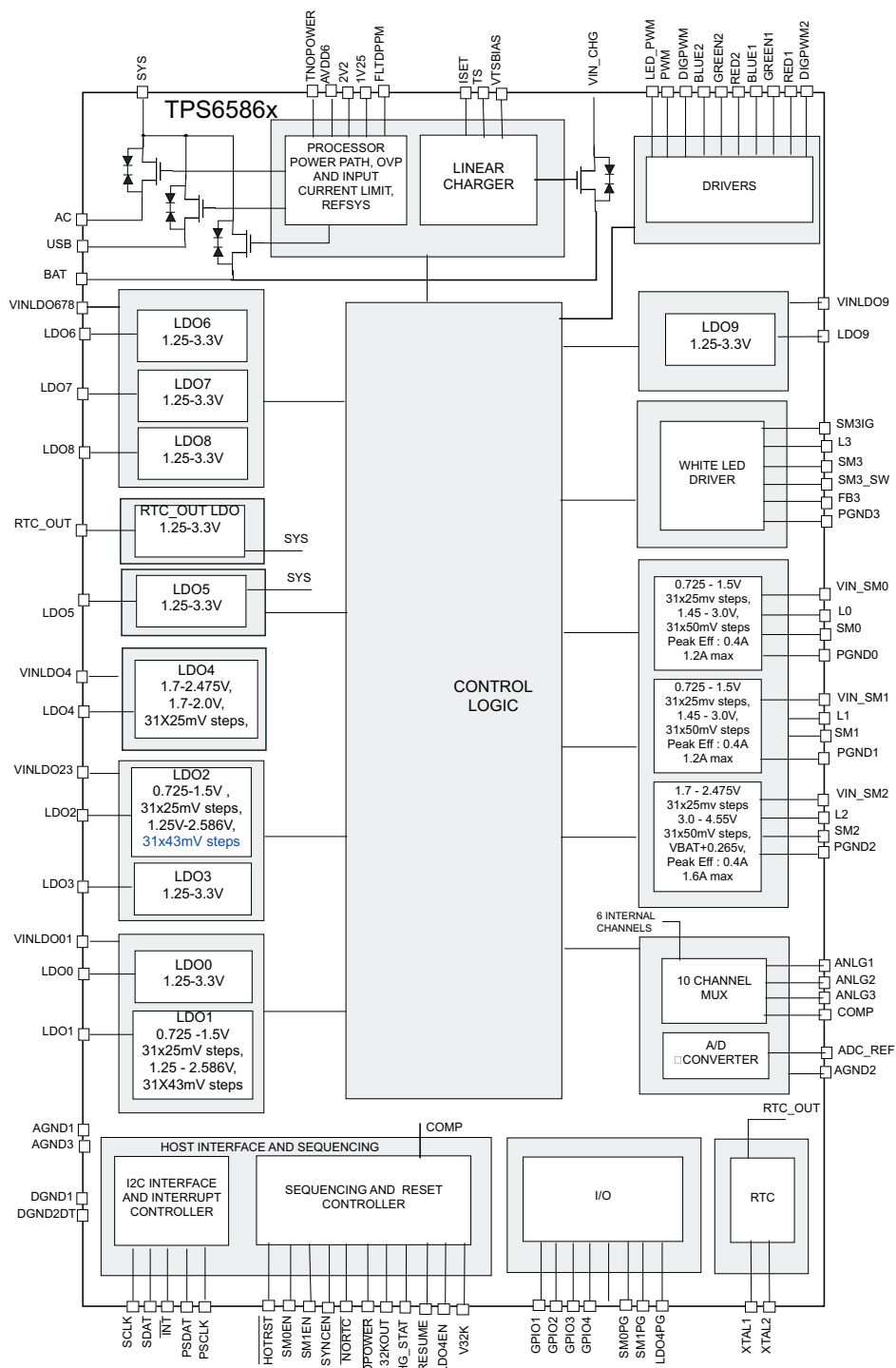
**PIN FUNCTIONS (continued)**

| NAME  | PIN      | I/O | DESCRIPTION  | EXTERNAL REQUIRED COMPONENTS<br>(See Application Diagram)   |
|---|----------|-----|--|---|
| L2  | A9,B9,C9 | O   | SM2 synchronous buck converter power stage output                        | 1.5μH inductor to SM2 pin   |
| PGND2   | A8,B8,C8 | I   | Power ground pin, SM2 converter  | Connect to power ground plane   |
| ADC   |          |     |  |   |
| AGND2   | K4       | I   | Analog ground, ADC subsystem   | Connect to analog ground plane  |
| ANLG1   | M1       | I   | Analog input1 to ADC, programmable current source output                 | Can be used to monitor additional system or pack parameters   |
| ANLG2   | L3       | I   | Analog input2 to ADC, programmable current source output                 |   |
| ANLG3   | M2       | I   | Analog input3 to ADC, programmable current source output                 |   |
| ADC_REF   | K3       | I/O | ADC internal reference filter or ADC external reference input            | Connect a maximum capacitance of 6.8uF referenced to the AGND2 pin.   |
| EXTERNAL SYSTEM RESET AND CLOCK OUTPUTS, ADJUSTABLE LEVEL |          |     |  |   |
| V32K  | D7       | I   | Power supply for host interface buffers                                  |   |
| INT   | L10      | O   | Interruption pin nINT pin is LO when interrupt is requested by TPS658XX. | Open drain output   |
| OUT32K  | C7       | O   | 32kHz clock from external XTAL   | Push-pull output, V32K level  |
| NOPOWER   | M11      | O   | Host reset output, LO level, adjustable width                            |   |
| NORTC   | D4       | O   | RTC_OUT POR pulse, LO level, fixed width                                 |   |
| SEQUENCING CONTROL INPUTS                                 |          |     |  |   |
| HOT_RST   | A2       | I/O | Reboot cycle request   | Hardware reboot cycle control   |
| RESUME  | B2       | I   | Sleep on/off request   | Hardware sleep on/off control   |
| LDO4EN  | B3       | I   | LDO4 enable control  |   |
| SM0EN<br>(CORECTRL)                                       | F10      | I   | Supply enable control  | Active low signal.  |
| SM1EN   | E11      | I   | Supply enable control  |   |
| SYNCEN  | E10      | I   | Supply enable control  |   |
| I <sup>2</sup> C INTERFACE                                |          |     |  |   |
| PSDAT   | J4       | I/O | Power I <sup>2</sup> C clock line  | Connect to external host power I <sup>2</sup> C clock. Connect 2K external pull-up resistor. Connect to 2V2 pin if not used |
| PSCLK   | J3       | I   |  |   |
| SDAT  | J2       | I/O | I <sup>2</sup> C interface data line                                     | Connect 2K external pull-up resistor.   |
| SCLK  | H4       | I   | I <sup>2</sup> C interface clock line                                    |   |
| RTC OSCILLATOR  |          |     |  |   |
| XTAL1   | M6       | I   | Xtal oscillator  | Connect to external xtal  |
| XTAL2   | N6       | I   |  |   |
| INPUT / OUTPUT  |          |     |  |   |
| GPIO1   | M3       | I/O | General purpose input/output   | Input: SM0, SM1, SM2 power saving mode and output voltage setting control   |
| GPIO2   | N3       | I/O | General purpose input/output   | Input: ADC external trigger or LDO0, LDO1 enable  |
| GPIO3   | M4       | I/O |  | Input: LDO2, LDO3 enable  |
| GPIO4   | N4       | I/O |  | Input: ADC external trigger or LDO6, LDO7, LDO8 enable  |
| COMP  | N1       | I   | General purpose comparator input, ADC input                              |   |
| SM0PG   | B4       | O   | SM0 power good status  |   |
| SM1PG   | A5       | O   | SM1 power good status  |   |
| LDO4PG  | L1       | O   | LDO4 power good status   |   |
| LINEAR REGULATORS   |          |     |  |   |
| VIN_LDO01   | N5       | I   | Positive supply input for LDO0, LDO1                                     | 1μF (minimum) decoupling capacitor to AGND1   |
| LDO0  | M5       | O   | LDO0 output  | 1μF(minimum) capacitor to AGND1   |
| LDO1  | L6       | O   | LDO1 output  | 1μF(minimum) capacitor to AGND1   |
| VIN_LDO23   | A6       | I   | Positive supply input for LDO2, LDO3                                     | 1μF (minimum) decoupling capacitor to AGND1   |
| LDO2  | B7       | O   | LDO2 output  | 1μF(minimum) capacitor to AGND1   |

**PIN FUNCTIONS (continued)**

| NAME                                  | PIN                 | I/O | DESCRIPTION  | EXTERNAL REQUIRED COMPONENTS<br>(See Application Diagram) |
|---------------------------------------|---------------------|-----|--|---|
| LDO3                                  | B6                  | O   | LDO3 output  | 1μF(minimum) capacitor to AGND1                           |
| VIN_LDO4                              | N7                  | I   | Positive supply input for LDO4   | 1μF (minimum) decoupling capacitor to AGND1               |
| LDO4                                  | L7                  | O   | LDO4 output  | 1μF(minimum) capacitor to AGND1                           |
| LDO5                                  | A7                  | O   | LDO5 output  | 1μF(minimum) capacitor to AGND1                           |
| VIN_LDO678                            | J1                  | I   | Positive supply input for LDO0, LDO1   | 1μF (minimum) decoupling capacitor to AGND1               |
| LDO6                                  | G4                  | O   | LDO6 output  | 1μF(minimum) capacitor to AGND1                           |
| LDO7                                  | K2                  | O   | LDO7 output  | 1μF(minimum) capacitor to AGND1                           |
| LDO8                                  | K1                  | O   | LDO8 output  | 1μF(minimum) capacitor to AGND1                           |
| VIN_LDO9                              | N8                  | I   | Positive supply input for LDO9   | 1μF (minimum) decoupling capacitor to AGND1               |
| LDO9                                  | M7                  | O   | LDO9 output  | 1μF(minimum) capacitor to AGND1                           |
| RTC_OUT                               | H10                 | O   | Low leakage LDO output. Can be connected to a super-capacitor or secondary cell, if used as a RTC backup output.   | 1μF (minimum) capacitor to AGND1 pin or supercap          |
| <b>ANALOG AND DIGITAL GROUND PINS</b> |                     |     |  |   |
| DGND1                                 | K6                  | I   | Digital ground pin   | Connect to digital ground plane                           |
| AGND1                                 | J10                 | I   | Analog ground pin  | Connect to analog ground plane                            |
| AGND3                                 | A4,B5,C5            | I   | Analog ground pin  | Connect to analog ground plane                            |
| DGND2DT                               | D6                  | I/O | Digital ground pin   | Connect to analog ground plane                            |
| HSK                                   | See Package Drawing | N/A | There is an internal electrical connection between all HSK pins of the IC. The HSK pins must be connected to the same potential as the AGND1 pin on the printed circuit board. <b><i>Do not use the HSK pins as the primary ground input for the IC.</i></b> |   |

## 2.11.2 Block Diagram



## 2.12 TYPICAL CHARACTERISTICS

LDO9 Vout vs. Iout (Temp. = 25°C) 1.250V

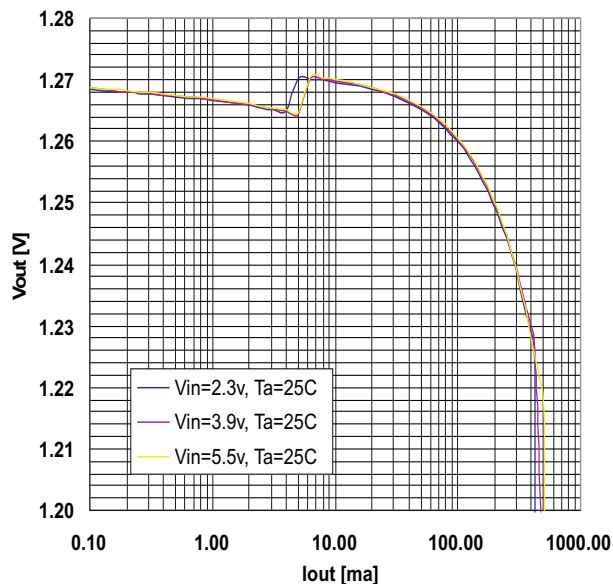


Figure 2-1.

LDO9 Vout vs. Iout (Temp. = 25°C) 3.30V

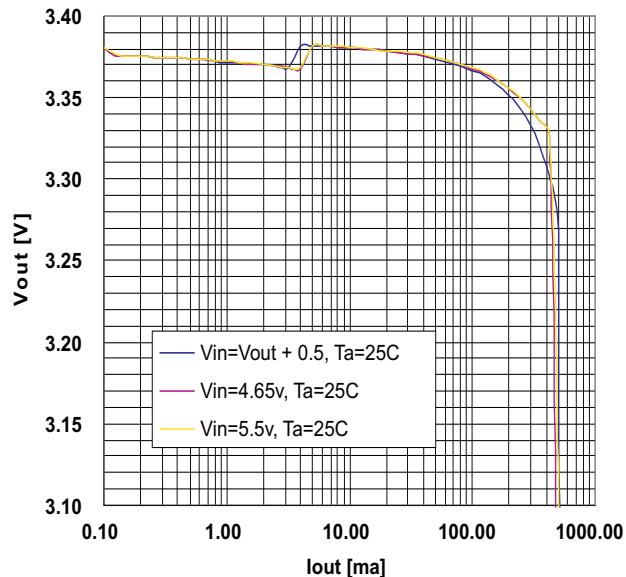


Figure 2-2.

LDO0 Vout vs. Iout (Temp. = 25°C) 1.250V

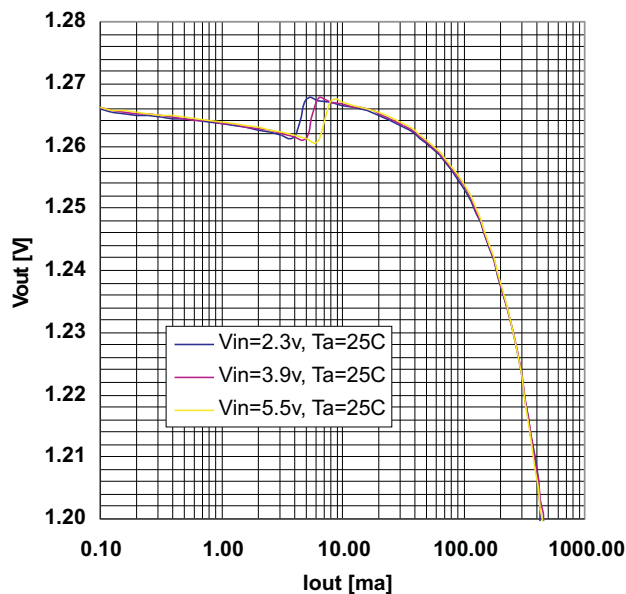


Figure 2-3.

LDO0 Vout vs. Iout (Temp. = 25°C) 3.30V

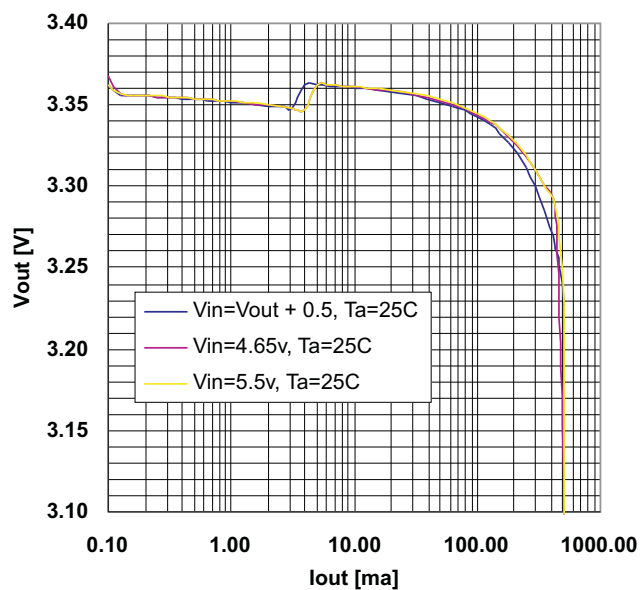


Figure 2-4.

(continued)

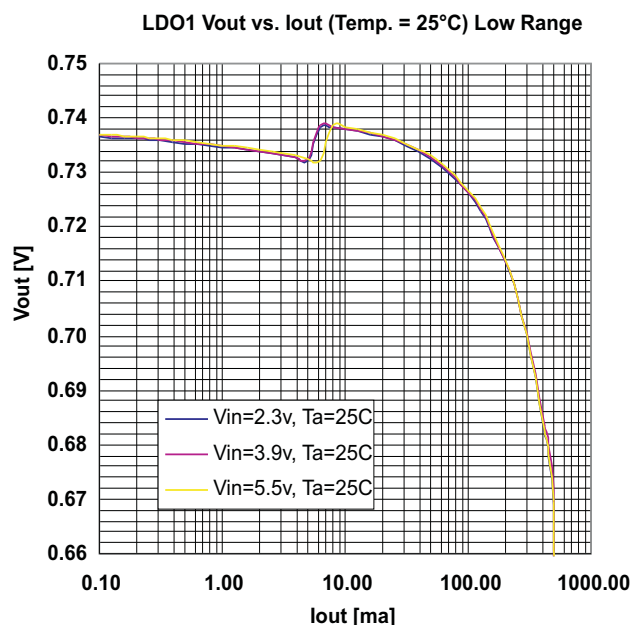


Figure 2-5.

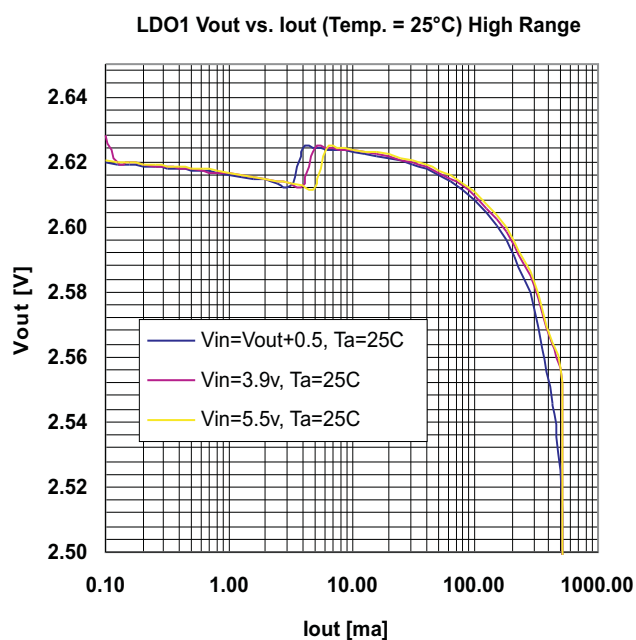


Figure 2-6.

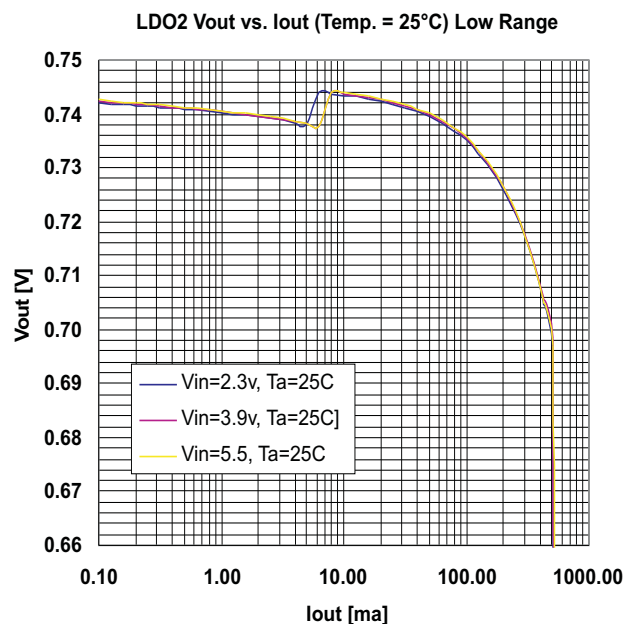


Figure 2-7.

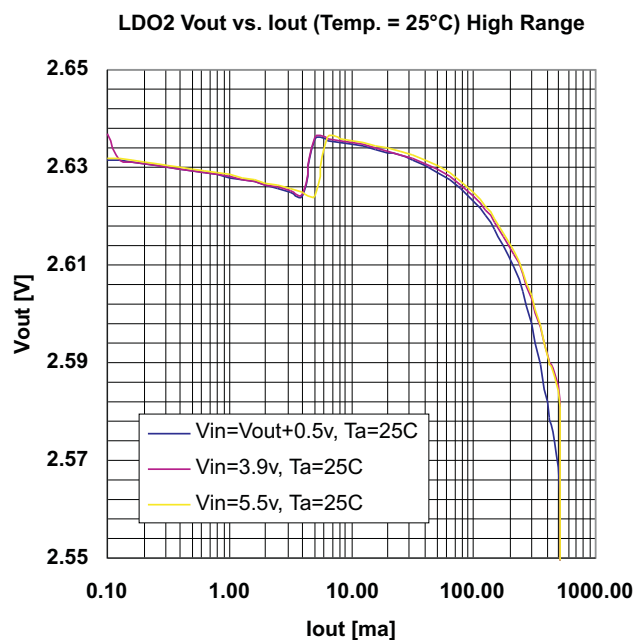


Figure 2-8.

(continued)

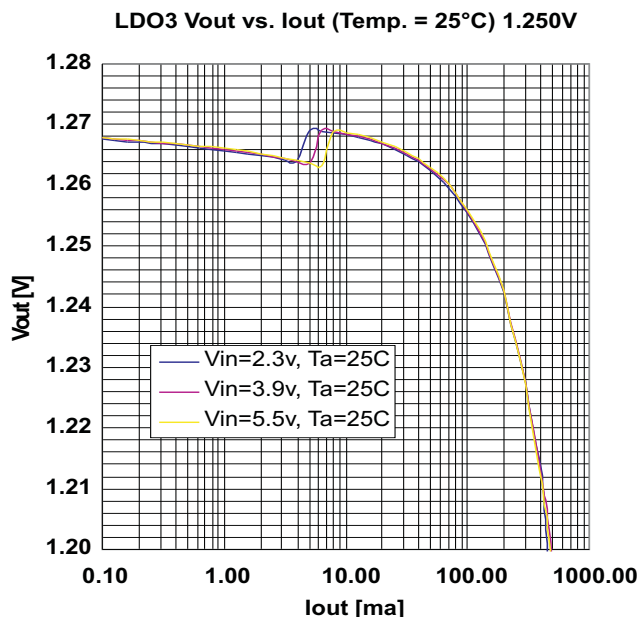


Figure 2-9.

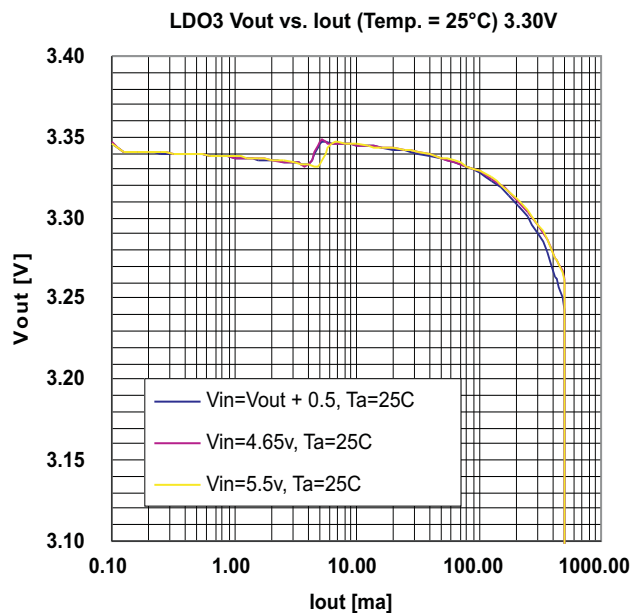


Figure 2-10.

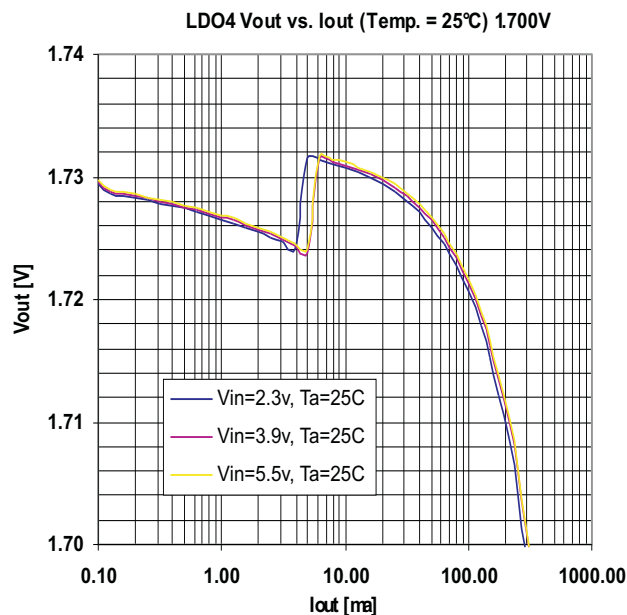


Figure 2-11.

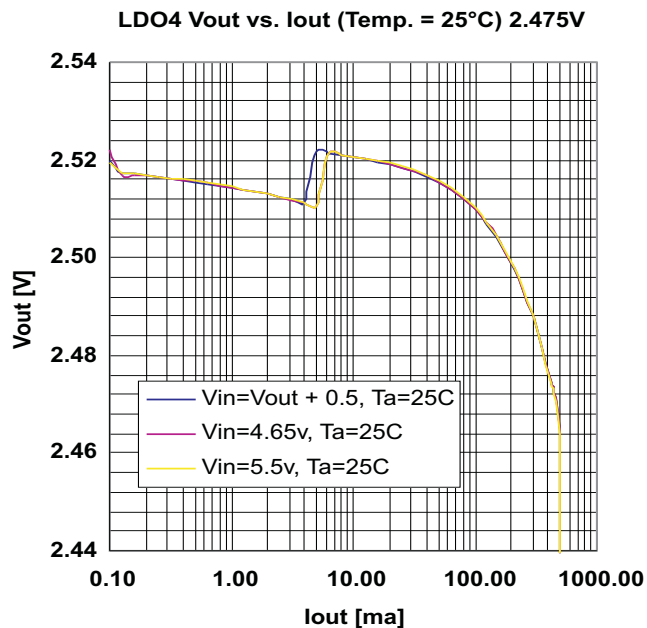


Figure 2-12.

(continued)

LDO5 Vout vs. Iout (Temp. = 25°C) 1.250V

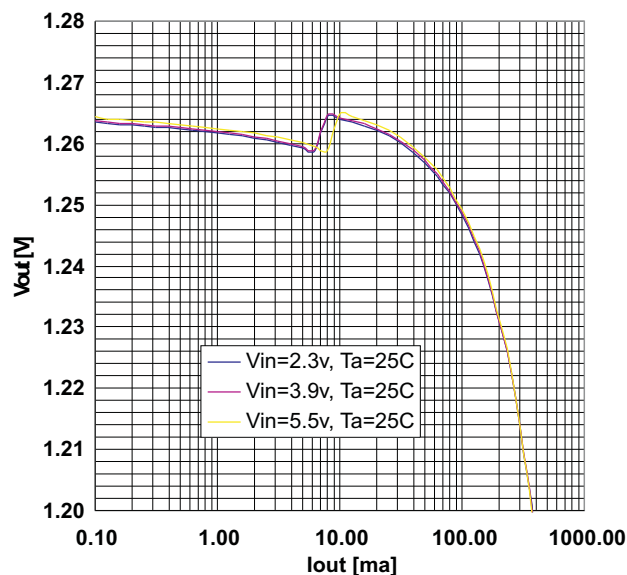


Figure 2-13.

LDO5 Vout vs. Iout (Temp. = 25°C) 3.30V

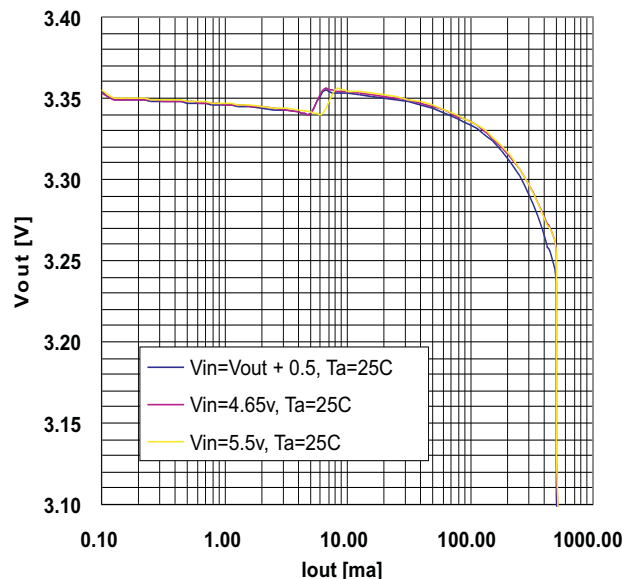


Figure 2-14.

LDO6 Vout vs. Iout (Temp. = 25°C) 1.250V

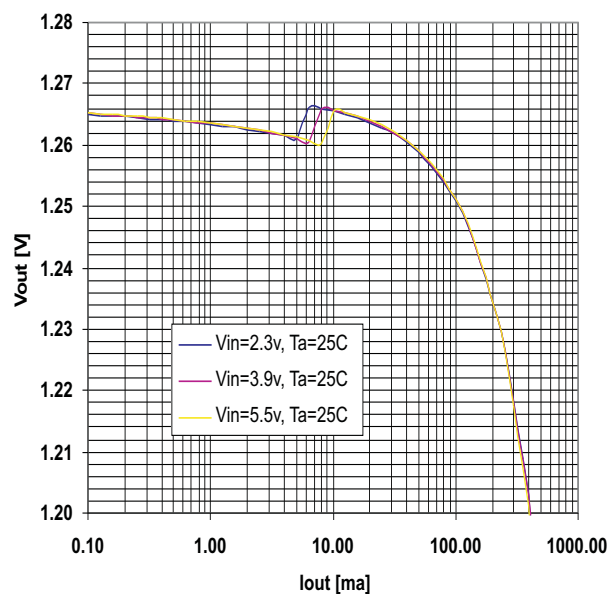


Figure 2-15.

LDO6 Vout vs. Iout (Temp. = 25°C) 3.30V

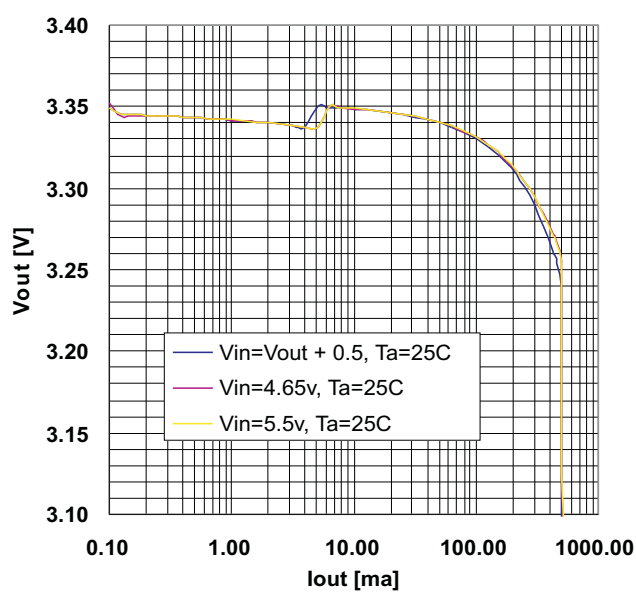


Figure 2-16.



(continued)

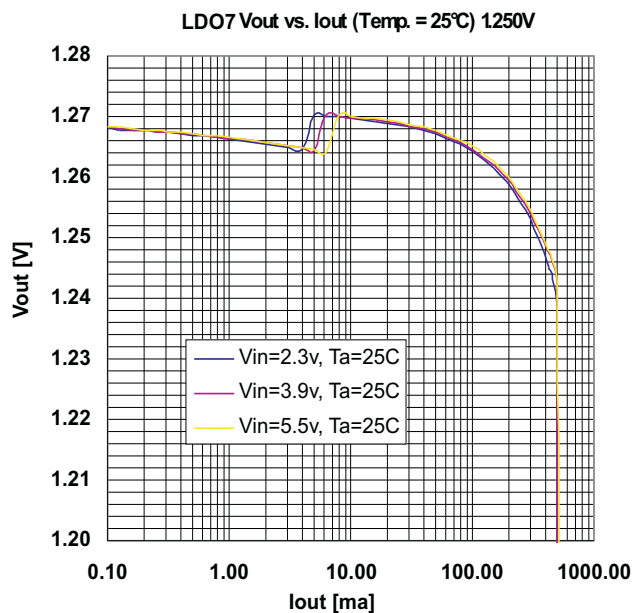


Figure 2-17.

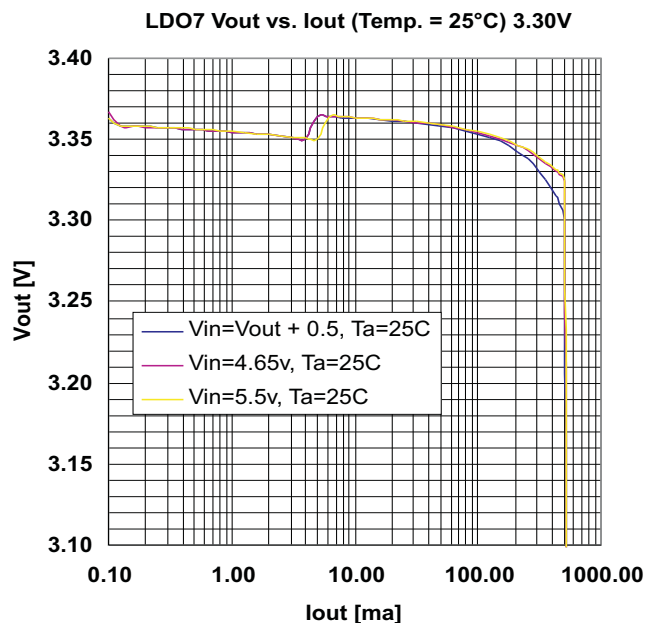


Figure 2-18.

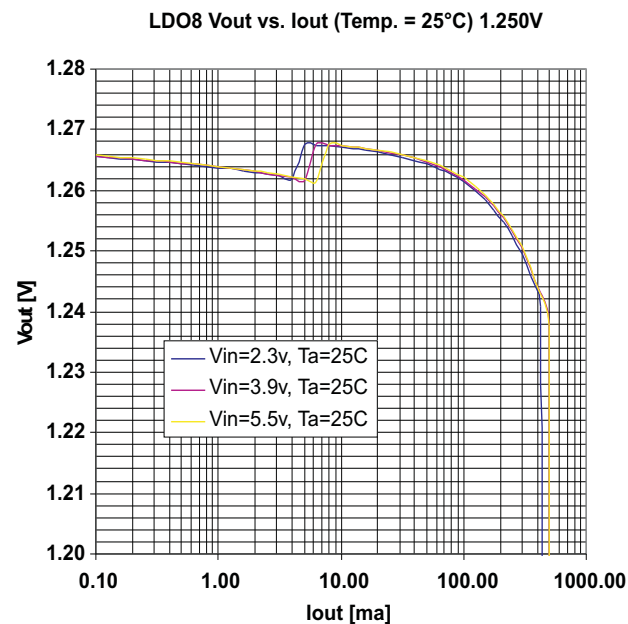


Figure 2-19.

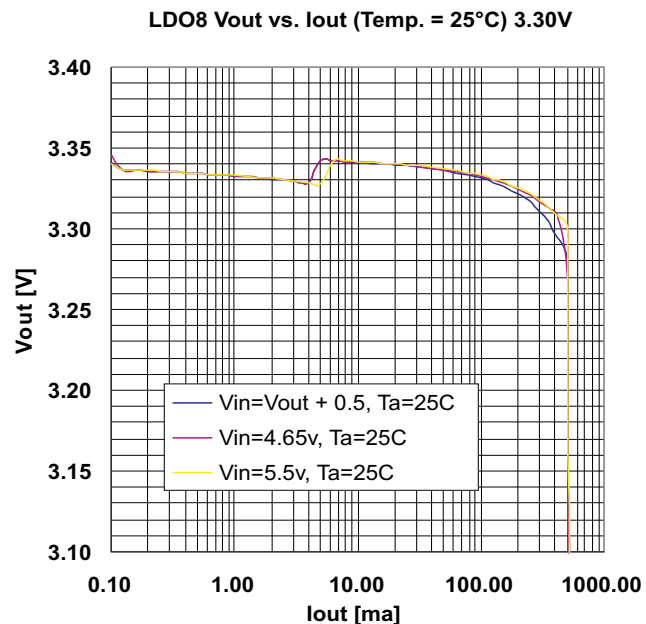


Figure 2-20.

(continued)

LDO2 0.725V DropOut at 25°C

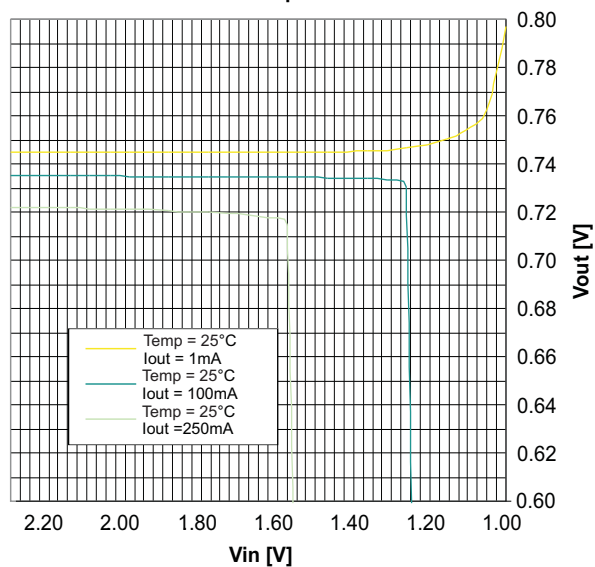


Figure 2-21.

LDO0 1.25V DropOut at 25°C

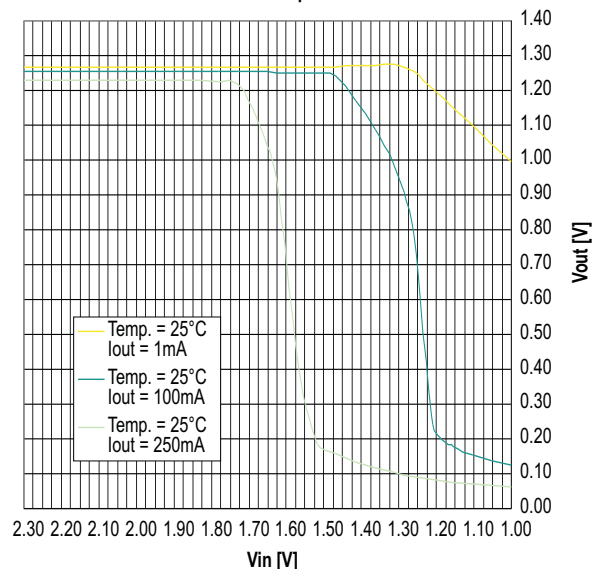


Figure 2-22.

LDO0 3.3V DropOut at 25°C

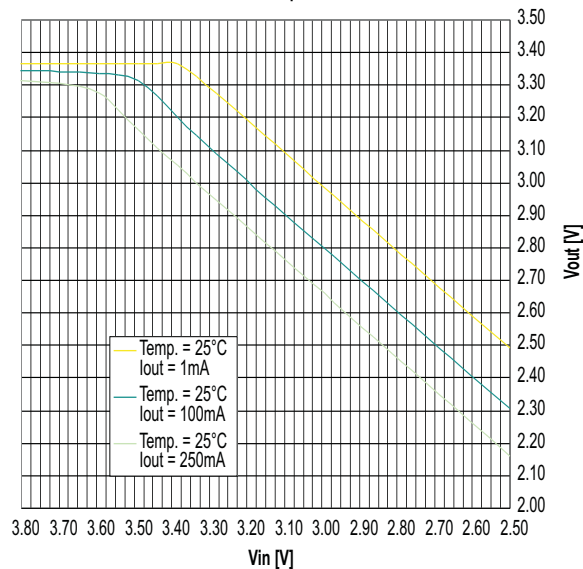


Figure 2-23.

Efficiency SMO Auto PFM Vout 1.8V at 25°C

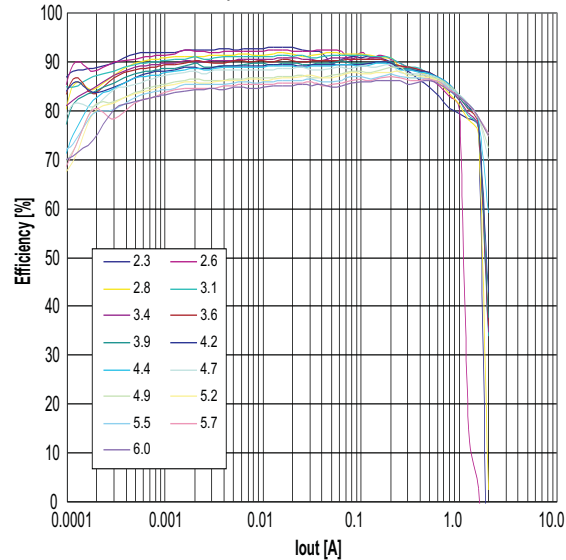


Figure 2-24.

(continued)

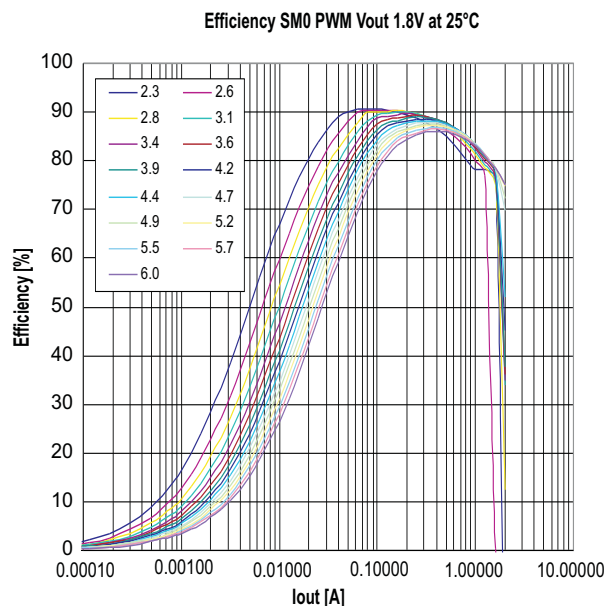


Figure 2-25.

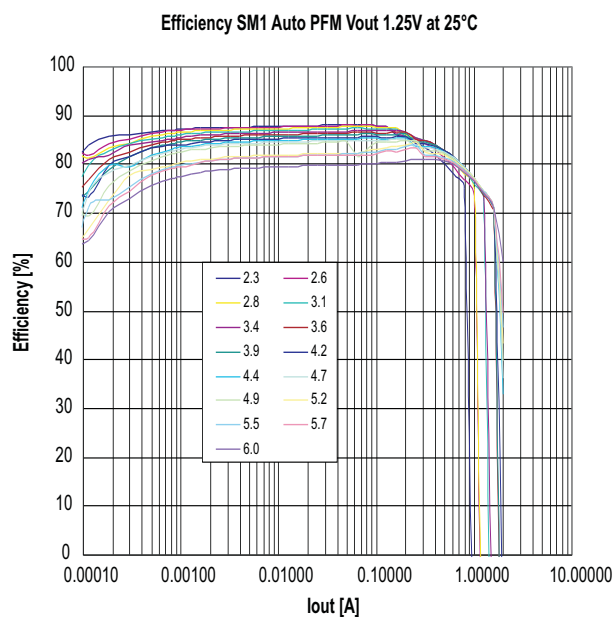


Figure 2-26.

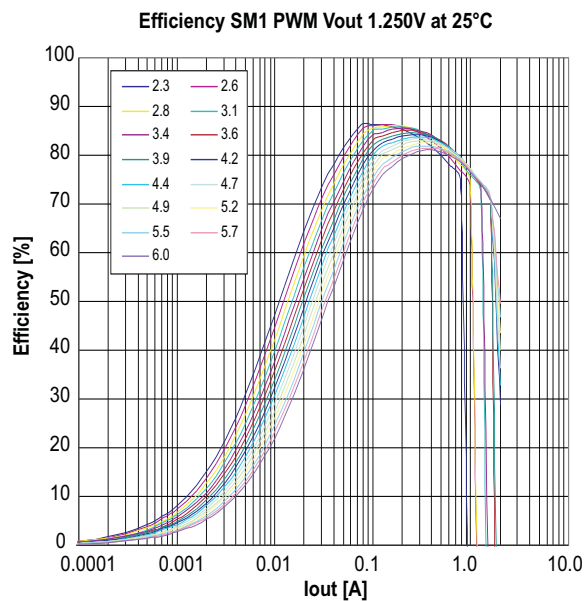


Figure 2-27.

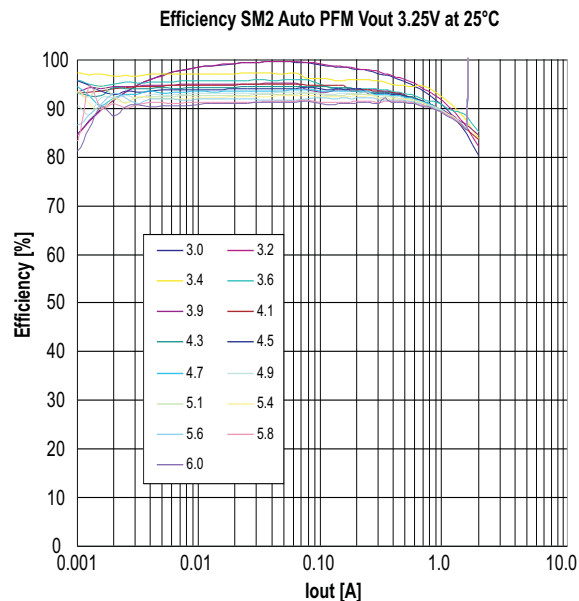


Figure 2-28.

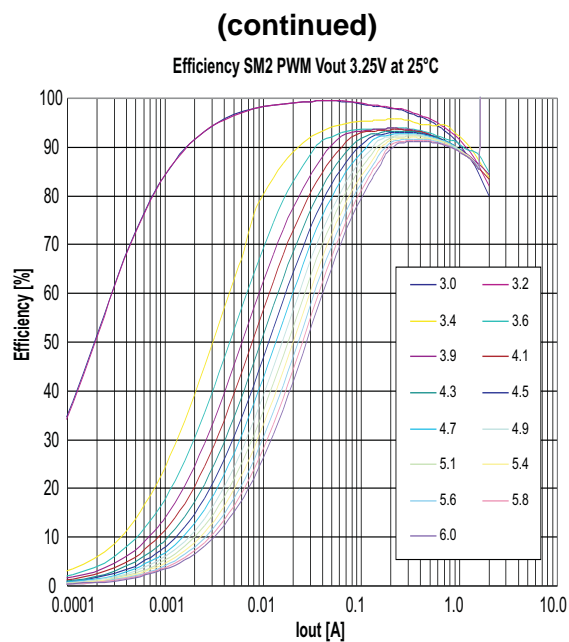


Figure 2-29.

### 3 DETAILED DESCRIPTION

#### 3.1 I<sup>2</sup>C INTERFACE

Two I<sup>2</sup>C configurations are implemented in the TPS658621A device:

**A –Standard I<sup>2</sup>C interface (SDAT/SCLK engine) :** A single I<sup>2</sup>C communication port provides a simple way for an I<sup>2</sup>C compatible host to access system status information, reset fault modes, and set supply output voltages. The I<sup>2</sup>C port functions as a SLAVE enabling I<sup>2</sup>C compatible hosts (MASTER) to perform WRITES and READS to/from internal registers. The I<sup>2</sup>C port is a 2-wire bidirectional interface using the SCLK (clock) and SDAT (data) pins. The I<sup>2</sup>C is designed to operate at SCLK frequencies up to 400 kHz. The standard 8 bit command is supported. The CMD part of the sequence is the 8 bit register address to read or write.

**B – Power I<sup>2</sup>C interface (PSDAT/PSCLK engine):** The TPS658621A supports processors that use a dedicated I<sup>2</sup>C bus to dynamically adjust critical supply voltages by adding a second I<sup>2</sup>C bus (Power I<sup>2</sup>C) connected to a second, dedicated I<sup>2</sup>C engine. The Power I<sup>2</sup>C port is a 2-wire bidirectional interface using the PSCLK (clock) and PSDAT (data) pins. The Power I<sup>2</sup>C is designed to operate at PSCLK frequencies up to 400 kHz. A multiple-byte data-register pair command protocol, not compatible with the standard I<sup>2</sup>C protocol, is supported by the Power I<sup>2</sup>C engine. The Power I<sup>2</sup>C engine does not support read operations.

---

#### NOTE

The Standard and Power I<sup>2</sup>C engines are always reset by the sequencer when the TPS658621A is in the POWER-UP state and when the SLEEP state is set.

---

#### 3.2 I<sup>2</sup>C ADDRESS

The TPS658621A will acknowledge (ACK) addresses 0x68 (writes) and 0x69 (reads) and will NACK any other address.

#### 3.3 DVM REGISTER ACCESS

The sequencer state machine disables write access to specific supply voltage setting registers when the TPS658621A is initially powered and when the integrated supplies are being sequenced. See the sequencer functional description for details.

#### 3.4 SCLK/SDAT AND PSCLK/PSDAT TIMEOUT

The TPS658621A monitors the SCLK/PSCLK clock lines, and it identifies a timeout condition if the clock line is held at a logic low for longer than 30ms. The I<sup>2</sup>C engine is NOT reset when the clock line timeout is identified.

The TPS658621A monitors the SDAT/PSDAT data lines. The I<sup>2</sup>C engine will be reset when the data line is held at a logic low for more than 30ms.

#### 3.5 I<sup>2</sup>C BUS RELEASE

The TPS658621A I<sup>2</sup>C engine does not create START or STOP states on the I<sup>2</sup>C bus during normal operation.

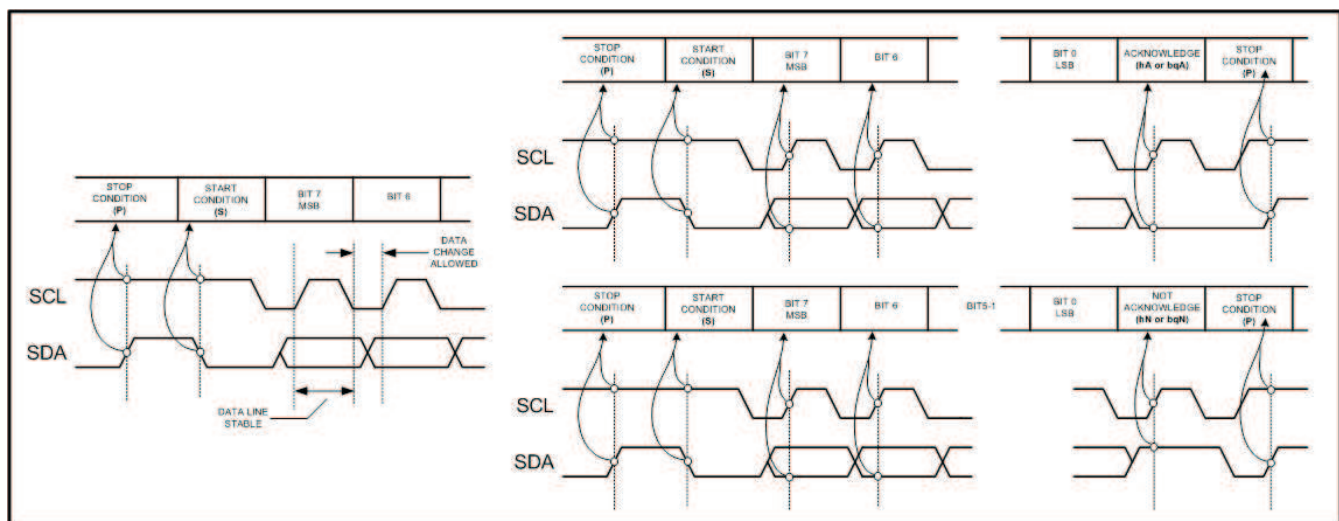
#### 3.6 I<sup>2</sup>C BUS ERROR RECOVERY

The I<sup>2</sup>C bus specification does not define a method to be used when recovering from a host side bus error. During a read operation the SDAT pin can be left in a LO state if the host has not sent enough SCLK pulses to complete a transaction (i.e. host side bus error). The TPS658621A will clear any SDAT LO condition if 10 SCLK pulses are sent by the host, enabling recovery from host side bus error events.

### 3.7 I<sup>2</sup>C COMMUNICATION PROTOCOL

The following conventions will be used when describing the communication protocol:

| CONDITION  | CODE   |
|--|--------|
| START sent from host   | S      |
| STOP sent from host  | P      |
| TPS658621A I <sup>2</sup> C slave address sent from host (WRITE) | hA0    |
| TPS658621A register address sent from TPS658621A (READ)          | hA1    |
| Non-valid I <sup>2</sup> C slave address sent from host          | hA_N   |
| Valid TPS658621A register address sent from host                 | HCMD   |
| Non-valid TPS658621A register address sent from host             | HCMD_N |
| I/O data byte (8 bits) sent from host to TPS658621A              | hDATA  |
| I/O data byte (8 bits) sent from TPS658621A to host              | bqDATA |
| Acknowledge (ACK) from host                                      | hA     |
| Not acknowledge (NACK) from host                                 | hN     |
| Acknowledge (ACK) from TPS658621A                                | bqA    |
| Not acknowledge (NACK) from TPS658621A                           | bqN    |



**Figure 3-1. I<sup>2</sup>C Conditions**

For normal data transfers, the data line (SDAT or PSDAT) is allowed to change only when the clock line (SCLK or PSCLK) is low, and one clock pulse is used per bit of data. The data line must remain stable whenever the clock line is high, as data changes when the clock is high are reserved for indicating the start and stop conditions. Each data transfer is initiated with a start condition and terminated with a stop condition.

When addressed, the TPS658621A device generates an acknowledge bit after the reception of each byte by pulling the data line Low. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. After the acknowledge/not acknowledge bit, the TPS658621A leaves the data line high, enabling a STOP condition generation.

### 3.8 I<sup>2</sup>C READ AND WRITE OPERATIONS

The TPS658621A supports the standard I<sup>2</sup>C one byte Write. The basic I<sup>2</sup>C read protocol has the following steps:

1. Host sends a start and sends TPS658621A address

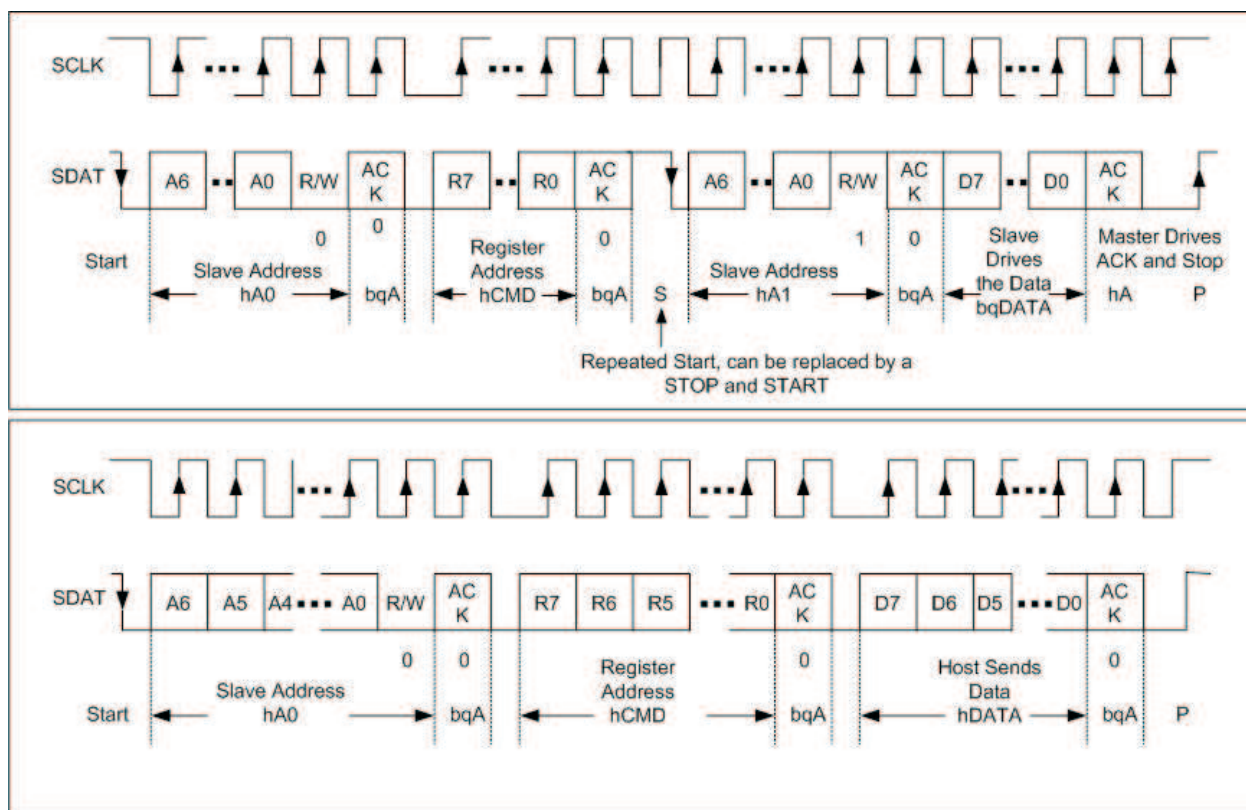
2. TPS658621A ACK's that this is a valid I<sup>2</sup>C address and that the bus is configured for write
3. Host sends TPS658621A register address
4. TPS658621A ACK's that this is a valid register and stores the register address to be read
5. Host sends a repeated start and TPS658621A I<sup>2</sup>C slave address, reconfiguring the bus for read
6. TPS658621A ACK's that this is a valid address and that bus is reconfigured
7. Bus is in read mode, TPS658621A starts sending data from selected register

The I<sup>2</sup>C write protocol is similar to the read, without the need for a repeated start and bus being set in write mode. In a WRITE, it is not necessary to end each 1 byte WRITE command with a STOP as a START will have the same effect (repeated start).

The host can complete a READ or a WRITE sequence with either a STOP or a START.

**NOTE**

Read operations are not supported for the PSDAT/PSCLK I<sup>2</sup>C engine.



**Figure 3-2. I<sup>2</sup>C Read/Write Example**

### 3.9 VALID WRITE SEQUENCES (SDAT/SCLK, PSDAT/PSCLK)

The TPS658621A will always ACK its own address. If CMD points to an allowable READ or WRITE address, the device writes the address into its RAM address register and sends an ACK. If CMD points to a non-allowed address, the device does NOT write the address into its RAM address register and sends a NACK.



|   |     |     |  |   |     |     |      |     |  |   |     |     |        |     |
|---|-----|-----|--|---|-----|-----|------|-----|--|---|-----|-----|--------|-----|
| S | hA0 | bqA |  | S | hA0 | bqA | hCMD | bqA |  | S | hA0 | bqA | hCMD_N | bqN |
|---|-----|-----|--|---|-----|-----|------|-----|--|---|-----|-----|--------|-----|

### 3.10 ONE BYTE WRITE (SDAT/SCLK, PSDAT/PSCLK)

The data is written to the addressed register at the end of the bq ACK, ending the one byte write sequence when the RAM address and the data byte are stored in the I<sup>2</sup>C registers. The host can cancel a WRITE by sending a STOP or START before the trailing edge of the ACK clock pulse.

|   |     |     |      |     |       |     |
|---|-----|-----|------|-----|-------|-----|
| S | hA0 | bqA | hCMD | bqA | hDATA | bqA |
|---|-----|-----|------|-----|-------|-----|

### 3.11 VALID READ SEQUENCES (SDAT/SCLK ONLY)

The TPS658621A will always ACK its own address.

|   |     |     |
|---|-----|-----|
| S | hA1 | bqA |
|---|-----|-----|

Upon receiving hA1, TPS658621A starts at the current location of the RAM address register. The START and the STOP both act as priority interrupts. If the host has been interrupted and is not sure where it left off, it can send a STOP and reset the TPS658621A state machine to the WAIT state; once in the WAIT state, the TPS658621A will ignore all activity on the SCLK and SDAT lines until it receives a START. A repeated START and START in the I<sup>2</sup>C specification are both treated as a START.

|   |     |     |      |     |   |
|---|-----|-----|------|-----|---|
| S | hA0 | bqA | hCMD | bqA | P |
|---|-----|-----|------|-----|---|

|   |     |     |      |     |   |     |     |        |    |   |
|---|-----|-----|------|-----|---|-----|-----|--------|----|---|
| S | hA0 | bqA | hCMD | bqA | S | hA1 | bqA | bqDATA | hN | P |
|---|-----|-----|------|-----|---|-----|-----|--------|----|---|

### 3.12 VALID READ SEQUENCES (SDAT/SCLK ONLY)

|   |     |     |        |    |   |
|---|-----|-----|--------|----|---|
| S | hA1 | bqA | bqDATA | hN | P |
|---|-----|-----|--------|----|---|

#### Incremental read sequences

|   |     |     |        |    |        |    |     |        |    |   |
|---|-----|-----|--------|----|--------|----|-----|--------|----|---|
| S | hA1 | bqA | bqData | hA | bqDATA | hA | ... | bqDATA | hN | P |
|---|-----|-----|--------|----|--------|----|-----|--------|----|---|

### 3.13 NON-VALID SEQUENCES

START and non-hA0 or non-hA1 Address: A START followed by an address which is not hA0 or hA1 will be NACKED.

|   |      |     |
|---|------|-----|
| S | hA_1 | bqN |
|---|------|-----|

#### Attempt to Specify Non-Allowed READ Address

If the CMD points to a non-allowed READ address (reserved registers), bq will send a NACK back to the host and it will not load the address in the RAM address register. Note that the TPS658621A NACKS whether a stop is sent or not.

|   |     |     |        |     |   |  |   |     |     |        |     |
|---|-----|-----|--------|-----|---|--|---|-----|-----|--------|-----|
| S | hA0 | bqA | hCMD_N | bqA | P |  | S | hA0 | bqA | hCMD_N | bqN |
|---|-----|-----|--------|-----|---|--|---|-----|-----|--------|-----|



### Attempt to Specify Non-Allowed WRITE Address

If the host attempts to WRITE to a READ-ONLY or non-accessible address, the TPS658621A ACKS the CMD containing the allowed READ address, loads the address into the address register and ACKS after the host sends the next data byte. A subsequent hA1 READ could read this address, but the data sent by the host will not have been written.

|   |     |     |      |     |       |     |
|---|-----|-----|------|-----|-------|-----|
| S | hA0 | bqA | hCMD | bqA | hDATA | bqA |
|---|-----|-----|------|-----|-------|-----|

### 3.14 INCREMENTAL READ (SDAT/SCLK ONLY)

The SDAT/SCLK I<sup>2</sup>C interface supports incremental read operations. Each register must be accessed in a single read operation. A valid WRITE address is required to write to the RAM, and a valid READ address is required to specify the initial RAM address where the READ starts. Once a read command is received, the RAM data for the specified address is output to the host. If the host chooses, it can loop through the remaining addresses; the address is automatically incremented by one at the end of each read. If the loop gets to the top address, it automatically rolls over to address 0x00 and the sequence stops.

### 3.15 I<sup>2</sup>C COMMUNICATION PROTOCOL – POWER I<sup>2</sup>C INTERFACE, PINS PSDAT/PSCLK

The Power I<sup>2</sup>C interface is designed to support fast write operations using multiple register-data pair sequences. The Power I<sup>2</sup>C engine is a write-only engine, and it does not support read operations.

During a write sequence, the host sends the start command, followed by the TPS658621A address. Then the host sends the register address byte, followed by eight bits of the data for the respective register (Register1 Address/Data in Figure 3-3). From this point on the TPS658621A will accept all the following 2 byte pairs as a random register address, followed by the data content to be written to that register. This process continues until the host sends a valid stop condition after the last register (Register N in Figure 3-3) is written. A typical multi-byte sequence is shown in Figure 3-3.

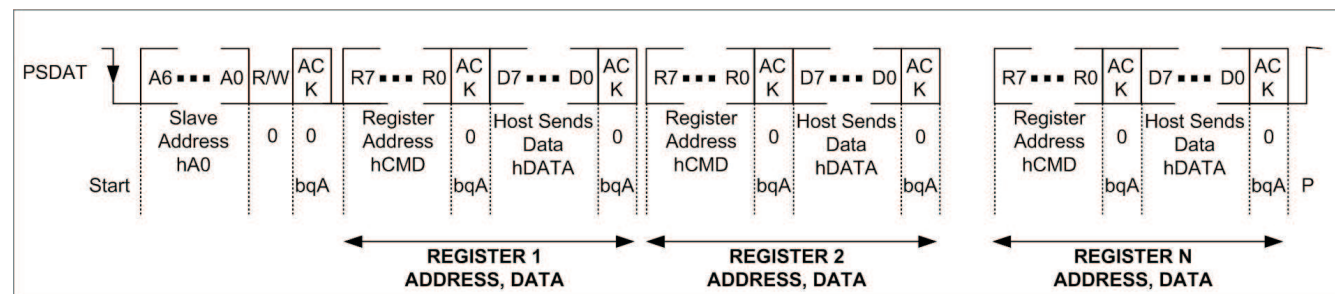


Figure 3-3. Power I<sup>2</sup>C Protocol

### 3.16 SIMULTANEOUS STANDARD AND POWER I<sup>2</sup>C OPERATION

The TPS658621A has individual address pointers for the Power I<sup>2</sup>C engine and Standard I<sup>2</sup>C engine. The value written to the register will be defined by the relative timing between read/write pulses when simultaneous I<sup>2</sup>C read/write operations happen. Simultaneous write/read operations to the same register will be handled as follows:

- Both Standard I<sup>2</sup>C and Power I<sup>2</sup>C are executing operations accessing distinct registers at the same time (simultaneous read/read, read/write, write/read or write/write): No conflict exists in this case.
- Power I<sup>2</sup>C writes and Standard I<sup>2</sup>C reads the same register at the same time
  - Standard I<sup>2</sup>C will read the old register value if the Standard I<sup>2</sup>C read pulse is generated at least 110nsec (typ) before the Power I<sup>2</sup>C write pulse happens.
  - Standard I<sup>2</sup>C will read the new register value if the Standard I<sup>2</sup>C read pulse is generated at least 110nsec (typ) after the Power I<sup>2</sup>C write pulse happens.
- Power I<sup>2</sup>C and Standard I<sup>2</sup>C write to the same register at the same time

- (a) If both write operations are more than 110nsec (typ) apart, the register final value will be set by the engine that executes the last write operation.
- (b) a. If both write operations are less than 110nsec (typ) apart, the priority will be given to the Power I<sup>2</sup>C engine. The value from the Power I<sup>2</sup>C engine will be written into the register, and the data received by the Standard I<sup>2</sup>C operation is not written to the TPS658621A internal memory.

**THERE IS NO CLOCK STRETCH FUNCTION IN EITHER SCLK OR PSCLK WHEN A CONFLICT SITUATION HAPPENS. THE CONFLICT IS HANDLED INTERNALLY BY GIVING PRIORITY TO PSDAT/PSCLK ENGINE.**

## 3.17 POWER PATH

### 3.17.1 RAM Control Bits

The power path circuit connects one of the power sources plugged into the AC, USB or BAT pins to the SYS pin. The supply selection is made based on system parameters monitored by the power path circuit and internal RAM control bits in register 0x4C.

**Table 3-1. Power Path Control**

| PPATH1 [Addr 0x4C] |                    |                 |                 | Defaults in BOLD     |                                    |                                 |                         |                          |
|--------------------|--------------------|-----------------|-----------------|----------------------|------------------------------------|---------------------------------|-------------------------|--------------------------|
| Bit Number         | B7                 | B6              | B5              | B4                   | B3                                 | B2                              | B1                      | B0                       |
| Bit Name           | USBSUSP            | USBDCH          | ACDCH           | RSVD4B4              | BOOTOFF                            | USBLIMIT                        | USBMODE                 | PWRSYS                   |
| Function           | USB SUSPEND MODE   | SPARE           | SPARE           | CHARGE VOLTAGE RANGE | USB INPUT ILIMIT at BOOT PHASE     | USB INPUT CURRENT LIMIT SETTING | USB INPUT CURRENT LIMIT | AUTO SYS POWER SELECTION |
| When 0             | <b>SUSPEND OFF</b> | NOT USED        | NOT USED        | <b>3.95V-4.2V</b>    | SET BY USBLIMIT ONLY               | <b>100mA</b>                    | <b>SET BY USBLIMIT</b>  | BAT TO SYS               |
| When 1             | SUSPEND ON         | <b>NOT USED</b> | <b>NOT USED</b> | 4.3V-4.45V           | <b>SET BY USBMODE AND USBLIMIT</b> | 500mA                           | 2.25 A                  | <b>AUTO MODE ENABLED</b> |

The input power priority is hard-wired internally, with the AC input having the higher priority, followed by the USB input (2nd) and the battery pack (3rd). The SYS pin voltage is **not** regulated and it will be equal to the input voltage (AC, USB or BAT value) minus the voltage drop across the switch that is ON when the selected input current limit is not active.

Setting the control bit PWRSYS (bit 0) to **0**, the user can override the power path priority, connecting the battery to the SYS pin even if AC or USB are detected. When PWRSYS is **0** and the battery is removed, the SYS pin **will not** be connected back to the AC or USB inputs and thereby will discharge to ground.

The USB power will be ignored when USBSUSP (bit 7) is **1**, connecting only the AC or BAT power sources to the SYS pin. If neither AC nor BAT is connected the SYS pin, it will discharge to ground.

The USB input current is limited to the maximum value programmed by the host via the I<sup>2</sup>C interface by setting bits USBLIMIT (bit 2) and USBMODE (bit 1) as shown in [Table 3-2](#).

**Table 3-2. Power Path Current Limit**

| USBMODE | USBLIMIT | USB INPUT CURRENT LIMIT | AC INPUT CURRENT LIMIT |
|---------|----------|-------------------------|------------------------|
| 0       | 0        | 100 mA max              | 2.2 A min              |
| 0       | 1        | 500 mA max              |                        |
| 1       | X        | 2.1A min                |                        |

If the system current requirements exceed the input current limit, the SYS pin voltage will be reduced until the power path is set in supplement mode (if pack is connected).

### 3.18 SYSTEM STATUS DETECTION

The TPS658621A has integrated comparators that monitor the BAT, AC, USB and SYS pin voltages. The data generated by the comparators is used by the power path control logic to define which of the integrated power path switches will be active. Table 3-3 lists the system power detection conditions:

Table 3-3. Power Path Detection Functions

| SYSTEM STATUS                         | DETECTION CONDITIONS <sup>(1)</sup>                        |
|---------------------------------------|--|
| AC input voltage detected             | $V_{IN(OVP)} > V(AC) > V(BAT) + V_{IN(DT)}$                |
| USB input voltage detected            | $V_{IN(OVP)} > V(USB) > V(BAT) + V_{IN(DT)}$               |
| AC over-voltage detected              | $V(AC) > V_{IN(OVP)}$                                      |
| USB over-voltage detected             | $V(USB) > V_{IN(OVP)}$                                     |
| SYS pin short detected                | $V(SYS) < V_{SH(SYS)}$                                     |
| Battery switch over-current detection | $I(BAT) > I_{BATSYS}$                                      |
| Supplement mode detection             | $V(SYS) < V(BAT) - V_{SUP(SYS)}$ AND $I(BAT) < I_{BATSYS}$ |

(1)  $V_{IN(DT)}$ ,  $V_{SH(SYS)}$ ,  $V_{BATSH}$ ,  $V_{IN(OVP)}$ ,  $V_{SUP(SYS)}$  are TPS658621A internal references, refer to the electrical characteristics for additional details

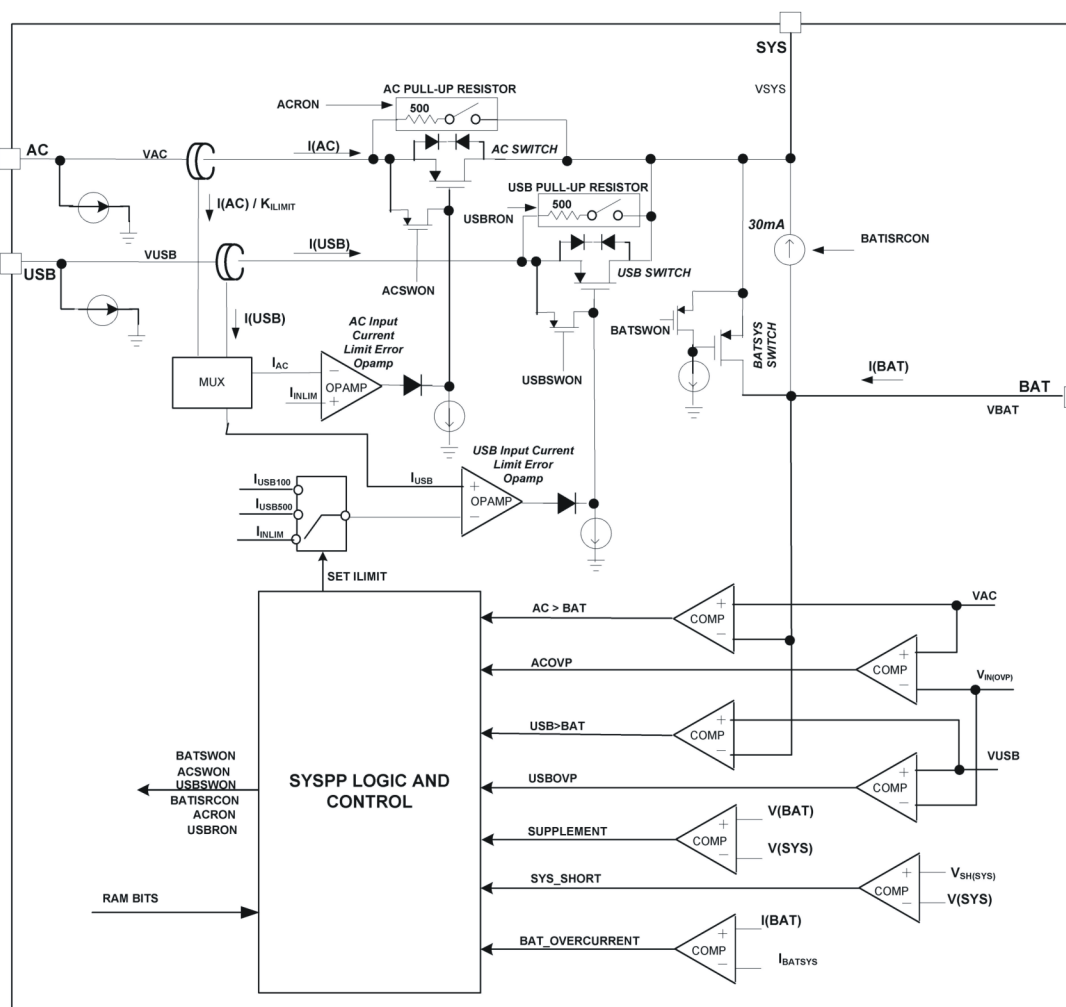


Figure 3-4. Simplified Power Path Block

The I<sup>2</sup>C control bits and system status are used by the power path control logic to define the state of the power path switches as shown below; a fault condition will be detected when the SYS pin is shorted or a battery switch over-current condition is detected.

**Table 3-4. Power Path Control**

| 6586x MODE | PWRSYS | USBSUSP | AC DETECTED | USB DETECTED | FAULT DETECTED | AC SWITCH | USB SWITCH | BATTERY SWITCH                                   | SYS PIN CONNECTED TO |
|------------|--------|---------|-------------|--------------|----------------|-----------|------------|--|----------------------|
| UVLO       | X      | X       | X           | X            | X              | OFF       | OFF        | OFF  | NONE                 |
| NOT UVLO   | X      | X       | X           | X            | YES            | OFF       | OFF        | OFF  | PULL-UP RES/ISRC     |
| NOT UVLO   | 1      | X       | YES         | X            | NO             | ON        | OFF        | ON if Supplement mode is required, OFF otherwise | AC                   |
| NOT UVLO   |        | 0       | NO          | YES          | NO             | OFF       | ON         |  | USB                  |
| NOT UVLO   |        | 1       | NO          | YES          | NO             | OFF       | OFF        | ON   | BATTERY              |
| NOT UVLO   |        | X       | NO          | NO           | NO             | OFF       | OFF        | ON   | BATTERY              |
| NOT UVLO   | 0      | X       | X           | X            | NO             | OFF       | OFF        | ON   | BATTERY              |

When a fault condition is detected, the fault recovery method (resistor or current source) is defined by the input power supply detection:

**Table 3-5. Power Path Fault Recovery Control**

| AC DETECTED | USB DETECTED | RECOVERY METHOD         |
|-------------|--------------|-------------------------|
| YES         | X            | AC PULL-UP RESISTOR ON  |
| NO          | YES          | USB PULL-UP RESISTOR ON |
| NO          | NO           | 30mA CURRENT SOURCE ON  |

### 3.19 POWER PATH STATUS

The power path status is available at register 0xB9, bits BATSYSON, ACSWON, USBSWON, and register 0xBB, bits LOWSYS, ACDDET, USBDET, AC\_OVP and USB\_OVP. See the STATUS REGISTER section for bit function description.

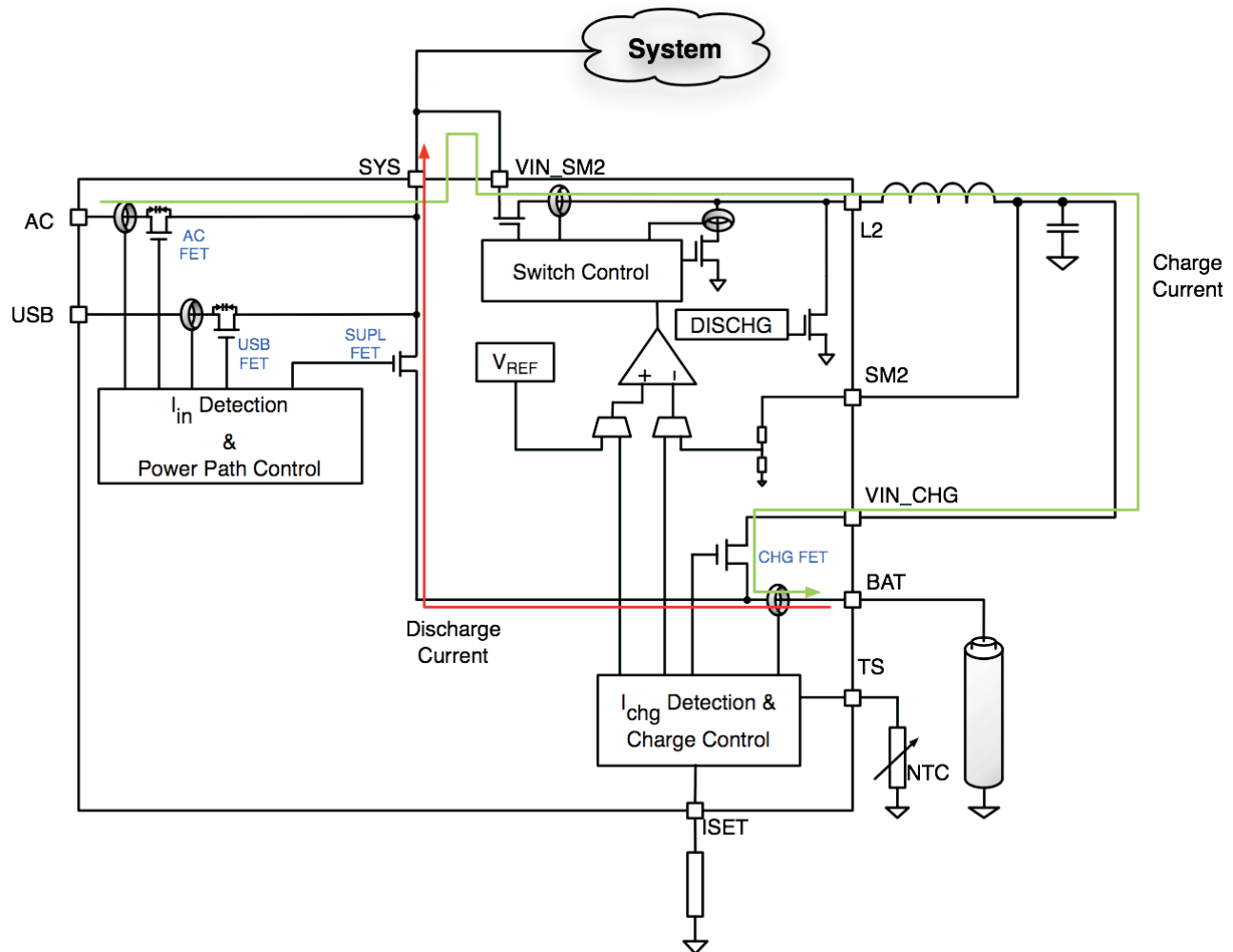
### 3.20 BATTERY CHARGER

The TPS658621A has an integrated linear charger that is designed to enable the implementation of two distinct configurations. The TPS658621A has been configured such that the Charger input power is supplied by the SM2 output. In this mode, the SM2 acts as a pre-regulator to the charger input. The Charger is active when the device is in the SLEEP state.

**Charger input power supplied by power path output :** The SM2 voltage is set to the voltage programmed by the host via register SUPPLYV2 control bits VSM2[4:0] at all times. The charger input pin VIN\_CHG must be connected to the power path output SYS pin. This topology has lower efficiency when compared to the pre-regulator configuration, but it enables the use of SM2 as a stand alone converter in systems where lower charge rates are required.



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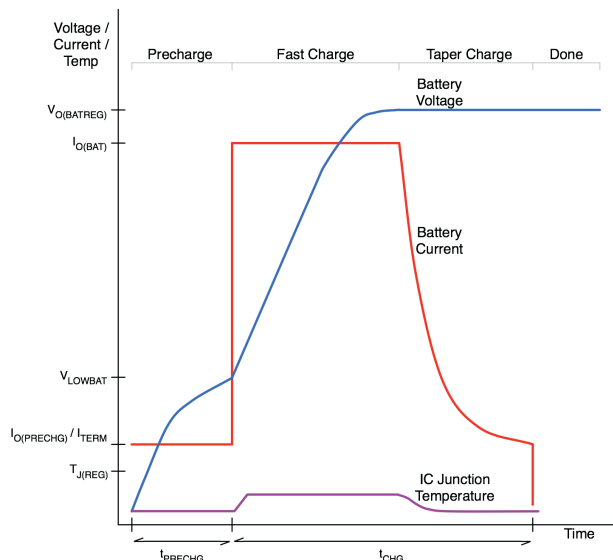
**Figure 3-6. Linear Charger Configured with SM2 as Pre-Regulator**

### 3.21 OPERATING MODES

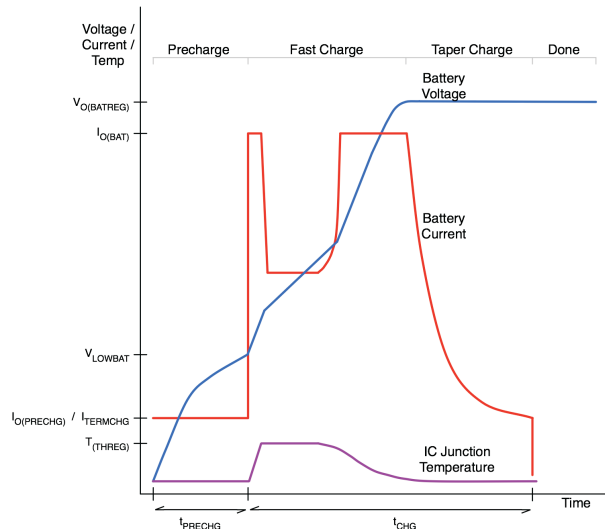
The TPS658621A supports charging of single-cell Li-Ion or Li-Pol battery packs. The charge process is executed in three phases: pre-charge (or pre-conditioning), constant current and constant voltage. Protection circuits reduce the charge current when the IC junction temperature exceeds 125°C (typ, thermal loop), or when the SYS pin voltage drops below a user-selectable threshold (DPPM loop).

When the charger is enabled, the control loops limit the BAT pin current to the programmed charge current value (charge current loop) or regulates the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If  $V(\text{BAT}) < V_{\text{LOWBAT}}$ , the BAT pin current is internally set to the programmed pre-charge current value. A typical charge profile is shown below, for an operation condition when the thermal and DPPM loops are not active.

If the operating conditions cause the IC junction temperature to exceed 125°C or the SYS pin voltage collapses, the charge cycle is modified, with the activation of additional control loops. The DPPM and thermal loops will override the other charger control loops and reduce the charge current. A modified charge cycle, with the thermal or DPPM loop active, is shown in [Figure 3-7](#) and [Figure 3-8](#).



**Figure 3-7. Charge Phases Without Thermal Foldback**



**Figure 3-8. Charge Phases With Thermal Foldback**

## 3.22 DETECTING THE SYSTEM STATUS

The TPS658621A has integrated comparators that monitor the voltages at the BAT, TS, and VIN\_CHG pins, as well as the charge current. The data generated by those comparators is used by the control logic to detect fault conditions and control SM2 operation. Table 3-6 lists the system power detection conditions.  $V_{SH(VIN\_CHG)}$ ,  $V_{LOWBAT}$ , and  $V_{SH(BAT)}$  are TPS658621A internal references (refer to the electrical characteristics for additional details).

**Table 3-6. System Status Detection Conditions**

| STATUS                                     | DETECTION REQUIREMENTS           |
|--|----------------------------------|
| VIN_CHG pin short detected                 | $V(VIN\_CHG) < V_{SH(VIN\_CHG)}$ |
| Battery voltage below pre-charge threshold | $V(BAT) < V_{LOWBAT}$            |
| Battery short detected                     | $V(BAT) < V_{SH(BAT)}$           |

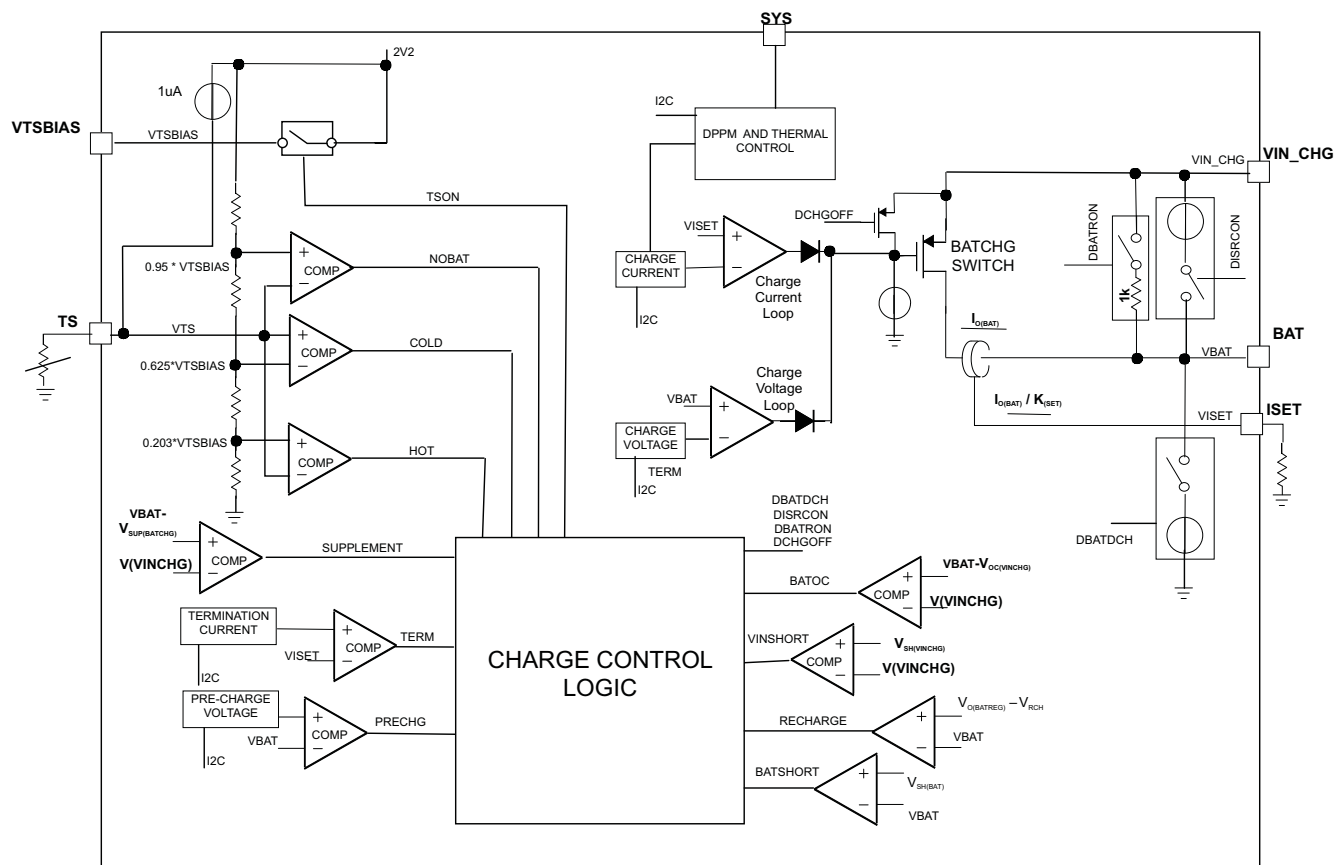


Figure 3-9. Simplified Charger Block Diagram



### 3.23 CHARGER RAM REGISTERS

The charger has control bits that enable user configuration of multiple charger parameters, as shown below:

**Table 3-7. Charger Control**

| CHG1 [Addr 0x49] |  |                                      |                          |                          |  |          |                                  | Defaults in <b>BOLD</b>       |
|------------------|--|--------------------------------------|--------------------------|--------------------------|--|----------|----------------------------------|-------------------------------|
| Bit Number       | B7   | B6                                   | B5                       | B4                       | B3   | B2       | B1                               | B0                            |
| Bit Name         | CHGTMR[1]                                      | CHTMR[0]                             | BATDCH                   | TSON                     | ISSET[1]                                   | ISSET[0] | TERMOFF                          | CHSUSP                        |
| Function         | CHARGE SAFETY TIMER VALUE                      |                                      | BATTERY DISCHARGE SWITCH | THERMISTOR BIAS CONTROL  | CHARGE CURRENT SCALING FACTOR              |          | CHARGE TERMINATION STATE         | SUSPEND CHARGE                |
| When 0           | 00 = 4 Hrs 01 = 5 Hrs<br>10 = 6 Hrs 11 = 8 Hrs |                                      | OFF                      | OFF                      | 00 = 0.25 10 = 0.75<br>01 = 0.50 11 = 1.00 |          | TERM ON                          | NOT SUSPENDED                 |
| When 1           |  |                                      | ENABLED                  | ON                       |  |          | TERM OFF                         | SUSPENDED                     |
| CHG2 [Addr 0x4A] |  |                                      |                          |                          |  |          | Defaults in <b>BOLD</b>          |                               |
| Bit Number       | B7   | B6                                   | B5                       | B4                       | B3   | B2       | B1                               | B0                            |
| Bit Name         | DTCN   | VPCHG                                | TSBYP                    | CHTMREN                  | VCHG[1]                                    | VCHG[0]  | CHGON[1]                         | CHBOOT                        |
| Function         | DYNAMIC TIMER FUNCTION                         | PRE-CHARGE VOLTAGE                   | ENABLE CHARGER LDO MODE  | CHARGE SAFETY TIMER      | CHARGE VOLTAGE SELECTION                   |          | CHARGER ON/OFF                   | CHARGER OPERATION DURING BOOT |
| When 0           | OFF  | 2.5V                                 | OFF                      | OFF                      | SEE VCHG SETTING TABLE                     |          | SEE CHARGE ENABLE TABLE          | OFF                           |
| When 1           | ON   | 2.9V                                 | ON                       | ON                       | SEE VCHG SETTING TABLE                     |          |                                  | ON                            |
| CHG3 [Addr 0x4B] |  |                                      |                          |                          |  |          |                                  | Defaults in <b>BOLD</b>       |
| Bit Number       | B7   | B6                                   | B5                       | B4                       | B3   | B2       | B1                               | B0                            |
| Bit Name         | CHGON[0]                                       | SYSDPPM[1]                           | SYSDPPM[0]               | TPCHG                    | ITERM[1]                                   | ITERM[0] | IPCHG[1]                         | IPCHG[0]                      |
| Function         | CHARGER ON/OFF                                 | SYSTEM POWER PATH DPPM THRESHOLD     |                          | PRE-CHARGE TIMER SCALING | TERMINATION CURRENT FACTOR                 |          | PRE-CHARGE CURRENT FACTOR        |                               |
| When 0           | SEE CHARGE ENABLE TABLE                        | 00=3.5V 01=3.75V<br>10=4.0V 11=4.25V |                          | 30 MIN                   | 00=0.04 01=0.10<br>10=0.15 11=0.20         |          | 00=0.04 01=0.1<br>10=0.15 11=0.2 |                               |
| When 1           |  |                                      |                          | 60 MIN                   |  |          |                                  |                               |

**Table 3-8. VCHG Settings**

| RSVD4B4 <sup>(1)</sup> | VCHG[1] | VCHG[0] | CHARGER REGULATION VOLTAGE <sup>(1)</sup> |
|------------------------|---------|---------|---|
| 0                      | 0       | 0       | 4.10                                      |
| 0                      | 0       | 1       | 4.15                                      |
| 0                      | 1       | 0       | 4.20                                      |
| 0                      | 1       | 1       | 3.95                                      |
| 1                      | 0       | 0       | 4.30                                      |
| 1                      | 0       | 1       | 4.35                                      |
| 1                      | 1       | 0       | 4.40                                      |
| 1                      | 1       | 1       | 4.45                                      |

(1) The charge voltage range is set by bit RSVD4B4, located on register PPATH1, 0x4C (bit B4)

**Table 3-9. Charge Enable Control**

| SM2 | CHGON[1] | CHGON[0] | CHARGER MODE IN SLEEP | CHARGER MODE IN NORMAL |
|-----|----------|----------|-----------------------|------------------------|
| OFF | X        | X        | OFF                   | OFF                    |
| ON  | 0        | 0        | OFF                   | OFF                    |
| ON  | 0        | 1        | OFF                   | OFF                    |
| ON  | 1        | 0        | ON                    | OFF                    |

**Table 3-9. Charge Enable Control (continued)**

| SM2 | CHGON[1] | CHGON[0] | CHARGER MODE<br>IN SLEEP | CHARGER MODE<br>IN NORMAL |
|-----|----------|----------|--------------------------|---------------------------|
| ON  | 1        | 1        | ON                       | ON                        |

### 3.24 SUPPLEMENT MODE DETECTION

The TPS658621A charger does not have a supplement mode. The charger power mosfet will NOT turn on when the charger is disabled and  $V(\text{VIN\_CHG}) < V(\text{BAT})$ .

### 3.25 SHORT CIRCUIT DETECTION

The BAT pin is monitored for a short circuit condition. If  $V(\text{BAT}) < V_{\text{SH}(\text{BAT})}$ , the BATCHG switch is turned OFF and an internal resistor is connected from VIN\_CHG pin to BAT pin.

### 3.26 DPPM FUNCTION

Internal circuits monitor the voltage at the SYS pin and reduce the charge current when  $V(\text{SYS}) < V_{\text{SYS}(\text{DPPM})}$ . This function assures that the external power is used to run the system. The threshold  $V_{\text{SYS}(\text{DPPM})}$  can be programmed using the I<sup>2</sup>C bits SYSDPPM<1:0> in register CHG3.

### 3.27 BATTERY DETECTION, TEMPERATURE QUALIFICATION

Battery pack insertion and battery pack temperature are detected by three comparators that monitor the thermistor voltage. The thermistor supply is enabled via I<sup>2</sup>C when control bit TSON=HI in register CHG1. This control bit enables the host software to turn on the thermistor bias when the charger is off and the pack temperature needs to be measured via the ADC, minimizing system quiescent current when operating under battery power. When the charger is activated, the thermistor power is enabled independent of the state of bit TSON.

The host software must disable the charger by setting bit CHGON(1)=0 when the battery pack removal is detected by the TPS658621A. This procedure is required in order to avoid undesired transients when a battery pack is hot-plugged in the system.

### 3.28 BATTERY PRE-CONDITIONING

The TPS658621A applies a pre-charge current  $I_{\text{O}(\text{PRECHG})}$  to the battery if the battery voltage is below the  $V_{\text{LOWBAT}}$  threshold, pre-conditioning deeply discharged cells. The resistor,  $R_{\text{ISET}}$ , connected between the ISET and AGND pins, determines the pre-charge rate. The pre-charge rate programmed by  $R_{\text{ISET}}$  is always applied to a deeply discharged battery pack, independent of the input power selection (AC or USB). The pre-charge current can be calculated as shown in [Equation 1](#):

$$I_{\text{O}(\text{PRECHG})} = \frac{K_{\text{PRECHG}}}{R_{\text{ISET}}} \quad (1)$$

where  $K_{\text{PRECHG}}$  is the pre-charge current scaling factor in AΩ.

The pre-charge current is set by the resistor on the ISET pin and can be scaled via I<sup>2</sup>C register CHG3 bits IPCH\_1, IPCH\_0 to a percentage (20%, 15%, 10%, or 4%) of the value set by  $R_{\text{ISET}}$ . The pre-charge voltage is selectable via bit VPCHG, register CHG2.

### 3.29 CONSTANT CURRENT CHARGING

The constant charge current mode (fast charge) is set when the battery voltage is higher than the pre-charge voltage threshold. The fast charge current regulation point is defined by the external resistor,  $R_{\text{ISET}}$ , connected to the ISET pin as shown in [Equation 2](#).

$$I_{O(BAT)} = \frac{K_{SET}}{R_{ISET}} \quad (2)$$

where  $K_{SET}$  is the charge current scaling factor in  $A\Omega$ .

The charge current is set by the resistor on the ISET pin and can be scaled via I<sup>2</sup>C register CHG1 bits ISET1[1:0] to a percentage (100%, 75%, 50% or 25%) of the value set by  $R_{ISET}$ .

The ISET resistor will always set the maximum charge current if the AC input is selected. When the USB input is selected the maximum charge current will be defined by the USB input current limit and the programmed charge current. If the USB input current limit is lower than the  $I_{O(BAT)}$  value, the battery switch will be set in the dropout region and the charge current will be defined by the input current limit value and system load, as shown in Figure 3-10.

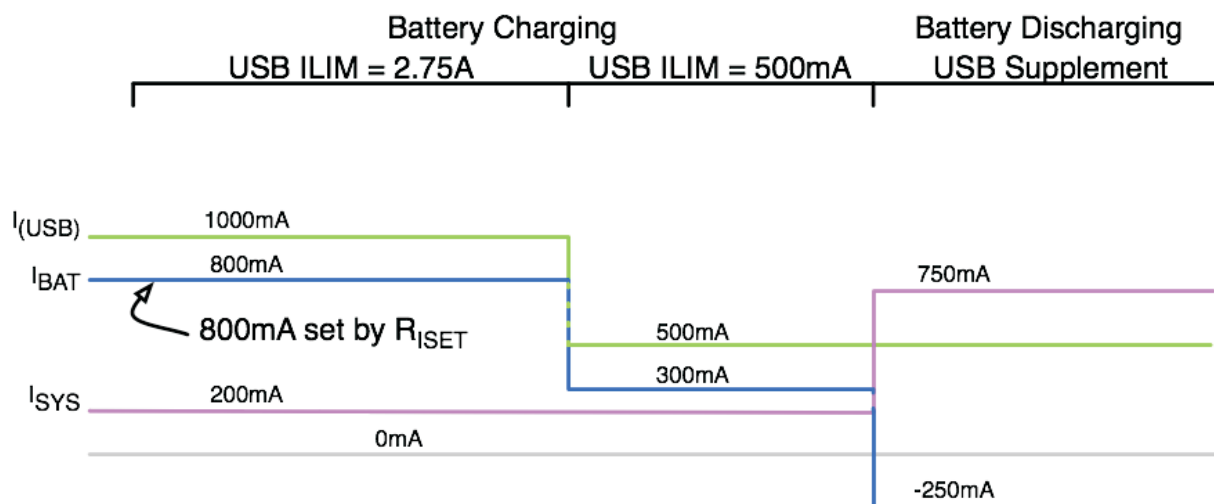


Figure 3-10. USB Supplement Mode

### 3.30 BATTERY VOLTAGE REGULATION, CHARGE VOLTAGE

The Voltage regulation feedback is implemented by sensing the BAT pin voltage, which is connected to the positive side of the battery pack. The TPS658621A monitors the battery-pack voltage between the BAT and AGND1 pins. When the battery voltage rises to the  $V_{O(BATREG)}$  threshold, the voltage regulation phase begins and the charging current tapers down.

The charging voltage can be selected via I<sup>2</sup>C, with bits VCHG<1:0> (register VCHG1) and RSVD4B4 (register PPATH1, 0x4C)

### 3.31 LDO MODE OPERATION

The LDO mode makes it possible to run critical subsystems connected directly to the battery node (BAT pin) when the battery is removed and the end equipment is powered by the AC or USB input.

The SM2 voltage must be programmed by the host via register SUPPLYV2 control bits VSM2<4:0> to a value 100mv above the programmed charge voltage before the LDO mode is enabled, and it should be left at that value while LDO mode is in use. The SM2 voltage can be set to any other value after the LDO mode is disabled.

The charger LDO Mode operation is enabled when termination is disabled (TERMOFF bit is 1 in CHG1) and thermistor removal detection is ignored (setting TSBYP bit to 1 in CHG2).

When the LDO mode is set, termination is disabled, all safety timers are held in reset, and the battery discharge switch is disabled. The BAT pin voltage will regulate to  $V_{O(BATREG)}$  when **all** the following conditions are true: the charger is enabled ( $VIN\_CHG > V_{O(BATREG)}$ ) and input power is present (AC or USB input power detected). Under these conditions the BAT pin voltage will be regulated to the charge voltage  $V_{O(BATREG)}$  if the charger current loops are not active.

The charger current limit loop will still be enabled, and the current that can be supplied by the BAT pin in LDO mode will be dependent on the BAT pin voltage, as shown in [Table 3-10](#).

**Table 3-10. Battery Charge Current**

| BAT PIN VOLTAGE | BATTERY CHARGE CURRENT |
|-----------------|------------------------|
| $< V_{LOWBAT}$  | $I_{O(PRECHG)}$        |
| $> V_{LOWBAT}$  | $I_{O(BAT)}$           |

In LDO mode, both the thermal loop and DPPM loop are also enabled. These loops, when active, limit the current available at the BAT pin. The BAT pin voltage will collapse if the charge current available is lower than the current required to run subsystems connected to the BAT pin.

The battery tracking function is disabled when the thermistor is not detected; the BAT pin will, as a result, track the SM2 output voltage when  $V(SM2)$  is set below  $V_{O(BATREG)}$ .

### 3.32 CHARGER CONTROL LOGIC AND OPERATING MODES

The charger control logic monitors system parameters and control signals to define when the charger is enabled. The table below lists the charger operating modes. Note that when the charger is set to OFF all timers are reset. The charge is enabled by setting bit CHGON to **1** in register CHG2.

The timer fault and termination detection events are latched internally to the charger control logic, and after that the charger is set to OFF. The only way to reset a timer fault and termination detection is to start a new charge cycle.

**Table 3-11. Charger Mode Control**

| TPS658621A MODE | INPUT POWER DETECTED | SM2 MODE <sup>(1)</sup> | CHARGER THSHUT DETECTED | CHARGE ENABLED | CHARGE SUSPEND CMD | TIMER FAULT DETECTED | PACK TEMP FAULT | TERM DETECTED | CHARGER MODE |
|-----------------|----------------------|-------------------------|-------------------------|----------------|--------------------|----------------------|-----------------|---------------|--------------|
| UVLO            | X                    | X                       | X                       | X              | X                  | X                    | X               | X             | OFF          |
| NOT UVLO        | NO                   | X                       | X                       | X              | X                  | X                    | X               | X             | OFF          |
|                 | YES                  | OFF                     | X                       | X              | X                  | X                    | X               | X             | OFF          |
|                 | YES                  | ON                      | YES                     | X              | X                  | X                    | X               | X             | OFF          |
|                 | YES                  | ON                      | NO                      | NO             | X                  | X                    | X               | X             | OFF          |
|                 | YES                  | ON                      | NO                      | YES            | NO                 | NO                   | NO              | NO            | ON           |
|                 | YES                  | ON                      | NO                      | YES            | NO                 | YES                  | X               | X             | OFF          |
|                 | YES                  | ON                      | NO                      | YES            | NO                 | X                    | X               | YES           | OFF          |
|                 | YES                  | ON                      | NO                      | YES            | YES                | NO                   | X               | NO            | SUSPEND      |
|                 | YES                  | ON                      | NO                      | YES            | NO                 | NO                   | YES             | NO            | SUSPEND      |

(1) When SM2 is not configured as the charger pre-regulator the SM2 mode does not affect the charger mode.

### 3.33 CHARGE SUSPEND

The charge may be suspended anytime by setting CHSUSP to **1** in register CHG1 or when the pack temperature is out of range and I<sup>2</sup>C control bit TSBYP is **0**. This will disable the charger stage and hold the safety timers at their current count. Normal operation resumes when a temperature fault is not detected.

### 3.34 CHARGE TERMINATION

The TPS658621A monitors the charging current during the voltage regulation phase. Charge is terminated when the charge current is lower than an internal threshold, set to 10% (typ) of the fast charge current rate. The termination point applies to both AC and USB charging, and it can be calculated as shown in Equation 3.

$$I_{\text{TERM}} = \frac{K_{\text{TERM}}}{R_{\text{ISET}}} \quad (3)$$

where  $K_{\text{TERM}}$  is the termination constant detection factor.

The termination current may be scaled using I<sup>2</sup>C register CHG3 bits ITERM[1:0].

The termination detection is internally deglitched by  $T_{\text{DGL(TERM)}}$ , 25ms typ. When the charge current drops below the internal termination threshold for  $t > T_{\text{DGL(TERM)}}$ , the bit ITERM is set to 1 in the status register STAT, indicating that termination was detected. ITERM is not affected by the state of TERMOFF control bit, and it will always report the charge current status. If the termination is enabled (TERMOFF cleared to 0) and termination is detected, the charge cycle ends and the charger is turned off.

**Table 3-12. Termination Detection Conditions**

| CHARGE CURRENT<br>BELOW TERMINATION<br>THRESHOLD | DPM OR DPPM OR<br>THERMAL LOOP<br>ACTIVE | CHARGER MODE | TERMINATION<br>DETECTION ENABLED<br>VIA I <sup>2</sup> C | TERMINATION<br>DETECTED,<br>$I(\text{BAT}) < I_{\text{TERM}}$ |
|--|--|--------------|--|---|
| NO   | X  | X            | X  | NO  |
| YES  | X  | OFF          | X  | NO  |
| YES  | X  | SUSPEND      | X  | NO  |
| YES  | X  | ON           | NO   | NO  |
| YES  | YES                                      | ON           | YES  | NO  |
| YES  | NO                                       | ON           | YES  | YES   |

The termination detection is latched and it will be reset only when a new charge cycle starts.

The I<sup>2</sup>C charge status bits in the STAT2 register only indicate DONE state when termination is detected.

### 3.35 STARTING A NEW CHARGE CYCLE

A new charge cycle will start only if the voltage on the BAT pin falls below the  $V_{(\text{RCH})}$  threshold for a time longer than  $T_{\text{DGL(RCH)}}$ , 25ms (typ). A new charge cycle also starts when bit CHGON (CHG1 register) changes from 0 to 1, or if both AC and USB input power are removed and then one or both are re-inserted.

After termination is detected a new battery pack insertion detection will not start a new charge cycle, even if  $V(\text{BAT}) < V_{(\text{RCH})}$ .

### 3.36 PRE-CHARGE SAFETY TIMER

The TPS658621A activates an internal safety timer during the battery pre-conditioning phase. The pre-charge safety timer value is set internally to a fixed value,  $T_{\text{PRECHG}}$ , 30 min or 60 min typ, selectable via I<sup>2</sup>C. The pre-charge safety timer is disabled when the termination is disabled via I<sup>2</sup>C (bit TERMOFF=HI, register CHG1) or when CHTMREN=0 at the I<sup>2</sup>C register CHG2.

When the charger is in suspend mode the pre-charge safety timer is put on hold (i.e., charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If  $V(\text{BAT})$  does not reach the internal voltage threshold  $V_{(\text{PRECHG})}$  within the pre-charge timer period a fault condition is detected and the charger is turned off.

### 3.37 CHARGE SAFETY TIMER

As a safety mechanism the TPS658621A has a user-selectable timer that measures the total fast charge time. This timer (charge safety timer) is started at the end of the pre-conditioning period. The following values are available: 4, 5, 6, 8 hours, selectable via I<sup>2</sup>C register CHG1 bits  $\overline{\text{CHGTMR}}$ . The charge safety timer is kept in reset mode when CHTMREN=0 at the I<sup>2</sup>C register CHG2. The charge safety timer is disabled when TERMOFF=1, in register CHG1. When the charger is in suspend mode, set via I<sup>2</sup>C register CHG\_CONFIG bit CHGON or set by a pack temperature fault, the charge safety timer is put on hold (i.e., charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If charge termination is not reached within the timer period a fault condition is detected, and the charger is turned off.

### 3.38 TIMER FAULT RECOVERY

The TPS658621A provides a recovery method to deal with timer fault conditions. The following summarizes this method:

**Condition 1:** Charge voltage above recharge threshold ( $V_{(RCH)}$ ) and timeout fault occurs.

|                  |   |
|------------------|---|
| Recovery method: | The IC waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the IC clears the fault and starts a new charge cycle. |
|------------------|---|

**Condition 2:** Charge voltage below recharge threshold ( $V_{(RCH)}$ ) and timeout fault occurs.

|                  |  |
|------------------|--|
| Recovery method: | Under this scenario, the IC connects an internal pull-up resistor from VIN_CHG pin to BAT pin. This pull-up resistor is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disables the pull-up resistor connection and executes the recovery method described for condition 1. |
|------------------|--|

***All timers will be reset and all timer fault conditions are cleared when a new charge cycle is started either via I<sup>2</sup>C (toggling bit CHGON in register CHG1) or by cycling the input power. All timers are reset and all timer fault conditions are cleared when the TPS658621A enters the UVLO mode or if the LDO mode is set.***

### 3.39 DYNAMIC TIMER CONTROL

When the charger, thermal loop or DPPM loop are active the charge current is reduced. To avoid a false termination detection when those loops are active the charger logic doubles the period of the clock used by the charge safety timer.

The clock frequency is divided by 2 when any of those loops are active and DTCON=1. The dynamic timer control may be disabled by setting control bit DTCON=0, at the CHG2 I<sup>2</sup>C register.

### 3.40 BATTERY DISCHARGE SWITCH

An internal switch will discharge the BAT pin to ground when the battery is not detected. This switch is enabled via I<sup>2</sup>C control bit BATDCH on register CHG1.

### 3.41 CHARGER STATUS

Charger status information is available at registers 0xB9, bits PACK\_HOT, PACK\_COLD, BATDET and BATCHGSWON; register 0xBA, bits TMRFLT, DPPM\_ON, TH\_ON, ITERM, STAT1 and STAT2. See STATUS REGISTERS section for bit functional description. The charger status also is indicated at pin CHG\_STAT, this pin can be used as a logic level output (2v2 level) or it can be connected to an external LED.

**Table 3-13. Charger Status Pin States**

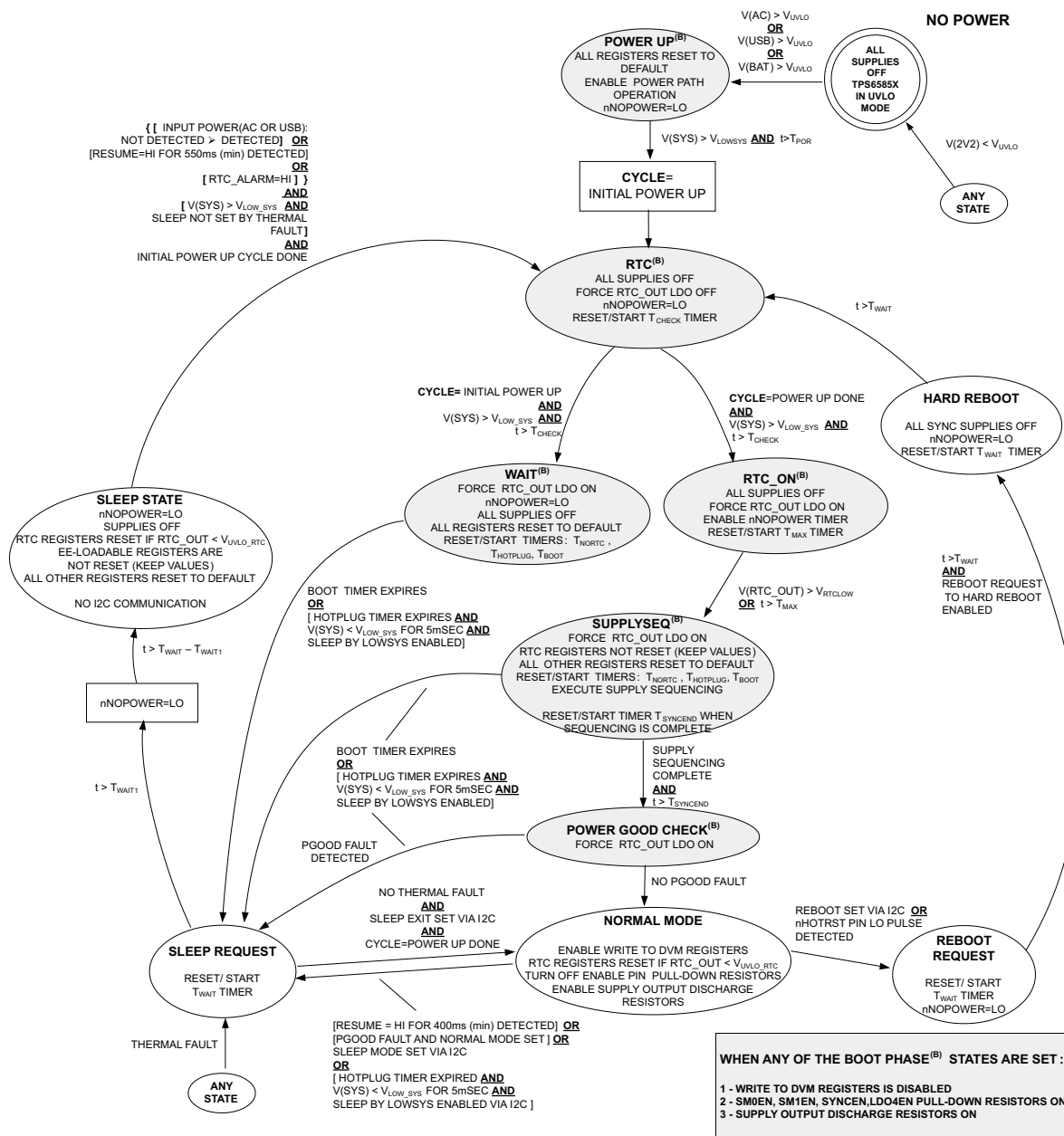
| 0xBA[2]<br>(STAT1) | 0xBA[1]<br>(STAT2) | CHARGER STATE               | CHG_STAT LEVEL |
|--------------------|--------------------|-----------------------------|----------------|
| 0                  | 0                  | Pre-Charge                  | HI             |
| 0                  | 1                  | Charge Done                 | LO             |
| 1                  | 0                  | Fast Charge                 | HI             |
| 1                  | 1                  | Charge Suspend, Timer fault | LO             |

### 3.42 TPS658621A OPERATING MODES

The TPS658621A has an internal state machine that sets the operating modes based on the system status and host commands. The state machine directly controls the state of the integrated supplies during power-up sequences and normal operation. It also can change the on/off state of all integrated power supplies and peripherals to implement protection functions or execute external hardware control or host software commands.



### 3.43 STATE MACHINE DIAGRAM



### Figure 3-11. TPS658621A Operation Mode State Machine

The state machine transitions for the TPS658621A have been defined as shown below.

1. Supply sequencing started only when LDO4EN voltage level is a logic high
2. REBOOT REQUEST state transitions to the HARD REBOOT state
3. Supply sequencing is considered complete only if SM0 is turned ON
4. Sequencer goes into sleep during initial power-up cycle and ONLY RESUME pin can trigger exit from sleep state

### 3.44 STATE MACHINE DESCRIPTION

In a normal power-up sequence the state machine will step through the following states:



**POWER-UP:** If the internal digital supply (2V2) is below the internal UVLO threshold,  $V_{UVLO}$  (2V typ), all IC blocks are disabled and the TPS658621A is not operational. When the 2V2 supply voltage rises above  $V_{UVLO}$ , the POWER-UP state is entered, an internal delay ( $T_{POR}$ , 8ms typ) is started and the SYS power path is enabled. The SYS pin voltage is sensed by an internal comparator, and compared to the internal threshold  $V_{LOW\_SYS}$ . When the power-on-reset delay expires and  $V(SYS) > V_{LOW\_SYS}$  the TPS658621A enters the RTC mode.

**RTC:** When the RTC state is set the nNOPOWER pin is pulled to ground, discharging the external capacitor connected to pin TNOPOWER and resetting the NOPOWER timer. The RTC\_OUT LDO is turned off, and the voltage at pin RTC\_OUT is flagged as low if  $V(RTC\_OUT) < V_{RTCLow}$ . The RTC state ends when the timer  $T_{CHECK}$  expires.

**RTC\_ON:** When the state RTC\_ON is set the integrated current source connected to the TNOPOWER pin and the RTC\_OUT LDO are enabled. If the RTC\_OUT voltage was flagged as low in the RTC state the  $T_{NORTC}$  timer is enabled, and the  $\overline{NORTC}$  pin is pulled low until  $V(RTC\_OUT) > V_{RTC\_PGOOD}$ . The  $T_{NORTC}$  timer starts counting when  $RTC\_OUT > V_{RTCLow}$ , and  $\overline{NORTC}$  will be set to hi when  $t > T_{NORTC}$ .

The TNOPOWER current source will remain ON until a new reboot cycle or sleep cycle is set, charging the external capacitor connected to the TNOPOWER pin. The  $\overline{NOPOWER}$  pin will be at a low logic level until the TNOPOWER pin voltage is above an internal threshold (1.23V typ). When  $\overline{NOPOWER}$  pin transitions from LO→HI, a 250μsec (typ) positive going pulse is generated at CHG\_STAT pin. The TNOPOWER external capacitor is discharged whenever the sequencer sets the  $\overline{NOPOWER}$  pin to a low state.

The RTC\_ON state ends when  $V(RTC\_OUT) > V_{RTC\_PGOOD}$  or when the internal watchdog timer  $T_{MAX}$  expires.

**WAIT:** The TPS658621A will go into the WAIT state when exiting the RTC state during the initial power-up cycle. To avoid undesired lockup conditions this operational mode should be used only when the boot timer is enabled.

Three internal timers are started when the state machine enters the WAIT state. These timers run independent of the sequencing state and have the following functionality:

- **BOOT Timer ( $T_{BOOT}$ ):** Sets the TPS658621A in the SLEEP REQUEST state if it expires during WAIT state.
- **HOTPLUG Timer ( $T_{HOTPLUG}$ ):** SLEEP REQUEST state set by  $V(SYS) < V_{LOW\_SYS}$  is inhibited until this timer expires
- **NORTC Timer ( $T_{NORTC}$ ):**  $\overline{NORTC}$  pin will be set to a logic low level until this timer expires

The BOOT timer value is set to 500ms and the  $\overline{NORTC}$  pulse width is set to 10ms.

**SUPPLYSEQ:** During the SUPPLYSEQ state all the internal supplies, with exception of RTC\_OUT, are initially turned off and then turned on according to a pre-programmed internal sequencing. Three internal timers are started when the state machine enters the SUPPLYSEQ state. These timers run independent of the sequencing state and have the following functionality:

- **BOOT Timer ( $T_{BOOT}$ ):** Sets the TPS658621A in the SLEEP REQUEST state if it expires during SUPPLYSEQ state.
- **HOTPLUG Timer ( $T_{HOTPLUG}$ ):** SLEEP REQUEST state set by  $V(SYS) < V_{LOW\_SYS}$  is inhibited until this timer expires
- **NORTC Timer ( $T_{NORTC}$ ):**  $\overline{NORTC}$  pin will be set to a logic low level until this timer expires

The BOOT timer value is set to 500ms and the  $\overline{NORTC}$  pulse width is set to 10ms.

The I<sup>2</sup>C engines are available while the device is in the SUPPLYSEQ state, however write operations to the DVM registers are disabled, refer to DVM register section for more details. The TPS658621A remains in this state until all the supplies are sequenced and the internal delay  $T_{SYNCEnd}$  (5ms typ) has expired.

**POWER GOOD CHECK:** Supplies that were powered up during the SUPPLYSEQ state will have their power good flags checked during the POWER GOOD CHECK state (with exception of RTC\_OUT Ldo). The POWER GOOD CHECK state ends and the NORMAL state is set when a power good fault is not present. If a power good fault is detected, the POWER GOOD CHECK state will move to the SLEEP REQUEST state when the boot timer expires.

**NORMAL STATE:** In this state write operations to the DVM registers are enabled and the external host controls all the TPS658621A functions. The normal state operation ends if a fault condition (defined as either a thermal fault,  $V(\text{SYS}) < V_{\text{LOW\_SYS}}$  or a supply power good fault) is detected or if hardware or software commands trigger a sleep or reboot request. While in NORMAL mode, the host can mask any of the power supply power good fault detection via I<sup>2</sup>C registers PGFLTMASK1 and PGFLTMASK2. Supplies that have their power good fault detection masked will not end the normal state operation. However, the status bit for the supply indicates that the output voltage is out of regulation. A RTC\_OUT LDO power good fault does not trigger a transition to SLEEP REQUEST.

**Table 3-14. Sequencer Power Good Fault Masking**

| PGFLTMASK1 [Addr 0x4D] |                 |                 |                 |                 |                 |                 | Defaults in <b>BOLD</b> |                 |
|------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------------|-----------------|
| Bit Number             | B7              | B6              | B5              | B4              | B3              | B2              | B1                      | B0              |
| Bit Name               | MASK_PLDO8      | MASK_PLDO7      | MASK_PLDO6      | MASK_PLDO4      | MASK_PLDO3      | MASK_PLDO2      | MASK_PLDO1              | MASK_PLDO0      |
| Function               | MASK PGOODLDO8  | MASK PGOODLDO7  | MASK PGOODLDO6  | MASK PGOODLDO4  | MASK PGOODLDO3  | MASK PGOODLDO2  | MASK PGOODLDO1          | MASK PGOODLDO0  |
| When 0                 | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b>         | <b>UNMASKED</b> |
| When 1                 | MASKED          | MASKED          | MASKED          | MASKED          | MASKED          | MASKED          | MASKED                  | MASKED          |

| PGFLTMASK2 [Addr 0x4E] |                 |               |                 |                 |                 |                 | Defaults in <b>BOLD</b> |                 |
|------------------------|-----------------|---------------|-----------------|-----------------|-----------------|-----------------|-------------------------|-----------------|
| Bit Number             | B7              | B6            | B5              | B4              | B3              | B2              | B1                      | B0              |
| Bit Name               | MASK_PSM3       | MASK_PSM2     | MASK_PSM1       | MASK_PSM0       | MASK_PLDO9      | MASK_PLDO5      | RSVD4E1                 | RSVD4E0         |
| Function               | MASK PGOODSM3   | MASK PGOODSM2 | MASK PGOODSM1   | MASK PGOODSM0   | MASK PGOODLDO9  | MASK PGOODLDO5  | NOT USED                | NOT USED        |
| When 0                 | <b>UNMASKED</b> | <b>MASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>UNMASKED</b> | <b>NOT USED</b>         | <b>NOT USED</b> |
| When 1                 | MASKED          | UNMASKED      | MASKED          | MASKED          | MASKED          | MASKED          | NOT USED                | NOT USED        |

**SLEEP REQUEST:** The SLEEP REQUEST state is set at anytime when a thermal fault condition is detected. It is also set when the TPS658621A is in the NORMAL state followed by one of the events shown below.

1. A hardware sleep request is detected at the RESUME pin.
2. A power good fault is detected at any of the integrated supplies
3.  $V(\text{SYS\_IN}) < V_{\text{LOW\_SYS}}$  and the HOTPLUG timer has expired ( $t > T_{\text{HOTPLUG}}$ )
4. SLEEP MODE is 1 (register 0x14, bit B3)

When the SLEEP REQUEST state is set an internal timer is started and bit SLEEPREQ=1 is set in register STAT3 (address 0xBB). Writing EXITSLREQ to 1 (0x14, bit B1) returns the TPS658621A to the NORMAL state. If no action is taken by the host, while SLEEP\_REQUEST state is set, the NOPOWER pin is pulled low when  $T_{\text{WAIT1}}$  expires and the SLEEP state is entered after the  $T_{\text{WAIT}}$  timer expires.

**Table 3-15. Sequencer Control, LDO5/LDO9 Enable**

| SUPPLYENE [Addr 0x14] |                     |                     |                                    |                       |                              |      | Defaults in <b>BOLD</b>                                   |                        |
|-----------------------|---------------------|---------------------|------------------------------------|-----------------------|------------------------------|------|---|------------------------|
| Bit Number            | B7                  | B6                  | B5                                 | B4                    | B3                           | B2   | B1  | B0                     |
| Bit Name              | LDO9_ON             | LDO5_ON             | SYSINEN                            | HOTDLY                | SLEEP MODE                   | RSVD | EXITSLREQ   | SOFT RST               |
| Function              | LDO9 ON/OFF CONTROL | LDO5 ON/OFF CONTROL | SYS_IN LOW VOLTAGE SETS SLEEP MODE | HOT RESET DEGLITCH    | SET TPS658621A IN SLEEP MODE |      | SLEEP REQUEST EXIT CONTROL                                | SOFTWARE RESET CONTROL |
| When 0                | <b>OFF</b>          | <b>OFF</b>          | DISABLED                           | 5µsec min, 16µsec max | <b>NOT ACTIVE</b>            |      | <b>GO TO SLEEP at <math>T &gt; T_{\text{wait}}</math></b> | <b>NOT ACTIVE</b>      |

Table 3-15. Sequencer Control, LDO5/LDO9 Enable (continued)

|        |    |    |         |     |           |  |   |                   |
|--------|----|----|---------|-----|-----------|--|---|-------------------|
| When 1 | ON | ON | ENABLED | 5ms | SET SLEEP |  | FORCE<br>TRANSITION<br>TO NORMAL<br>STATE | REBOOT<br>REQUEST |
|--------|----|----|---------|-----|-----------|--|---|-------------------|

**SLEEP STATE:** When the SLEEP state is set all supplies are set to OFF mode (with exception of RTC\_LDO) and the  $\overline{\text{NOPOWER}}$  output is pulled low. A few internal blocks are still active, enabling detection of system status changes that trigger the SLEEP state exit.

All I<sup>2</sup>C engines are reset and all RAM registers are reset to their default condition when the SLEEP state is set. The RAM bits that have a default set via the non-volatile memory will keep the value they had before the SLEEP state was set.

The SLEEP state ends when one of the following sequences is executed:

- A. *If SLEEP was set by thermal fault:* The SLEEP state will end only when all external input supplies and battery pack are removed and an UVLO condition is detected by the TPS658621A, setting the POWER UP state.
- B. *If SLEEP was not set by thermal fault:* The SLEEP state will end when a hardware sleep exit request is detected at RESUME pin

**EXITING THE SLEEP STATE:** The figure below shows the timing relationship needed on the RESUME pin to exit the sleep mode. This applies for all cases where the sleep mode entry was triggered by any event other than a thermal fault.

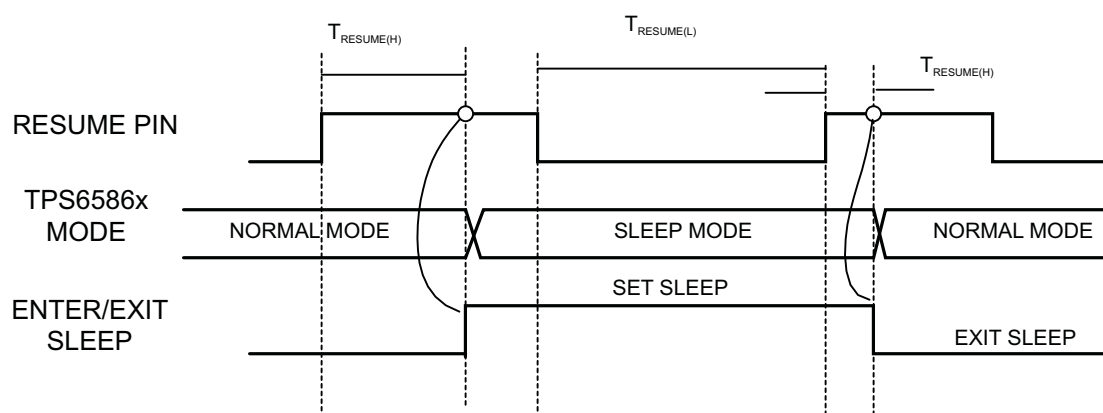


Figure 3-12. Entering and Exiting Sleep Mode Resume

**REBOOT REQUEST:** The REBOOT REQUEST state is entered from the NORMAL state. It can be set via software (SOFT\_RST set to 1, register 0x14 Bit B0) or by a  $V_{IL}$  level detection at  $\overline{\text{HOTRST}}$  pin. When the reboot request state is set an internal timer  $T_{\text{WAIT}}$  (10ms typ) is started, and the  $\overline{\text{NOPOWER}}$  pin is pulled to ground. The reboot request ends when  $t > T_{\text{WAIT}}$ . The REBOOT REQUEST will transition the device state machine to the HARD REBOOT state. The REBOOT REQUEST is set if the  $\overline{\text{HOTRST}}$  low pulse width is greater than 10μsec (typ).

The status bit COMPDET=1 (register STAT2, address 0xBA) when the NORMAL state is entered after a reboot cycle triggered by the  $\overline{\text{HOTRST}}$  pin. The status bit COMPDET=0 when the NORMAL state is entered, after a power-up, sleep cycle or software triggered reboot cycle.

The bit COMPDET is reset to 0 when bit SPARECC0=1, in register SPARE2 (address 0xCC). After resetting the COMPDET bit the host needs to set SPARECC0=0 to enable detection of another reboot cycle set via the  $\overline{\text{HOTRST}}$  pin.

An interrupt is generated when the TPS658621A transitions from the POWER GOOD CHECK state to the NORMAL state, COMPDET=1 and IMASK\_COMP=0 in register INTMASK4 (address 0xB3). An interrupt request is generated after the NORMAL state is set if IMASK\_COMP=0 and COMPDET value changes from 1 to 0.

**Table 3-16. Reboot Flag Control**

| SPARE2 [Addr 0xCC] |                 |                 |                 |                 |                 |                 |                 | Defaults in <b>BOLD</b>                    |
|--------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|--|
| Bit Number         | B7              | B6              | B5              | B4              | B3              | B2              | B1              | B0   |
| Bit Name           | SPARECC7        | SPARECC6        | SPARECC5        | SPARECC4        | SPARECC3        | SPARECC2        | SPARECC1        | SPARECC0                                   |
| Function           | SPARE           | SPARE           | SPARE           | SPARE           | SPARE           | SPARE           | SPARE           | RESET<br>REBOOT BY<br>HOTRST<br>STATUS BIT |
| When 0             | NOT USED        | NOT USED        | NOT USED        | NOT USED        | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | <b>DO NOT<br/>RESET</b>                    |
| When 1             | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | NOT USED        | NOT USED        | NOT USED        | RESET                                      |

**HARD REBOOT:** The HARD REBOOT state powers down all the TPS658621A supplies, with exception of the RTC\_OUT LDO.

**SUPPLYLOAD:** When the SUPPLYLOAD state is set all the registers are reset to their defaults, and the non-volatile memory is reloaded into the RAM. The supplies are not sequenced, and they will return to their on/off and output voltage defaults upon entering the SUPPLYLOAD state (on/off, default voltages). The timers  $T_{BOOT}$ ,  $T_{HOTPLUG}$  and  $T_{SYNCEND}$  are reset and started. The SUPPLYSEQ state ends when  $t > T_{SYNCEND}$ , and the POWER GOOD CHECK state is set.

### 3.45 **C<sub>NOPOWER</sub> CAPACITOR DISCHARGE**

The external capacitor connected to the TNOPOWER pin is always discharged when the sequencer sets NOPOWER=LO in the following states: POWER-UP, RTC, REBOOT REQUEST, HARD REBOOT and SLEEP. For large capacitance values (above 330nF) the external capacitor may not be fully discharged during reboot cycles, and as a result the NOPOWER pulse width may be slightly reduced when compared to the value indicated in the parametric tables.

### 3.46 **SEQUENCER STATUS**

Sequencer status information is available at registers 0xBA, bit COMPDET and register 0xBB bits SLEEPREQ and RESUME. See STATUS REGISTERS section for functional description of these bits.

### 3.47 **SUPPLY SEQUENCING AND HOST INTERFACE**

#### 3.47.1 **Integrated Supply Sequencing**

The TPS658621A enables the implementation of complex supply sequencing. With the exception of RTC\_OUT, the integrated power-up sequencing starts when the TPS658621A state machine enters the SUPPLYSEQ state. The RTC\_OUT LDO is always enabled in the RTC state, which occurs before the SUPPLYSEQ state, and the output of this LDO can be used to power an external processor or circuitry in systems where the supply sequencing is controlled externally using pins SM0EN, SM1EN or SYNCEN.

Each supply rail is controlled by a combination of its default status (ON or OFF), its assigned sequencing trigger group (INTERNAL, SM0EN, SM1EN or SYNCEN), and a delay time.

The default status (ON or OFF) of each rail is shown in [Table 3-17](#).

If the default for a supply rail is ON the trigger group associated to the supply determines the control signal that initiates the delay time to the start of the rail power up. There are four trigger groups, one internal and three external pins:

- INTERNAL** This group is controlled by an internal signal that goes high when the TPS658621A goes from the RTC\_ON state to the SUPPLYSEQ state.
- SM0EN** This group is controlled by the falling edge of the SM0EN pin and starts when the pin voltage is below its  $V_{IL}$  level.
- SM1EN** This group is controlled by the rising edge of the SM1EN pin and starts when the pin voltage is above its  $V_{IH}$  level.
- SYNCEN** This group is controlled by the rising edge of the SYNCEN pin and starts when the pin voltage is above its  $V_{IH}$  level.

The trigger group of each rail and its associated delay is shown in [Table 3-17](#). If a supply rail has a default state of ON and the appropriate trigger is high, the rail will be turned on after the delay time for that rail has expired. The delay time starts when the trigger signal for that supply has gone high, while SUPPLYSEQ state is set. No delays are available after NORMAL mode is set.

**Table 3-17. TPS658621A Integrated Supply Power-Up Defaults**

| TPS658621A SETTINGS |               |                 |   |  |
|---------------------|---------------|-----------------|---|--|
| SUPPLY              | DEFAULT STATE | DEFAULT VOLTAGE | TRIGGER   | DELAY  |
| LDO0                | OFF           | 1.2V            | SYNCEN  | 3.75ms<br>Value applies to LDO0, LDO1        |
| LDO1                | ON            | 1.1V            | INTERNAL  |  |
| LDO2                | ON            | 1.2V            | INTERNAL  | 2.5ms<br>Value applies to LDO2, LDO3         |
| LDO3                | ON            | 3.3V            | SYNCEN  |  |
| LDO4                | ON            | 1.8V            | INTERNAL  | 15ms   |
| LDO6                | OFF           | 2.85V           | SYNCEN  | 15ms<br>Value applies to LDO6, LDO7 and LDO8 |
| LDO7                | OFF           | 3.3V            | SYNCEN  |  |
| LDO8                | OFF           | 1.8V            | SYNCEN  |  |
| LDO5                | ON            | 2.85V           | SYNCEN<br>Trigger applies to both LDO5 and LDO9 | 2.5ms<br>Value applies to LDO5, LDO9         |
| LDO9                | ON            | 2.85V           |   |  |
| SM0                 | ON            | 1.2V            | SM0EN   | 3.75ms                                       |
| SM1                 | ON            | 1.0V            | SM1EN   | 3.75ms                                       |
| SM2                 | ON            | 3.7V            | INTERNAL  | 0ms  |

### 3.48 INTEGRATED SUPPLY SEQUENCING – SUPPLY ENABLE CONTROL

The ON or OFF mode for each supply is defined by the supply enable RAM control bits and enable pins SM0EN, SM1EN and LDO4EN. The supply enable bits are located in registers SUPPLYENA, SUPPLYENB, SUPPLYENC, SUPPLYEND, SUPPLYENE (see supply functional description for more details). The functionality of the RAM bits and enable pins is dependent on the state set in the state machine as follows:

**When the NORMAL state is NOT set :** The pins SM1EN , SM0EN and LDO4EN will always control the ON or OFF modes for all supplies that use them as triggers. The supply enable RAM bits will control the ON or OFF modes for the supplies.

**When the NORMAL state is set:** The supply enable RAM bits will always control the ON or OFF modes for the supplies. The pins SM1EN, SM0EN and LDO4EN may control the ON or OFF modes for supplies SM1, SM0 and LDO4. The enable pins do not control the ON or OFF modes of any other supplies.

During sequencing, the following RAM bits control the supply ON/OFF mode: LDO2 RAM bits, LDO4 RAM bits, SM0 RAM bits and SM1 RAM bits.

When the NORMAL mode is set, SM0EN controls the SM0 ON/OFF mode, SM1EN controls the SM1 ON/OFF mode and LDO4EN controls the LDO4 ON/OFF mode.

### 3.49 INTEGRATED SUPPLY SEQUENCING – POWER-DOWN

To start a power down sequence the SLEEP REQUEST or REBOOT REQUEST states must be set. Once one of those two states is set the trigger pins are active again and they will control the ON/OFF state of the supplies associated with that trigger group. The device will enter the SLEEP or HARD REBOOT state 10ms after the SLEEP REQUEST or REBOOT REQUEST is initiated. Any supply still active when the SLEEP or HARD REBOOT state is entered will be immediately disabled. This is the default turn off condition for any supply associated with the INTERNAL sequencing trigger group.

For example, if a supply has a default state of OFF and it has SM1EN as the selected factory trigger: this supply will not power up during the SUPPLYSEQ state when SM1EN goes high. If it is enabled during the NORMAL state and is still enabled when the SLEEP REQUEST or REBOOT REQUEST states are entered, this supply will be turned off on the falling edge of SM1EN as this is its assigned trigger group programmed at the factory.

If LDO4EN is set LO by the host when the TPS658621A enters the SLEEP REQUEST or REBOOT REQUEST states, the LDO4 supply will turn off only when the HARD REBOOT or SLEEP states are set. The LDO4PG pin will be pulled low when LDO4EN is below  $V_{IL}$ , with no delay.

All the supplies are turned off at the same time when the TPS658621A enters the SLEEP or HARD REBOOT state.

### 3.50 HOST INTERFACE

The TPS658621A devices have multiple signals that can be used by the external system to execute power sequencing operations or verify the system status. Those signals are generated as follows:

1. Power supply status (2V2 logic level) : SM0PG, SM1PG, LDO4PG – A HI level indicates that the supply is on and the regulation voltage is valid. A LO level indicates either that the supply voltage is out of regulation or that the supply has been disabled.
2. External system and host control (V32K pin logic level): The  $\overline{\text{NOPOWER}}$ ,  $\overline{\text{NORTC}}$ , and OUT32K pins may be used to interface to external hosts, controlling the host reset and executing host-controlled power-up sequencing.

#### 3.51 EXTERNAL 32 kHz

The TPS658621A outputs a 32 kHz clock (pin OUT32K) that can be used by the external system. The OUT32K output starts when the  $\overline{\text{NORTC}}$  pin is above  $V_{IH}$  and V32K is valid. The 32 kHz can be derived either from an internal 32kHz oscillator or from a crystal-based clock, selectable via I<sup>2</sup>C using bit 6 of the RTC\_CTRL (Addr 0xC0) register (see the Real Time Clock section). However, only the crystal-based clock is output to the OUT32K pin.

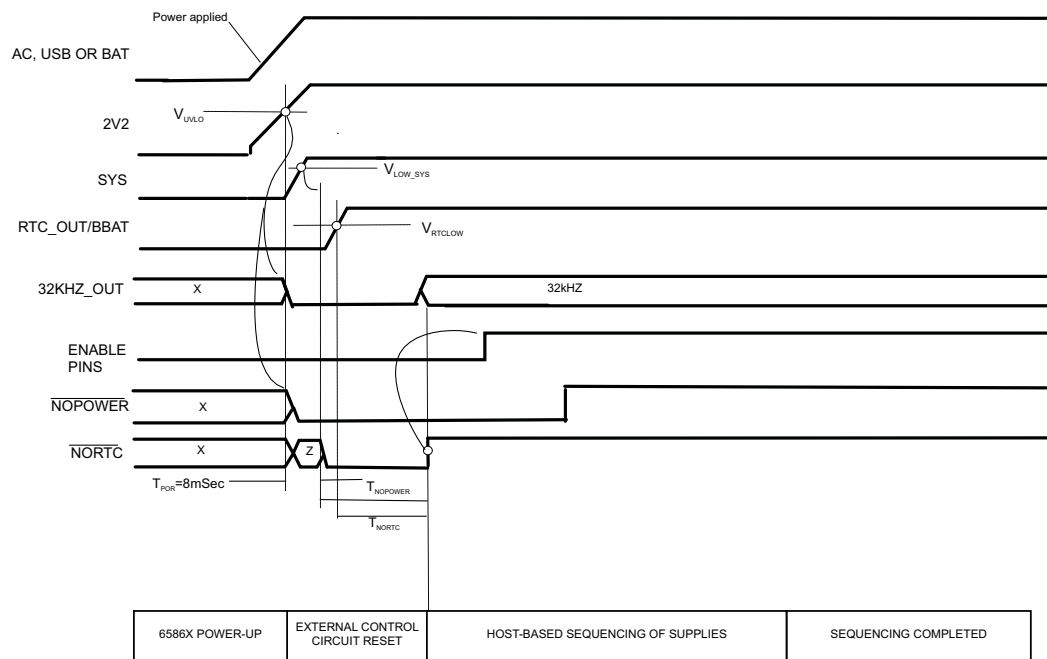
#### 3.52 SUPPLY INPUT PIN CONNECTION

The input pins for all supplies (VIN\_LDO01, VIN\_LDO23, VIN\_LDO4, VIN\_LDO678, VIN\_LDO9) enable optimization of the overall system power architecture by connecting lower output voltage supplies to intermediate rails or external rails. Care must be taken to ensure that the input pin for each integrated supply is powered when the supply is enabled during the power-up sequencing. Failure to do so will result in a power good fault detection with a potential lock-up situation. The input pins VIN\_SM0, VIN\_SM1, VIN\_SM2 must be connected to the SYS pin

#### 3.53 HOST INTERFACE

The TPS658621A may be used in systems where the sequencing is controlled by an external host or housekeeping circuit, as well as in systems where stand-alone sequencing is a requirement. For host controlled systems the RTC\_OUT LDO can be used as the supply that powers the external sequencing control and the NOPOWER and NORTC pin signals are used as resets for the external circuit.

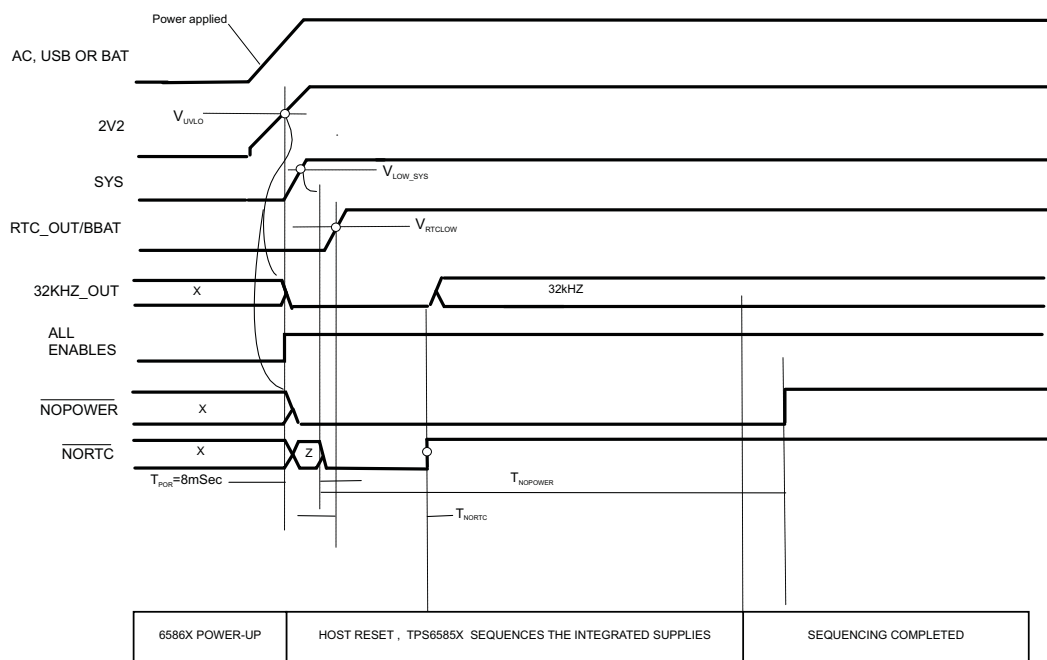




HOST CONTROLLED  
SEQUENCING :

RTC\_OUT SUPPLIES  
EXTERNAL CIRCUIT  
THAT DRIVES SUPPLY  
POWER-UP USING  
TRIGGER PINS SM0EN,  
SM1EN, SYNCEN

**Figure 3-13. Host Controlled Startup**



6586X SEQUENCING :

HOST IS KEPT IN  
RESET MODE UNTIL  
6586X SEQUENCES ALL  
SUPPLIES FOLLOWING  
INTERNAL,  
PRE-DEFINED TIMING.  
ALL ENABLE PINS  
CONNECTED TO 2V2

**Figure 3-14. TPS658621A Controlled Startup**

## 3.54 INTEGRATED SUPPLIES – ENABLE CONTROL, DVM CONTROL

### 3.54.1 DVM and Non-DVM Supplies

The TPS658621A has two types of voltage control for the integrated supplies:

1. DVM supplies: SM0, SM1, LDO2 and LDO4 are DVM supplies with dedicated register sets that enable a controlled transition from an initial voltage to a final voltage. The initial voltage, final voltage, and voltage transition start time are set via I<sup>2</sup>C. SM0 and SM1 have I<sup>2</sup>C programmable slew rate.

2. NON-DVM supplies: LDO0, LDO1, LDO3, LDO5, LDO6, LDO7, LDO8, LDO9, SM2 and RTC\_OUT outputs can be changed, but without slew rate and transition start time control. The output of these supplies will be changed to the new value as soon as TPS658621A sends the ACK of the I<sup>2</sup>C command setting the new output voltage.

### 3.54.2 DVM and Non-DVM Supply Enable

All the integrated supplies can be turned on/off by RAM enable bits. All the supplies (with exception of LDO5, LDO9 and RTC\_OUT LDO's) have two enable bits on distinct registers (registers 0x10, 0x11, 0x12, 0x13, 0x14). A supply will be enabled when ANY of its enable bits, in the registers below, are set to **1**. Each supply will be disabled when ALL of the enable bits for that supply are set to **0**. For example: SM0 enabled: SM0\_ENA=1 **OR** SM0\_ENB=1, SM0 disabled: SM0\_ENA=0 **AND** SM0\_ENB=0

**Table 3-18. SM0-2, LDO0-9 Control**

| SUPPLYENA [Addr 0x10] |                     |                     |                                    |                       |                              |                               | Defaults in <b>BOLD</b>          |                        |
|-----------------------|---------------------|---------------------|------------------------------------|-----------------------|------------------------------|-------------------------------|----------------------------------|------------------------|
| Bit Number            | B7                  | B6                  | B5                                 | B4                    | B3                           | B2                            | B1                               | B0                     |
| Bit Name              | RSVD107             | RSVD106             | RSVD105                            | RSVD104               | LDO2_ENA1                    | LDO2_ENA0                     | SM0_ENA                          | SM1_ENA                |
| Function              | <b>NOT USED</b>     | <b>NOT USED</b>     | <b>NOT USED</b>                    | <b>NOT USED</b>       | LDO2 CONTROL                 | LDO2 CONTROL                  | SM0 CONTROL                      | SM1 CONTROL            |
| SUPPLYENB [Addr 0x11] |                     |                     |                                    |                       |                              |                               | Defaults in <b>BOLD</b>          |                        |
| Bit Number            | B7                  | B6                  | B5                                 | B4                    | B3                           | B2                            | B1                               | B0                     |
| Bit Name              | RSVD117             | RSVD116             | RSVD115                            | RSVD114               | LDO2_ENB1                    | LDO2_ENB0                     | SM0_ENB                          | SM1_ENB                |
| Function              | <b>NOT USED</b>     | <b>NOT USED</b>     | <b>NOT USED</b>                    | <b>NOT USED</b>       | LDO2 CONTROL                 | LDO2 CONTROL                  | SM0 CONTROL                      | SM1 CONTROL            |
| SUPPLYENC [Addr 0x12] |                     |                     |                                    |                       |                              |                               |                                  |                        |
| Bit Number            | B7                  | B6                  | B5                                 | B4                    | B3                           | B2                            | B1                               | B0                     |
| Bit Name              | SM2_ONC             | LDO8_ONC            | LDO7_ONC                           | LDO6_ONC              | LDO4_ONC                     | LDO3_ONC                      | LDO1_ONC                         | LDO0_ONC               |
| Function              | SM2 CONTROL         | LDO8 CONTROL        | LDO7 CONTROL                       | LDO6 CONTROL          | LDO4 CONTROL                 | LDO3 CONTROL                  | LDO1 CONTROL                     | LDO0 CONTROL           |
| SUPPLYEND [Addr 0x13] |                     |                     |                                    |                       |                              |                               |                                  |                        |
| Bit Number            | B7                  | B6                  | B5                                 | B4                    | B3                           | B2                            | B1                               | B0                     |
| Bit Name              | SM2_OND             | LDO8_OND            | LDO7_OND                           | LDO6_OND              | LDO4_OND                     | LDO3_OND                      | LDO1_OND                         | LDO0_OND               |
| Function              | SM2 CONTROL         | LDO8 CONTROL        | LDO7 CONTROL                       | LDO6 CONTROL          | LDO4 CONTROL                 | LDO3 CONTROL                  | LDO1 CONTROL                     | LDO0 CONTROL           |
| SUPPLYENE [Addr 0x14] |                     |                     |                                    |                       |                              |                               | Defaults in <b>BOLD</b>          |                        |
| Bit Number            | B7                  | B6                  | B5                                 | B4                    | B3                           | B2                            | B1                               | B0                     |
| Bit Name              | LDO9_ON             | LDO5_ON             | SYSINEN                            | HOTDLY                | SLEEP MODE                   | SETNORMAL                     | EXITSLREQ                        | SOFT RST               |
| Function              | LDO9 ON/OFF CONTROL | LDO5 ON/OFF CONTROL | SYS_IN LOW VOLTAGE SETS SLEEP MODE | HOT RESET DEGLITCH    | SET TPS658621A IN SLEEP MODE | SET TPS658621A IN NORMAL MODE | SLEEP REQUEST EXIT CONTROL       | SOFTWARE RESET CONTROL |
| When 0                | OFF                 | OFF                 | DISABLED                           | 5μsec min, 16μsec max | <b>NOT ACTIVE</b>            | <b>NORMAL MODE NOT SET</b>    | <b>GO TO SLEEP at T&gt;Twait</b> | <b>NOT ACTIVE</b>      |
| When 1                | ON                  | ON                  | <b>ENABLED</b>                     | 5ms                   | SET SLEEP                    | ENABLE NORMAL MODE            | FORCE TRANSITION TO NORMAL STATE | REBOOT REQUEST         |



LDO5 and LDO9 will be turned on when LDO5\_ON is 1 or LDO9\_ON is 1, respectively. The RTC\_OUT LDO enable bits are located in the RTC control register, see real time clock section for details.

The supply enable defaults are unique for each device. See App Notes for device specific settings.

### 3.54.3 DVM Supplies - Voltage Transition Control

The output voltage for the DVM supplies can be set to one of the values programmed in the voltage setting registers SM0V1, SM0V2, SM1V1, SM2V2, LDO2AV1, LDO2AV2, LDO2BV1, LDO2BV2, LDO4V1 and LDO4V2 in registers VCC1 and VCC2.

The voltage change for the DVM supplies is usually done with 2 I<sup>2</sup>C write commands:

1. The host writes the new voltage to the voltage setting register for the supply(s) that will have an output voltage modification.
2. The voltage change starts by setting specific control bits in registers VCC1 and VCC2.

Bits  $\overline{VS}$  in registers VCC1 and VCC2 select the next voltage for the DVM supplies. A voltage change is started when ANY of the  $\overline{GO}$  bits for the supply is set to 1. At the end of the voltage transition the GO bits are cleared by the internal logic.

**Table 3-19. DVM Supply Control**

| VCC1 [Addr 0x20] |                                     |                                    |                        |                                      |                                    |                                    | Defaults in <b>BOLD</b>            |                                    |
|------------------|-------------------------------------|------------------------------------|------------------------|--------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| Bit Number       | B7                                  | B6                                 | B5                     | B4                                   | B3                                 | B2                                 | B1                                 | B0                                 |
| Bit Name         | LDO4VS                              | LDO4GO                             | LDO2AVS2               | LDO2AGO2                             | SM0VS1                             | SM0GO1                             | SM1VS1                             | SM1GO1                             |
| Function         | LDO4 VOLTAGE SELECTION              |                                    | LDO2 VOLTAGE SELECTION |                                      | SM0 VOLTAGE SELECTION              |                                    | SM1 VOLTAGE SELECTION              |                                    |
| When 0           | <b>SELECT VOLTAGE SET BY LDO4V1</b> | <b>HOLD CURRENT VOLTAGE</b>        | <b>NOT USED</b>        | <b>HOLD CURRENT VOLTAGE</b>          | <b>SELECT VOLTAGE SET BY SM0V1</b> | <b>HOLD CURRENT VOLTAGE</b>        | <b>SELECT VOLTAGE SET BY SM1V1</b> | <b>HOLD CURRENT VOLTAGE</b>        |
| When 1           | SELECT VOLTAGE SET BY LDO4V2        | RAMP TO VOLTAGE SELECTED BY LDO4VS | NOT USED               | RAMP TO VOLTAGE SELECTED BY LDO2BVS1 | SELECT VOLTAGE SET BY SM0V2        | RAMP TO VOLTAGE SELECTED BY SM0VS1 | SELECT VOLTAGE SET BY SM1V2        | RAMP TO VOLTAGE SELECTED BY SM1VS1 |

| VCC2 [Addr 0x21] |                                      |                                      |                          |                                      |                                    |                                    | Defaults in <b>BOLD</b>            |                                    |
|------------------|--------------------------------------|--------------------------------------|--------------------------|--------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| Bit Number       | B7                                   | B6                                   | B5                       | B4                                   | B3                                 | B2                                 | B1                                 | B0                                 |
| Bit Name         | LDO2BVS1                             | LDO2BGO1                             | LDO2AVS1                 | LDO2AGO1                             | SM0VS2                             | SM0GO2                             | SM1VS2                             | SM1GO2                             |
| Function         | LDO2 VOLTAGE SELECTION               |                                      | LDO2 VOLTAGE SELECTION I |                                      | SM0 VOLTAGE SELECTION              |                                    | SM1 VOLTAGE SELECTION              |                                    |
| When 0           | <b>SELECT VOLTAGE SET BY LDO2BV1</b> | <b>HOLD CURRENT VOLTAGE</b>          | <b>NOT USED</b>          | <b>HOLD CURRENT VOLTAGE</b>          | <b>SELECT VOLTAGE SET BY SM0V1</b> | <b>HOLD CURRENT VOLTAGE</b>        | <b>SELECT VOLTAGE SET BY SM1V1</b> | <b>HOLD CURRENT VOLTAGE</b>        |
| When 1           | SELECT VOLTAGE SET BY LDO2BV2        | RAMP TO VOLTAGE SELECTED BY LDO2BVS1 | NOT USED                 | RAMP TO VOLTAGE SELECTED BY LDO2BVS1 | SELECT VOLTAGE SET BY SM0V2        | RAMP TO VOLTAGE SELECTED BY SM0VS2 | SELECT VOLTAGE SET BY SM1V2        | RAMP TO VOLTAGE SELECTED BY SM1VS2 |

**Table 3-20. SM0 and SM1 Voltage Selection Register Settings**

| SM0 OUTPUT VOLTAGE SELECTION |        |   | SM1 OUTPUT VOLTAGE SELECTION |        |   |
|------------------------------|--------|---|------------------------------|--------|---|
| SM0VS1                       | SM0VS2 | SM0GO1=1 OR SM0GO2=1 STARTS VOLTAGE TRANSITION TO VALUE SET BY REGISTER : | SM1VS1                       | SM1VS2 | SM1GO1=1 OR SM1GO2=1 STARTS VOLTAGE TRANSITION TO VALUE SET BY REGISTER |
| 0                            | 0      | SM0V1   | 0                            | 0      | SM1V1   |
| 0                            | 1      | SM0V2   | 0                            | 1      | SM1V2   |

**Table 3-20. SM0 and SM1 Voltage Selection Register Settings (continued)**

| SM0 OUTPUT VOLTAGE SELECTION |   |       | SM1 OUTPUT VOLTAGE SELECTION |   |       |
|------------------------------|---|-------|------------------------------|---|-------|
| 1                            | 0 | SM0V2 | 1                            | 0 | SM1V2 |
| 1                            | 1 | SM0V2 | 1                            | 1 | SM1V2 |

**Table 3-21. SM0 Voltage Selection by SM0EN**

| SM0 ACTIVE LEVEL | SM0EN | SM0 OUTPUT VOLTAGE |
|------------------|-------|--------------------|
| 0                | 0     | 1.2V               |
| 0                | 1     | OFF                |

The SM0 output voltage value and transition is controlled by the SM0EN pin and SM0VS1/SMVS2.

**NOTE**

During a HI to LO transition of SM0EN (enabling SM0), the SM0 output will power up to the pre-defined default state regardless of the setting set via I<sup>2</sup>C prior to SM0 being disabled.

**Table 3-22. SM0 Output Voltage Settings Available for SM0EN Selection**

| RANGE               | [4:0] | VOUT (V) | [4:0] | VOUT (V) | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) |
|---------------------|-------|----------|-------|----------|--------------|--------------|-------|----------|
| <b>0.725V–1.50V</b> | 00000 | 0.725    | 01000 | 0.925    | 10000        | 1.125        | 11000 | 1.325    |
|                     | 00001 | 0.750    | 01001 | 0.950    | 10001        | 1.150        | 11001 | 1.350    |
|                     | 00010 | 0.775    | 01010 | 0.975    | 10010        | 1.175        | 11010 | 1.375    |
|                     | 00011 | 0.800    | 01011 | 1.000    | <b>10011</b> | <b>1.200</b> | 11011 | 1.400    |
|                     | 00100 | 0.825    | 01100 | 1.025    | 10100        | 1.225        | 11100 | 1.425    |
|                     | 00101 | 0.850    | 01101 | 1.050    | 10101        | 1.250        | 11101 | 1.450    |
|                     | 00110 | 0.875    | 01110 | 1.075    | 10110        | 1.275        | 11110 | 1.475    |
|                     | 00111 | 0.900    | 01111 | 1.100    | 10111        | 1.300        | 11111 | 1.500    |

**Table 3-23. LDO4 Voltage Selection Register Settings**

| LDO4 OUTPUT VOLTAGE SELECTION |   |
|-------------------------------|---|
| LDO4VS                        | LDO4GO=1 STARTS VOLTAGE TRANSITION TO VALUE SET BY REGISTER |
| 0                             | LDO4V1  |
| 1                             | LDO4V2  |

The LDO2 output voltage selection and GO bit functionality is shown below.

1. LDO2AGOn bits are not active
2. LDO2BGO1=1 starts a voltage transition to the voltage selected by LDO2BV1, LDO2BV2 and LDO2BVS1
3. LDO2 voltage transition starts when SM0EN is set to LO

When the LDO2 output voltage is controlled by the SM0EN ( $\overline{\text{CORECTRL}}$ ) pin, registers LDO2AV2 and LDO2AV1 define the output voltage:

### 3.54.4 DVM Supply Voltage Transition

During a voltage transition the output voltage will be stepped from the currently programmed voltage to the new target voltage as shown below. The slew rate from the initial voltage to the final voltage for SM0 and SM1 can be selected using the I<sup>2</sup>C registers SM0SL (ADDRESS = 0x25) and SM1SL (ADDRESS = 0x28) respectively. LDO2 and LDO4 have the slew rate fixed internally to 7mV/μSec(typ).

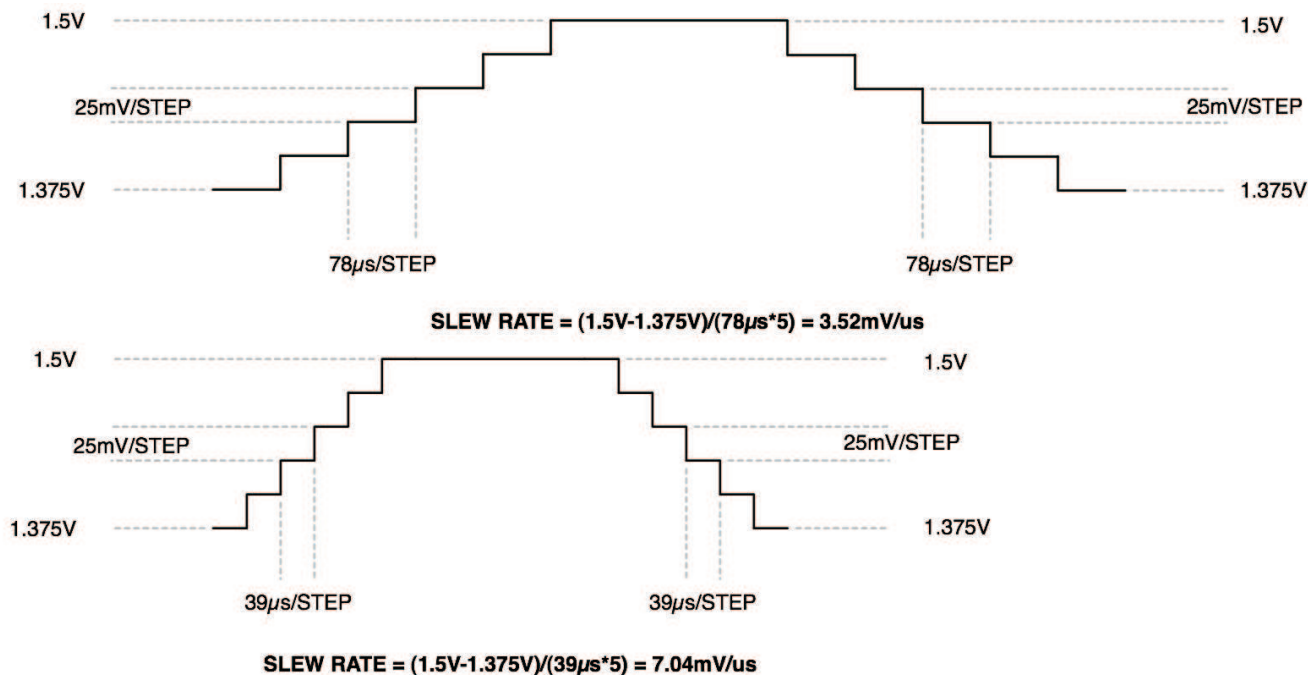


Figure 3-15. SM0 and SM1 Dynamic Voltage Slew Rate Example

## 3.55 SM0, SM1, SM2 CONVERTERS

The TPS658621A has three highly efficient step down synchronous converters. The integration of the power stage switching FETs reduces the external component count, and only the external output inductor and filter capacitor are required. The integrated power stage supports 100% duty cycle operation. The converters have two possible modes of operation: a 2.25MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy loads, and a pulse frequency modulation (PFM) mode at light loads. The converters SM0, SM1 and SM2 output voltages are programmable via I<sup>2</sup>C registers SMnV1 and SMnV2 (SM0 and SM1) and SUPPLYV2 (SM2):

### NOTE

VIN\_SM0, VIN\_SM1 AND VIN\_SM2 PINS SHOULD ALWAYS BE EXTERNALLY CONNECTED TO SYS PIN

### 3.55.1 SM0, SM1 DVM Buck Converters - Output Voltage Registers

Table 3-24. DVM Supply Voltage and Slew Rate Selection – SM0 and SM1

| SM1V1 [Addr 0x23] |          |          |          |                           |          |          |          |          |
|-------------------|----------|----------|----------|---------------------------|----------|----------|----------|----------|
| Bit Number        | B7       | B6       | B5       | B4                        | B3       | B2       | B1       | B0       |
| Bit Name          | RSVD237  | RSVD236  | RSVD235  | SM1V1[4]                  | SM1V1[3] | SM1V1[2] | SM1V1[1] | SM1V1[0] |
| Function          | NOT USED | NOT USED | NOT USED | SM1 SUPPLY OUTPUT VOLTAGE |          |          |          |          |
| SM1V2 [Addr 0x24] |          |          |          |                           |          |          |          |          |
| Bit Number        | B7       | B6       | B5       | B4                        | B3       | B2       | B1       | B0       |

**Table 3-24. DVM Supply Voltage and Slew Rate Selection – SM0 and SM1 (continued)**

|                   |          |          |          |                           |          |                      |          |          |
|-------------------|----------|----------|----------|---------------------------|----------|----------------------|----------|----------|
| Bit Name          | RSVD247  | RSVD246  | RSVD245  | SM1V2[4]                  | SM1V2[3] | SM1V2[2]             | SM1V2[1] | SM1V2[0] |
| Function          | NOT USED | NOT USED | NOT USED | SM1 SUPPLY OUTPUT VOLTAGE |          |                      |          |          |
| SM1SL [Addr 0x25] |          |          |          |                           |          |                      |          |          |
| Bit Number        | B7       | B6       | B5       | B4                        | B3       | B2                   | B1       | B0       |
| Bit Name          | RSVD257  | RSVD256  | RSVD255  | RSVD254                   | RSVD253  | SM1SL[2]             | SM1SL[1] | SM1SL[0] |
| Function          | NOT USED | NOT USED | NOT USED | NOT USED                  | NOT USED | SM1 SUPPLY RAMP RATE |          |          |
| SM0V1 [Addr 0x26] |          |          |          |                           |          |                      |          |          |
| Bit Number        | B7       | B6       | B5       | B4                        | B3       | B2                   | B1       | B0       |
| Bit Name          | RSVD267  | RSVD266  | RSVD265  | SM0V1[4]                  | SM0V1[3] | SM0V1[2]             | SM0V1[1] | SM0V1[0] |
| Function          | NOT USED | NOT USED | NOT USED | SM0 SUPPLY OUTPUT VOLTAGE |          |                      |          |          |
| SM0V2 [Addr 0x27] |          |          |          |                           |          |                      |          |          |
| Bit Number        | B7       | B6       | B5       | B4                        | B3       | B2                   | B1       | B0       |
| Bit Name          | RSVD277  | RSVD276  | RSVD275  | SM0V2[4]                  | SM0V2[3] | SM0V2[2]             | SM0V2[1] | SM0V2[0] |
| Function          | NOT USED | NOT USED | NOT USED | SM0 SUPPLY OUTPUT VOLTAGE |          |                      |          |          |
| SM0SL [Addr 0x28] |          |          |          |                           |          |                      |          |          |
| Bit Number        | B7       | B6       | B5       | B4                        | B3       | B2                   | B1       | B0       |
| Bit Name          | RSVD287  | RSVD286  | RSVD285  | RSVD284                   | RSVD283  | SM0SL[2]             | SM0SL[1] | SM0SL[0] |
| Function          | NOT USED | NOT USED | NOT USED | NOT USED                  | NOT USED | SM0 SUPPLY RAMP RATE |          |          |

The available output voltages and slew rates are shown below.

**Table 3-25. SM0V1[4:0] / SM0V2[4:0] / Output Voltage Settings**

| RANGE               | [4:0] | VOUT (V) | [4:0] | VOUT (V) | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) |
|---------------------|-------|----------|-------|----------|--------------|--------------|-------|----------|
| <b>0.725V–1.50V</b> | 00000 | 0.725    | 01000 | 0.925    | 10000        | 1.125        | 11000 | 1.325    |
|                     | 00001 | 0.750    | 01001 | 0.950    | 10001        | 1.150        | 11001 | 1.350    |
|                     | 00010 | 0.775    | 01010 | 0.975    | 10010        | 1.175        | 11010 | 1.375    |
|                     | 00011 | 0.800    | 01011 | 1.000    | <b>10011</b> | <b>1.200</b> | 11011 | 1.400    |
|                     | 00100 | 0.825    | 01100 | 1.025    | 10100        | 1.225        | 11100 | 1.425    |
|                     | 00101 | 0.850    | 01101 | 1.050    | 10101        | 1.250        | 11101 | 1.450    |
|                     | 00110 | 0.875    | 01110 | 1.075    | 10110        | 1.275        | 11110 | 1.475    |
|                     | 00111 | 0.900    | 01111 | 1.100    | 10111        | 1.300        | 11111 | 1.500    |

**Table 3-26. SM1V1[4:0] / SM1V2[4:0] Output Voltage Settings**

| RANGE               | [4:0] | VOUT (V) | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) | [4:0] | VOUT (V) |
|---------------------|-------|----------|--------------|--------------|-------|----------|-------|----------|
| <b>0.725V–1.50V</b> | 00000 | 0.725    | 01000        | 0.925        | 10000 | 1.125    | 11000 | 1.325    |
|                     | 00001 | 0.750    | 01001        | 0.950        | 10001 | 1.150    | 11001 | 1.350    |
|                     | 00010 | 0.775    | 01010        | 0.975        | 10010 | 1.175    | 11010 | 1.375    |
|                     | 00011 | 0.800    | <b>01011</b> | <b>1.000</b> | 10011 | 1.200    | 11011 | 1.400    |
|                     | 00100 | 0.825    | 01100        | 1.025        | 10100 | 1.225    | 11100 | 1.425    |
|                     | 00101 | 0.850    | 01101        | 1.050        | 10101 | 1.250    | 11101 | 1.450    |
|                     | 00110 | 0.875    | 01110        | 1.075        | 10110 | 1.275    | 11110 | 1.475    |
|                     | 00111 | 0.900    | 01111        | 1.100        | 10111 | 1.300    | 11111 | 1.500    |

**Table 3-27. SM0SL[2:0] and SM1SL[2:0] Slew Rate Settings**

| SMxSL [2:0] | SLEW RATE (mV/μs) | SMxSL [2:0] | SLEW RATE (mV/μs) | SMxSL [2:0] | SLEW RATE (mV/μs) | SMxSL [2:0] | SLEW RATE (mV/μs) |
|-------------|-------------------|-------------|-------------------|-------------|-------------------|-------------|-------------------|
| 000         | INSTANTLY         | 001         | 0.11              | 010         | 0.22              | 011         | 0.44              |

**Table 3-27. SM0SL[2:0] and SM1SL[2:0] Slew Rate Settings (continued)**

| SMxSL<br>[2:0] | SLEW RATE<br>(mV/μs) | SMxSL<br>[2:0] | SLEW RATE<br>(mV/μs) | SMxSL<br>[2:0] | SLEW RATE<br>(mV/μs) | SMxSL<br>[2:0] | SLEW RATE<br>(mV/μs) |
|----------------|----------------------|----------------|----------------------|----------------|----------------------|----------------|----------------------|
| 100            | 0.88                 | 101            | 1.76                 | 110            | 3.52                 | 111            | 7.04                 |

**Table 3-28. Non-DVM supply Voltage selection - SM2, LDO8**

| SUPPLYV2 [Addr 0x42] |                     |          |          |                    |         |         |         |         |
|----------------------|---------------------|----------|----------|--------------------|---------|---------|---------|---------|
| Bit Number           | B7                  | B6       | B5       | B4                 | B3      | B2      | B1      | B0      |
| Bit Name             | VLDO8[2]            | VLDO8[1] | VLDO8[0] | VSM2[4]            | VSM2[3] | VSM2[2] | VSM2[1] | VSM2[0] |
| Function             | LDO8 OUTPUT VOLTAGE |          |          | SM2 OUTPUT VOLTAGE |         |         |         |         |

**Table 3-29. VSM2[4:0] Output Voltage Settings**

| RANGE             | [4:0] | VOUT (V) | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) | [4:0] | VOUT (V) |
|-------------------|-------|----------|--------------|--------------|-------|----------|-------|----------|
| <b>3.0V–4.55V</b> | 00000 | 3.000    | 01000        | 3.400        | 10000 | 3.800    | 11000 | 4.200    |
|                   | 00001 | 3.050    | 01001        | 3.450        | 10001 | 3.850    | 11001 | 4.250    |
|                   | 00010 | 3.100    | 01010        | 3.500        | 10010 | 3.900    | 11010 | 4.300    |
|                   | 00011 | 3.150    | 01011        | 3.550        | 10011 | 3.950    | 11011 | 4.350    |
|                   | 00100 | 3.200    | 01100        | 3.600        | 10100 | 4.000    | 11100 | 4.400    |
|                   | 00101 | 3.250    | 01101        | 3.650        | 10101 | 4.050    | 11101 | 4.450    |
|                   | 00110 | 3.300    | <b>01110</b> | <b>3.700</b> | 10110 | 4.100    | 11110 | 4.500    |
|                   | 00111 | 3.350    | 01111        | 3.750        | 10111 | 4.150    | 11111 | 4.550    |

### 3.55.2 PWM Operation

During PWM operation the converters use a fast response voltage mode controller scheme with input voltage feed-forward, enabling the use of small ceramic input and output capacitors. At the beginning of each clock cycle the high side channel MOSFET switch is turned on, and the oscillator starts the voltage ramp. The inductor current will ramp-up until the ramp voltage reaches the error amplifier output voltage, when the comparator trips and the high-side channel MOSFET switch is turned off. Internal adaptive break-before-make circuits turn on the integrated low-side MOSFET switch after an internal, fixed dead-time delay, and the inductor current ramps down, until the next cycle is started. When the next cycle starts the ramp voltage is reset to its low value and the high-side channel MOSFET switch is turned on again.

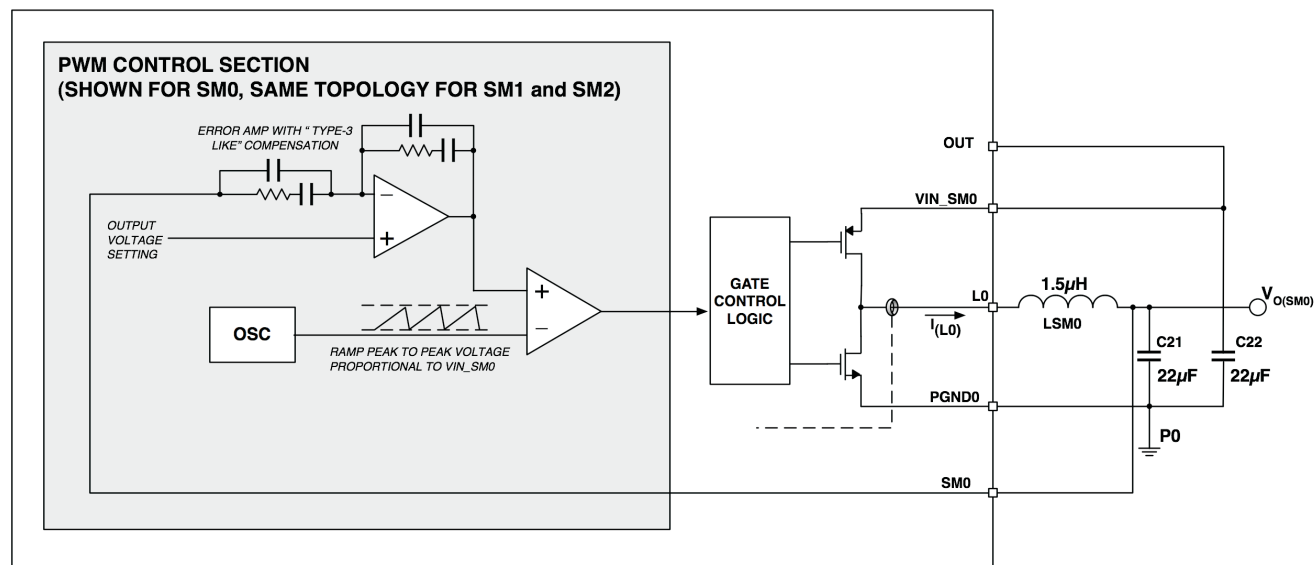


Figure 3-16. PWM Control

### 3.55.3 PFM Mode Operation

The TPS658621A SM0, SM1 and SM2 buck converters can be set to operate only in PWM mode or to switch automatically between PFM and PWM modes, via the I<sup>2</sup>C interface. While in the Pulsed Frequency Mode the converters operate with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

In PFM mode the converter will regulate the output voltage to 1% above the nominal output voltage. To determine when to transition between the modes, the inductor current is monitored, and the PFM mode is set when the inductor ripple current approaches zero. For duty cycles above 85% the PFM mode is entered for load currents below the threshold  $I_{PFM(ENTER)}$ .

$$I_{PFM(ENTER)} = \frac{V_{(VIN\_SMx)}}{34\Omega} \quad (4)$$

In PFM mode the output voltage is monitored by a voltage comparator, which regulates the output voltage to the programmed value  $V_{O(SM1)}$ . If the output voltage is below  $V_{O(SM1)}$  the PFM control circuit turns on the power stage, applying a burst of pulses to increase the output voltage. When the output voltage exceeds the target regulation voltage  $V_{O(SM1)}$  the power stage is disabled, and the output voltage will drop until it is below the regulation voltage target, when the power stage is enabled again.

The PFM operation is disabled and PWM operation set if one of the following events happens during PFM operation:

1. The burst operation exceeds 7µs, typ.
2. The output voltage falls below 3% of the target regulation voltage in PFM mode (2% of the nominal output voltage in PWM mode)

### 3.55.4 Setting the PWM/PFM Mode

In TPS658621A the PWM mode can be forced for each converter by setting the bit  $SMn\_PWM$  to 1 in the  $SMODE1$  register. If bits  $SMn\_GPIO$  is 1, the GPIO will control the PWM or PFM mode setting, and bits  $SMn\_PWM$  are ignored.

**Table 3-30. SM0,SM1, SM2 PWM/PFM Mode Selection**

| SMODE1 [Addr 0x47] |         |                                |                                |                                |         |                 |                 | Default to 0    |
|--------------------|---------|--------------------------------|--------------------------------|--------------------------------|---------|-----------------|-----------------|-----------------|
| Bit Number         | B7      | B6                             | B5                             | B4                             | B3      | B2              | B1              | B0              |
| Bit Name           | RSVD477 | SM2_GPIO                       | SM1_GPIO                       | SM0_GPIO                       | RSVD473 | SM2_PWM         | SM1_PWM         | SM0_PWM         |
| Function           | SPARE   | SM2 AUTO PFM CONTROL SELECTION | SM1 AUTO PFM CONTROL SELECTION | SM0 AUTO PFM CONTROL SELECTION | SPARE   | SM2 PWM MODE ON | SM1 PWM MODE ON | SM0 PWM MODE ON |

Table 3-31 details how the GPIO control is implemented. Note that the GPIO1 polarity indicated in Table 3-31 is controlled by bit GPIOINV, register 0x5E.

**Table 3-31. GPIO1 PWM/PFM Mode Control**

| SMx_GPIO | SMx_PWM | GPIO1 POLARITY | GPIO1 | CONVERTER MODE |
|----------|---------|----------------|-------|----------------|
| 0        | 0       | x              | x     | Auto PWM/PFM   |
| 0        | 1       | x              | x     | PWM Only       |
| 1        | x       | Inverted       | 0     | PWM Only       |
| 1        | x       | Inverted       | 1     | Auto PWM/PFM   |
| 1        | x       | Not Inverted   | 0     | Auto PWM/PFM   |
| 1        | x       | Not Inverted   | 1     | PWM Only       |

### 3.55.5 Output Discharge Switches

When the SM0, SM1 and SM2 converters are disabled, an integrated switch automatically discharges the converter output capacitor.

The converter output discharge switches are always enabled when NORMAL state is set and during the SUPPLYSEQ state.

### 3.55.6 Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It provides more headroom for both the voltage drop at a load step and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage will drop until it reaches the COMP LOW threshold set to 2% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the low-side channel switch.

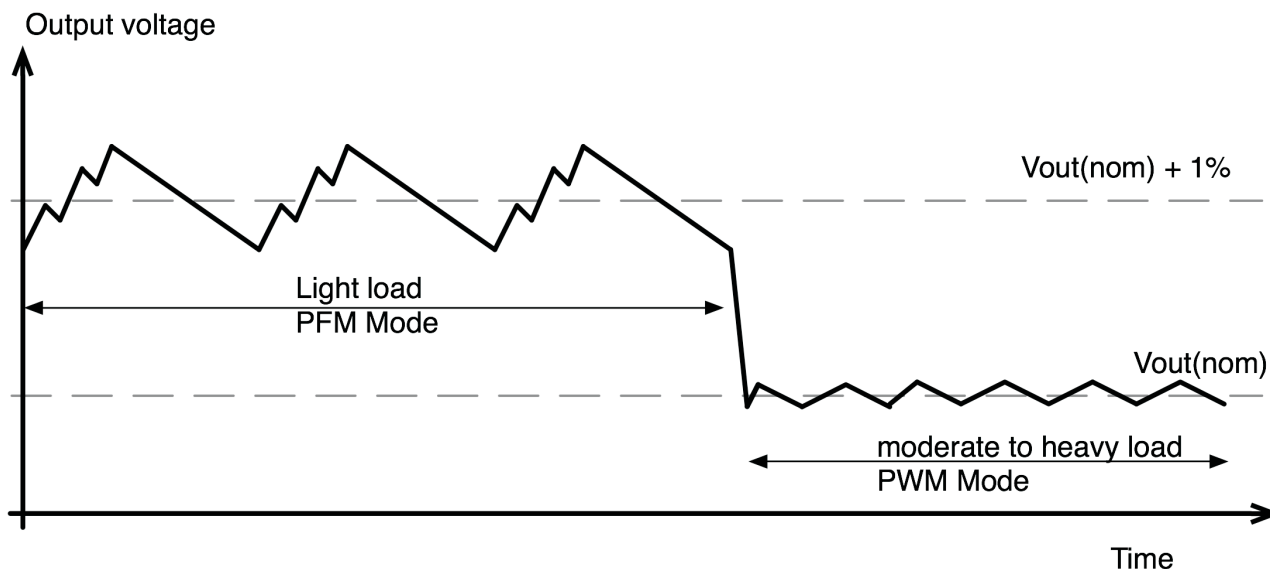


Figure 3-17. Voltage Positioning

### 3.55.7 Soft Start

SM0, SM1 and SM2 have an internal soft start circuit that limits the inrush current during start-up. An initial delay (170µs typ) from the converter enabled command to the converter effectively being operational is required to ensure that the internal circuits of the converter are properly biased. At the end of that initial delay the soft start is initiated and the internal compensation capacitor is charged with a low value current source. The soft start time is typically 250µs, with the output voltage ramping from 5% to 95% of the final target value.

### 3.55.8 Dropout Operation at 100% Duty Cycle

The TPS658621A buck converters offer a low input to output voltage difference while still maintaining operation when the duty cycle is set to 100%. In this mode of operation the high-side FET is constantly turned on to enable operation with a low input voltage. The dropout operation will start if :

$$V_{(VIN\_SMx)} \leq V_{(SMx)} + I_{Lx} \times R_{DS(on)(PSMx)} + R_L$$

where  $I_{Lx}$  is the output current plus ½ inductor ripple current and  $R_L$  is the DC resistance of the inductor.

### 3.55.9 Output Voltage Monitoring

The output voltage of converters SM0, SM1 and SM2 is monitored by internal comparators, and an output low voltage condition is detected when the output voltage is below 90% of the programmed value. The power good comparator is disabled for all converters during output voltage transitions. The power good comparator on SM2 power good is also disabled when battery tracking mode is set.

### 3.55.10 Phase Control in PWM Mode

By default the SM0, SM1 and SM2 converters operate with phased clocking when they are in PWM mode, with converter SM0 as the master. Converters SM0 and SM1, when enabled, will run 90 and 180 degrees out of phase with SM0.

### 3.55.11 Integrated Snubber and Current Limit

The SM2 converter has an integrated electronic snubber that is used to improve transient response when operating under conditions which cause the inductor current to flow in the negative direction (into the  $L_n$  node) . This is especially true when SM2 is configured as the pre-regulator stage to the charger.



### 3.56 LINEAR REGULATORS

The TPS658621A offers ten integrated linear dropout regulators (LDOs), designed to be stable over the operating load range with use of external ceramic capacitors. The output voltage can be programmed via I<sup>2</sup>C. All of the LDOs, with the exception of LDO5 and RTC\_OUT LDO, have uncommitted input power supply pins (VIN\_LDO01, VIN\_LDO23, VIN\_LDO4, VIN\_LDO678, VIN\_LDO9) which should be externally connected to a number of system rails including SYS and the output of SM2.

The LDO5 and RTC\_OUT regulators are internally connected to the SYS pin.

#### 3.56.1 Output Voltage Monitoring

Internal power good comparators monitor the LDO outputs and detect when the output voltage is below 95% of the programmed value. This information is used by the TPS658621A to generate interrupts or to trigger distinct operating modes, depending on specific I<sup>2</sup>C register settings. See interrupt and sequencing controller section for additional details.

#### 3.56.2 LDO2 DVM LDO - Output Voltage Registers

Registers 0x29, 0x2A, 0x2F and 0x30 set the output voltage for LDO2. The slew rate is internally fixed to 7mV/μSec (typ).

**Table 3-32. DVM Supply Voltage Selection – LDO2**

| LDO2AV1 [Addr 0x29] |                 |                 |                 |  |            |            |            | Defaults in <b>BOLD</b> |
|---------------------|-----------------|-----------------|-----------------|--|------------|------------|------------|-------------------------|
| Bit Number          | B7              | B6              | B5              | B4   | B3         | B2         | B1         | B0                      |
| Bit Name            | RSVD297         | RSVD296         | RSVD295         | LDO2AV1[4]   | LDO2AV1[3] | LDO2AV1[2] | LDO2AV1[1] | LDO2AV1[0]              |
| Function            | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | LDO2 SUPPLY OUTPUT VOLTAGE (See <a href="#">Table 3-33</a> ) |            |            |            |                         |
| SM1V2 [Addr 0x24]   |                 |                 |                 |  |            |            |            | Defaults in <b>BOLD</b> |
| Bit Number          | B7              | B6              | B5              | B4   | B3         | B2         | B1         | B0                      |
| Bit Name            | RSVD2A7         | RSVD2A6         | RSVD2A5         | LDO2AV2[4]   | LDO2AV2[3] | LDO2AV2[2] | LDO2AV2[1] | LDO2AV2[0]              |
| Function            | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | LDO2 SUPPLY OUTPUT VOLTAGE (See <a href="#">Table 3-33</a> ) |            |            |            |                         |
| LDO2BV1 [Addr 0x2F] |                 |                 |                 |  |            |            |            | Defaults in <b>BOLD</b> |
| Bit Number          | B7              | B6              | B5              | B4   | B3         | B2         | B1         | B0                      |
| Bit Name            | RSVD2F7         | RSVD2F6         | RSVD2F5         | LDO2BV1[4]   | LDO2BV1[3] | LDO2BV1[2] | LDO2BV1[1] | LDO2BV1[0]              |
| Function            | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | LDO2 SUPPLY OUTPUT VOLTAGE (See <a href="#">Table 3-33</a> ) |            |            |            |                         |
| LDO2BV2 [Addr 0x30] |                 |                 |                 |  |            |            |            | Defaults in <b>BOLD</b> |
| Bit Number          | B7              | B6              | B5              | B4   | B3         | B2         | B1         | B0                      |
| Bit Name            | RSVD307         | RSVD306         | RSVD305         | LDO2BV2[4]   | LDO2BV2[3] | LDO2BV2[2] | LDO2BV2[1] | LDO2BV2[0]              |
| Function            | <b>NOT USED</b> | <b>NOT USED</b> | <b>NOT USED</b> | LDO2 SUPPLY OUTPUT VOLTAGE (See <a href="#">Table 3-33</a> ) |            |            |            |                         |

The available output voltages for LDO2 are shown below:

**Table 3-33. LDO2AV1/2[4:0] and LDO2BV1/2[4:0] Settings**

| RANGE               | [4:0] | VOUT (V) | [4:0] | VOUT (V) | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) |
|---------------------|-------|----------|-------|----------|--------------|--------------|-------|----------|
| <b>0.725V–1.50V</b> | 00000 | 0.725    | 01000 | 0.925    | 10000        | 1.125        | 11000 | 1.325    |
|                     | 00001 | 0.750    | 01001 | 0.950    | 10001        | 1.150        | 11001 | 1.350    |
|                     | 00010 | 0.775    | 01010 | 0.975    | 10010        | 1.175        | 11010 | 1.375    |
|                     | 00011 | 0.800    | 01011 | 1.000    | <b>10011</b> | <b>1.200</b> | 11011 | 1.400    |
|                     | 00100 | 0.825    | 01100 | 1.025    | 10100        | 1.225        | 11100 | 1.425    |
|                     | 00101 | 0.850    | 01101 | 1.050    | 10101        | 1.250        | 11101 | 1.450    |
|                     | 00110 | 0.875    | 01110 | 1.075    | 10110        | 1.275        | 11110 | 1.475    |
|                     | 00111 | 0.900    | 01111 | 1.100    | 10111        | 1.300        | 11111 | 1.500    |

### 3.56.3 LDO4 DVM LDO – Output Voltage Registers

Registers 0x32 and 0x33 set the output voltage for LDO4. The slew rate is internally fixed to 7mV/μSec (typ).

**Table 3-34. DVM Supply Voltage Selection – LDO4**

| LDO4V1 [Addr 0x32] |          |          |          |  |           |           |           |           |
|--------------------|----------|----------|----------|--|-----------|-----------|-----------|-----------|
| Bit Number         | B7       | B6       | B5       | B4   | B3        | B2        | B1        | B0        |
| Bit Name           | RSVD327  | RSVD326  | RSVD325  | LDO4V1[4]  | LDO4V1[3] | LDO4V1[2] | LDO4V1[1] | LDO4V1[0] |
| Function           | NOT USED | NOT USED | NOT USED | LDO4 SUPPLY OUTPUT VOLTAGE (See <a href="#">Table 3-35</a> ) |           |           |           |           |
| LDO4V2 [Addr 0x33] |          |          |          |  |           |           |           |           |
| Bit Number         | B7       | B6       | B5       | B4   | B3        | B2        | B1        | B0        |
| Bit Name           | RSVD337  | RSVD336  | RSVD335  | LDO4V2[4]  | LDO4V2[3] | LDO4V2[2] | LDO4V2[1] | LDO4V2[0] |
| Function           | NOT USED | NOT USED | NOT USED | LDO4 SUPPLY OUTPUT VOLTAGE (See <a href="#">Table 3-35</a> ) |           |           |           |           |

The available output voltages are shown below:

**Table 3-35. LDO4V1[4:0] and LDO4V2[4:0] Output Voltage Settings**

| RANGE       | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) | [4:0] | VOUT (V) | [4:0] | VOUT (V) |
|-------------|--------------|--------------|-------|----------|-------|----------|-------|----------|
| 1.7V–2.475V | 00000        | 1.700        | 01000 | 1.900    | 10000 | 2.100    | 11000 | 2.300    |
|             | 00001        | 1.725        | 01001 | 1.925    | 10001 | 2.125    | 11001 | 2.325    |
|             | 00010        | 1.750        | 01010 | 1.950    | 10010 | 2.150    | 11010 | 2.350    |
|             | 00011        | 1.775        | 01011 | 1.975    | 10011 | 2.175    | 11011 | 2.375    |
|             | <b>00100</b> | <b>1.800</b> | 01100 | 2.000    | 10100 | 2.200    | 11100 | 2.400    |
|             | 00101        | 1.825        | 01101 | 2.025    | 10101 | 2.225    | 11101 | 2.425    |
|             | 00110        | 1.850        | 01110 | 2.050    | 10110 | 2.250    | 11110 | 2.450    |
|             | 00111        | 1.875        | 01111 | 2.075    | 10111 | 2.275    | 11111 | 2.475    |

### 3.56.4 LDO Output Discharge Switches

All LDO's, with exception of RTC\_OUT LDO, have internal discharge resistors that are connected to ground via internal switches when the LDO is turned OFF, thus discharging the output capacitor.

The LDO output discharge switches are always enabled when NORMAL state is set and during the SUPPLYSEQ state.

### 3.56.5 Non-DVM Supply Voltage Settings

Registers SUPPLYV1, SUPPLYV2, SUPPLYV3, SUPPLYV4 and SUPPLYV6 define the voltage settings for the non-DVM supplies.

Register SUPPLYV4 has two bits that control the RTC\_OUT LDO functionality. The RTC\_OUT LDO will be enabled when LDORTC\_ON is 1. The power good threshold for the RTC\_OUT LDO can be set as follows: 2.4V (RTC\_PGOOD is 1), 2.0V (RTC\_PGOOD is 0).

**Table 3-36. Non-DVM Supply Voltage Selection**

| SUPPLYV1 [Addr 0x41] |   |          |   |   |          |   |          |          |
|----------------------|---|----------|---|---|----------|---|----------|----------|
| Bit Name             | VLDO0[2]  | VLDO0[1] | VLDO0[0]  | VLDO1[4]  | VLDO1[3] | VLDO1[2]  | VLDO1[1] | VLDO1[0] |
| Function             | LDO0 OUTPUT VOLTAGE (See <a href="#">Table 3-38</a> ) |          |   | LDO1 OUTPUT VOLTAGE (See <a href="#">Table 3-37</a> ) |          |   |          |          |
|                      |   |          |   |   |          |   |          |          |
| SUPPLYV3 [Addr 0x43] |   |          |   |   |          |   |          |          |
| Bit Name             | LDO7_SW   | LDO6_SW  | VLDO7[2]  | VLDO7[1]  | VLDO7[0] | VLDO6[2]  | VLDO6[1] | VLDO6[0] |
| Function             | SPARE   | SPARE    | LDO7 OUTPUT VOLTAGE (See <a href="#">Table 3-38</a> ) |   |          | LDO6 OUTPUT VOLTAGE (See <a href="#">Table 3-38</a> ) |          |          |

**Table 3-36. Non-DVM Supply Voltage Selection (continued)**

| SUPPLYV4 [Addr 0x44] |                        |                               |                                     |         |         |                                      |          |          |
|----------------------|------------------------|-------------------------------|-------------------------------------|---------|---------|--------------------------------------|----------|----------|
| Bit Name             | LDORTC_ON              | RTC_PGOOD                     | VRTC[2]                             | VRTC[1] | VRTC[0] | VLDO3[2]                             | VLDO3[1] | VLDO3[0] |
| Function             | RTC_LDO ON/OFF CONTROL | RTC_OUT LOW VOLTAGE THRESHOLD | RTC OUTPUT VOLTAGE (See Table 3-38) |         |         | LDO3 OUTPUT VOLTAGE (See Table 3-38) |          |          |

| SUPPLYV6 [Addr 0x46] |          |          |                                      |          |          |                                      |          |          |
|----------------------|----------|----------|--------------------------------------|----------|----------|--------------------------------------|----------|----------|
| Bit Name             | RSVD467  | RSVD466  | VLDO9[2]                             | VLDO9[1] | VLDO9[0] | VLDO5[2]                             | VLDO5[1] | VLDO5[0] |
| Function             | NOT USED | NOT USED | LDO9 OUTPUT VOLTAGE (See Table 3-38) |          |          | LDO5 OUTPUT VOLTAGE (See Table 3-38) |          |          |

The available output voltages for the non-DVM supplies are shown below:

**Table 3-37. VLDO1[4:0] Settings**

| RANGE               | [4:0] | VOUT (V) | [4:0]        | VOUT (V)     | [4:0] | VOUT (V) | [4:0] | VOUT (V) |
|---------------------|-------|----------|--------------|--------------|-------|----------|-------|----------|
| <b>0.725V–1.50V</b> | 00000 | 0.725    | 01000        | 0.925        | 10000 | 1.125    | 11000 | 1.325    |
|                     | 00001 | 0.750    | 01001        | 0.950        | 10001 | 1.150    | 11001 | 1.350    |
|                     | 00010 | 0.775    | 01010        | 0.975        | 10010 | 1.175    | 11010 | 1.375    |
|                     | 00011 | 0.800    | 01011        | 1.000        | 10011 | 1.200    | 11011 | 1.400    |
|                     | 00100 | 0.825    | 01100        | 1.025        | 10100 | 1.225    | 11100 | 1.425    |
|                     | 00101 | 0.850    | 01101        | 1.050        | 10101 | 1.250    | 11101 | 1.450    |
|                     | 00110 | 0.875    | 01110        | 1.075        | 10110 | 1.275    | 11110 | 1.475    |
|                     | 00111 | 0.900    | <b>01111</b> | <b>1.100</b> | 10111 | 1.300    | 11111 | 1.500    |

**Table 3-38. VLDO3/5/6/7/8/9[2:0] and VRTC[2:0] Settings**

| VLDOx[2:0] | VOUT (V) | VLDOx[2:0] | VOUT (V) |
|------------|----------|------------|----------|
| 000        | 1.25     | 100        | 2.70     |
| 001        | 1.50     | 101        | 2.85     |
| 010        | 1.80     | 110        | 3.10     |
| 011        | 2.50     | 111        | 3.30     |

**Table 3-39. VLDO0[2:0] Settings**

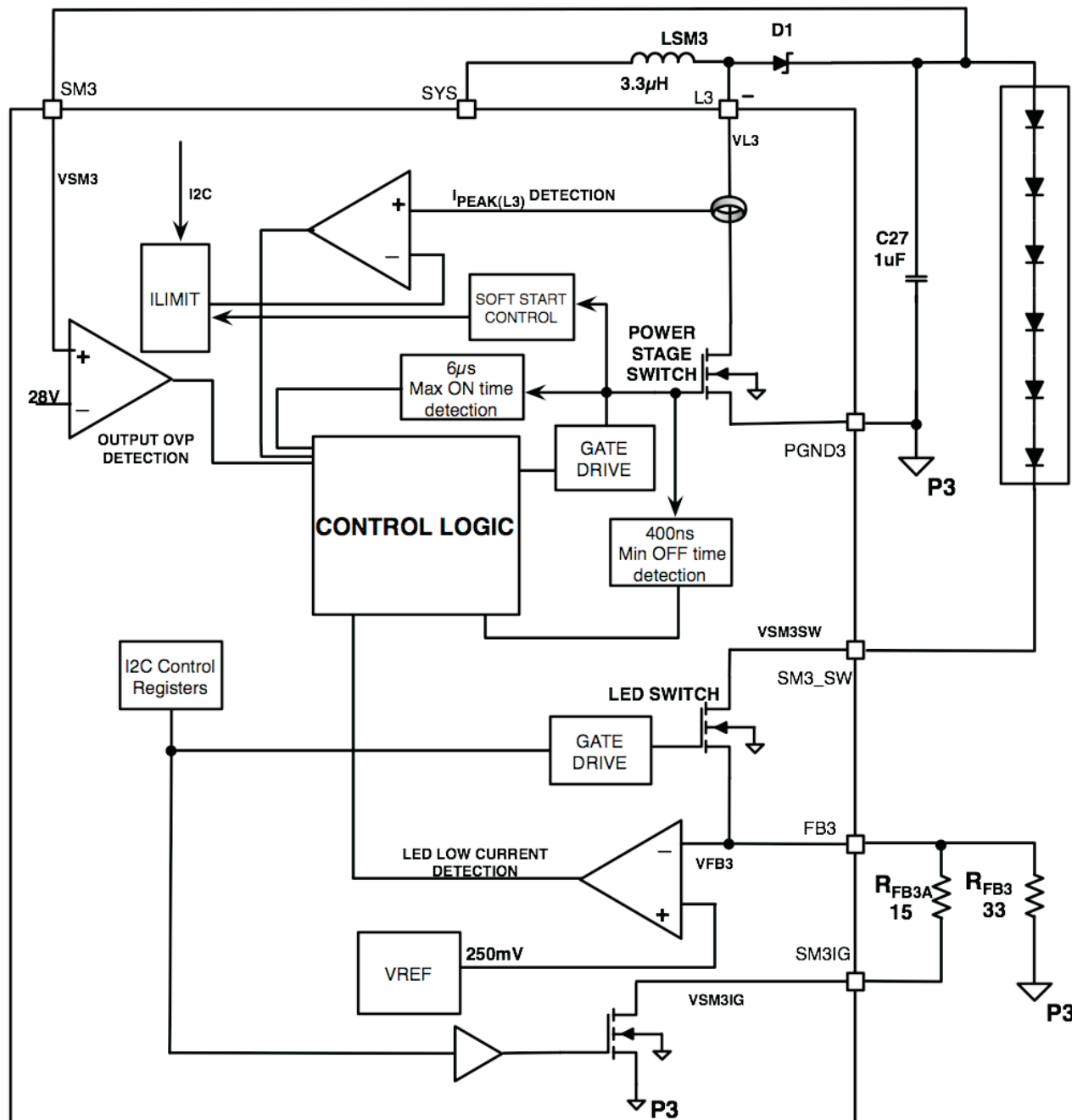
| VLDOx[2:0] | VOUT (V) | VLDOx[2:0] | VOUT (V) |
|------------|----------|------------|----------|
| 000        | 1.20     | 100        | 2.70     |
| 001        | 1.50     | 101        | 2.85     |
| 010        | 1.80     | 110        | 3.10     |
| 011        | 2.50     | 111        | 3.30     |

Setting the RTC\_OUT output voltage below the RTC\_OUT power good threshold will result in a  $\overline{\text{NORTC}}$  pulse always being generated during the reboot cycle or when exiting sleep. Setting the RTC\_OUT output voltage below  $V_{\text{UVLO\_RTC}}$  disables the use of the internal real time clock counter and xtal oscillator.

### 3.57 BOOST CONVERTER

The TPS658621A has an integrated boost converter (SM3) that is optimized to drive white LED's connected in a series configuration. Up to six series white LED's can be driven, with programmable current and duty cycle adjustable via a dedicated I<sup>2</sup>C register.

The SM3 boost Converter (SM3) has a 29V, 500mA low side integrated power stage switch, which drives the external inductor. Another integrated 29V, 25mA switch (LED switch) is used to modulate the external white LED's brightness.



**Figure 3-18. Boost Converter Block Diagram**

The SM3 boost converter operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and enables the use of small external components, as the switching frequency can reach up to 1 MHz depending on the load conditions. The LED current ripple is defined by the external inductor size.

The converter monitors the sense voltage at pin FB3, and turns on the integrated power stage switch when V(FB3) is below the 250mV (typ) internal reference voltage. The integrated power switch turns off when the inductor current reaches the internal peak current limit or if the switch is on for a period longer than the maximum on-time of 6  $\mu$ s (typ).

As the integrated power switch is turned off the external Schottky diode is forward biased, delivering the stored inductor energy to the output. The main switch remains off until the FB3 pin voltage is below the internal 250mV reference voltage, when it is turned on again.

This PFM peak current control sets the converter in discontinuous conduction mode (DCM), and the switching frequency depends on the inductor, input/output voltage and LED current. Lower LED currents reduce the switching frequency, with high efficiency over the entire LED current range. This regulation scheme is inherently stable, allowing a wide range for the selection of the inductor and output capacitor.

### 3.57.1 SM3 RAM Registers

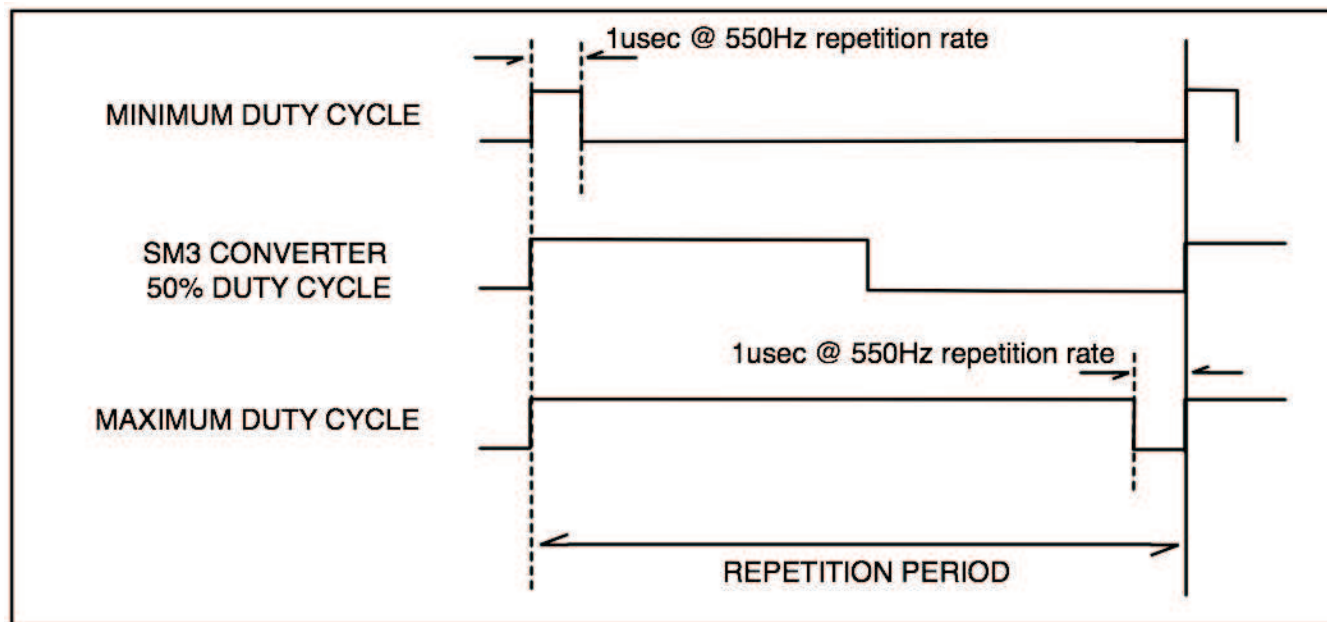
**Table 3-40. SM3 Control**

| <b>SM3_SET0 [Addr 0x57]</b> |                            |                         |   |                                 |                                |                            | Defaults in <b>BOLD</b> |            |
|-----------------------------|----------------------------|-------------------------|---|---------------------------------|--------------------------------|----------------------------|-------------------------|------------|
| Bit Number                  | B7                         | B6                      | B5                                      | B4                              | B3                             | B2                         | B1                      | B0         |
| Bit Name                    | SM3_SET7                   | SM3_SET6                | SM3_SET5                                | SM3_SET4                        | SM3_SET3                       | SM3_SET2                   | SM3_SET1                | SM3_SET0   |
| Function                    | SM3 PWM SWITCH DUTY CYCLE  |                         |   |                                 |                                |                            |                         |            |
| When 0                      | <b>ADD 0 TO DUTY CYCLE</b> |                         |   |                                 |                                |                            |                         |            |
| When 1                      | ADD 6.25%                  | ADD 3.125%              | ADD 1.5625%                             | ADD 0.78125%                    | ADD 0.390%                     | ADD 0.195%                 | ADD 0.0976%             | ADD 0.048% |
| <b>SM3_SET1 [Addr 0x58]</b> |                            |                         |   |                                 |                                |                            | Defaults in <b>BOLD</b> |            |
| Bit Number                  | B7                         | B6                      | B5                                      | B4                              | B3                             | B2                         | B1                      | B0         |
| Bit Name                    | SM3SOFTOFF                 | SM3_ILIM                | SM3_PRESC1                              | SM3_PRESC0                      | SM3_IGAIN                      | SM3_SET10                  | SM3_SET9                | SM3_SET8   |
| Function                    | SOFTSTART<br>ENABLE        | SM3<br>CURRENT<br>LIMIT | SM3PWM<br>REPETITION<br>RATE[1]         | SM3PWM<br>REPETITION<br>RATE[0] | ISM3G<br>OUTPUTBUFF<br>ER MODE | SM3 PWM DUTY CYCLE         |                         |            |
| When 0                      | <b>ENABLED</b>             | <b>300 mA</b>           | <b>SEE SM3 PWM REPETITION<br/>TABLE</b> |                                 | <b>Hi-Z</b>                    | <b>ADD 0 TO DUTY CYCLE</b> |                         |            |
| When 1                      | DISABLED                   | 500 mA                  | SEE SM3 PWM REPETITION<br>TABLE         |                                 | LO                             | ADD 50%                    | ADD 25%                 | ADD 12.5%  |

**Table 3-41. SM3 PWM Repetition Settings**

| SM3PRESC[1] | SM3PRESC[0] | REPETITION RATE (Hz) |
|-------------|-------------|----------------------|
| 0           | 0           | 550                  |
| 0           | 1           | 366                  |
| 1           | 0           | 275                  |
| 1           | 1           | 220                  |

The internal LED switch, in series with the external LED's, disconnects the LEDs from ground during shutdown. In addition, the LED switch is driven by a PWM signal generated internally, enabling adjusting the average LED current by setting the LED switch duty cycle. The duty cycle is adjusted with control bits SM3\_SET, on register SM3\_SET0. With this control method the LED brightness depends on the LED switch duty cycle only and is independent of the boost converter operating frequency. The duty cycle control used in the SM3 converter LED switch is implemented by a single PWM pulse with a fixed repetition rate. An example of distinct duty cycles is shown IN [Figure 3-19](#)



**Figure 3-19. SM3 Duty Cycle Example**

The repetition period can be set using control bits SM3\_PRESCn in the register SM3\_SET1 to either 220/275/366/550 Hz (HI). Each repetition period has a total of 2048 steps, enabling a resolution of 0.05% when programming the duty cycle.

### 3.57.2 Peak Current Control (Boost Converter)

The SM3 integrated power stage switch is turned on until the inductor current reaches the DC current limit  $I_{MAX(L3)}$  (500 mA or 300mA, typ), selectable via bit SM3\_ILIM, register SM3\_SET1. Due to internal delays, typically around 100ns, the actual current exceeds the DC current limit threshold by a small amount. The typical peak current limit can be calculated as follows:

$$I_{P(typ)} = I_{MAX(L3)} + \frac{V_{SM3}}{L} \times 100 \text{ ns} \quad (6)$$

The peak current will be directly proportional to the input voltage and inversely proportional to the inductor value. The internal current limit may be set to either 300mA or 500mA via  $I^2C$ .

Note that under PWM operation the slew rate of the converter output (SM3) is dependent of the  $I_{MAX(L3)}$  value selected.

### 3.57.3 Soft Start

All inductive step-up converters exhibit high in-rush current during start-up. If no special precautions are taken voltage drops can be observed at the input supply rail during start-up, with unpredictable results in the overall system operation.

The SM3 boost converter limits the inrush current during start-up by increasing the current limit in two steps, starting from  $I_{MAX(L3)} / 4$  for 256 power stage switch cycles (1cycle=power stage switch OFF→ON→OFF) to  $I_{MAX(L3)} / 2$  for the next 256 power stage switch cycles and then full current limit  $I_{MAX(L3)}$ . The softstart function can be disabled via control bit SM3SOFTOFF, in register SM3\_SET1.

### 3.57.4 Enabling the SM3 Converter

The converter is enabled when an  $I^2C$  command sets the duty cycle to a value different than zero.

### 3.57.5 Overvoltage Protection

The output voltage of the boost converter is sensed at pin SM3, and the integrated power stage switch is turned OFF when  $V(\text{SM3})$  exceeds the internal over-voltage threshold  $V_{(\text{OVP3})}$ . The converter returns to normal operation when  $V(\text{SM3}) < V_{(\text{OVP3})} - V_{\text{HYS}(\text{OVP3})}$ .

### 3.57.6 Under Voltage Lockout Operation

The power stage mosfet switch and the LED switch are open (off) when the TPS658621A enters the sleep mode or if the SM3 converter is set to OFF mode.

### 3.57.7 SM3 Output Current - High and Low Current Settings

A dedicated, open-drain pin (ISM3G) enables I<sup>2</sup>C selection of a low and high brightness setting for the SM3 output current, by modifying the external FB3 resistor value. See application diagram for details. This pin is configured as an open drain and it can be turned on/off with bit SM3\_IGAIN on register SM3\_SET1.

## 3.58 RGB AND PWM DRIVERS

The TPS658621A has integrated open drain and push-pull drivers with programmable duty cycle and frequency, targeted at driving external RGB drivers, keyboard LED's, vibrator motor and other system peripherals.

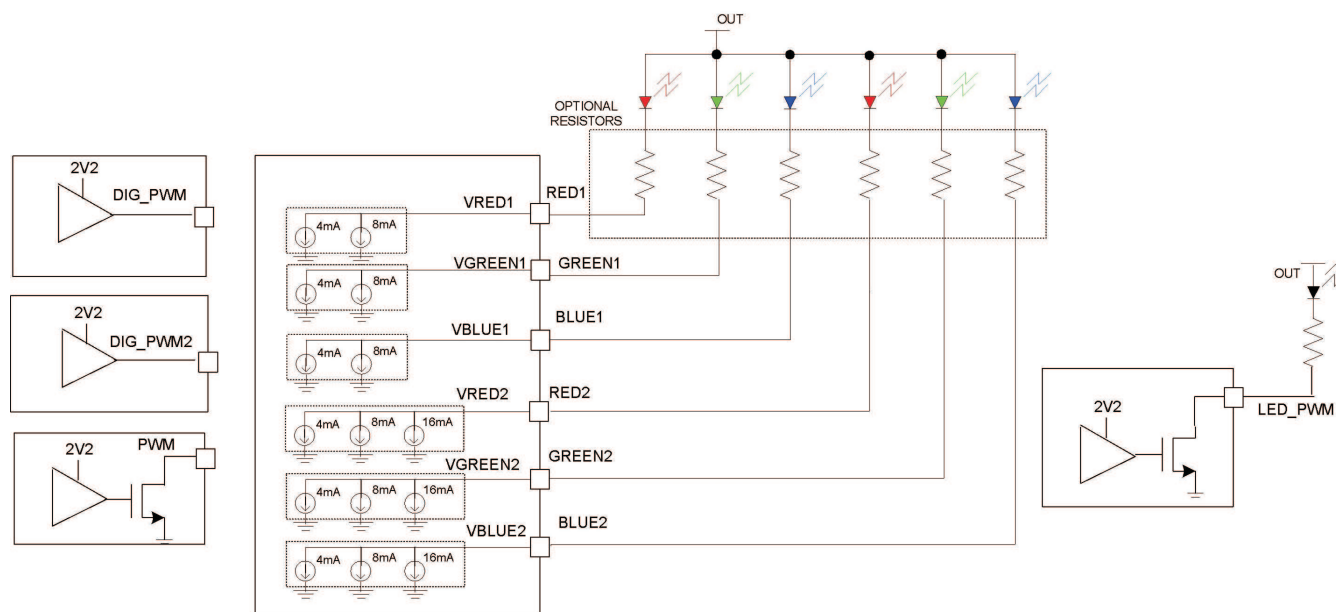


Figure 3-20. RGB and PWM Driver Blocks

### 3.58.1 PWM Pin Driver

The TPS658621A offers one high current (150mA max) open-drain PWM driver. The PWM driver is enabled when PWM\_EN is 1 in register PWM.

Table 3-42. PWM Control

| PWM [Addr 0x5B] |                   |                      |          |          |                       |          |          | Default to 0 |
|-----------------|-------------------|----------------------|----------|----------|-----------------------|----------|----------|--------------|
| Bit Number      | B7                | B6                   | B5       | B4       | B3                    | B2       | B1       | B0           |
| Bit Name        | PWM_EN            | PWM_F[2]             | PWM_F[1] | PWM_F[0] | PWM_D[3]              | PWM_D[2] | PWM_D[1] | PWM_D[0]     |
| Function        | PWM DRIVER ON/OFF | PWM DRIVER FREQUENCY |          |          | PWM DRIVER DUTY CYCLE |          |          |              |



The PWM frequency and duty cycle are defined by the PWM register settings as shown below.

**Table 3-43. PWM Settings**

| PWM_F[2:0] | FREQUENCY(kHz) | PWM_D[3:0] | DUTY CYCLE (%) | PWM_D[3:0] | DUTY CYCLE (%) |
|------------|----------------|------------|----------------|------------|----------------|
| 000        | 23.4           | 0000       | 6.25           | 1000       | 56.25          |
| 001        | 11.7           | 0001       | 12.5           | 1001       | 62.5           |
| 010        | 6.7            | 0010       | 18.75          | 1010       | 68.75          |
| 011        | 4.5            | 0011       | 25             | 1011       | 75             |
| 100        | 3.0            | 0100       | 31.25          | 1100       | 81.25          |
| 101        | 2.3            | 0101       | 37.5           | 1101       | 87.5           |
| 110        | 1.5            | 0110       | 43.75          | 1110       | 93.75          |
| 111        | 0.75           | 0111       | 50             | 1111       | 100            |

### 3.58.2 DIG\_PWM, DIG\_PWM2 Drivers

The TPS658621A provides two push-pull outputs with programmable duty cycle at pins DIGPWM and DIGPWM2. The DIG\_PWM register controls the DIGPWM pin duty cycle, register DIG\_PWM2 controls the DIGPWM2 pin duty cycle. The DIG\_PWM functions and register bit controls detailed below apply to the DIGPWM2 pin and DIG\_PWM2 register as well. Both registers default to 0x00 upon power-up.

**Table 3-44. DIGPWM, DIGPWM2 Control**

| DIG_PWM [Addr 0x5A] |           |             |             |             |             |             |             | Default to 0 |
|---------------------|-----------|-------------|-------------|-------------|-------------|-------------|-------------|--------------|
| Bit Number          | B7        | B6          | B5          | B4          | B3          | B2          | B1          | B0           |
| Bit Name            | DPWM_MODE | DPWM_SET[6] | DPWM_SET[5] | DPWM_SET[4] | DPWM_SET[3] | DPWM_SET[2] | DPWM_SET[1] | DPWM_SET[0]  |

| DIG_PWM2 [Addr 0x5C] |            |              |              |              |              |              |              | Default to 0 |
|----------------------|------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit Number           | B7         | B6           | B5           | B4           | B3           | B2           | B1           | B0           |
| Bit Name             | DPWM2_MODE | DPWM2_SET[6] | DPWM2_SET[5] | DPWM2_SET[4] | DPWM2_SET[3] | DPWM2_SET[2] | DPWM2_SET[1] | DPWM2_SET[0] |

Mode 0 (DPWM\_MODE is 0): The pulse width modulated output is a single PWM pulse of the selected duty cycle, with a nominal 250Hz repetition rate. The DIG\_PWM register bits [6:0] sets the pulse width value as shown below:

$$T_{ON}(ms) = \frac{DPWM\_SET[6:0]}{32}, \text{ if } DPWM\_SET[6:0] \leq 126 \quad (7)$$

$$T_{ON}(ms) = \text{Always On, if } DPWM\_SET[6:0] = 127$$

Mode 1 (DPWM\_MODE is 1): The bit DPWMx\_SET[6] of the DIG\_PWMx register selects the pulse time range, bits DIG\_PWMx[5:3] set the ON times and bits DIG\_PWMx[2:0] set the off times.

**Table 3-45. Digital PWM Settings, DPWM\_MODE=1**

| DPWMx_SET[ 6] = 0 |              |               |               | DPWMx_SET[ 6] = 1 |              |               |               |
|-------------------|--------------|---------------|---------------|-------------------|--------------|---------------|---------------|
| DIG_PWMx[5:3]     | ON TIME (μs) | DIG_PWMx[2:0] | OFF TIME (ms) | DIG_PWMx[5:3]     | ON TIME (ms) | DIG_PWMx[2:0] | OFF TIME (ms) |
| 000               | 31           | 000           | 0.49          | 000               | 5            | 000           | 40            |
| 001               | 61           | 001           | 1.01          | 001               | 10           | 001           | 60            |
| 010               | 92           | 010           | 1.50          | 010               | 15           | 010           | 80            |
| 011               | 122          | 011           | 2.01          | 011               | 20           | 011           | 100           |
| 100               | 153          | 100           | 2.50          | 100               | 30           | 100           | 120           |
| 101               | 183          | 101           | 2.99          | 101               | 40           | 101           | 140           |
| 110               | 214          | 110           | 4.00          | 110               | 50           | 110           | 160           |
| 111               | 244          | 111           | 5.00          | 111               | 60           | 111           | 180           |



### 3.58.3 LED\_PWM Driver

The LED PWM open drain pin has the duty cycle set by a pulse width modulation circuit. The LED\_SET register bits (7:0) set the pulse width value in 256 steps. The pulse width modulated output is not a single pulse of the selected duty cycle but a collection of semi-equally spaced pulses that sum to the required duty cycle, with repetition rate of 125Hz (typ)

**Table 3-46. LEDPWM Control**

| LED_PWM [Addr 0x59] |            |            |            |            |            |            |            | Default to 0 |
|---------------------|------------|------------|------------|------------|------------|------------|------------|--------------|
| Bit Number          | B7         | B6         | B5         | B4         | B3         | B2         | B1         | B0           |
| Bit Name            | LED_SET[7] | LED_SET[6] | LED_SET[5] | LED_SET[4] | LED_SET[3] | LED_SET[2] | LED_SET[1] | LED_SET[0]   |

$$T_{ON}(ms) = \frac{LED\_SET[7:0]}{32}, \text{ if } LED\_SET[7:0] \leq 254 \quad (9)$$

$$T_{ON}(ms) = \text{Always On, if } LED\_SET[7:0] = 255$$

### 3.58.4 RGB Drivers

The TPS658621A has two dedicated drivers for RGB external LED's. Three outputs are available for each driver (pins REDn, GREENn, BLUEn), with I<sup>2</sup>C selection of operation mode and LED current.

#### 3.58.5 RGB1 Driver

The RGB1 driver is enabled when RGB1\_EN=HI, in RGB1\_GREEN register. Each RGB1 pin (RED1, GREEN1 or BLUE1) will sink the current selected by RGB1\_ISET[1:0], RGB1\_RED register.

The RGB1 driver can be set in a flashing mode, the flash operation parameters are configured in register RGB1FLASH. During the flashing ON time the duty cycle for each driver can be set individually using control bits PWMIR[4:0], PWMIG[4:0] and PWMIB[4:0] on registers RGB1\_RED, RGB1\_GREEN and RGB1\_BLUE. The modulated output is not a single pulse of the selected duty cycle but a collection of semi-equally spaced pulses that sum to the required duty cycle, with repetition rate of 160Hz (typ). The start of 1 of the modulated pulses on RGB1 can be phased by 200 μs from the others so that for duty cycles below 50% the ON times of 2 of the LEDs will not overlap. When RGB1\_PHASE is 0 (RGB1\_GREEN[6]), the Red and Blue are drivers are in phase and Green is out of phase. For RGB1\_PHASE is 1 the Red and Green are in phase and Blue is out of phase.

**Table 3-47. RGB1 Control**

| RGB1FLASH [Addr 0x50] |                             |   |              |                                     |                                     |               |               | Default is 0  |
|-----------------------|-----------------------------|---|--------------|-------------------------------------|-------------------------------------|---------------|---------------|---------------|
| Bit Number            | B7                          | B6                                      | B5           | B4                                  | B3                                  | B2            | B1            | B0            |
| Bit Name              | RSVD507                     | FLASH1_ON[2]                            | FLASH1_ON[1] | FLASH1_ON[0]                        | FLASH1_PER[3]                       | FLASH1_PER[2] | FLASH1_PER[1] | FLASH1_PER[0] |
| Function              | SPARE                       | RGB1 RED/BLUE/GREEN FLASHING ON-TIME    |              |                                     | RGB1 RED/BLUE/GREEN FLASHING PERIOD |               |               |               |
| RGB1RED [Addr 0x51]   |                             |   |              |                                     |                                     |               |               | Default is 0  |
| Bit Number            | B7                          | B6                                      | B5           | B4                                  | B3                                  | B2            | B1            | B0            |
| Bit Name              | RSVD517                     | RGB1_ISET[1]                            | RGB1_ISET[0] | PWM1R[4]                            | PWM1R[3]                            | PWM1R[2]      | PWM1R[1]      | PWM1R[0]      |
| Function              | NOT USED                    | RGB1 RED/BLUE/GREEN DRIVER CURRENT SINK |              | RGB1 RED DRIVER INTENSITY CONTROL   |                                     |               |               |               |
| RGB1GREEN [Addr 0x52] |                             |   |              |                                     |                                     |               |               | Default is 0  |
| Bit Number            | B7                          | B6                                      | B5           | B4                                  | B3                                  | B2            | B1            | B0            |
| Bit Name              | RGB1_EN                     | RGB1_PHASE                              | RSVD535      | PWM1G[4]                            | PWM1G[3]                            | PWM1G[2]      | PWM1G[1]      | PWM1G[0]      |
| Function              | RGB1 DRIVERS ON/OFF CONTROL | DRIVER ON TIME PHASE CONTROL            | NOT USED     | RGB1 GREEN DRIVER INTENSITY CONTROL |                                     |               |               |               |
| RGB1BLUE [Addr 0x53]  |                             |   |              |                                     |                                     |               |               | Default is 0  |
| Bit Number            | B7                          | B6                                      | B5           | B4                                  | B3                                  | B2            | B1            | B0            |
| Bit Name              | RSVD537                     | RSVD536                                 | RSVD535      | PWM1B[4]                            | PWM1B[3]                            | PWM1B[2]      | PWM1B[1]      | PWM1B[0]      |
| Function              | NOT USED                    | NOT USED                                | NOT USED     | RGB1 BLUE DRIVER INTENSITY CONTROL  |                                     |               |               |               |

**Table 3-48. RGB1 Sink Current Settings**

| RGB1_ISET[1:0] | RGB1 SINK CURRENT (mA) |
|----------------|------------------------|
| 00             | 0                      |
| 01             | 3.7                    |
| 10             | 7.4                    |
| 11             | 11.1                   |

**Table 3-49. FLASH1\_ON Settings**

| FLASH1_ON[2:0] | FLASH ON TIME (s) |
|----------------|-------------------|
| 000            | 0.10              |
| 001            | 0.15              |
| 010            | 0.20              |
| 011            | 0.25              |
| 100            | 0.30              |
| 101            | 0.40              |
| 110            | 0.50              |
| 111            | 0.60              |

**Table 3-50. FLASH1\_PER Settings**

| FLASH1_PER[3:0] | FLASH PERIOD (s) | FLASH1_PER[3:0] | FLASH PERIOD (s) |
|-----------------|------------------|-----------------|------------------|
| 0000            | 1.0              | 1000            | 5.0              |
| 0001            | 1.5              | 1001            | 5.5              |
| 0010            | 2.0              | 1010            | 6.0              |
| 0011            | 2.5              | 1011            | 6.5              |
| 0100            | 3.0              | 1100            | 7.0              |
| 0101            | 3.5              | 1101            | 7.5              |
| 0110            | 4.0              | 1110            | 8.0              |
| 0111            | 4.5              | 1111            | Always On        |

[Equation 11](#) and [Equation 12](#) indicates the duty cycle values for each driver, set with bit PWM1R[4:0], PWM1G[4:0] and PWM1B[4:0]:

$$T_{ON}(ms) = \frac{PWM1R/G/B[4:0]}{5.4}, \text{ if } PWM1R/G/B[4:0] \leq 30 \quad (11)$$

$$T_{ON}(ms) = \text{Always On, if } pwm1r/g/b[4:0] = 31$$

### 3.58.6 RGB2 Driver

The RGB2 driver is enabled when RGB2\_EN is 1, in RGB2\_GREEN register. Each RGB2 pin (RED2, GREEN2 or BLUE2) will sink the current selected by RGB2\_ISET[2:0], set in RGB2\_RED register.

The RGB2 does not support a flashing mode, and will be turned on when RGB2\_EN is 1. When turned ON the duty cycle for each driver can be set individually using control bits PWMIR[4:0], PWMIG[4:0] and PWMIB[4:0] on registers RGB2\_RED, RGB2\_GREEN and RGB2\_BLUE. The modulated output is not a single pulse of the selected duty cycle but a collection of semi-equally spaced pulses that sum to the

required duty cycle, with repetition rate of 160Hz (typ). The start of one of the modulated pulses on RGB2 can be phased by 200  $\mu$ s from the others, so that for duty cycles below 50% the ON times of 2 of the LEDs will not overlap. When RGB2\_PHASE is **0** (RGB2\_GREEN[6]), the Red and Blue drivers are in phase and Green is out of phase. When RGB2\_PHASE is **1** the Red and Green are in phase and Blue is out of phase.

**Table 3-51. RGB2 Control**

| RGB2RED [Addr 0x54]   |   |                                    |              |                                     |          |          | Default to 0 |          |
|-----------------------|---|------------------------------------|--------------|-------------------------------------|----------|----------|--------------|----------|
| Bit Number            | B7                                      | B6                                 | B5           | B4                                  | B3       | B2       | B1           | B0       |
| Bit Name              | RGB2_ISET[2]                            | RGB2_ISET[1]                       | RGB2_ISET[0] | PWM2R[4]                            | PWM2R[3] | PWM2R[2] | PWM2R[1]     | PWM2R[0] |
| Function              | RGB2 RED/BLUE/GREEN DRIVER CURRENT SINK |                                    |              | RGB2 RED DRIVER INTENSITY CONTROL   |          |          |              |          |
| RGB2GREEN [Addr 0x55] |   |                                    |              |                                     |          |          | Default to 0 |          |
| Bit Number            | B7                                      | B6                                 | B5           | B4                                  | B3       | B2       | B1           | B0       |
| Bit Name              | RGB2_EN                                 | RGB2_PHASE                         | RSVD565      | PWM2G[4]                            | PWM2G[3] | PWM2G[2] | PWM2G[1]     | PWM2G[1] |
| Function              | RGB2 DRIVERS ON/OFF CONTROL             | RGB2 DRIVERS ON TIME PHASE CONTROL | SPARE        | RGB2 GREEN DRIVER INTENSITY CONTROL |          |          |              |          |
| RGB2BLUE [Addr 0x56]  |   |                                    |              |                                     |          |          | Default to 0 |          |
| Bit Number            | B7                                      | B6                                 | B5           | B4                                  | B3       | B2       | B1           | B0       |
| Bit Name              | RSVD577                                 | RSVD576                            | RSVD575      | PWM2B[4]                            | PWM2B[3] | PWM2B[2] | PWM2B[1]     | PWM2B[1] |
| Function              | NOT USED                                | NOT USED                           | NOT USED     | RGB2 GREEN DRIVER INTENSITY CONTROL |          |          |              |          |

**Table 3-52. RGB2 Sink Current Settings**

| RGB2_ISET[2:0] | RGB2 SINK CURRENT (mA) |
|----------------|------------------------|
| 000            | 0                      |
| 001            | 3.7                    |
| 010            | 7.4                    |
| 011            | 11.1                   |
| 100            | 14.9                   |
| 101            | 18.6                   |
| 110            | 23.2                   |
| 111            | 27.3                   |

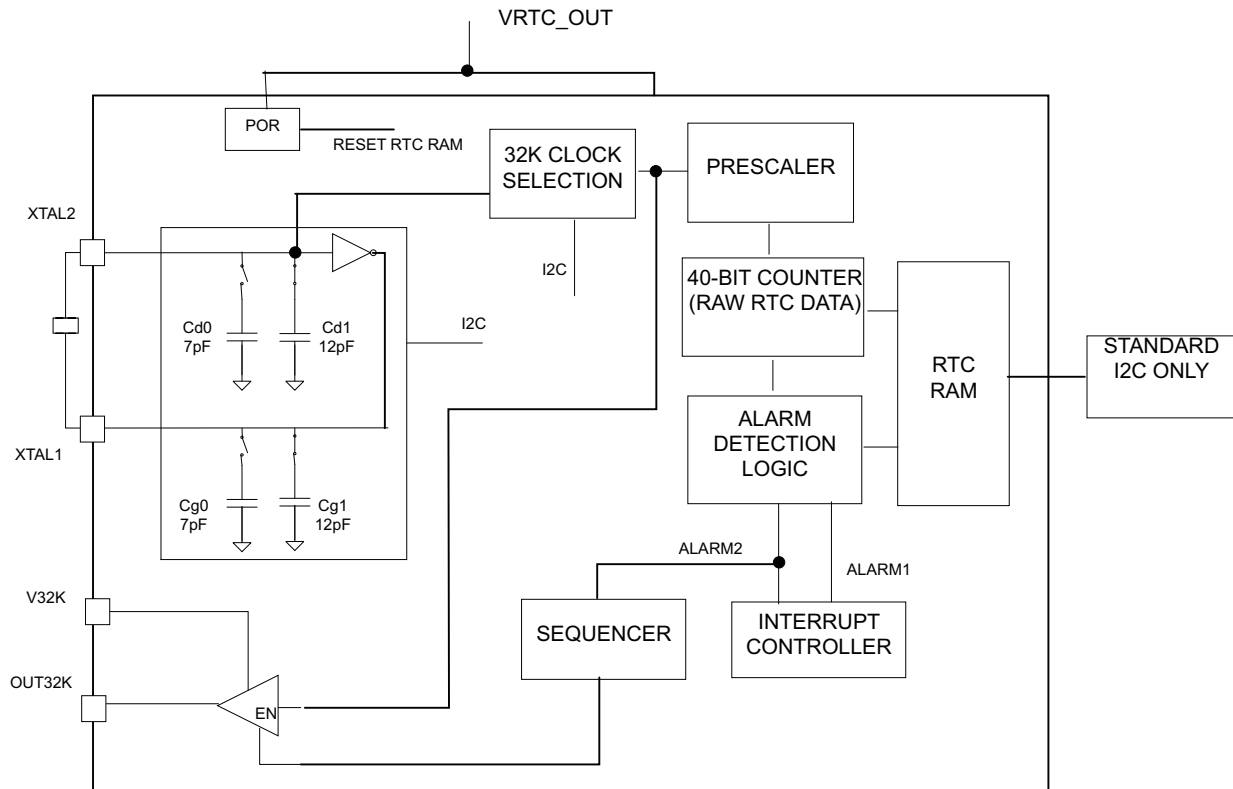
The on time for each driver, set with bits PWM2R[4:0], PWM2G[4:0] and PWM2B[4:0], is set by the equations:

$$T_{ON}(ms) = \frac{PWM2R/G/B[4:0]}{5.4}, \text{ if } PWM2R/G/B[4:0] \leq 30 \quad (13)$$

$$T_{ON}(ms) = \text{Always On, if } PWM2R/G/B[4:0] = 31$$

### 3.59 REAL TIME CLOCK

The TPS658621A has an integrated real time clock circuit that maintains an accurate timer/counter register under all potential operating conditions (AC power input, USB power input, main battery power, backup coin cell / SuperCap power source, or any combination of the above). The internal oscillator for the RTC can be driven by an external 32.768 kHz crystal. The TPS658621A has also been design with integrated, I<sup>2</sup>C selectable, capacitors which can be used with the external 32.768 kHz crystal such that a wide range of commercial crystals can be used without the need for external load capacitors.



**Figure 3-21. Simplified RTC Block**

The following functions are provided:

- A 40-bit counter, driven by a low-power 32 kHz oscillator
- The 32 kHz oscillator can be switched using I<sup>2</sup>C, RTC\_CTRL Register bit 6 (OSC\_SRC\_SEL), between the TPS658621A internal (RC) oscillator source and the crystal driven oscillator source.
- Externally biased buffer to supply the crystal driven oscillator to an external device via the OUT32K pin.
- Selectable pre-scaler divides the raw (32KHz) oscillator output, enabling clocking the RTC counter at 1.024 kHz or 32 kHz
- A 24-bit alarm register (ALARM1)
- A 16-bit alarm register (ALARM2)

The RTC registers are accessible only via the I<sup>2</sup>C bus. When an I<sup>2</sup>C read access is in progress, the RTC counter update is postponed. At the end of the I<sup>2</sup>C read access, the accumulated missing counts are added to the RTC counter.

#### NOTE

The RTC registers (0xC0-0xCA) **ARE NOT** reset when the TPS658621A is in the POWER DOWN or SLEEP STATE as long as V(RTC\_OUT) is greater than V<sub>UVLO\_RTC</sub>. All the RTC registers will be reset to their default settings, independent of the TPS658621A state, when V(RTC\_OUT) is less than V<sub>UVLO\_RTC</sub>.

The host software must read all five RTC counter bytes when accessing the RTC counter data, as the counter update is postponed starting at the first I<sup>2</sup>C byte read of a sequential I<sup>2</sup>C read of the five RTC\_COUNT bytes and negated on the fifth I<sup>2</sup>C byte read.

To assure proper operation of the RTC counter the following steps should always be followed:

1. The I<sup>2</sup>C address pointer must not be left pointing in the range 0xC6 to 0xCA

2. The maximum time for the address pointer to be in this range is 1 ms
3. Always read RTC\_ALARM2 in the following order to prevent the address pointer from stopping at 0xC6: RTC\_ALARM2\_LO, then RTC\_ALARM2\_HI

When the RTC\_OUT voltage falls below the internal RTC circuit Power On Reset threshold,  $V_{UVLO\_RTC}$ , the RTC\_CTRL register is reset. The host can identify this situation by reading the bit, POR\_RESET\_N, which will be 0.

The clock selection is controlled by OSC\_SRC\_SEL (RTC\_CTRL [6]). The internal 32kHz oscillator is connected to the RTC when the OSC\_SRC\_SEL bit is reset. Once the processor is running, the software can set this bit to 1, thereby connecting the 32.768 kHz crystal oscillator clock to the RTC. After being set, the OSC\_SRC\_SEL bit will remain 1 selecting the crystal oscillator clock, as long as the VRTC\_OUT voltage remains above the RTC\_OUT Power On Reset threshold. POR\_RESET\_N=HI when OSC\_SRC\_SEL is set HI, indicating to the host that the crystal clock is being delivered to the RTC.

The RTC\_ENABLE (RTC\_CTRL [5]) bit is cleared to 0 by the RTC\_OUT Power On Reset, disabling the RTC counter. To enable incrementing of the RTC\_COUNT [39:0] from an initial value set by the host, the RTC\_ENABLE bit should be written to 1 only after the RTC\_OUT voltage reaches the operating range. The RTC\_ENABLE bit must be cleared to 0 before any new value is written to the RTC\_COUNT register.

**Table 3-53. RTC Control<sup>(1)</sup>**

| RTC_CTRL [Addr 0xC0] |                          |                     |                                |                     |                     |                           |                 | Defaults in BOLD                 |
|----------------------|--------------------------|---------------------|--------------------------------|---------------------|---------------------|---------------------------|-----------------|----------------------------------|
| Bit Number           | B7                       | B6                  | B5                             | B4                  | B3                  | B2                        | B1              | B0                               |
| Bit Name             | POR_RESET_N              | OSC_SRC_SEL         | RTC_ENABLE                     | BUF_ENABLE          | PRE_BYPASS          | CL_SEL[1]                 | CL_SEL[0]       | RSVDC00                          |
| Function             | RESET RTC COUNTER        | 32K CLOCK SELECTION | RTC COUNTER CLOCK AND ALARM1/2 | 32KHZ BUFFER ENABLE | RTC COUNTER SCALING | INTERNAL XTAL1, XTAL2     | PIN CAPACITANCE | RTC_ALARM2 DETECTION EXITS SLEEP |
| When 0               | <b>RESET RTC COUNTER</b> | <b>INTERNAL 32K</b> | <b>DISABLED</b>                | DISABLED            | <b>USE 32K/32</b>   | SEE CL_SEL SETTINGS TABLE |                 | <b>DISABLED</b>                  |
| When 1               | OSC_SRC_SEL BIT = 1      | CRYSTAL 32K         | ENABLED                        | <b>ENABLED</b>      | USE 32K             | SEE CL_SEL SETTINGS TABLE |                 | ENABLED                          |

(1) B7 is READ ONLY, all other bits have Read/Write access

The selected 32KHz clock is applied to a prescaler that can divide it by 32, resulting in a timer tick resolution of either 32,768 ticks per second (pre-scaler disabled, PRE\_BYPASS is 1) or 1,024 ticks per second (pre-scaler enabled, PRE\_BYPASS is 0). The 32,768 Hz or 1024 Hz clock increments a 40 bit counter that tracks the real time and which can be read at anytime via I<sup>2</sup>C. With the prescaler enabled, the RTC count has a range of approximately 34 years. The RTC counter and alarm registers are shown below, the 40 bit RTC Counter is cleared only on when RTC\_OUT is below the UVLO threshold.

**Table 3-54. RTC Counter**

| RTC_COUNT4 [Addr 0xC6] |         |         |         |         |         |         |         | Default to 0 |
|------------------------|---------|---------|---------|---------|---------|---------|---------|--------------|
| Bit Number             | B7      | B6      | B5      | B4      | B3      | B2      | B1      | B0           |
| Bit Name               | RTC[39] | RTC[38] | RTC[37] | RTC[36] | RTC[35] | RTC[34] | RTC[33] | RTC[32]      |
| RTC_COUNT3 [Addr 0xC7] |         |         |         |         |         |         |         | Default to 0 |
| Bit Name               | RTC[31] | RTC[30] | RTC[29] | RTC[28] | RTC[27] | RTC[26] | RTC[25] | RTC[24]      |
| RTC_COUNT2 [Addr 0xC8] |         |         |         |         |         |         |         | Default to 0 |
| Bit Name               | RTC[23] | RTC[22] | RTC[21] | RTC[20] | RTC[19] | RTC[18] | RTC[17] | RTC[16]      |
| RTC_COUNT1 [Addr 0xC9] |         |         |         |         |         |         |         | Default to 0 |
| Bit Name               | RTC[15] | RTC[14] | RTC[13] | RTC[12] | RTC[11] | RTC[10] | RTC[9]  | RTC[8]       |
| RTC_COUNT0 [Addr 0xCA] |         |         |         |         |         |         |         | Default to 0 |
| Bit Name               | RTC[7]  | RTC[6]  | RTC[5]  | RTC[4]  | RTC[3]  | RTC[2]  | RTC[1]  | RTC[0]       |

The alarm logic compares the RTC\_ALARM1 register bits to the RTC\_COUNT registers as follows:

*With prescaler enabled:* ALM1[23:0] is compared to RTC[23:0]

*With prescaler disabled:* ALM1[23:0] is compared to RTC[28:5]

An interrupt is sent to the host (if enabled via I<sup>2</sup>C, see interrupt controller section) when the alarm logic detects that the RTC\_COUNT value is equal to the pre-programmed ALARM1 register value.

The alarm logic compares the RTC\_ALARM2 register bits to the RTC\_COUNT registers as follows:

*With prescaler enabled:* ALM2[23:0] is compared to RTC[22:7]

*With prescaler disabled:* ALM2[15:0] is compared to RTC[27:12]

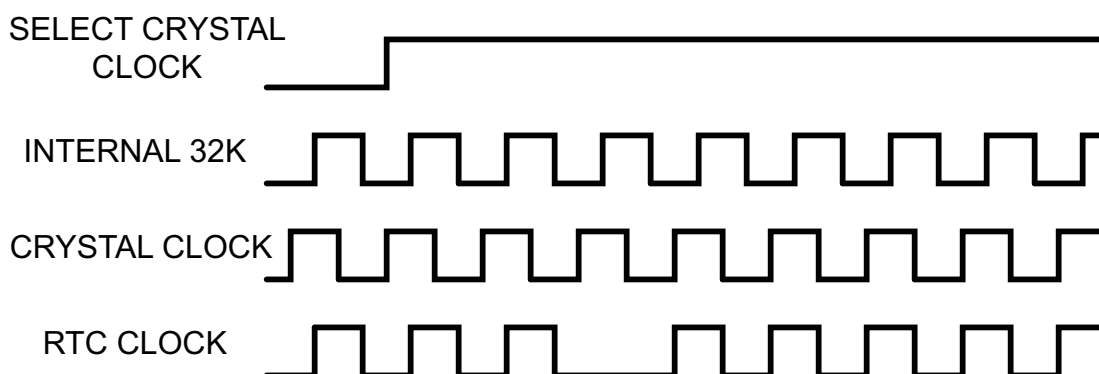
An interrupt is sent to the host (if enabled via I<sup>2</sup>C, see interrupt controller section) and the sleep mode ends when the alarm logic detects that the RTC\_COUNT value is equal to the pre-programmed ALARM2 register value.

**Table 3-55. RTC Alarm**

| RTC_ALARM1_HI [ADDRESS=0xC1] |          |          |          |          |          |          |          | Default to 0 |
|------------------------------|----------|----------|----------|----------|----------|----------|----------|--------------|
| Bit Number                   | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0           |
| Bit Name                     | ALM1[23] | ALM1[22] | ALM1[21] | ALM1[20] | ALM1[19] | ALM1[18] | ALM1[17] | ALM1[16]     |
| RTC_ALARM1_MID [Addr 0xC2]   |          |          |          |          |          |          |          | Default to 0 |
| Bit Name                     | ALM1[15] | ALM1[14] | ALM1[13] | ALM1[12] | ALM1[11] | ALM1[10] | ALM1[9]  | ALM1[8]      |
| RTC_ALARM1_LO [Addr 0xC3]    |          |          |          |          |          |          |          | Default to 0 |
| Bit Name                     | ALM1[7]  | ALM1[6]  | ALM1[5]  | ALM1[4]  | ALM1[3]  | ALM1[2]  | ALM1[1]  | ALM1[0]      |
| RTC_ALARM2_HI [Addr 0xC4]    |          |          |          |          |          |          |          | Default to 0 |
| Bit Name                     | ALM2[15] | ALM2[14] | ALM2[13] | ALM2[12] | ALM2[11] | ALM2[10] | ALM2[9]  | ALM2[8]      |
| RTC_ALARM2_LO [Addr 0xC5]    |          |          |          |          |          |          |          | Default to 0 |
| Bit Name                     | ALM2[7]  | ALM2[6]  | ALM2[5]  | ALM2[4]  | ALM2[3]  | ALM2[2]  | ALM2[1]  | ALM2[0]      |

### 3.60 SWITCHING BETWEEN INTERNAL AND CRYSTAL CLOCK

When switching between the internal clock to the crystal clock, an internal logic extends the LO time of the clock sent to the counter to avoid undesired glitches. A typical clock switching timing diagram is shown below:



### 3.61 CRYSTAL OSCILLATOR

The crystal oscillator has internal load capacitances, in order to allow a typical 32K crystal to operate as described in the electrical characteristics tables. The TPS658621A has four integrated capacitors that can be connected to the XTAL1, XTAL2 pins as defined by control bits CL\_SEL[1:0] in register RTC\_CTRL, effectively applying a load capacitance to the external crystal.

**Table 3-56. CL\_SEL[1:0] Setting  
(Default in bold)**

| CL_SEL[1] | CL_SEL[0] | Total C_LOAD [pF]<br>(typ) |
|-----------|-----------|----------------------------|
| 0         | 0         | 1.5                        |
| 0         | 1         | 6.5                        |
| <b>1</b>  | <b>0</b>  | <b>7.5</b>                 |
| 1         | 1         | 12.5                       |

### 3.62 ADC FUNCTIONAL OVERVIEW

The TPS658621A ADC is capable of running in a variety of modes programmable via I<sup>2</sup>C. The ADC control and data registers are accessible only by the standard I<sup>2</sup>C interface (SDA/SCLK). An internal 11:1 analog multiplexer is used to allow a single SAR converter to sequentially monitor up to 11 analog inputs, as shown in [Table 3-57](#).

**Table 3-57. ADC Channel Settings**

| CHANNEL | CONNECTION  | PARAMETER SAMPLED                           | VOLTAGE RANGE                            | SPECIAL FEATURES  | FULL SCALE READING |
|---------|-------------|---|--|---|--------------------|
| CH1     | ANLG1 pin   | User defined                                | 0–2.6V<br>AVDD6-V(ANLGn)><br>400mV       | Internal pull-up current<br>source programmable<br>via<br>I <sup>2</sup> C: 0/ 3/10/50 µA | 2.6 V              |
| CH2     | ANLG2 pin   |   |  |   | 2.6 V              |
| CH3     | ANLG3 pin   |   |  |   | 2.6 V              |
| CH4     | ISET pin    | Voltage proportional to<br>charge current   | 0V (charger off) to<br>2.5V(fast charge) | —   | 2.6 V              |
| CH5     | TS pin      | Voltage proportional to pack<br>temperature | 0V (short) to 2.2V (no<br>thermistor)    | See Charger Section   | 2.6 V              |
| CH6     | RSVD        | N/A   | N/A                                      | —   | 2.6 V              |
| CH7     | LDO_RTC pin | Internal LDO output voltage                 | 0V to 3.3V                               | —   | 4.622 V            |
| CH8     | SYS pin     | System Power bus voltage                    | 0V to 5.5V                               | —   | 5.547 V            |
| CH9     | VIN_CHG pin | System Power bus voltage                    | 0V to 5.5V                               | —   | 5.547 V            |
| CH10    | BAT pin     | Battery pack positive<br>terminal voltage   | 0V to 4.6V                               | —   | 4.622 V            |
| CH11    | COMP pin    | COMP pin voltage                            | 0V – 2.6V                                | —   | 2.6 V              |

A simplified block diagram for the ADC analog section is show in Figure 3-22.

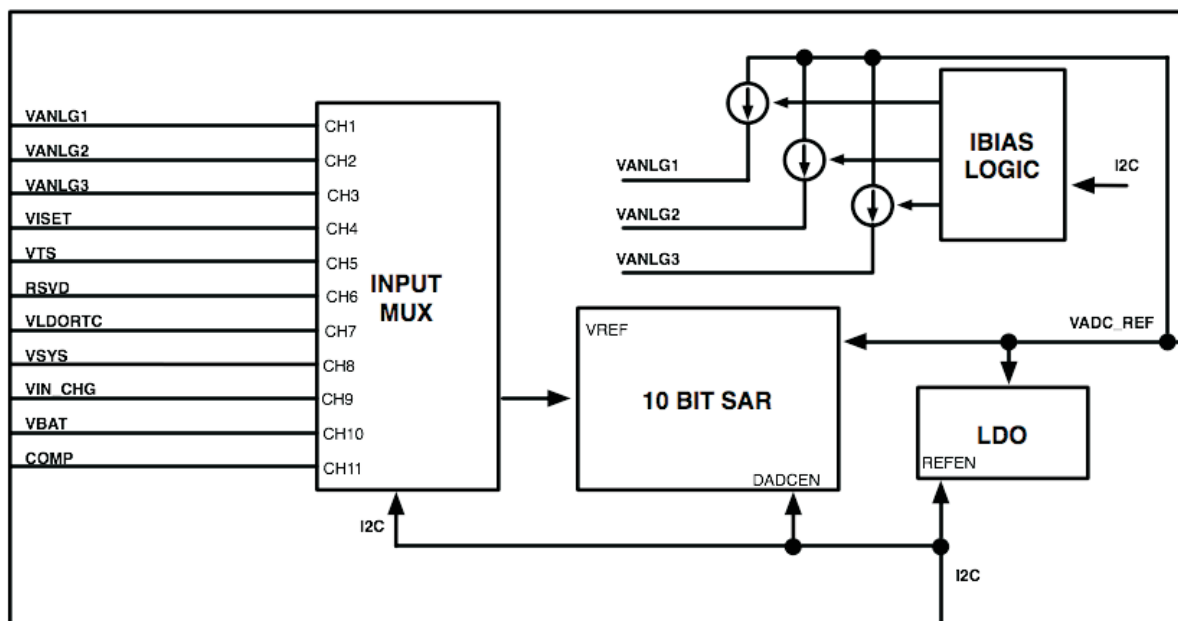


Figure 3-22. Simplified ADC Block

### 3.62.1 ADC External Input Pins – Bias Current Settings

The external pins ANLG1, ANLG2 and ANLG3 may be biased using internal pull-up current sources, with current source value set by register ADCANLG. The current sources are turned OFF when the ADC reference is disabled.

Table 3-58. ADC Input Bias Selection

| ADCANLG [Addr 0x60] |          |          |                           |           |                           |           |                           | Default to 0 |
|---------------------|----------|----------|---------------------------|-----------|---------------------------|-----------|---------------------------|--------------|
| Bit Name            | ANLG2FLT | ANLG3FLT | IANLG3[1]                 | IANLG3[0] | IANLG2[1]                 | IANLG2[0] | IANLG1[1]                 | IANLG1[0]    |
| Function            | SPARE    | SPARE    | ANLG3 BIAS CURRENT SOURCE |           | ANLG2 BIAS CURRENT SOURCE |           | ANLG1 BIAS CURRENT SOURCE |              |

Table 3-59. ANLG3/2/1 Current Source Settings

| IANLG[1] | IANLG[0] | Current (μA) |
|----------|----------|--------------|
| 0        | 0        | 0            |
| 0        | 1        | 3            |
| 1        | 0        | 10           |
| 1        | 1        | 50           |

The COMP pin has no internal pull-up current source.

### 3.62.2 ADC Timing Engine Overview

The ADC timing engine can be configured to perform either one reading, a single-trigger multiple set of readings, or to operate continuously until high or low limits are violated on any channel.

A *conversion cycle* includes the following steps:

1. Program the timing engine mode (single sample, multiple sample, etc.) and triggers
2. Enable the internal ADC reference and conversion start delay



3. Select the channel to be used as the SAR input and start the conversion cycle

The timing engine has an internal ALU that stores the converted data in an internal accumulator, executing mathematical operations with the stored data. A conversion cycle ends when the accumulator data is transferred to the TPS658621A ADC RAM data registers.

When the conversion cycle is completed, an interrupt request corresponding to indicate end of conversion operation is generated. The interrupt controller subsystem will set the ACK\_ADC (bit B1, register 0xB6) to indicate the source of the interrupt was the ADC subsystem. Additional information is available in the ADC0\_INT register (0x9A).

### 3.62.3 Configuring the ADC Conversion Cycle

#### 3.62.3.1 Number of Samples and ADC Input Setup

Register ADC0\_SET controls the following parameters for a conversion cycle: conversion start, continuous or fixed-interval sampling mode, number of samples to be taken and channel selection.

Setting the ADC0\_EN bit to **1** will start the conversion process. While a conversion cycle is being executed (and conversions are being taken) the ADC0\_INT register cannot be externally accessed.

The ADC engine has a BUSY signal generated by the ADC Digital Control Logic to indicate this condition. If the ADC0\_EN bit is cleared to 0 during a conversion, the conversion cycle will continue until the number of samples specified with the RD\_MODE bits has been taken so that the SUM (average) value from the accumulator will be valid. The ADC0\_EN bit must be set to 0 before a new conversion configuration is set up.

**Table 3-60. ADC0 Conversion Selection**

| ADC0_SET [Addr 0x61] |                       |                         |                          |             |                                 |           |           | Default in BOLD |
|----------------------|-----------------------|-------------------------|--------------------------|-------------|---------------------------------|-----------|-----------|-----------------|
| Bit Number           | B7                    | B6                      | B5                       | B4          | B3                              | B2        | B1        | B0              |
| Bit Name             | ADC0_EN               | REPEAT0                 | RD0_MODE[1]              | RD0_MODE[0] | CHSEL0[3]                       | CHSEL0[2] | CHSEL0[1] | CHSEL0[0]       |
| Function             | ADC0 CONVERSION START | ADC0 REPEAT MODE ENABLE | READINGS IN A CONVERSION |             | ADC0 INPUT CHANNEL SELECTION    |           |           |                 |
| When 0               | <b>DISABLED</b>       | <b>DISABLED</b>         | SEE ADC READING SETTINGS |             | SEE ADC CHANNEL SELECT SETTINGS |           |           |                 |
| When 1               | ENABLED               | ENABLED                 |                          |             |                                 |           |           |                 |

**Table 3-61. ADC Readings Setting (Default in bold)**

| RD0_MODE[1] | RD0_MODE[0] | NUMBER OF READINGS |
|-------------|-------------|--------------------|
| <b>0</b>    | <b>0</b>    | <b>1</b>           |
| 0           | 1           | 16                 |
| 1           | 0           | 32                 |
| 1           | 1           | 64                 |

**Table 3-62. ADC Channel Select Settings (Default in bold)**

| CHSELn[3:0] | CHANNEL    | CHSELn[3:0] | CHANNEL |
|-------------|------------|-------------|---------|
| <b>0000</b> | <b>CH1</b> | 1000        | CH9     |
| 0001        | CH2        | 1001        | CH10    |
| 0010        | CH3        | 1010        | CH11    |
| 0011        | CH4        | 1011        | AGND    |
| 0100        | CH5        | 1100        | AGND    |

**Table 3-62. ADC Channel Select Settings (Default in bold) (continued)**

| CHSELn[3:0] | CHANNEL | CHSELn[3:0] | CHANNEL |
|-------------|---------|-------------|---------|
| 0101        | CH6     | 1101        | AGND    |
| 0110        | CH7     | 1110        | AGND    |
| 0111        | CH8     | 1111        | AGND    |

Continuous sampling mode can be set by writing  $\overline{\text{REPEAT}}$  to **1** and RD0\_MODE[1:0]=00. With those settings the conversions will be performed as single samples, without wait times, until the ADC\_EN bit is cleared by the host or a limit violation occurs. If fixed-interval sampling mode (REPEAT0 = **0**) is chosen, the conversion cycle will consist of a specific number of samples (1, 16, 32, or 64) as specified by the RD0\_MODE[1:0] bits. When a multiple sample conversion cycle is selected the time interval between individual samples is defined by the WAIT bits (register ADC0\_WAIT). To exit the continuous conversion mode before a limit violation occurs, the host must first set the  $\overline{\text{REPEAT}}$  bit to LO, and then set the ADC0\_EN bit to **0**.

### 3.62.4 Timing and ADC Reference Setup

The ADC0\_WAIT register controls the ADC0 timing engine reset, wait time value and the converter internal reference voltage enable. The ADC reference and SAR are disabled when AUTO\_REF=0 AND REF\_EN=0. The use of external references for the ADC is not supported.

**Table 3-63. ADC0 Conversion Timing**

| ADC0_WAIT [Addr 0x62] |                               |                 |   |        |  |          | Defaults in BOLD |          |
|-----------------------|-------------------------------|-----------------|---|--------|--|----------|------------------|----------|
| Bit Number            | B7                            | B6              | B5  | B4     | B3   | B2       | B1               | B0       |
| Bit Name              | ADC_RESET                     | RSVD626         | AUTO_REF                                    | REF_EN | WAIT0[3]   | WAIT0[2] | WAIT0[1]         | WAIT0[0] |
| Function              | RESET CONVERSION CYCLE        | NOT USED        | ADC Conversion Control                      |        | WAIT TIME BETWEEN INDIVIDUAL CONVERSIONS, REPEAT MODE ENABLED (ms) |          |                  |          |
| When 0                | <b>ALL ADC ENGINES ACTIVE</b> | <b>NOT USED</b> | Function is based on ADC Conversion Control |        | SEE WAIT0 SETTINGS TABLE   |          |                  |          |
| When 1                | RESET ALL ADC ENGINES         | NOT USED        |   |        |  |          |                  |          |

**Table 3-64. ADC Conversion Control (Default in bold)**

| AUTO_REF | REF_EN   | DESCRIPTION   |
|----------|----------|---|
| <b>0</b> | <b>0</b> | <b>Reference and ADC disabled</b>   |
| 0        | 1        | Manual control of the Reference. WAIT=0 is not valid. 8ms must occur between REF_EN=1 and ADC0_EN=1 |
| 1        | 0        | Automatic control of the Reference. Automatically enabled 8 ms before an ADC conversion is started. |
| 1        | 1        | Not a valid state   |

The relative timing between enabling the internal ADC reference / ANLGn pin bias currents and the start of a conversion cycle is controlled by bits AUTO\_REF and REF\_EN. Those bits allow implementation of a software only reference enable control or automatic reference enable control, as shown below:

*Software enables ADC reference:* Clear AUTO\_REF bit to **0**. Software must set REF\_EN to **1** at least 8 ms before enabling an ADC engine and not clear REF\_EN until all ADC engines are stopped.

*Automatic ADC reference enable, internal or external trigger, wait time < 8ms :* Set AUTO\_REF bit to **1**. The ADC logic will keep the ADC reference always on.

*Automatic ADC reference enable, internal trigger, wait time > 8ms :* Set AUTO\_REF bit to **1**. The ADC logic enables the ADC reference 8 ms before the programmed wait time is reached

Setting ADC\_RESET to 1 will return ALL the ADC timing engine to the idle state, ready to be re-enabled for a new conversion cycle. During the conversion cycle the ADC\_RESET bit is internally set to LO prior to the first ADC conversion being started. WAIT[3:0] sets the time interval between samples in the case where a multiple-sample conversion cycle is being executed. WAIT[3:0] should be set LO in single sample conversion cycles.

**Table 3-65. ADC0 Conversion Wait Settings (Default in bold);  
Valid for All Timing Engines**

| WAIT0[3:0]  | WAIT TIME (ms) | WAIT0[3:0] | WAIT TIME (ms) |
|-------------|----------------|------------|----------------|
| <b>0000</b> | <b>0.000</b>   | 1000       | 8.000          |
| 0001        | 0.062          | 1001       | 16.00          |
| 0010        | 0.125          | 1010       | 32.00          |
| 0011        | 0.250          | 1011       | 64.00          |
| 0100        | 0.500          | 1100       | 128.0          |
| 0101        | 1.000          | 1101       | 256.0          |
| 0110        | 2.000          | 1110       | 512.0          |
| 0111        | 4.000          | 1111       | 1024           |

### 3.62.5 External Trigger Setup

The ADC conversion cycle can be started via an internal or external trigger when using the ADC0 timing engine. The trigger is selectable by setting bits ADC0\_TRIG4, ADC0\_TRIG2 in registers ADC0\_DELAY.

**Table 3-66. Trigger Settings**

| ADC0_DELAY [Addr 0x67] |                           |                           |                            |                 |                 |                                       | Default to 0 |           |
|------------------------|---------------------------|---------------------------|----------------------------|-----------------|-----------------|---------------------------------------|--------------|-----------|
| Bit Number             | B7                        | B6                        | B5                         | B4              | B3              | B2                                    | B1           | B0        |
| Bit Name               | ADC0_TRIG4                | ADC0_TRIG2                | ADC0HOLD                   | ADC0_EDGE       | RSVD673         | DELAY0[2]                             | DELAY0[1]    | DELAY0[0] |
| Function               | GPIO4 IS ADC0 EXT TRIGGER | GPIO2 IS ADC0 EXT TRIGGER | ADC HOLDOFF ON/OFF CONTROL | NOT USED        | NOT USED        | ADC EXTERNAL TRIGGER DELAY (μs)       |              |           |
| When 0                 | <b>DISABLED</b>           | <b>DISABLED</b>           | <b>OFF</b>                 | <b>NOT USED</b> | <b>NOT USED</b> | <b>000=00</b> 001=50 010= 100 011=150 |              |           |
| When 1                 | ENABLED                   | ENABLED                   | ON                         | NOT USED        | NOT USED        | 100=200 101=250 110=350 111=450       |              |           |

When more than one GPIO trigger source is selected the GPIO signals are OR'ed prior to trigger detection. When both of those bits are cleared to 0 the internal trigger is selected.

ADC0\_HOLDOFF (ADC0\_DELAY[5]) enables the GPIOx trigger source to be used as a level-sensed gating signal which will suspend conversion cycles when the trigger source is low. The default for this bit is 0. When ADC0HOLD is 0, the conversion cycle will continue for the preset number of conversions selected with the RD\_MODE bits once the initial trigger occurs. If the ADC0HOLD bit is 1, any pending conversion cycle can be suspended if the GPIO trigger goes low (and resumes once the trigger signal goes high again and the trigger delay time has been met). ADC0\_DELAY[2:0] are used to set the initial wait interval from the trigger event until the first conversion in a cycle is started. This delay may be from 0 to 450μs.

When the GPIO's are selected as external triggers the ADC conversion start will be dependent on the GPIO configuration. Table 3-67 shows the possible options:

**Table 3-67. ADC0 GPIO Trigger Settings**

| ADC0_TRIG2 = 1, ADC0_TRIG4 = 0 |                     |                             | ADC0_TRIG2 = 0, ADC0_TRIG4 = 1 |                     |                             |
|--------------------------------|---------------------|-----------------------------|--------------------------------|---------------------|-----------------------------|
| GPIO2 PIN                      | ADC TRIGGER SOURCE  | WHEN HOLDOFF=HI             | GPIO4 PIN                      | ADC TRIGGER SOURCE  | WHEN HOLDOFF=HI             |
| NON-INVERTED                   | GPIO2 POSITIVE EDGE | SUSPEND TRIGGER at GPIO2=LO | NON-INVERTED                   | GPIO4 POSITIVE EDGE | SUSPEND TRIGGER at GPIO4=LO |

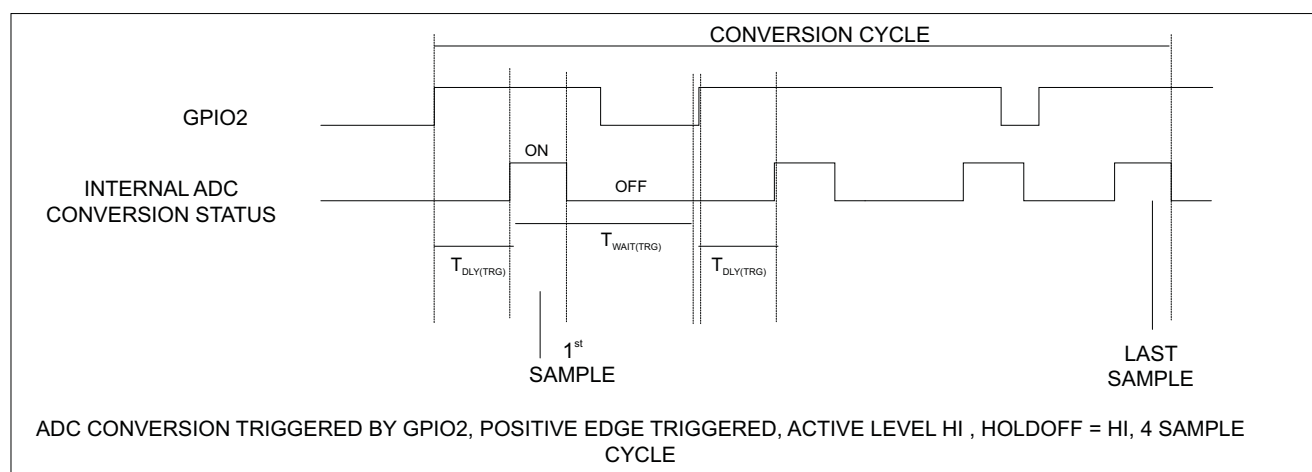
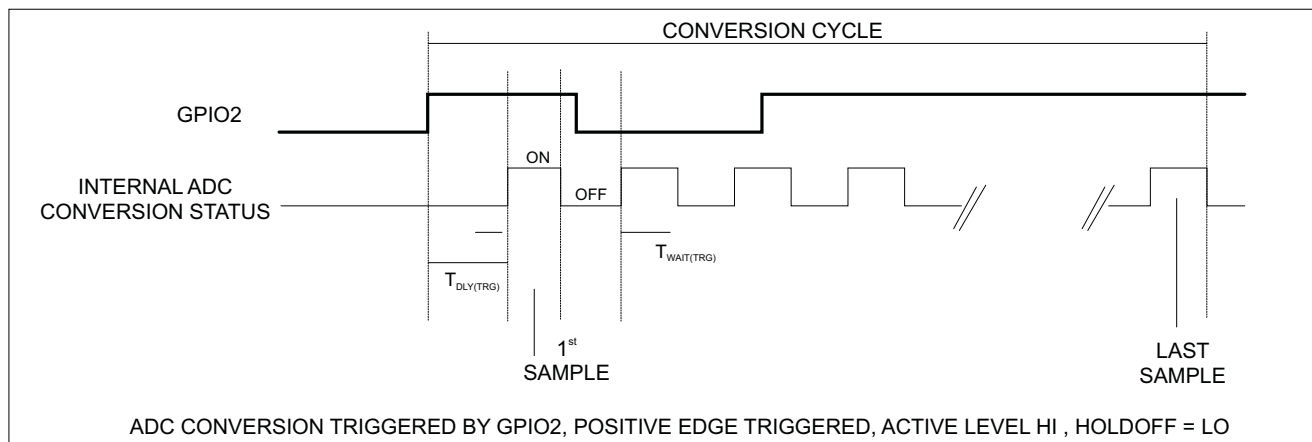
**Table 3-67. ADC0 GPIO Trigger Settings (continued)**

| ADC0_TRIG2 = 1, ADC0_TRIG4 = 0 |                           |  | ADC0_TRIG2 = 0, ADC0_TRIG4 = 1                  |                        |                                   |
|--------------------------------|---------------------------|--|---|------------------------|-----------------------------------|
| INVERTED                       | GPIO2<br>NEGATIVE<br>EDGE | SUSPEND TRIGGER at<br>GPIO2=HI                       | INVERTED  | GPIO4 NEGATIVE<br>EDGE | SUSPEND<br>TRIGGER at<br>GPIO4=HI |
| ADC0_TRIG2=HI,ADC0_TRIG4=HI    |                           |  |   |                        |                                   |
| GPIO2 PIN                      | GPIO4 PIN                 | ADC TRIGGER SOURCE                                   | WHEN HOLDOFF=HI                                 |                        |                                   |
| NON-INVERTED                   | NON-INVERTED              | GPIO2 <b>OR</b> GPIO4 POSITIVE<br>EDGE               | SUSPEND TRIGGER at GPIO2<br>= LO AND GPIO4 = LO |                        |                                   |
| NON-INVERTED                   | INVERTED                  | GPIO2 POSITIVE EDGE <b>OR</b><br>GPIO4 NEGATIVE EDGE | SUSPEND TRIGGER at GPIO2<br>= LO AND GPIO4 = HI |                        |                                   |
| INVERTED                       | NON-INVERTED              | GPIO2 NEGATIVE EDGE <b>OR</b><br>GPIO4 POSITIVE EDGE | SUSPEND TRIGGER at GPIO2<br>= HI AND GPIO4 = LO |                        |                                   |
| INVERTED                       | INVERTED                  | GPIO2 <b>OR</b> GPIO4 NEGATIVE<br>EDGE               | SUSPEND TRIGGER at GPIO2<br>= HI AND GPIO4 = HI |                        |                                   |

The procedure to start an externally-triggered conversion cycle has the following steps:

1. Verify that the current conversion cycle has ended (ADC0\_BUSY is **0**, I<sup>2</sup>C register STAT4)
2. Clear ADC0\_EN to **0** (ADC0\_SET[7]).
3. Set the appropriate bit in the corresponding ADC0\_DELAY register (example – write **1** to ADC0\_DELAY bit B7 to use GPIO4 as trigger source for ADC0). Ensure that the selected GPIOs have the appropriate input and polarity selection – see GPIOSET1 and GPIOSET2 registers.
4. Set ADC0\_EN to **1**

After step 4 the ADC will be armed, waiting for an external trigger detection to start a conversion cycle. In triggered mode the current cycle will not expire if the converter is armed and an external trigger is not detected.



**Figure 3-23. ADC Operation Example**

### 3.62.6 ADC ALU Unit and Result Registers

The ALU performs mathematical operations on the ADC output data. It can execute average (SUM) calculations and minimum / maximum detection for a conversion cycle. The result of the SUM calculations is stored in a 16 bit accumulator register (ADC0SUM2, ADC0\_SUM1) and the MIN/MAX data is stored in 10-bit registers (ADC0\_MAX2, ADC0\_MAX1, ADC0\_MIN2, ADC0\_MIN1).

**Equation 15** indicates how to translate the register data into a voltage reading for each channel:

$$\text{ADC\_OUTPUT\_COUNTS} = [\text{ADC\_INPUT\_VOLTAGE} / \text{FULL\_SCALE\_READING}] \times 1023$$

**Table 3-68. ADC0 Output Data**

| ADC0_SUM2 <sup>(1)</sup> [Addr 0x94] |         |         |         |         |         |         |        |        |
|--------------------------------------|---------|---------|---------|---------|---------|---------|--------|--------|
| Bit Number                           | B7      | B6      | B5      | B4      | B3      | B2      | B1     | B0     |
| Bit Name                             | AVG[15] | AVG[14] | AVG[13] | AVG[12] | AVG[11] | AVG[10] | AVG[9] | AVG[8] |
| ADC0_SUM1 [Addr 0x95]                |         |         |         |         |         |         |        |        |
| Bit Name                             | AVG[7]  | AVG[6]  | AVG[5]  | AVG[4]  | AVG[3]  | AVG[2]  | AVG[1] | AVG[0] |
| ADC0_MAX2 [Addr 0x96]                |         |         |         |         |         |         |        |        |
| Bit Name                             | RSVD967 | RSVD966 | RSVD965 | RSVD964 | RSVD963 | RSVD962 | MAX[9] | MAX[8] |
| ADC0_MAX1 [Addr 0x97]                |         |         |         |         |         |         |        |        |

(1) All bits in ADC0\_SUM2 are read only.

**Table 3-68. ADC0 Output Data (continued)**

| Bit Name                     | MAX[7]  | MAX[6]  | MAX[5]  | MAX[4]  | MAX[3]  | MAX[2]  | MAX[1] | MAX[0] |
|------------------------------|---------|---------|---------|---------|---------|---------|--------|--------|
| <b>ADC0_MIN2 [Addr 0x98]</b> |         |         |         |         |         |         |        |        |
| Bit Name                     | RSVD987 | RSVD986 | RSVD985 | RSVD984 | RSVD983 | RSVD982 | MIN[9] | MIN[8] |
| <b>ADC0_MIN1 [Addr 0x99]</b> |         |         |         |         |         |         |        |        |
| Bit Name                     | MIN[7]  | MIN[6]  | MIN[5]  | MIN[4]  | MIN[3]  | MIN[2]  | MIN[1] | MIN[0] |

### 3.62.7 Limit Check Setup

The ADC0 timing engine has configurable low and high thresholds to interrupt the host when conversion values, stored in registers ADC0\_MAX and ADC0\_MIN exceed a pre-selected range. A limit violation will be detected and an interrupt sent to the host when the sampled value stored in registers ADC0\_MAX2, ADC0\_MAX1 exceeds the maximum value set in registers ADC0\_HILIM2, ADC0\_HILIM1 or when the minimum sampled value stored in registers ADC0\_MIN2, ADC0\_MIN1 is lower than the minimum value programmed in registers and ADC0\_HILIM2, ADC0\_HILIM1.

Limit violations can not occur if Low Limit = 0x000 and High Limit = 0xFFFF.

**Table 3-69. ADC0 Limit Selection**

| <b>ADC0_HILIM2 [Addr 0x63]</b> |           |           |           |           |            |            |           |           |
|--------------------------------|-----------|-----------|-----------|-----------|------------|------------|-----------|-----------|
| Bit Number                     | B7        | B6        | B5        | B4        | B3         | B2         | B1        | B0        |
| Bit Name                       | RSVD637   | RSVD636   | RSVD635   | RSVD634   | HILIMA[11] | HILIMA[10] | HILIMA[9] | HILIMA[8] |
| <b>ADC0_HILIM1 [Addr 0x64]</b> |           |           |           |           |            |            |           |           |
| Bit Name                       | HILIMA[7] | HILIMA[6] | HILIMA[5] | HILIMA[4] | HILIMA[3]  | HILIMA[2]  | HILIMA[1] | HILIMA[0] |
| <b>ADC0_LOLIM2 [Addr 0x65]</b> |           |           |           |           |            |            |           |           |
| Bit Name                       | RSVD657   | RSVD656   | RSVD655   | RSVD654   | LOLIMA[11] | LOLIMA[10] | LOLIMA[9] | LOLIMA[8] |
| <b>ADC0_LOLIM1 [Addr 0x66]</b> |           |           |           |           |            |            |           |           |
| Bit Name                       | LOLIMA[7] | LOLIMA[6] | LOLIMA[5] | LOLIMA[4] | LOLIMA[3]  | LOLIMA[2]  | LOLIMA[1] | LOLIMA[0] |

The limit detection ADC conversion cycle should be configured with internal trigger and sampling sequences as follows:

1. To detect when an individual sample violates the max/min limits: Set  $\overline{RD\_MODE}[1:0]$  to **00** and  $\overline{REPEAT}$  to **1**. With these settings the ALU will compare the 10-bit ADC data returned from the SAR engine to the 10 bit values loaded in the ADC0\_LIMIT values. The conversion sequence will repeat until either a violation interrupt occurs or the ADC0\_EN bit is written to 0.
2. To detect when the average value violates the max/min limits: Set  $\overline{RD\_MODE}[1:0]$  to **01**, **10** or **11** and  $\overline{REPEAT}$  to **1**. At the end of the multiple sample conversion cycle the ALU will calculate the 12 bit average of the sample values by shifting the  $\overline{AVG}[15:0]$  register (shift right 2 if 16 samples, shift right 3 if 32 samples and shift right 4 if 64 samples). The shifted 12-bit average value is then compared to the value programmed in registers ADC0\_LIMIT.

### 3.62.8 ADC Status Registers

The ADC conversion status for the timing engine is available in the ADC0\_INT register. The ADC0\_INT register is read-only. Reading the ADC0\_INT register clears the ADC0INT bit in the STAT4 register (ADC0INT=0).

**Table 3-70. ADC Conversion Status**

| <b>ADC0_INT [Addr 0x9A]</b> |                         |            |                |                |          |          |                         |                         |
|-----------------------------|-------------------------|------------|----------------|----------------|----------|----------|-------------------------|-------------------------|
| Bit Number                  | B7                      | B6         | B5             | B4             | B3       | B2       | B1                      | B0                      |
| Bit Name                    | ADC0_DONE               | ADC0_ERROR | HILIM0_FLT     | LOLIM0_FLT     | RSVD9A3  | RSVD9A2  | ADC0_GPIO4ST            | ADC0_GPIO2ST            |
| Function                    | CONVERSION CYCLE STATUS | ADC_STATUS | HI LIMIT FAULT | LO LIMIT FAULT | NOT USED | NOT USED | GPIO4 LEVEL AT ADC0 EOC | GPIO2 LEVEL AT ADC0 EOC |

**Table 3-70. ADC Conversion Status (continued)**

| ADC0_INT [Addr 0x9A] |      |          |              |             |          |          |      |      |
|----------------------|------|----------|--------------|-------------|----------|----------|------|------|
| When 0               | BUSY | NO ERROR | NOT DETECTED | NO DETECTED | NOT USED | NOT USED | LOW  | LOW  |
| When 1               | DONE | ERROR    | DETECTED     | DETECTED    | NOT USED | NOT USED | HIGH | HIGH |

### 3.63 GPIO

The TPS658621A integrates 4 general purpose push-pull ports (GPIOs) which can be configured as selectable inputs or outputs via register GPIOSET1 bits. When the GPIO is not configured the pull-down current source (2.5uA typ) is connected to the GPIO pin. When configured as an input the GPIO can be set as inverting or non-inverting via bits GPIOINV in the GPIOSET2 register.

When configured as an output, the GPIO output level is defined by bits GPIOOUT in the GPIOSET2 register.

**Table 3-71. GPIO Control<sup>(1)</sup>**

| GPIOSET1 [Addr 0x5D] |                     |                 |                     |                 |                     |                 |                     | Default to 0    |
|----------------------|---------------------|-----------------|---------------------|-----------------|---------------------|-----------------|---------------------|-----------------|
| Bit Number           | B7                  | B6              | B5                  | B4              | B3                  | B2              | B1                  | B0              |
| Bit Name             | GPIO4_MODE<br>1     | GPIO4_MODE<br>0 | GPIO3_MODE<br>1     | GPIO3_MODE<br>0 | GPIO2_MODE<br>1     | GPIO2_MODE<br>0 | GPIO1_MODE<br>1     | GPIO1_MODE<br>0 |
| Function             | GPIO4 CONFIGURATION |                 | GPIO3 CONFIGURATION |                 | GPIO2 CONFIGURATION |                 | GPIO1 CONFIGURATION |                 |

| GPIOSET2 [Addr 0x5E] |                               |                               |                               |                               |  |  |  |  |
|----------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|--|--|--|--|
| Bit Number           | B7                            | B6                            | B5                            | B4                            | B3   | B2   | B1   | B0   |
| Bit Name             | GPIO4INV                      | GPIO3INV                      | GPIO2INV                      | GPIO1INV                      | GPIO2_MODE<br>1                              | GPIO2_MODE<br>0                              | GPIO1_MODE<br>1                              | GPIO1_MODE<br>0                              |
| Function             | GPIO4 INPUT<br>BUFFER<br>MODE | GPIO3 INPUT<br>BUFFER<br>MODE | GPIO2 INPUT<br>BUFFER<br>MODE | GPIO1 INPUT<br>BUFFER<br>MODE | GPIO4<br>VOLTAGE,<br>CONFIGURED<br>AS OUTPUT | GPIO3<br>VOLTAGE,<br>CONFIGURED<br>AS OUTPUT | GPIO2<br>VOLTAGE,<br>CONFIGURED<br>AS OUTPUT | GPIO1<br>VOLTAGE,<br>CONFIGURED<br>AS OUTPUT |
| When 0               | <b>NON-<br/>INVERTING</b>     | <b>NON-<br/>INVERTING</b>     | <b>NON-<br/>INVERTING</b>     | <b>NON-<br/>INVERTING</b>     | <b>LO</b>                                    | <b>LO</b>                                    | <b>LO</b>                                    | <b>LO</b>                                    |
| When 1               | INVERTING                     | INVERTING                     | INVERTING                     | INVERTING                     | HI   | HI   | HI   | HI   |

(1) All GPIO's default to the same configuration.

**Table 3-72. GPIO4/3/2/1\_MODE Settings**

| GPIOx_MODE[1] | GPIOx_MODE[0] | GPIO4 Config          | GPIO3 Config        | GPIO2 Config        | GPIO1 Config          |
|---------------|---------------|-----------------------|---------------------|---------------------|-----------------------|
| 0             | 0             | Not Configured        | Not Configured      | Not Configured      | Not Configured        |
| 0             | 1             | Output                | Output              | Output              | Output                |
| 1             | 0             | Input ADC Trigger     | Input Not Used      | Input ADC Trigger   | Input PWM/PFM Control |
| 1             | 1             | Input LDO6/7/8 Enable | Input LDO2/3 Enable | Input LDO0/1 ENABLE | Input Not Used        |

### 3.64 STATUS REGISTERS

The system status is accessible via I<sup>2</sup>C registers listed below. The STATn registers are read only.

**Table 3-73. Status Registers**

| ADC0_INT [Addr 0x9A] |                            |            |                |                |          |          |                            |                            |
|----------------------|----------------------------|------------|----------------|----------------|----------|----------|----------------------------|----------------------------|
| Bit Number           | B7                         | B6         | B5             | B4             | B3       | B2       | B1                         | B0                         |
| Bit Name             | ADC0_DONE                  | ADC0_ERROR | HILIM0_FLT     | LOLIM0_FLT     | RSVD9A3  | RSVD9A2  | ADC0_GPIO4ST               | ADC0_GPIO2ST               |
| Function             | CONVERSION<br>CYCLE STATUS | ADC_STATUS | HI LIMIT FAULT | LO LIMIT FAULT | NOT USED | NOT USED | GPIO4 LEVEL AT<br>ADC0 EOC | GPIO2 LEVEL AT<br>ADC0 EOC |
| When 0               | BUSY                       | NO ERROR   | NOT DETECTED   | NOT DETECTED   | NOT USED | NOT USED | LOW                        | LOW                        |
| When 1               | DONE                       | ERROR      | DETECTED       | DETECTED       | NOT USED | NOT USED | HIGH                       | HIGH                       |

| STAT1 [Addr 0xB9] |    |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|----|
| Bit Number        | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

**Table 3-73. Status Registers (continued)**

| Bit Name | BATSYSON                        | ACSWON                  | USBSWON                  | BATCHGSWON                          | RSVDB83  | PACK_HOT                        | PACK_COLD                      | BATDET                               |
|----------|---------------------------------|-------------------------|--------------------------|-------------------------------------|----------|---------------------------------|--------------------------------|--------------------------------------|
| Function | BAT TO SYS SWITCH ON/OFF STATUS | AC SWITCH ON/OFF STATUS | USB SWITCH ON/OFF STATUS | BAT TO VIN_CHG SWITCH ON/OFF STATUS | SPARE    | PACK TEMP EXCEEDS HOT THRESHOLD | PACK TEMP BELOW COLD THRESHOLD | BATTERY PACK TS THERMISTOR DETECTION |
| When 0   | OFF                             | OFF                     | OFF                      | OFF                                 | NOT USED | NO                              | NO                             | NOT DETECTED                         |
| When 1   | ON                              | ON                      | ON                       | ON                                  | NOT USED | YES                             | YES                            | DETECTED                             |

| STAT2 [Addr 0xBA] |                                    |                          |                             |  |            |  |       |                                      |
|-------------------|------------------------------------|--------------------------|-----------------------------|--|------------|--|-------|--------------------------------------|
| Bit Number        | B7                                 | B6                       | B5                          | B4   | B3         | B2   | B1    | B0                                   |
| Bit Name          | TMRFLT                             | DPPM_ON(4)               | TH_ON                       | ITERM                                      | SLEEPTSHUT | STAT1  | STAT2 | COMPDET                              |
| Function          | PRE-CHARGE OR CHARGE TIMER TIMEOUT | CHARGER DPPM LOOP STATUS | CHARGER THERMAL LOOP STATUS | CHARGE CURRENT BELOW TERMINATION THRESHOLD | NOT USED   | CHARGE STATUS  |       | nHOTRST PULSE GENERATED REBOOT CYCLE |
| When 0            | NO                                 | OFF                      | OFF                         | NO   | NOT USED   | 00= PRE-CHARGE ON<br>01=CHARGE DONE<br>10=FAST CHARGE ON<br>11= CHARGE SUSPEND, TIMER FAULT, CHARGER OFF |       | NO                                   |
| When 1            | YES                                | ON                       | ON                          | YES  | NOT USED   |  |       | YES                                  |

| STAT3 [Addr 0xBB] |                         |                         |                         |           |                       |                        |                        |                         |
|-------------------|-------------------------|-------------------------|-------------------------|-----------|-----------------------|------------------------|------------------------|-------------------------|
| Bit Number        | B7                      | B6                      | B5                      | B4        | B3                    | B2                     | B1                     | B0                      |
| Bit Name          | SLEEPREQ                | LOWSYS                  | RESUME                  | RTC_ALARM | ACDET                 | USBDET                 | AC_OVP                 | USB_OVP                 |
| Function          | SLEEP REQUEST STATE SET | LOWSYS DETECTION STATUS | RESUME DETECTION STATUS | SPARE     | AC INPUT POWER STATUS | USB INPUT POWER STATUS | AC INPUT OVP DETECTION | USB INPUT OVP DETECTION |
| When 0            | NO                      | NOT DETECTED            | NOT DETECTED            | SPARE     | NOT DETECTED          | NOT DETECTED           | NO OVP                 | NO OVP                  |
| When 1            | YES                     | DETECTED                | DETECTED                | SPARE     | DETECTED              | DETECTED               | OVP DETECTED           | OVP DETECTED            |

| STAT4 [Addr 0xBC] |         |         |         |                   |         |         |         |                        |
|-------------------|---------|---------|---------|-------------------|---------|---------|---------|------------------------|
| Bit Number        | B7      | B6      | B5      | B4                | B3      | B2      | B1      | B0                     |
| Bit Name          | RSVDBC7 | RSVDBC6 | RSVDBC5 | ADC0BUSY          | RSVDBC3 | RSVDBC2 | RSVDBC1 | ADC0INT                |
| Function          | SPARE   | SPARE   | SPARE   | ADC ENGINE 0 MODE | SPARE   | SPARE   | SPARE   | ADC ENGINE 0 INTERRUPT |
| When 0            | SPARE   | SPARE   | SPARE   | IDLE              | SPARE   | SPARE   | SPARE   | NOT ACTIVE             |
| When 1            | SPARE   | SPARE   | SPARE   | BUSY              | SPARE   | SPARE   | SPARE   | ACTIVE                 |

### 3.65 INTERRUPT CONTROLLER

The interrupt controller monitors the system status bus and internal signals continuously, generating an interrupt (INT = '0') when a system status change is detected. Individual bits that generated the interrupt will be set to **1** in the INT\_ACK registers (read only registers), indicating which parameters generated the interrupt.

All the parameters monitored by the interrupt controller can be masked by registers INT\_MASK (0=unmasked, 1=masked). Masked parameters do not generate an interrupt when their state changes. When the host reads the INT\_ACK registers, the interrupt is reset causing the INT pin to go to a logic 1 and the INT\_ACK register bits are cleared.

The power good signals from the integrated supplies are level sensitive, and they will continue to cause an interrupt until the power good condition returns or the signal is masked. For non-masked power good parameters the INT\_ACK bit will indicate the present state of the power good signals. The INTMASK register bits are cleared to **0** upon power-up.

**Table 3-74. INT\_ACK registers**

| INT_ACK1 [Addr 0xB5] |           |           |           |           |           |           |           |           |
|----------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Number           | B7        | B6        | B5        | B4        | B3        | B2        | B1        | B0        |
| Bit Name             | ACK_PLDO7 | ACK_PLDO6 | ACK_PLDO5 | ACK_PLDO4 | ACK_PLDO3 | ACK_PLDO2 | ACK_PLDO1 | ACK_PLDO0 |

| INT_ACK2 [Addr 0xB6] |          |          |          |          |           |           |         |                            |
|----------------------|----------|----------|----------|----------|-----------|-----------|---------|----------------------------|
| Bit Name             | ACK_PSM3 | ACK_PSM2 | ACK_PSM1 | ACK_PSM0 | ACK_PLDO9 | ACK_PLDO8 | ACK_ADC | ACK_COMPDET <sup>(1)</sup> |

| INT_ACK3 [Addr 0xB7] |  |  |  |  |  |  |  |  |
|----------------------|--|--|--|--|--|--|--|--|
|----------------------|--|--|--|--|--|--|--|--|

(1) ACK\_COMPDET= ACK INT BY HOTRST FLAG SET



**Table 3-74. INT\_ACK registers (continued)**

| Bit Name                    | ACK_PP  | ACK_CHGTEMP            | ACK_CHGSTAT | ACK_BATDET  | ACK_ACDET    | ACK_USBDT  | ACKACUSBOVP | ACK_RTCALM1 |
|-----------------------------|---------|------------------------|-------------|-------------|--------------|------------|-------------|-------------|
| <b>INT_ACK4 [Addr 0xB8]</b> |         |                        |             |             |              |            |             |             |
| Bit Name                    | RSVDB87 | RSVDB86 <sup>(2)</sup> | IMASKLOWSYS | IMASKRESUME | IMASKRTCALM1 | IMASKACDET | ACK_LOWSYS  | ACK_RESUME  |

(2) RSVDB86= ACK INT BY SLEEP REQUEST

**Table 3-75. INTMASK Registers**

|                             |              |             |             |              |             |             |              |              |
|-----------------------------|--------------|-------------|-------------|--------------|-------------|-------------|--------------|--------------|
| <b>INTMASK1 [Addr 0xB0]</b> |              |             |             |              |             |             |              |              |
| Default to 1 (Masked)       |              |             |             |              |             |             |              |              |
| Bit Name                    | IMASK_PLDO7  | IMASK_PLDO6 | IMASK_PLDO5 | IMASK_PLDO4  | IMASK_PLDO3 | IMASK_PLDO2 | IMASK_PLDO1  | IMASK_PLDO0  |
| <b>INTMASK2 [Addr 0xB1]</b> |              |             |             |              |             |             |              |              |
| Default to 1 (Masked)       |              |             |             |              |             |             |              |              |
| Bit Name                    | IMASK_PSM3   | IMASK_PSM2  | IMASK_PSM1  | IMASK_PSM0   | IMASK_PLDO9 | IMASK_PLDO8 | IMASKADC     | RSVDB10      |
| <b>INTMASK3 [Addr 0xB2]</b> |              |             |             |              |             |             |              |              |
| Default to 1 (Masked)       |              |             |             |              |             |             |              |              |
| Bit Name                    | IMASKSYSSW   | IMASKACSW   | IMASKUSBSW  | IMASKBCHGSW  | RSVDB83     | IMASK_HOT   | IMASK_COLD   | IMASKBATDET  |
| <b>INTMASK4 [Addr 0xB3]</b> |              |             |             |              |             |             |              |              |
| Default to 1 (Masked)       |              |             |             |              |             |             |              |              |
| Bit Name                    | IMASK_TMRFLT | IMASK_DPPM  | IMASK_THON  | IMASK_TERM   | IMASK_TSHUT | IMASKCHSTAT | IMASKRTCALM2 | IMASK_COMP   |
| <b>INTMASK5 [Addr 0xB4]</b> |              |             |             |              |             |             |              |              |
| Default to 1 (Masked)       |              |             |             |              |             |             |              |              |
| Bit Name                    | RSVDB47      | IMASKLOWSYS | IMASKRESUME | IMASKRTCALM1 | IMASKACDET  | IMASKUSBDT  | IMASKAC_OVP  | IMASKUSB_OVP |

The interrupt controller can monitor either level or edge transitions to generate the interrupt request:

| PARAMETER                  | STATUS BIT  | SET INT_ACK BIT ON        | MASK reg/bit            | INT_ACK reg/bit        | ACK clear at  |
|----------------------------|-------------|---------------------------|-------------------------|------------------------|---------------|
| LDO0 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO0  | INT_ACK1 / ACK_LDO0    | Read INT_ACK1 |
| LDO1 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO1  | INT_ACK1 / ACK_PLDO1   | Read INT_ACK1 |
| LDO2 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO2  | INT_ACK1 / ACK_PLDO2   | Read INT_ACK1 |
| LDO3 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO3  | INT_ACK1 / ACK_PLDO3   | Read INT_ACK1 |
| LDO4 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO4  | INT_ACK1 / ACK_PLDO4   | Read INT_ACK1 |
| LDO5 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO5  | INT_ACK1 / ACK_PLDO5   | Read INT_ACK1 |
| LDO6 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO6  | INT_ACK1 / ACK_PLDO6   | Read INT_ACK1 |
| LDO7 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK1 / IMASK_PLDO7  | INT_ACK1 / ACK_PLDO7   | Read INT_ACK1 |
| LDO8 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK2 / IMASK_PLDO8  | INT_ACK2 / ACK_PLDO8   | Read INT_ACK2 |
| LDO9 power good fault      | None        | PGOOD FAULT DETECTED      | INTMASK2 / IMASK_PLDO9  | INT_ACK2 / ACK_PLDO9   | Read INT_ACK2 |
| SM0 power good fault       | None        | PGOOD FAULT DETECTED      | INTMASK2 / IMASK_PSM0   | INT_ACK2 / ACK_PSM0    | Read INT_ACK2 |
| SM1 power good fault       | None        | PGOOD FAULT DETECTED      | INTMASK2 / IMASK_PSM1   | INT_ACK2 / ACK_PSM1    | Read INT_ACK2 |
| SM2 power good fault       | None        | PGOOD FAULT DETECTED      | INTMASK2 / IMASK_PSM2   | INT_ACK2 / ACK_PSM2    | Read INT_ACK2 |
| SM3 over-voltage detection | None        | SM3 OVER-VOLTAGE DETECTED | INTMASK2 / IMASK_PSM3   | INT_ACK2 / ACK_PSM3    | Read INT_ACK2 |
| HOT RESET FLAG STATUS      | STAT2 bit 0 | HI→LO OR LO→HI            | INTMASK4 / IMASK_COMP   | INT_ACK2 / ACK_COMPDET | Read INT_ACK2 |
| BATSYS switch STATUS       | STAT1 bit 7 | HI→LO OR LO→HI            | INTMASK3 / IMASKSYSSW   | INT_ACK3 / ACK_PP      | Read INT_ACK3 |
| ACSYS SWITCH STATUS        | STAT1 bit 6 | HI→LO OR LO→HI            | INTMASK3 / IMASKACSW    | INT_ACK3 / ACK_PP      | Read INT_ACK3 |
| USBSYS SWITCH STATUS       | STAT1 bit 5 | HI→LO OR LO→HI            | INTMASK3 / IMASKUSBSW   | INT_ACK3 / ACK_PP      | Read INT_ACK3 |
| BATCHG SW STATUS           | STAT1 bit 4 | HI→LO OR LO→HI            | INTMASK3 / IMASK_TERM   | INT_ACK3 / ACK_PP      | Read INT_ACK3 |
| PACK HOT DETECTION         | STAT1 bit 2 | HI→LO OR LO→HI            | INTMASK3 / IMASK_TSHUT  | INT_ACK3 / ACK_CHGTEMP | Read INT_ACK3 |
| PACK COLD DETECTION        | STAT1 bit 1 | HI→LO OR LO→HI            | INTMASK3 / IMASKCHSTAT  | INT_ACK3 / ACK_CHGTEMP | Read INT_ACK3 |
| BATTERY INSERTION          | STAT1 bit 0 | HI→LO OR LO→HI            | INTMASK3 / IMASKBATDET  | INT_ACK3 / ACK_BATDET  | Read INT_ACK3 |
| charger timer fault        | STAT2 bit 7 | HI→LO OR LO→HI            | INTMASK4 / IMASK_TMRFLT | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |

| PARAMETER                | STATUS BIT  | SET INT_ACK BIT ON | MASK reg/bit            | INT_ACK reg/bit        | ACK clear at  |
|--------------------------|-------------|--------------------|-------------------------|------------------------|---------------|
| DPPM loop STATUS         | STAT2 bit 6 | HI→LO OR LO→HI     | INTMASK4 / IMASK_DPPM   | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |
| thermal loop STATUS      | STAT2 bit 5 | HI→LO OR LO→HI     | INTMASK4 / IMASK_THON   | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |
| termination STATUS       | STAT2 bit 4 | HI→LO OR LO→HI     | INTMASK4 / IMASK_TERM   | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |
| charger STAT2            | STAT2 bit 1 | HI→LO OR LO→HI     | INTMASK4 / IMASKCHSTAT  | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |
| charger STAT1            | STAT2 bit 2 | HI→LO OR LO→HI     | INTMASK4 / IMASKCHSTAT  | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |
| SLEEP and tshut detected | STAT2 bit 3 | HI→LO OR LO→HI     | INTMASK4 / IMASK_TSHUT  | INT_ACK3 / ACK_CHGSTAT | Read INT_ACK3 |
| SLEEP REQUEST DETECTED   | STAT3 bit7  | LO→HI              | INTMASK2/RSVDB10        | INT_ACK4 / RSVDB86     | Read INT_ACK4 |
| AC DETection             | STAT3 bit 3 | HI→LO OR LO→HI     | INTMASK5 / IMASKACDET   | INT_ACK3 / ACK_ACDET   | Read INT_ACK3 |
| USB DETection            | STAT3 bit 2 | HI→LO OR LO→HI     | INTMASK5 / IMAKSUSBDET  | INT_ACK3 / ACKACUSBOVP | Read INT_ACK3 |
| AC OVP                   | STAT3 bit 1 | HI→LO OR LO→HI     | INTMASK5 / IMAKSAC_OVP  | INT_ACK3 / ACKACUSBOVP | Read INT_ACK3 |
| USB OVP                  | STAT3 bit 0 | HI→LO OR LO→HI     | INTMASK5 / IMASKUSB_OVP | INT_ACK3 / ACKACUSBOVP | Read INT_ACK3 |
| RTC ALARM1               | NONE        | ALARM1 DETECTED    | INTMASK5 / IMAKSRTCALM1 | INT_ACK3 / ACK_RTCALM1 | Read INT_ACK3 |
| RTC ALARM2               | NONE        | ALARM2 DETECTED    | INTMASK4 / IMASKRTCALM2 | INT_ACK4 / ACK_RTCALM2 | Read INT_ACK4 |
| RESUME command           | STAT3 bit 5 | HI→LO OR LO→HI     | INTMASK5 / IMASKRESUME  | INT_ACK4 / ACK_RESUME  | Read INT_ACK4 |
| LOWSYS detection         | STAT3 bit 6 | HI→LO OR LO→HI     | INTMASK5 / IMASKLOWSYS  | INT_ACK4 / ACK_LOWSYS  | Read INT_ACK4 |
| DADC0INT                 | STAT4 bit 0 | LO→HI ONLY         | INTMASK2 / IMASKADC     | INT_ACK4 / ACK_ADC     | Read ADC0_INT |

### 3.66 DEVICE ID RAM REGISTER

Each device has a unique 8-bit identifier stored in the read only register VERSIONID.

**Table 3-76. Device ID Register**

| VERSIONID [Addr 0xCD] |                                     |       |       |       |       |       |       |       |
|-----------------------|-------------------------------------|-------|-------|-------|-------|-------|-------|-------|
| Bit Number            | B7                                  | B6    | B5    | B4    | B3    | B2    | B1    | B0    |
| Bit Name              | VCRC7                               | VCRC6 | VCRC5 | VCRC4 | VCRC3 | VCRC2 | VCRC1 | VCRC0 |
| Device Number         | VERSION IDENTIFICATION, FACTORY SET |       |       |       |       |       |       |       |
| TPS658621A            | 0                                   | 0     | 0     | 1     | 0     | 1     | 0     | 1     |

### 3.67 RAM MEMORY MAP

| MEMORY AREA                               | ADDR | REGISTER NAME | R/W | DESCRIPTION  |
|---|------|---------------|-----|--|
| <b>SUPPLY CONTROL AND VOLTAGE SETTING</b> | 0x10 | SUPPLYENA     | R/W | LDO2, SM0, SM1 ENABLE CONTROL                                |
|   | 0x11 | SUPPLYENB     | R/W | LDO2, SM0, SM1 ENABLE CONTROL                                |
|   | 0x12 | SUPPLYENC     | R/W | LDO0, LDO1, LDO3, LDO4, LDO6, LDO7, LDO8, SM2 ENABLE CONTROL |
|   | 0x13 | SUPPLYEND     | R/W | LDO0, LDO1, LDO3, LDO4, LDO6, LDO7, LDO8, SM2 ENABLE CONTROL |
|   | 0x14 | SUPPLYENE     | R/W | TPS658621A OPERATION MODE, LDO5, LDO9 ENABLE CONTROL         |
|   | 0x20 | VCC1          | R/W | SM0, SM1, LDO2, LDO4 VOLTAGE SELECTION / CHANGE CONTROL      |
|   | 0x21 | VCC2          | R/W | SM0, SM1, LDO2, LDO4 VOLTAGE SELECTION / CHANGE CONTROL      |
|   | 0x23 | SM1V1         | R/W | SM1 VOLTAGE SETTING #1                                       |
|   | 0x24 | SM1V2         | R/W | SM1 VOLTAGE SETTING #2                                       |
|   | 0x25 | SM1SL         | R/W | SM1 SLEW RATE  |
|   | 0x26 | SM0V1         | R/W | SM0 VOLTAGE SETTING #1                                       |
|   | 0x27 | SM0V2         | R/W | SM0 VOLTAGE SETTING #2                                       |
|   | 0x28 | SM0SL         | R/W | SM0 SLEW RATE  |
|   | 0x29 | LDO2AV1       | R/W | LDO2 VOLTAGE SETTING #1                                      |
|   | 0x2A | LDO2AV2       | R/W | LDO2 VOLTAGE SETTING #2                                      |
|   | 0x2F | LDO2BV1       | R/W | LDO2 VOLTAGE SETTING #1                                      |
|   | 0x30 | LDO2BV2       | R/W | LDO2 VOLTAGE SETTING #2                                      |
|   | 0x32 | LDO4V1        | R/W | LDO4 VOLTAGE SETTING # 1                                     |
|   | 0x33 | LDO4V2        | R/W | LDO4 VOLTAGE SETTING # 2                                     |
| <b>CONVERTER SETTINGS</b>                 | 0x41 | SUPPLYV1      | R/W | LDO1, LDO0 OUPUT VOLTAGE                                     |
|   | 0x42 | SUPPLYV2      | R/W | SM2, LDO8 OUTPUT VOLTAGE                                     |
|   | 0x43 | SUPPLYV3      | R/W | LDO6, LDO7 OUTPUT VOLTAGE                                    |
|   | 0x44 | SUPPLYV4      | R/W | RTC_LDO, LDO3 OUTPUT VOLTAGE, RTC_LDO ON/OFF                 |
|   | 0x45 | SUPPLYV5      | R/W | SPARE  |
|   | 0x46 | SUPPLYV6      | R/W | LDO5, LDO9 OUTPUT VOLTAGE                                    |
|   | 0x47 | SMODE1        | R/W | SM0, SM1, SM2, PWM/PFM MODE SETTING                          |
|   | 0x48 | SMODE2        | R/W | SPARE  |
| <b>CHARGER SETUP RAM</b>                  | 0x49 | CHG1          | R/W | CHARGER SETTINGS   |
|   | 0x4A | CHG2          | R/W | CHARGER SETTINGS   |
|   | 0x4B | CHG3          | R/W | CHARGER SETTING  |
| <b>POWER PATH SETUP RAM</b>               | 0x4C | PPATH2        | R/W | OUT POWER PATH SETTINGS                                      |
| <b>TPS658621A SEQUENCING</b>              | 0x4D | PGFLTMSK1     | R/W | POWER GOOD FAULT MASK  |
|   | 0x4E | PGFLTMSK2     | R/W | POWER GOOD FAULT MASK  |
|   | 0xCC | SPARE2        | R/W | REBOOT CYCLE FLAG RESET                                      |

| MEMORY AREA                       | ADDR<br>hex | REGISTER NAME | ACC | DESCRIPTION                           |
|-----------------------------------|-------------|---------------|-----|---------------------------------------|
| <b>PERIPHERAL<br/>CONTROL RAM</b> | 0X50        | RGB1FLASH     | R/W | RGB1R/G/B DRIVERS FLASH MODE SETTINGS |
|                                   | 0X51        | RGB1RED       | R/W | RGB1 RED DRIVER INTENSITY CONTROL     |
|                                   | 0X52        | RGB1GREEN     | R/W | RGB1 GREEN DRIVER INTENSITY CONTROL   |
|                                   | 0X53        | RGB1BLUE      | R/W | RGB1 BLUE DRIVER INTENSITY CONTROL    |
|                                   | 0X54        | RGB2RED       | R/W | RGB2 RED DRIVER INTENSITY CONTROL     |
|                                   | 0X55        | RGB2GREEN     | R/W | RGB2 GREEN DRIVER INTENSITY CONTROL   |
|                                   | 0X56        | RGB2BLUE      | R/W | RGB2 BLUE DRIVER INTENSITY CONTROL    |
|                                   | 0X57        | SM3_SET0      | R/W | WHITE LED DUTY CYCLE SETTINGS         |
|                                   | 0X58        | SM3_SET1      | R/W | WHITE LED DUTY CYCLE SETTINGS         |
|                                   | 0X59        | LED_PWM       | R/W | LED_PWM DRIVER DUTY CYCLE SETTINGS    |
|                                   | 0X5A        | DIG_PWM       | R/W | DIG_PWM DRIVER DUTY CYCLE SETTINGS    |
|                                   | 0X5B        | PWM           | R/W | PWM DRIVER DUTY CYCLE SETTINGS        |
|                                   | 0X5C        | DIG_PWM1      | R/W | DIG_PWM1 DRIVER DUTY CYCLE SETTINGS   |
|                                   | 0X5D        | GPIOSET1      | R/W | GPIO CONFIGURATION                    |
|                                   | 0X5E        | GPIOSET2      | R/W | GPIO CONFIGURATION                    |
| <b>ADC0 ENGINE<br/>SETUP RAM</b>  | 0x60        | ADCANLG       | R/W | adc input bias and filter control     |
|                                   | 0X61        | ADC0_SET      | R/W | ADC0 CONVERSION CYCLE SETUP           |
|                                   | 0X62        | ADC0_WAIT     | R/W | ADC0 CONVERSION CYCLE SETUP           |
|                                   | 0X63        | ADC0_HILIMIT2 | R/W | ADC0 HI LIMIT THRESHOLD               |
|                                   | 0X64        | ADC0_HILIMIT1 | R/W | ADC0 HI LIMIT THRESHOLD               |
|                                   | 0X65        | ADC0_LOLIMIT2 | R/W | ADC0 LO LIMIT THRESHOLD               |
|                                   | 0X66        | ADC0_LOLIMIT1 | R/W | ADC0 LO LIMIT THRESHOLD               |
|                                   | 0X67        | ADC0_DELAY    | R/W | ADC0 TRIGGER MODE                     |
| <b>ADC0 ENGINE<br/>DATA RAM</b>   | 0x94        | ADC0_SUM2     | R   | SUM OF ALL SAMPLES                    |
|                                   | 0x95        | ADC0_SUM1     | R   | SUM OF ALL SAMPLES                    |
|                                   | 0x96        | ADC0_MAX2     | R   | MAX SAMPLE VALUE                      |
|                                   | 0x97        | ADC0_MAX1     | R   | MAX SAMPLE VALUE                      |
|                                   | 0x98        | ADC0_MIN2     | R   | MIN SAMPLE VALUE                      |
|                                   | 0x99        | ADC0_MIN1     | R   | MIN SAMPLE VALUE                      |
|                                   | 0x9A        | ADC0_INT      | R   | ADC0 STATUS                           |
| <b>INTERRUPT<br/>CONTROL RAM</b>  | 0xB0        | INT_MASK1     | R/W | INT_MASK                              |
|                                   | 0xB1        | INT_MASK2     | R/W | INT MASK                              |
|                                   | 0xB2        | INT_MASK3     | R/W | INT MASK                              |
|                                   | 0xB3        | INT_MASK4     | R/W | INT MANAGEMENT                        |
|                                   | 0xB4        | INT_MASK5     | R/W | INT MANAGEMENT                        |
|                                   | 0xB5        | INT_ACK1      | R/W | INT MANAGEMENT REGISTER               |
|                                   | 0xB6        | INT_ACK2      | R/W | INT MANAGEMENT REGISTER               |
|                                   | 0xB7        | INT_ACK3      | R/W | INT MANAGEMENT REGISTER               |
|                                   | 0xB8        | INT_ACK4      | R/W | INT MANAGEMENT REGISTER               |
| <b>SYSTEM<br/>STATUS RAM</b>      | 0xB9        | STAT1         | R   | power path switches, pack status      |
|                                   | 0xBA        | STAT2         | R   | charger status                        |
|                                   | 0xBB        | STAT3         | R   | rtc, input power status               |
|                                   | 0xBC        | STAT4         | R   | ADC STATUS                            |

| MEMORY AREA | ADDR<br>hex | REGISTER NAME | ACC | DESCRIPTION           |
|-------------|-------------|---------------|-----|-----------------------|
| RTC         | 0xC0        | RTC_CTRL      | R/W | RTC CONTROL REGISTER  |
|             | 0xC1        | RTC ALARM     |     | RTC ALARM             |
|             | 0xC2        |               |     |                       |
|             | 0xC3        |               |     |                       |
|             | 0xC4        |               |     |                       |
|             | 0xC5        |               |     |                       |
|             | 0xC6        | RTC COUNTER   | R/W | RTC DATA              |
|             | 0xC7        |               |     |                       |
|             | 0xC8        |               |     |                       |
|             | 0xC9        |               |     |                       |
|             | 0xCA        |               |     |                       |
| DEVICE ID   | 0XCD        | VERSIONCRC    | R   | Device identification |

## 4 APPLICATION INFORMATION

### 4.1 DC/DC CONVERTER OUTPUT FILTER

#### 4.1.1 Inductor Selection

The typical value for the converter inductor is 2.2μH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency. See document [SLVA157](#) for more information on inductor selection.

[Equation 16](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with [Equation 16](#). This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \qquad (16)$$

with:

f = Switching Frequency (2.25MHz typical)

L = Inductor Value

ΔI<sub>L</sub> = Peak to Peak inductor ripple current

I<sub>Lmax</sub> = Maximum Inductor current

The highest inductor current will occur at maximum V<sub>in</sub>.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor. A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Refer to [Table 4-1](#) and the typical applications for possible inductors.

**Table 4-1. Inductors**

| SUPPLY | INDUCTOR TYPE   | INDUCTANCE [μH] | SUPPLIER  | TYP DIMENSIONS [mm] |
|--------|-----------------|-----------------|-----------|---------------------|
| SM0    | LPS4012-152     | 1.5             | Coilcraft | 4x4x1               |
|        | VLS4012-1R5N1R5 | 1.5             | TDK       | 4x4x1               |
| SM1    | LPS4012-152     | 1.5             | Coilcraft | 4x4x1               |
|        | VLS4012-1R5N1R5 | 1.5             | TDK       | 4x4x1               |
| SM2    | LPS4414-152MLx  | 1.5             | Coilcraft | 4x4x1.5             |
|        | 1008PS-152Kx    | 1.5             | Coilcraft | 4x4x2.5             |
| SM3    | DO2010-472      | 4.7             | Coilcraft | 2x2x1               |
|        | VLS3012-47M1R0  | 4.7             | TDK       | 3x3x1               |

#### 4.1.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a typical value of 22μF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. Refer to for recommended components.

If ceramic output capacitors are used the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{\text{RMS}C_{\text{out}}} = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (17)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{\text{out}} = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \times \left( \frac{1}{8 \times C_{\text{out}} \times f} + \text{ESR} \right) \quad (18)$$

Where the highest output voltage ripple occurs at the highest input voltage  $V_{\text{in}}$ .

At light load currents the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

### 4.1.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10µF. The input capacitor can be increased without any limit for better input voltage filtering.

**Table 4-2. Capacitors**

|       |      |                           |         |
|-------|------|---------------------------|---------|
| 22 µF | 0805 | TDK C2012X5R0J226MT       | Ceramic |
| 22 µF | 0805 | Taiyo Yuden JMK212BJ226MG | Ceramic |
| 10 µF | 0805 | Taiyo Yuden JMK212BJ106M  | Ceramic |
| 10 µF | 0805 | TDK C2012X5R0J106M        | Ceramic |

## 4.2 XTAL OSCILLATOR PCB – GENERAL GUIDELINES

**Table 4-3. External Crystal Specifications**

| EXTERNAL CRYSTAL REQUIREMENTS [TYP CRYSTAL – EPSON MC146] |                                    |     |        |                       |                   |
|---|------------------------------------|-----|--------|-----------------------|-------------------|
| PARAMETER   | DESCRIPTION                        | MIN | TYP    | MAX                   | UNIT              |
| F <sub>OSC</sub>  | Nominal crystal resonant frequency |     | 32.768 |                       | kHz               |
| Frequency Tolerance                                       | ΔF/F <sub>OSC</sub>                | –20 |        | 20                    | ppm               |
| B   | Parabolic Temp Co                  |     |        | 0.04×10 <sup>–6</sup> | 1/°C <sup>2</sup> |
| ESR   | Equivalent Series Resistance       |     |        | 65                    | kΩ                |
| C <sub>LOAD</sub>   | Load Capacitance                   |     | 7      |                       | pF                |
| C <sub>SHUNT</sub>  | Shunt capacitance                  | 0.5 | 0.8    | 1.2                   | pF                |
| P <sub>DRIVE</sub>  | Drive power                        |     | 0.5    | 1                     | µW                |
| Aging   |                                    | –3  |        | 3                     | ppm/Yr            |

The jitter observed in the OUT32K pin is heavily dependent on the board layout close to the XTAL1 and XTAL2 pins. The following layout/assembly procedures are recommended :

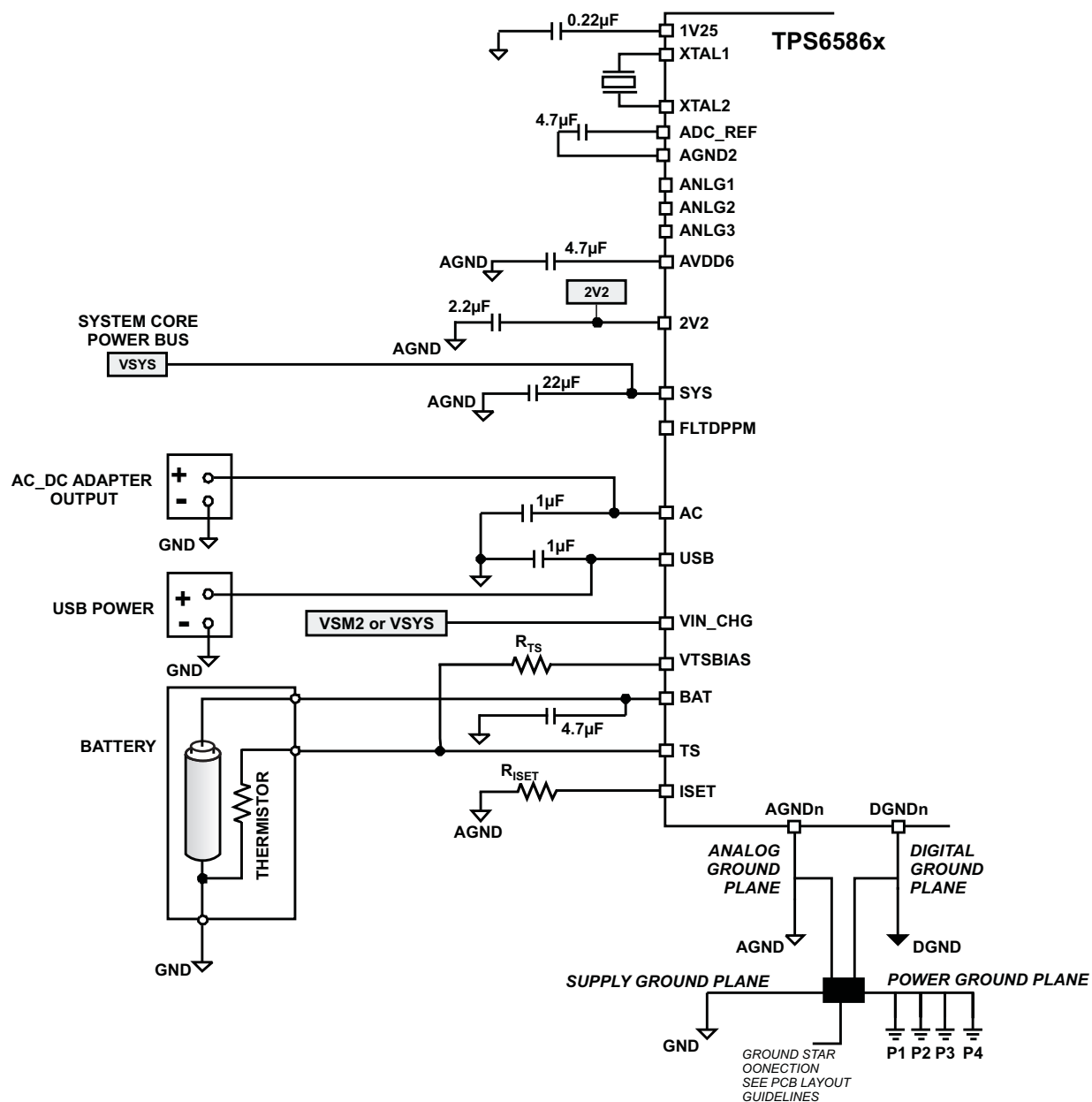
- Layout a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.

- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- External capacitance is recommended for precision real-time clock applications.



## 4.3 APPLICATION CIRCUIT

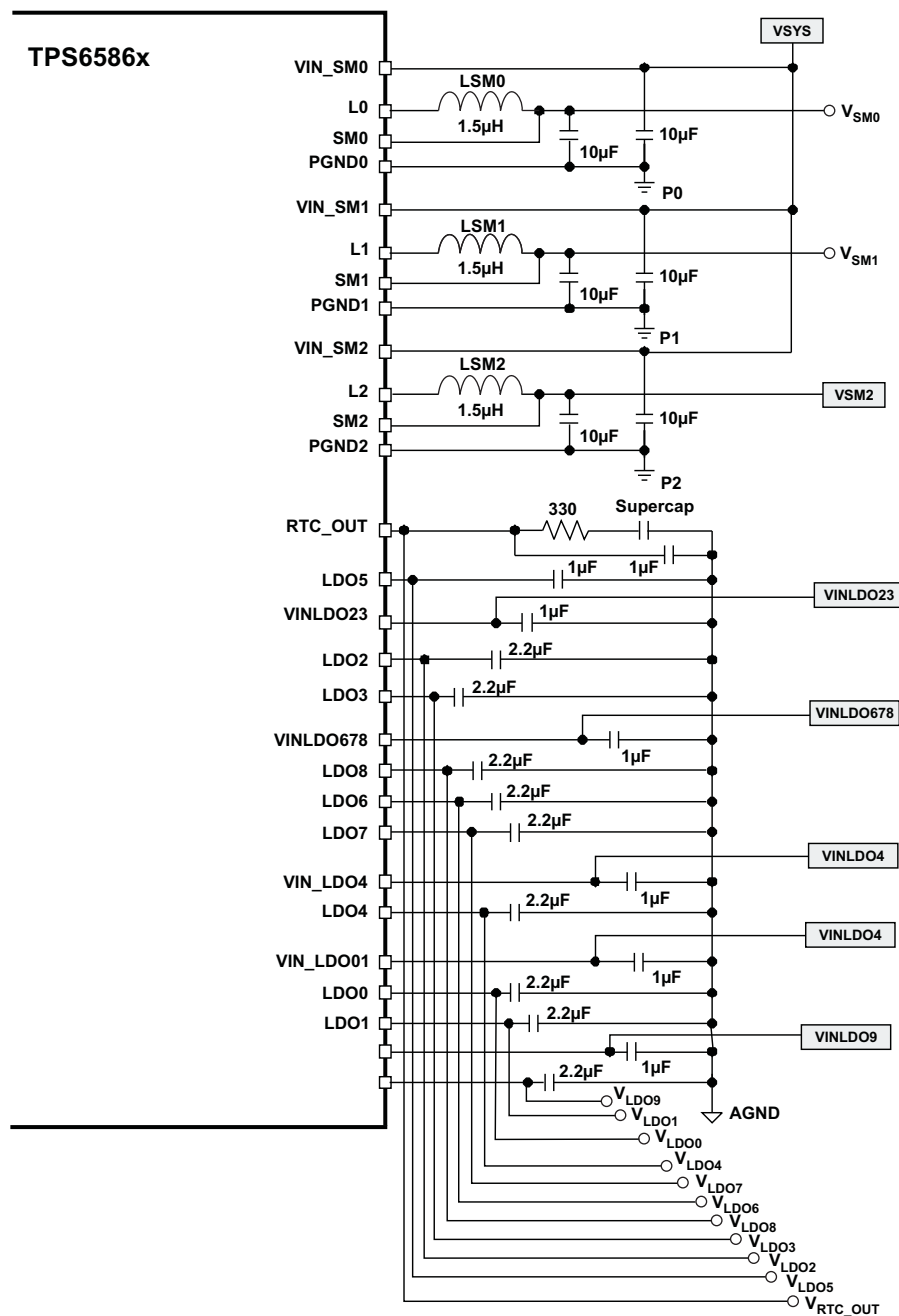
### 4.3.1 Power Path , Charger, ADC, RTC and Ground Plane



(1) VIN\_CHG should be connected to VSYS when SM2 is not configured as the charger pre-regulator stage

**Figure 4-1. Power Path, Charger, ADC, RTC Connections**

### 4.3.2 Integrated Supplies

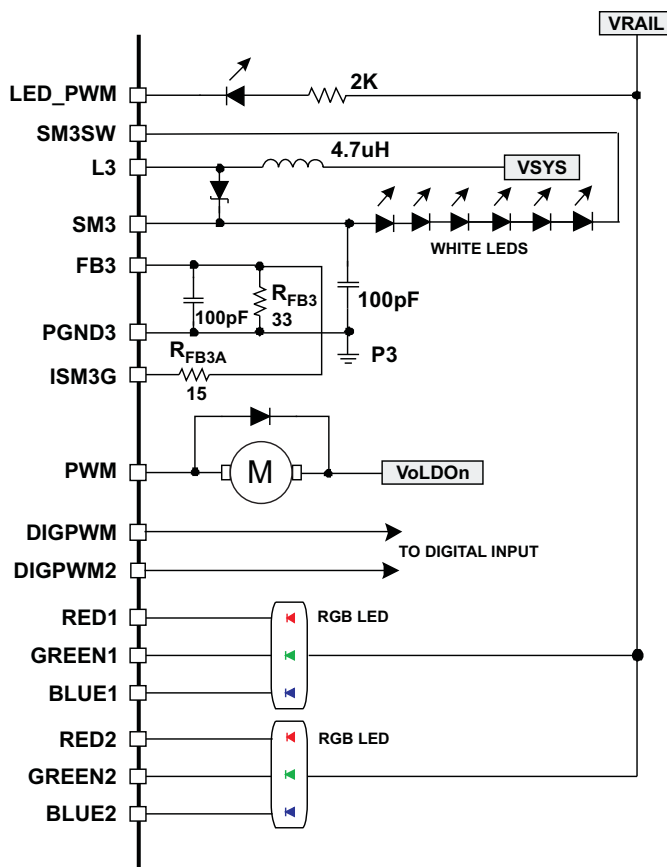


- (1) VIN\_SMn pins must be always connected to VSYS .
- (2) The supply input pins must be connected to VSYS or to the output of a supply which is powered from VSYS

**Figure 4-2. Supply Rail Connections**

### 4.3.3 Display and Peripherals

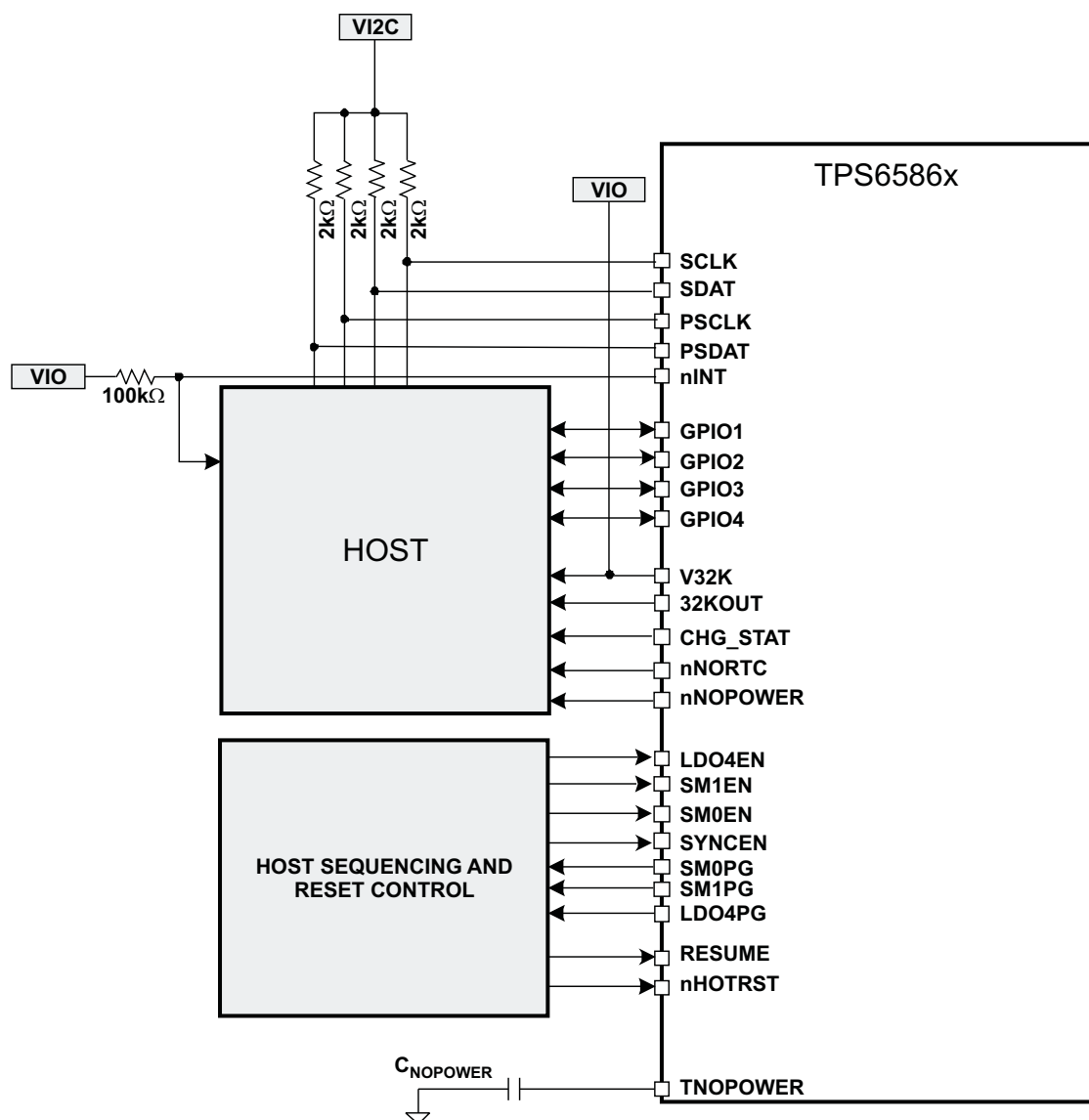
TPS6586x



- (1) PWM pin shown as driving an external vibrator motor, with vibrator supply connected to LDO output
- (2) VRAIL can be the output of any of the TPS658621A integrated supplies or the SYS pin
- (3) 1. DIGPWM, DIGPWM2 are push-pull outputs

Figure 4-3. Display and PWM Connections

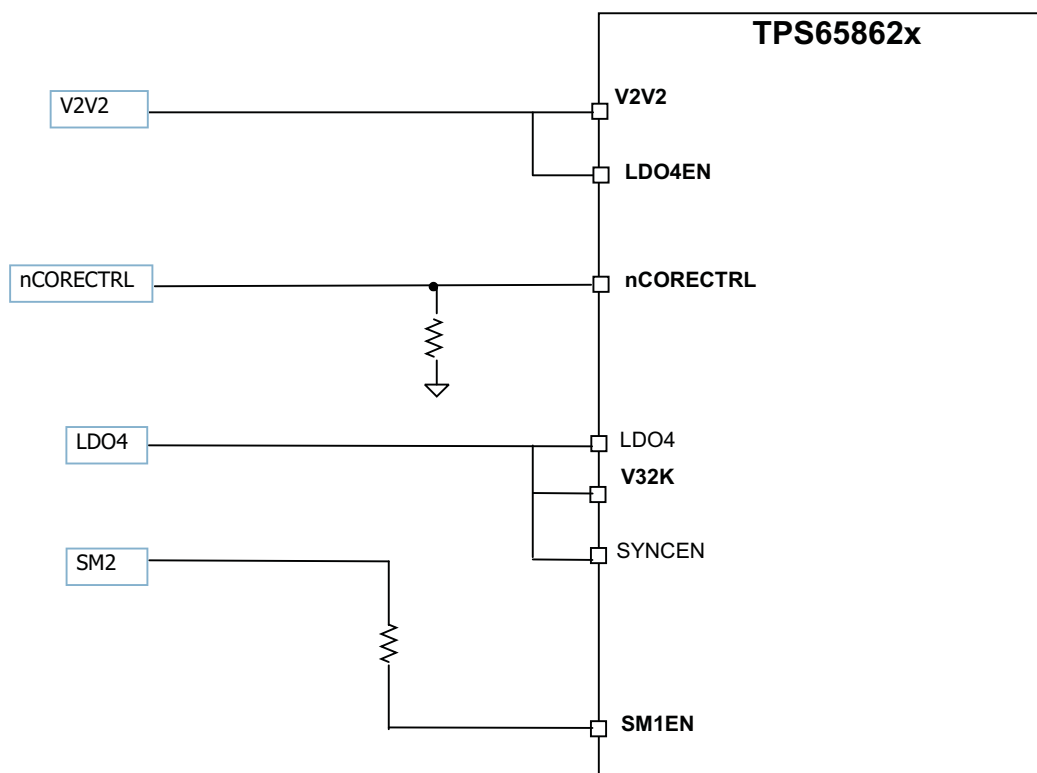
### 4.3.4 Host Connections



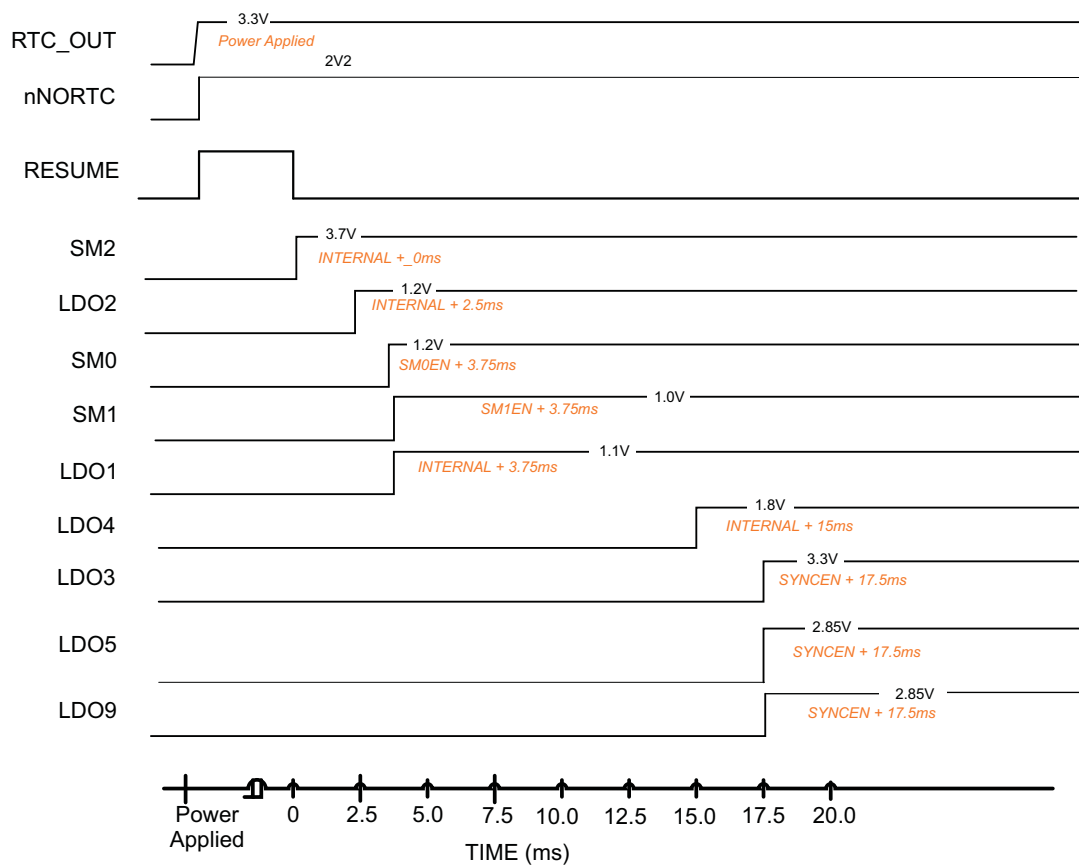
- (1) Those are generic connections only, see App Notes for host specific connectivity
- (2) VIO should be connected to the TPS658621A rail that powers the host I/O domain
- (3) VI2C should be connected to 2v2 or to the TPS658621A rail that powers the host I<sup>2</sup>C engine domain

**Figure 4-4. Generic Host and Sequencing Circuit Connections**

### 4.3.5 Sequence Connections



### 4.3.6 Sequence Timing (TPS658621A)



**Figure 4-5. Sequence Timing**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type     | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login)          |
|------------------|-----------------------|------------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|--------------------------------------|
| TPS658621AZGUR   | ACTIVE                | BGA<br>MICROSTAR | ZGU             | 169  | 1000        | Green (RoHS<br>& no Sb/Br) | SNAGCU               | Level-3-260C-168 HR          | <a href="#">Purchase Samples</a>     |
| TPS658621AZGUT   | ACTIVE                | BGA<br>MICROSTAR | ZGU             | 169  | 250         | Green (RoHS<br>& no Sb/Br) | SNAGCU               | Level-3-260C-168 HR          | <a href="#">Request Free Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type  | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|---------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS658621AZGUR | BGA MICROSTAR | ZGU             | 169  | 1000 | 330.0              | 24.4               | 12.3    | 12.3    | 2.3     | 16.0    | 24.0   | Q1            |
| TPS658621AZGUT | BGA MICROSTAR | ZGU             | 169  | 250  | 330.0              | 24.4               | 12.3    | 12.3    | 2.3     | 16.0    | 24.0   | Q1            |



## TAPE AND REEL BOX DIMENSIONS

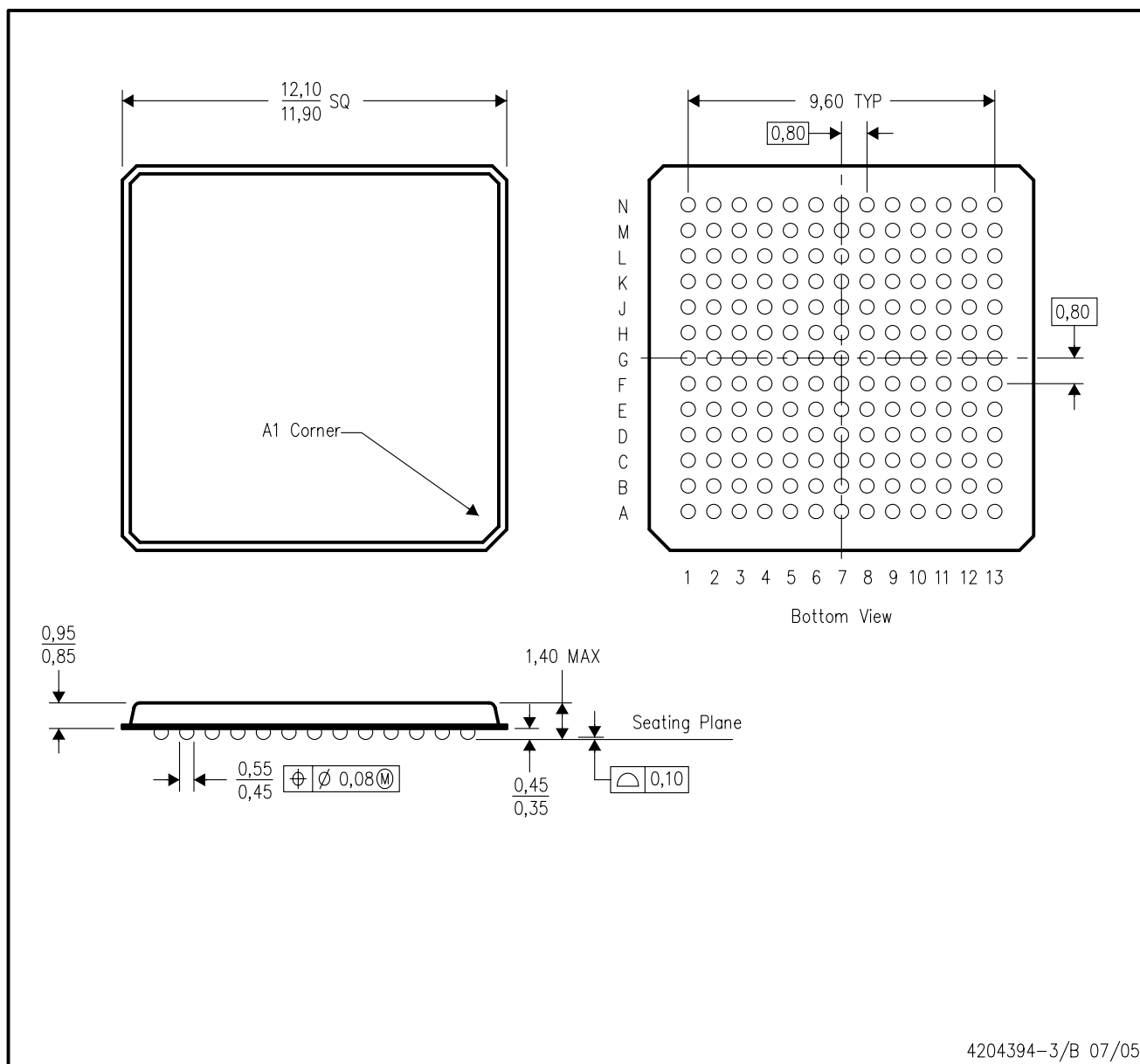


\*All dimensions are nominal

| Device         | Package Type  | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|---------------|-----------------|------|------|-------------|------------|-------------|
| TPS658621AZGUR | BGA MICROSTAR | ZGU             | 169  | 1000 | 333.2       | 345.9      | 31.8        |
| TPS658621AZGUT | BGA MICROSTAR | ZGU             | 169  | 250  | 333.2       | 345.9      | 31.8        |

## ZGU (S-PBGA-N169)

## PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Micro Star BGA configuration
  - D. This is a lead-free solder ball design.

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