



TPS6581x Single-Cell Li-Ion Battery and Power Management IC

1 Features

- Battery Charger
 - Complete Charge Management Solution for Single Li-Ion or Li-Pol Cell:
 - With Thermal Foldback, Dynamic Power Management, and Pack Temperature-Sensing
 - Supports Up to 1.5-A Maximum Charge Current
 - Programmable Charge Parameters for AC Adapter and USB Port Operation
- Integrated Power Supplies
 - Total of 9 integrated LDOs:
 - 6 Adjustable-Output LDOs (1.25 V to 3.3 V)
 - 2 Fixed-Voltage LDOs (3.3 V)
 - 1 RTC Backup Supply With Low Leakage (1.5 V)
 - 2 0.6-V to 3.4-V Programmable DC–DC Buck Converters (600 mA for TPS65810, 750 mA for TPS65811)
 - With Enable, Standby Mode Operation, and Automatic Low-Power Mode Setting
- Display Functions
 - 2 Open-Drain PWM Outputs With Programmable Frequency and Duty Cycle
 - Control of Keyboard Backlight, Vibrator, or Other External Peripheral Functions
 - RGB LED Driver With Programmable Flashing Period and Individual RGB Brightness Control
 - Constant-Current White LED Driver
 - With Programmable Current Level, Brightness Control, and Overvoltage Protection
 - Can Drive up to 6 LEDs in Series Configuration
- System Management
 - Dual Input Power Path Function With Input Current-Limiting and OVP Protection
 - POR Function With Programmable Masking Monitors All Integrated Supplies Outputs
 - Software and Hardware Reset Functions
 - 8-Channel Integrated A/D Samples System Parameters
 - With Single Conversion, Peak Detection, or Averaging Operating Modes

- Host Interface
 - Host Can Set System Parameters and Access System Status Using I²C Interface
 - Interrupt Function With Programmable Masking Signals System Status Modification to Host
 - 3 GPIO Ports, Programmable as Drivers, Integrated A/D Trigger or Buck Converters Standby Mode Control

2 Applications

- PDAs
- Smart Phones
- MP3s
- Internet Appliances
- Handheld Devices

3 Description

The TPS65810 device provides an easy-to-use, fully-integrated solution for handheld devices, integrating charge management, multiple regulated power supplies, system management, and display functions in a small, thermally-enhanced 8-mm × 8-mm package. The high level of integration enables space savings of 70% of the typical board area when compared to equivalent discrete solutions, while implementing a high-performance and flexible solution that is portable across multiple platforms.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-----------------------|----------|-------------------|
| TPS65810, TPS65811 | QFN (56) | 8.00 mm × 8.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

QFN Package

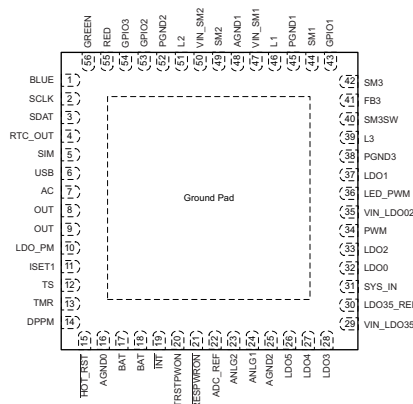


Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 Features | 1 | 7.16 Timing Requirements – I ² C Interface..... | 18 |
| 2 Applications | 1 | 7.17 Trigger Timing Characteristics | 19 |
| 3 Description | 1 | 7.18 Dissipation Ratings | 19 |
| 4 Revision History | 2 | 7.19 Typical Characteristics | 20 |
| 5 Description (continued) | 3 | 8 Detailed Description | 23 |
| 6 Pin Configuration and Functions | 3 | 8.1 Overview | 23 |
| 7 Specifications | 6 | 8.2 Functional Block Diagram | 23 |
| 7.1 Absolute Maximum Ratings | 6 | 8.3 Feature Description..... | 24 |
| 7.2 ESD Ratings..... | 6 | 8.4 Device Functional Modes..... | 69 |
| 7.3 Recommended Operating Conditions..... | 7 | 8.5 Programming..... | 69 |
| 7.4 Thermal Information | 7 | 8.6 Register Maps | 73 |
| 7.5 Electrical Characteristics – System Sequencing and Operating Modes | 8 | 9 Application and Implementation | 84 |
| 7.6 Electrical Characteristics – Power Path and Charge Management | 9 | 9.1 Application Information..... | 84 |
| 7.7 Electrical Characteristics – Power Path and Charge Management (Continued) | 10 | 9.2 Typical Applications | 85 |
| 7.8 Electrical Characteristics – Power Path and Charge Management (Continued) | 11 | 10 Power Supply Recommendations | 91 |
| 7.9 Electrical Characteristics – Linear Regulators | 12 | 11 Layout | 91 |
| 7.10 Electrical Characteristics – Switched-Mode SM1 Step-Down Converter | 14 | 11.1 Layout Guidelines | 91 |
| 7.11 Electrical Characteristics – Switched-Mode SM2 Step-Down Converter | 15 | 11.2 Layout Example | 92 |
| 7.12 Electrical Characteristics – GPIOs..... | 15 | 12 Device and Documentation Support | 93 |
| 7.13 Electrical Characteristics – ADC | 16 | 12.1 Device Support..... | 93 |
| 7.14 Electrical Characteristics – LED and PWM Drivers..... | 17 | 12.2 Related Documentation..... | 93 |
| 7.15 Electrical Characteristics – I ² C Interface | 18 | 12.3 Related Links | 93 |
| | | 12.4 Community Resources..... | 93 |
| | | 12.5 Trademarks | 93 |
| | | 12.6 Electrostatic Discharge Caution..... | 93 |
| | | 12.7 Glossary | 93 |
| | | 13 Mechanical, Packaging, and Orderable Information | 94 |

4 Revision History

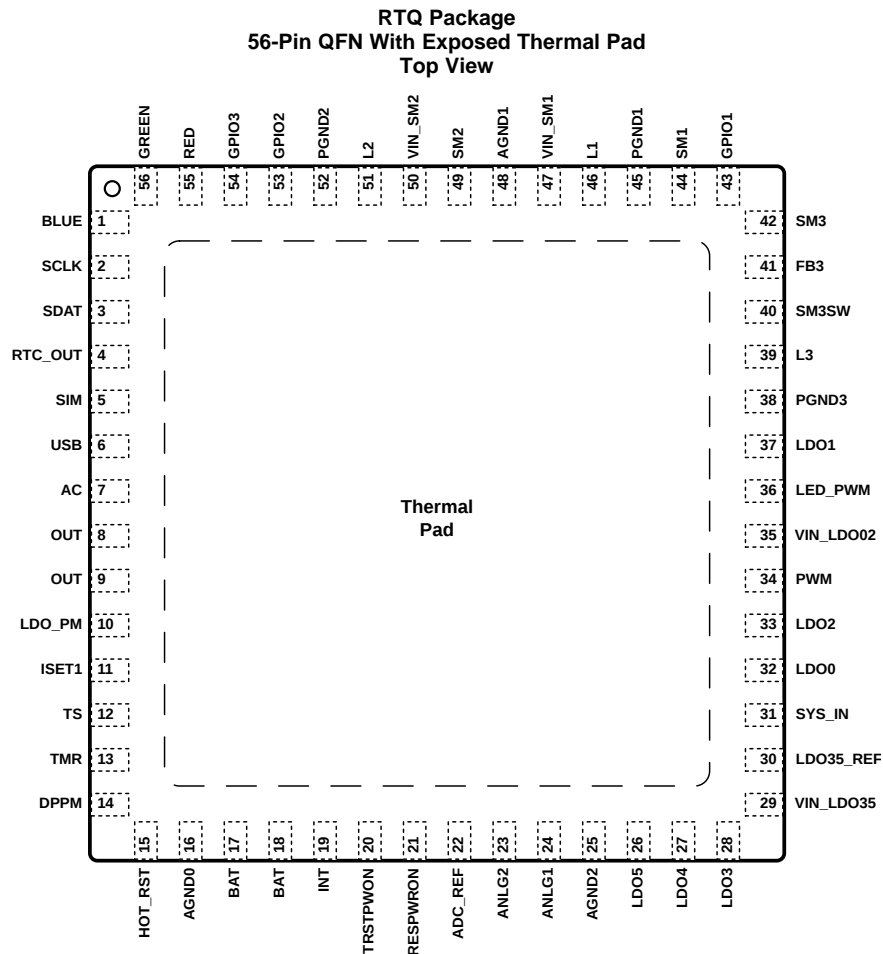
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (February 2007) to Revision C | Page |
|--|----------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted the lead temperature from the <i>Absolute Maximum Ratings</i> table | 6 |

5 Description (continued)

If required, an external host can control the TPS65810 device through I²C interface with access to all integrated systems. The I²C enables the setting of the output voltages, current thresholds, and operation modes. The internal registers have a complete set of status information, enabling easy diagnostics, and host-controlled handling of fault conditions. The TPS65810 device can operate in standalone mode, with no external host control, if the internal power-up defaults are compatible with the system requirements.

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION | EXTERNAL REQUIRED COMPONENTS (See Figure 51) |
|---------|-----|-----|--|---|
| NAME | NO. | | | |
| AC | 7 | I | Adapter charge input voltage, connect to AC_DC adapter positive output terminal (DC voltage) | 1-μF (minimum) capacitor to AGND1 pin to minimize overvoltage transients during AC power hot-plug events. |
| ADC_REF | 22 | I/O | ADC internal reference filter or ADC external reference input | 4.7-μF (minimum) to 10-μF (maximum) capacitor connected to AGND2 pin |
| AGND0 | 16 | — | Analog ground connection | Connect to analog ground plane |
| AGND1 | 48 | — | Analog ground pin | Connect to analog ground plane |
| AGND2 | 25 | — | Analog ground pin | Connect to analog ground plane |
| ANLG1 | 24 | I | Analog input to ADC, programmable current source output | Can be used to monitor additional system or pack parameters |
| ANLG2 | 23 | I | Analog input to ADC, programmable current source output | Can be used to monitor additional system or pack parameters |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION | EXTERNAL REQUIRED COMPONENTS (See Figure 51) |
|---------------------|-----|-----|---|--|
| NAME | NO. | | | |
| BAT | 17 | I/O | Battery power | Connect to battery positive terminal. Connect a 10-μF capacitor (minimum) from BAT pin to AGND1 pin. |
| | 18 | | | |
| BLUE | 1 | O | Programmable blue driver, open-drain output, current sink output when active. | Connect to BLUE input of RGB LED |
| DPPM | 14 | I | Dynamic power path management set-point | External resistor from DPPM pin to AGND1 pin sets the DPPM regulation threshold. 1-nF (minimum) capacitor to from DPPM to AGND1 sets BAT to OUT short circuit blanking delay when battery is hot-plugged into system |
| Exposed thermal pad | 57 | — | An internal electrical connection exists between the exposed thermal pad and AGNDn pins of the device. The exposed thermal pad must be connected to the same potential as the AGND1 pin on the printed-circuit-board. Do not use the thermal pad as the primary ground input for the device. AGNDn pins must be connected to a clean ground plane at all times. | |
| FB3 | 41 | I/O | White LED duty cycle switch output, LED current setting | External resistor from FB3 pin to PGND3 pin sets LED peak current. Connect a 100-pF (minimum) filter capacitor to PGND3 pin. |
| GPIO1 | 43 | I/O | General-purpose programmable I/O | Power-up default: SM1 enable control, SM1 ON at GPIO1 = HI. |
| GPIO2 | 53 | I/O | General-purpose programmable I/O | Power-up default: SM2 enable control, SM2 ON at GPIO2 = HI. |
| GPIO3 | 54 | I/O | General-purpose programmable I/O. | Example: ADC conversion start trigger. |
| GREEN | 56 | O | Programmable LED driver, open-drain output, current sink output when active. | Connect to GREEN input of RGB LED |
| HOT_RST | 15 | I/O | Hardware reset input, reset generated when connected to ground | Connect to an external push-button switch. Connect to external pullup resistor. |
| INT | 19 | O | Interruption pin, open-drain output | Connect 100-kΩ external pullup resistor between INT and OUT. INT pin is LO when interrupt is requested by the TPS65810 device. |
| ISSET1 | 11 | I | Current set point when charging in auto mode with AC selected. Precharge and charge termination set point for all charge modes | External resistor from ISET1 pin to AGND1 pin sets charge current value |
| L1 | 46 | O | SM1 synchronous buck converter power-stage output | 3.3-μH inductor to SM1 pin |
| L2 | 51 | O | SM2 synchronous buck converter power-stage output | 3.3-μH inductor to SM2 pin |
| L3 | 39 | O | Drain of the integrated boost power-stage switch | 4.7-μH inductor to OUT pin, external Schottky diode to SM3 pin |
| LDO0 | 32 | O | LDO0 output, fixed voltage | 1-μF (minimum) capacitor to AGND1 |
| LDO1 | 37 | O | LDO1 output | 1-μF (minimum) capacitor to AGND1 |
| LDO2 | 33 | O | LDO2 output | 1-μF (minimum) capacitor to AGND1 |
| LDO3 | 28 | O | LDO3 output | 2.2-μF (minimum) capacitor to AGND2 |
| LDO35_REF | 30 | I | Linear regulators LDO3-5 reference filter | 100-nF capacitor to AGND2 |
| LDO4 | 27 | O | LDO4 output | 2.2-μF (minimum) capacitor to AGND2 |
| LDO5 | 26 | O | LDO5 output | 2.2-μF (minimum) capacitor to AGND2 |
| LDO_PM | 10 | O | General-purpose LDO output | 1-μF (minimum) capacitor to AGND1 pin |
| LED_PWM | 36 | O | PWM driver output, open-drain | Can be used to drive a keyboard backlight LED |
| OUT | 8 | O | Power-path output. Connect to system main power rail (system power bus) | 10-μF capacitor to AGND1 pin |
| | 9 | | | |
| PGND1 | 45 | — | SM1 synchronous buck converter power ground | Connect to power ground plane |
| PGND2 | 52 | | | |
| PGND3 | 38 | — | White LED driver power ground input. | Connect to a power ground plane |
| PWM | 34 | O | PWM driver output, open-drain | Can be used to drive a vibrator or other external functions |
| RED | 55 | O | Programmable LED driver, open-drain output, current sink output when active | Connect to RED input of RGB LED |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION | EXTERNAL REQUIRED COMPONENTS (See Figure 51) |
|------------------------------|-----|-----|--|--|
| NAME | NO. | | | |
| $\overline{\text{RESPWRON}}$ | 21 | O | System reset, open-drain output | 100-k Ω external pullup resistor to OUT. $\overline{\text{RESPWRON}}$ pin is LO when the TPS65810 device is resetting the system. |
| RTC_OUT | 4 | O | Low leakage LDO output. Can be connected to a super-capacitor or secondary cell, if used as a RTC backup output. | 1- μ F (minimum) capacitor to AGND1 pin or supercapacitor |
| SCLK | 2 | I | I ² C interface clock line | 2-k Ω pullup resistor to OUT pin |
| SDAT | 3 | I/O | I ² C interface data line | 2-k Ω pullup resistor to OUT pin |
| SIM | 5 | O | General-purpose LDO output | 1- μ F (minimum) capacitor to AGND1 pin |
| SM1 | 44 | I | SM1 synchronous buck converter output voltage sense | LC filter: 10- μ F capacitor to PGND1 pin |
| SM2 | 49 | I | SM2 synchronous buck converter output voltage sense | LC filter: 10- μ F capacitor to PGND2 pin |
| SM3 | 42 | I | White LED driver output overvoltage detection | Connect 1- μ F capacitor to PGND3 pin. Connect SM3 pin to the positive side of white LED ladder. |
| SM3SW | 40 | I | Integrated white LED duty cycle switch input | Connect to negative side of external LED ladder |
| SYS_IN | 31 | I | System power bus low-voltage detection | External resistive divider sets minimum system operational voltage. The TPS65810 device enters sleep mode when voltage below minimum system voltage threshold is detected. 1-nF filter capacitor to AGND1 recommended. |
| TMR | 13 | I | Charge safety timer program input | External resistor from TMR pin to AGND1 pin sets the charge safety timer time-out value |
| TRSTPWON | 20 | I | System reset pulse-duration setting | 100-nF (minimum) capacitor to AGND. External capacitor from TRSTPWON pin to AGND1 pin sets $\overline{\text{RESPWRON}}$ pulse duration. |
| TS | 12 | I/O | Temperature sense input, current source output | Connect to battery pack thermistor to sense battery pack temperature. Connect to external pullup resistor. |
| USB | 6 | I | USB charge input voltage, connect to USB port positive power output | 1- μ F (minimum) capacitor to AGND1 pin, to minimize overvoltage transients during USB power hot-plug events. |
| VIN_LDO35 | 29 | — | Input to LDOs 3 to 5 | 1- μ F (minimum) decoupling capacitor to AGND2 |
| VIN_LDO02 | 35 | — | Positive supply input for LDO0, LDO1, LDO2 | 1- μ F (minimum) decoupling capacitor to AGND1 |
| VIN_SM1 | 47 | — | SM1 synchronous buck converter positive supply input | 10- μ F capacitor to PGND1 pin |
| VIN_SM2 | 50 | — | SM2 synchronous buck converter positive supply input | 10- μ F capacitor to PGND2 pin |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|--|------|---------------------------|------|
| AC and USB with respect to AGND1 | −0.3 | 18 | V |
| ANLG1, ANLG2 with respect to AGND2 | −0.3 | V(OUT) | V |
| V(OUT) with respect to AGND1 | | 5 | V |
| VIN_LDO12, VIN_LDO35, LDO3, LDO4, LDO5 with respect to AGND2 | −0.3 | V(OUT) | V |
| LDO35_REF, ADC_REF with respect to AGND2 | −0.3 | Smaller of: 3.6 or V(OUT) | V |
| SIM, RTC_OUT with respect to AGND1 | −0.3 | Smaller of: 3.6 or V(OUT) | V |
| SM1, L1, VIN_SM1 with respect to PGND1 | −0.3 | V(OUT) | V |
| SM2, L2, VIN_SM2 with respect to PGND2 | −0.3 | V(OUT) | V |
| SM3, L3 with respect to PGND3 | −0.3 | 29 | V |
| SM3SW with respect to PGND3 | −0.3 | V(OUT) | V |
| FB3 with respect to PGND3 | −0.3 | 0.5 | V |
| All other pins (except AGND and PGND), with respect to AGND1 | −0.3 | V(OUT) | V |
| AGND2, AGND0, PGND1, PGND2, PGND3 with respect to AGND1 | −0.3 | 0.3 | V |
| Input Current, AC pin | | 2750 | mA |
| Input Current, USB pin | | 600 | mA |
| Output continuous current, OUT pin | | 3000 | mA |
| Output continuous current, BAT pin | | −3000 | mA |
| Continuous Current at L1, PGND1, L2, PGND2 | | 1800 | mA |
| T _A Operating free-air temperature | −40 | 85 | °C |
| T _J Maximum junction temperature | | 125 | °C |
| T _{stg} Storage temperature | −65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | VALUE | UNIT |
|--|-------|------|
| V _(ESD) Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 1500 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|-----------------------------------|--|--------------------|---------------------|------|
| AC and USB with respect to AGND1 | | 4.35 | 16.5 ⁽¹⁾ | V |
| ANLG1,ANLG2 with respect to AGND2 | | 0 | 2.6 | V |
| VIN_LDO35 with respect to AGND2 | | See ⁽²⁾ | 4.7 | V |
| VIN_LDO12 with respect to AGND1 | | See ⁽²⁾ | 4.7 | V |
| VIN_SM1 with respect to PGND1 | | See ⁽²⁾ | 4.7 | V |
| VIN_SM2 with respect to PGND2 | | See ⁽²⁾ | 4.7 | V |
| SM3 with respect to PGND3 | | | 28 | V |
| T _A | Operating free-air temperature | –40 | 85 | °C |
| T _{J(op)} | Junction temperature, functional operation ensured | –40 | 125 | °C |
| T _J | Junction temperature, electrical characteristics ensured | 0 | 125 | °C |

(1) Thermal operating restrictions are reduced or avoided if input voltage does not exceed 5 V.

(2) Greater of: 3.6 V OR minimum input voltage required for LDO/converter operation outside dropout region.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS6581x | UNIT |
|-------------------------------|--|-----------|------|
| | | RTQ (QFN) | |
| | | 56 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 26.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 10.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 4.9 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.2 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 4.8 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics – System Sequencing and Operating Modes

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|------|-----|------|------------------|
| QUIESCENT CURRENT | | | | | | |
| $I_{\text{BAT(SLEEP)}}$ | BAT pin current, sleep mode set | Input power not detected, $V(\text{BAT}) = 4.2\text{ V}$, Sleep mode set | | 400 | | μA |
| $I_{\text{BAT(DONE)}}$ | BAT pin current, charge terminated | Charger function enabled by $I^2\text{C}$, termination detected, input power detected and selected | | 3 | | μA |
| $I_{\text{BAT(CHGOFF)}}$ | BAT pin current, charge function OFF | Charger function disabled by $I^2\text{C}$, termination not detected, input power detected and selected | | 3 | | μA |
| $I_{\text{INP(CHGOFF)}}$ | AC or USB pin current, charge function OFF | Charger function disabled by $I^2\text{C}$, termination not detected, input power detected and selected. All integrated supplies and drivers OFF, no load at OUT pin. | | | 200 | μA |
| UNDERVOLTAGE LOCKOUT | | | | | | |
| V_{UVLO} | Internal UVLO detection threshold | NO POWER mode set at $V(\text{OUT}) < V_{\text{UVLO}}$, $V(\text{OUT})$ decreasing | -3% | 2.5 | 3% | V |
| $V_{\text{UVLO_HYS}}$ | UVLO detection hysteresis | $V(\text{OUT})$ increasing | | 120 | | mV |
| $t_{\text{DGL(UVLO)}}$ | UVLO detection deglitch time | Falling voltage only | | 5 | | ms |
| SYSTEM LOW VOLTAGE THRESHOLD | | | | | | |
| $V_{\text{LOW_SYS}}$ | Minimum system voltage detection threshold | System voltage $V(\text{SYS_IN})$ decreasing, SLEEP mode set if $V(\text{SYS_IN}) < V_{\text{LOW_SYS}}$ | 0.97 | 1 | 1.03 | V |
| $V_{\text{HYS(LOWSYS)}}$ | Minimum system voltage detection hysteresis | $V(\text{SYS_IN})$ increasing | | 50 | | mV |
| $t_{\text{DGL(LOWSYS)}}$ | Minimum system voltage detection deglitch time | $V(\text{SYS_IN})$ decreasing | | 5 | | ms |
| THERMAL FAULT | | | | | | |
| T_{SHUT} | Thermal shutdown | Increasing junction temperature | | 165 | | $^\circ\text{C}$ |
| $T_{\text{HYS(SHUT)}}$ | Thermal shutdown hysteresis | Decreasing junction temperature | | 30 | | $^\circ\text{C}$ |
| INTEGRATED SUPPLY POWER FAULT DETECTION | | | | | | |
| V_{PGOOD} | Power-good fault detection threshold | Falling output voltage, applies to all integrated supply outputs. Referenced to the programmed output voltage value | 84% | 90% | 96% | |
| $V_{\text{HYS(PGOOD)}}$ | Power-good fault detection hysteresis | Rising output voltage, applies to all integrated supply outputs. Referenced to V_{PGOOD} threshold | 3% | 5% | 7% | |
| HOT RESET FUNCTION | | | | | | |
| V_{HRSTON} | Low level input voltage | RESET mode set at $V(\text{HOT_RESET}) < V_{\text{HRSTON}}$ | | | 0.4 | V |
| V_{HRSTOFF} | High level input voltage | HOT reset not active at $V(\text{HOT_RESET}) > V_{\text{HRSTOFF}}$ | 1.3 | | | V |
| $t_{\text{DGL(HOTRST)}}$ | Hot reset input deglitch | | | 5 | | ms |
| SYSTEM RESET – OPEN-DRAIN OUTPUT RESPWRON | | | | | | |
| V_{RSTLO} | Low level output voltage | $I_{\text{IL}} = 10\text{ mA}$, $V(\text{RESPWRON}) < V_{\text{RSTLO}}$ | 0 | | 0.3 | V |
| I_{TRSTPWON} | Pullup current source | Internally connected to TRSTPWON pin | 0.9 | 1 | 1.2 | μA |
| K_{RESET} | Reset timer constant | $T_{\text{RESET}} = K_{\text{RESET}} \times C_{\text{TRSTPWON}}$ | | 1 | | ms/nF |

7.6 Electrical Characteristics – Power Path and Charge Management

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-----|------|------|------------|
| VOLTAGE DETECTION THRESHOLDS | | | | | | |
| $V_{IN(DT)}$ | Input Voltage detection threshold | AC detected at $V(AC) - V(BAT) > V_{IN(DT)}$ USB detected at $V(USB) - V(BAT) > V_{IN(DT)}$ | 190 | | | mV |
| $V_{IN(NDT)}$ | Input Voltage removal threshold | AC not detected at $V(AC) - V(BAT) < V_{IN(NDT)}$ USB not detected at $V(USB) - V(BAT) < V_{IN(NDT)}$ | | | 125 | mV |
| $t_{DGL(NDT)}$ | Power not detected deglitch | | | 22.5 | | ms |
| $V_{SUP(DT)}$ | Supplement detection threshold | Battery switch ON at $V(BAT) - V(OUT) > V_{SUP(DT)}$ | | 60 | | mV |
| $V_{SUP(NDT)}$ | Supplement not detected threshold | Battery switch OFF at $V(BAT) - V(OUT) < V_{SUP(NDT)}$ | | 20 | | mV |
| POWER PATH INTEGRATED MOSFETS CHARACTERISTICS | | | | | | |
| V_{ACDO} | AC switch dropout voltage | $V_{ACDO} = V(AC) - V(OUT)$; $V(AC) = 4.75\text{ V}$ AC input current limit set to 2.75 A (typical), $I_{O(OUT)} = 1\text{ A}$ | | 350 | 375 | mV |
| V_{USBDO} | USB switch dropout voltage | $V_{USBDO} = V(USB) - V(OUT)$; $V(USB) = 4.6\text{ V}$ USB input current limit set to 2.75 A (typical) | | 175 | 190 | mV |
| | | $I(OUT) + I(BAT) = 0.5\text{ A}$ $I(OUT) + I(BAT) = 0.1\text{ A}$ | | 35 | 45 | mV |
| $V_{BATDODCH}$ | Battery switch dropout voltage, discharge | $V(BAT): 3\text{ V} \rightarrow V_{CH(REG)}$, $I(BAT) = -1\text{ A}$ | | 60 | 100 | mV |
| $V_{BATDOCH}$ | Battery switch dropout voltage, charge | Charger on, $V(BAT): 3\text{ V} \rightarrow 4.2\text{ V}$, $I(BAT) = 1\text{ A}$ | | 60 | 100 | mV |
| POWER PATH INPUT CURRENT LIMIT | | | | | | |
| $I_{INP(LIM1)}$ | Selected input current limit, applies to USB input only | Selected input switch not in dropout, I ² C settings: ISET2 = LO, PSEL = LO | 80 | | 100 | mA |
| $I_{INP(LIM2)}$ | Selected Input current limit, applies to USB input only | Selected input switch not in dropout, I ² C settings: ISET2 = HI, PSEL = LO | 400 | | 500 | mA |
| $I_{INP(LIM3)}$ | Selected Input current limit, applies to either AC or USB input | Selected input switch not in dropout, I ² C settings: ISET2 = HI OR LO, PSEL = HI | | | 2.75 | A |
| SYSTEM REGULATION VOLTAGE | | | | | | |
| $V_{SYS(REG)}$ | Output regulation voltage | $V_{SYS(REG)} = V(OUT)$, DPPM loop not active, selected input current limit not reached. Selected input voltage (AC or USB) > 5.1 V | | 4.6 | 4.7 | V |
| POWER PATH PROTECTION AND RECOVERY FUNCTIONS | | | | | | |
| $V_{INOUTSH}$ | Input-to-output short-circuit detection threshold | AC and USB switches set to OFF if $V(OUT) < V_{INOUTSH}$ | | 0.6 | | V |
| $R_{SH(USBSH)}$ | OUT short circuit recovery pullup resistor | $V(OUT) < 1\text{ V}$, internal resistor connected from USB to OUT | | 500 | | Ω |
| $R_{SH(ACSH)}$ | OUT short circuit recovery pullup resistor | $V(OUT) < 1\text{ V}$, internal resistor connected from AC to OUT | | 500 | | Ω |
| V_{OVP} | Overvoltage detection threshold | Rising voltage, overvoltage detected when $V(AC) > V_{OVP}$ or $V(USB) > V_{OVP}$ | 6 | 6.5 | 6.8 | V |
| | Overvoltage detection hysteresis | Falling voltage, relative to detection threshold | | 0.1 | | V |
| $V_{BATOUTSH}$ | Battery-to-output short-circuit detection threshold | BAT switch set to OFF if $V(BAT) - V(OUT) > V_{BATOUTSH}$ | | 200 | | mV |
| $K_{BLK(SHBAT)}$ | Battery-to-output short-circuit blanking time constant | $V(DPPM) < 1\text{ V}$, $t_{BLK(SHBAT)} = K_{BLK(SHBAT)} \times C_{DPPM}$, C_{DPPM} capacitor is connected from DPPM pin to AGND1 | | 1 | | mS/nF |
| $I_{SH(BAT)}$ | OUT short circuit recovery pullup current source | $V(BAT) - V(OUT) > V_{BATOUTSH}$, Internal current source connected between OUT and BAT | | 10 | | mA |
| $R_{SH(BAT)}$ | BAT short circuit recovery resistor | $V(BAT) < 1\text{ V}$, Internal resistor connected from OUT to BAT | | 1 | | k Ω |
| $R_{DCH(BAT)}$ | BAT pulldown resistor | Internal resistor connected from BAT to AGND1 when battery is not detected by ANLG1 | | 500 | | Ω |

7.7 Electrical Characteristics – Power Path and Charge Management (Continued)

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|---|---|---|---|-------|-------|-----|
| POWER PATH TIMING CHARACTERISTICS, DPPM, AND THERMAL LOOPS NOT ACTIVE, R _{TMR} = 50 kΩ | | | | | | | |
| t _{BOOT} | Boot-up time | Measured from input power detection | 120 | 200 | 300 | ms | |
| t _{SW(ACBAT)} | Switching from AC to BAT | No USB: measured from V(AC) – V(BAT) < V _{IN(NDT)} , USB detected: CE = LO (after CE hold-off time) | | | 50 | μs | |
| t _{SW(USB BAT)} | Switching from USB to BAT | No AC: measured from V(USB) – V(BAT) < V _{IN(NDT)} , USB detected: CE = LO (after CE hold-off time) | | | 50 | μs | |
| t _{SW(PSEL)} | Switching from USB to AC | Toggling I ² C PSEL bit | | | 50 | μs | |
| t _{SW(ACUSB)} | Switching from AC to USB or USB to AC | AC power removed or USB power removed | | | 100 | μs | |
| BATTERY REMOVAL DETECTION | | | | | | | |
| V _{NOBATID} | Battery ID resistor detection | ID resistor not detected at V(OUT)– V(ANLG1) < V _{NOBATID} | | 0.5 | | V | |
| t _{DGL(NO BAT)} | Deglitch time for battery removal detection | | 0.6 | | 1.2 | ms | |
| I _{O(ANLG1)} | ANLG1 pullup current | Set through I ² C bits (BATID1,BATID2) ADC_WAIT register | 00, V _(OUT) : 2.5 V to 4.4 V | $\frac{V(OUT) - 1.2}{500\text{ k}\Omega}$ | | μA | |
| | | | 01 | 10 | | | |
| | | | 10 | 50 | | | |
| | | | 11 | 60 | | | |
| | | Total accuracy | | | 25% | | 25% |
| FAST CHARGE CURRENT, V(OUT) > V(BAT) + 0.1 V, V(BAT) > V _{LowV} | | | | | | | |
| I _{O(BAT)} | Charge current range | $I_{O(BAT)} = \frac{K_{(SET)} \times V_{(SET)}}{R_{SET}}$ | 100 | | 1500 | mA | |
| V _(SET) | Battery charge current set voltage | V _(SET) = V(SET1), (SET1_1, SET1_0) = | 11, 100% scaling | 2.475 | 2.500 | 2.525 | V |
| | | | 10, 75% scaling | 1.875 | 1.900 | 1.925 | |
| | | | 01, 50% scaling | 1.225 | 1.250 | 1.275 | |
| | | | 00, 25% scaling | 0.575 | 0.600 | 0.625 | |
| K _(SET) | Battery charge current set factor | 100 mA < I _{O(BAT)} ≤ 1 A | 350 | 400 | 450 | | |
| | | 1 mA < I _{O(BAT)} ≤ 100 mA | 100 | 400 | 1000 | | |
| PRECHARGE CURRENT, V(OUT) > V(BAT) + 0.1 V, V _{BATSH} < V(BAT) < V _{LowV} , t < t _(PRECHG) | | | | | | | |
| I _{O(PRECHG)} | Precharge current range | $I_{O(PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}}$ | 10 | | 150 | mA | |
| V _{PRECHG} | Precharge set voltage | V _{PRECHG} = V(SET1) | 220 | 250 | 270 | mV | |
| V _{LowV} | Precharge to fast-charge transition | Fast charge at V(BAT) > V _{LowV} | 2.8 | 3 | 3.2 | V | |
| t _{DGL(PRE)} | Deglitch time for fast charge to precharge transition | Decreasing battery voltage, R _{TMR} = 50 kΩ | | 22.5 | | ms | |
| CHARGE REGULATION VOLTAGE, V(OUT) > V _{O(BATREG)} + 0.1 V | | | | | | | |
| V _{O(BATREG)} | Battery charge voltage | Voltage options, selection through I ² C | 4.2 | | | V | |
| | | | 4.356 | | | V | |
| | | Accuracy, T _A = 25°C | –0.5% | | 0.5% | | |
| | | Total accuracy | –1% | | 1% | | |
| CHARGE TERMINATION, V(BAT) > V _{RCH} , VOLTAGE REGULATION MODE SET | | | | | | | |
| I _(TERM) | Charge termination current range | $I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}}$ | 10 | | 150 | mA | |
| V _(TERM) | Battery termination detection set voltage | V _(TERM) = V(SET1), (SET1_1, SET1_0) = | 11, 100% scaling | 240 | 260 | 280 | mV |
| | | | 10, 75% scaling | 145 | 160 | 175 | |
| | | | 01, 50% scaling | 90 | 110 | 130 | |
| | | | 00, 25% scaling | 40 | 60 | 75 | |
| t _{DGL(TERM)} | Deglitch time for termination detection | V(SET1) < V _(TERM) , R _{TMR} = 50 kΩ | | 22.5 | | ms | |

7.8 Electrical Characteristics – Power Path and Charge Management (Continued)

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-------|-----------------------|-------|------------------|
| BATTERY RECHARGE DETECTION | | | | | | |
| V_{RCH} | Recharge threshold voltage | New charge cycle starts if $V(\text{BAT}) < V_{O(\text{BATREG})} - V_{RCH}$, after termination was detected | 80 | 100 | 130 | mV |
| $t_{DGL(RCH)}$ | Deglintch time for recharge detection | $R_{TMR} = 50\text{ k}\Omega$ | | 22.5 | | ms |
| DPPM FUNCTION | | | | | | |
| V_{DPPM} | DPPM regulation point range | $V_{(DPPM)} = R_{DPPM} \times K_{DPPMM} \times I_{O(DPPM)}$ | 2.6 | | 4.4 | V |
| $I_{O(DPPM)}$ | DPPM pin current source | AC or USB Present | 95 | 100 | 105 | μA |
| K_{DPPM} | DPPM scaling factor | | 1.139 | 1.15 | 1.162 | |
| $t_{DGL(DPPM)}$ | DPPM de-glitch time | Status bit set indicating DPPM loop active after deglitch time, $R_{TMR} = 50\text{ k}\Omega$ | | 500 | | μs |
| CHARGE AND PRECHARGE SAFETY TIMER | | | | | | |
| t_{CHG} | Charge safety timer programmed value | Safety timer range, thermal and DPPM loop not active, $t_{CHG} = R_{TMR} \times K_{TMR}$ | 3 | 5 | 10 | h |
| K_{TMR} | Charge timer set factor | | 0.313 | 0.36 | 0.414 | s/ Ω |
| t_{CHGADD} | Total elapsed time when DPPM or thermal loop are active | Fast charge on, t_{CHGADD} is the maximum add-on time added to t_{CHG} | | $2 \times t_{CHG}$ | | h |
| t_{PRECHG} | Precharge safety timer programmed value | Pre charge safety timer range, thermal and DPPM loop not active, $t_{PRECHG} = K_{PRE} \times R_{TMR} \times K_{TMR}$ | 18 | 30 | 60 | min |
| K_{PRE} | Precharge timer set factor | | 0.09 | 0.1 | 0.11 | |
| $t_{PCHGADD}$ | Total elapsed time when DPPM or thermal loop are active | Precharge on, $t_{PCHGADD}$ is the maximum add-on time added to t_{PRECHG} | | $2 \times t_{PRECHG}$ | | h |
| R_{TMR} | External timer resistor limits | | 30 | | 100 | k Ω |
| $R_{TMR(FLT)}$ | Timer fault recovery pullup resistor | Internal resistor connected from OUT to BAT after safety timer timeout | | 1 | | k Ω |
| THERMAL REGULATION LOOP | | | | | | |
| T_{THREG} | Temperature regulation limit | Charge current decreased and timer extended when $T_J > T_{THREG}$ | 115 | | 135 | $^\circ\text{C}$ |
| CHARGER THERMAL SHUTDOWN | | | | | | |
| T_{THCHG} | Charger thermal shutdown | Charger turned off when $T_J > T_{THCHG}$ | | 150 | | $^\circ\text{C}$ |
| $T_{HCHGHYS}$ | Charger thermal shutdown hysteresis | | | 30 | | $^\circ\text{C}$ |

7.9 Electrical Characteristics – Linear Regulators

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-------|---|------|---------------|
| SELECTABLE OUTPUT VOLTAGE LDOs: LDO1, LDO2 | | | | | | |
| $I_{Q(LDO12)}$ | Quiescent current, either LDO1 or LDO2 enabled, LDO0 disabled | $I_{Q(LDO12)} = I(VIN_LDO02)$ | | 15 | | μA |
| | | $I_{(LDO1,2)} = -1\text{ mA}$ | | 160 | | |
| | | $I_{(LDO1,2)} = -150\text{ mA}$ | | | 150 | mA |
| $I_{O(LDO1,2)}$ | Output current range | | | | | |
| $V_{O(LDO1,2)}$ | LDO1, LDO2 Output Voltage | Output voltage, selectable through $I^2\text{C}$. | | Available output voltages: $V_{O(LDO1,2)TYP} = 1.25, 1.5, 1.8, 2.5, 2.85, 3, 3.2, 3.3$ | | V |
| | | Dropout voltage, 150-mA load | | | 300 | mV |
| | | Total accuracy, $V(VIN_LDO02) = 3.65\text{ V}$ | -3% | | 3% | |
| | | Line Regulation, 100-mA load, $V(VIN_LDO02): V_{(LDO1,2)TYP} + 0.5\text{ V} \rightarrow 4.7\text{ V}$ | -1% | | 1% | |
| | | Load regulation, load: 10 mA \rightarrow 150 mA $V(VIN_LDO02) > V_{O(LDO1,2)TYP} + 0.5\text{ V}$ | -1.5% | | 1.5% | |
| $P_{SR(LDO12)}$ | PSRR at 20 kHz | 150mA load at output, $V(VIN_LDO02) - V_{O(LDO1,2)} = 1\text{ V}$ | | 40 | | dB |
| $I_{SC(LDO1,2)}$ | LDO1&2 short circuit current limit | Output grounded | | 300 | | mA |
| $R_{DCH(LDO1,2)}$ | Discharge resistor | LDO disabled by $I^2\text{C}$ command | | 300 | | Ω |
| $I_{LKG(LDO1,2)}$ | Leakage current | LDO off | | 2 | | μA |
| SIM LINEAR REGULATOR | | | | | | |
| $I_{Q(SIM)}$ | Quiescent current | Internally connected to OUT pin | | 20 | | μA |
| $I_{O(SIM)}$ | Output current range | | | | 8 | mA |
| $V_{O(SIM)}$ | SIM LDO output voltage | Output voltage, selectable through $I^2\text{C}$. | | Available output voltages: $V_{O(SIM)TYP} = 1.8\text{ or }2.5$ | | V |
| | | Dropout voltage, 8-mA load | | | 0.2 | V |
| | | Total accuracy, $V(OUT): 3.2\text{ V to }4.7\text{ V}, 8\text{ mA}$ | -5% | | 5% | |
| | | Load regulation, load: 1 mA \rightarrow 8 mA, $V(OUT) > V_{O(SIM)TYP} + 0.5\text{ V}$ | -3% | | 3% | |
| | | Line regulation, 5-mA load, $V(OUT): V_{O(SIM)TYP} + 0.5\text{ V} \rightarrow 4.7\text{ V}$ | -2% | | 2% | |
| $I_{SC(SIM)}$ | Short-circuit current limit | Output grounded | | 20 | | mA |
| $I_{LKG(SIM)}$ | Leakage current | LDO off | | 1 | | μA |
| PROGRAMMABLE OUTPUT VOLTAGE LDOs: LDO3, LDO4, LDO5 | | | | | | |
| $I_{Q(LDO35)}$ | Quiescent current, only one of LDO3, LDO4, LDO5 is enabled | $I_{Q(LDO35)} = I(VIN_LDO35)$ | | 70 | | μA |
| $I_{O(LDO35)}$ | Output current range | | | | 100 | mA |
| $V_{O(LDO35)}$ | LDO3, LDO4, LDO5 output voltage | Output voltage, selectable through $I^2\text{C}$ | | Available output voltages: $V_{O(LDO35)TYP} = 1.224\text{ V to }4.46\text{ V}, 25\text{-mV steps}$ | | V |
| | | Dropout voltage, 100-mA load | | | 240 | mV |
| | | Total accuracy, 100-mA load $V(VIN_LDO35) = 5\text{ V}$ | -3% | | 3% | |
| | | Load regulation, $V(VIN_LDO35) > V_{O(LDO35)TYP} + 0.5\text{ V}$, load: 1 mA \rightarrow 50 mA | -1% | | 1% | |
| | | Line regulation, 10-mA load, $V(VIN_LDO35): V_{O(LDO35)TYP} + 0.5\text{ V} \rightarrow 4.7\text{ V}$ | -1% | | 1% | |
| $I_{SC(LDO35)}$ | Short-circuit current limit | Output grounded | | 250 | | mA |
| $PSR_{(LDO35)}$ | PSRR at 10 kHz | $V(VIN_LDO35) > V_{O(LDO3,5)} + 1\text{ V}, 50\text{-mA load at output}$ | | 40 | | dB |
| $R_{DCH(LDO35)}$ | Discharge resistor | LDO is disabled by $I^2\text{C}$ command | | 400 | | Ω |
| $I_{LKG(LDO35)}$ | Leakage current | LDO off | | 1 | | μA |

Electrical Characteristics – Linear Regulators (continued)

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------------|-------------------------------|--|-----------------------|-------|-----|------|------|
| RTC_OUT LINEAR REGULATOR | | | | | | | |
| I _{Q(RTC_OUT)} | Quiescent current for RTC LDO | Internally connected to OUT pin | | 20 | | | μA |
| I _{O(RTC_OUT)} | Output current range | | | 8 | | | mA |
| V _{O(RTC_OUT)} | RTC_OUT output voltage | Fixed output voltage value | | 1.5 | | | V |
| | | Dropout voltage, I(RTC_OUT) = −8 mA | | 200 | | | mV |
| | | Total accuracy, V(OUT): 2 V to 4.7 V, 8-mA load, sleep mode not set | | −5% | | 5% | |
| | | Load regulation, load: 1 mA → 8 mA, 2 V < V(OUT) < 4.7 V | | −3% | | 3% | |
| | | Line regulation, 5-mA load, V(OUT): 2 V → 4.7 V | | −2% | | 2% | |
| I _{SH(RTC_OUT)} | Short-circuit current limit | V(RTC_OUT) = 0 V | | 20 | | | mA |
| I _{LKG(RTC_OUT)} | Leakage current | V(RTC_OUT) = 1.5 V, V(OUT) = 0 V | T _J = 85°C | 880 | | | nA |
| | | | T _J = 25°C | 250 | | | |
| LDO0 LINEAR REGULATOR | | | | | | | |
| I _{Q(LDO0)} | Quiescent current | Internally connected to VIN_LDO12 pin | I(LDO0) = −1 mA | 15 | | | μA |
| | | | I(LDO0) = −150 mA | 160 | | | |
| I _{O(LDO0)} | Output current range | | | 150 | | | mA |
| V _{O(LDO0)} | Output voltage | Fixed output voltage value | | 3.3 | | | V |
| | | Dropout voltage, I(LDO0) = −150 mA | | 300 | | | mV |
| | | Total accuracy | | −3% | | 3% | |
| | | Line regulation, V(OUT): V _{O(LDO0)} + 0.5 → 4.7 V, I(LDO0) = −100 mA | | −1% | | 1% | |
| | | Load regulation, I(LDO0) = −10 mA → −150 mA | | −1.5% | | 1.5% | |
| PSR _(LDO0) | PSRR at 20 kHz | 150-mA load at output, V(VIN_LDO12) − V _{O(LDO1,2)} = 1 V | | 40 | | | dB |
| I _{SC(LDO0)} | Short circuit current limit | V(LDO0) = 0 V | | 300 | | | mA |
| I _{LKG(LDO0)} | Leakage current | LDO off | | 1 | | | μA |
| LDO_PM LINEAR REGULATOR | | | | | | | |
| I _{Q(LDO_PM)} | Output current range | | | 20 | | | mA |
| V _{O(LDO_PM)} | Output voltage | Fixed output voltage value, V(OUT) > 4 V | | 3.3 | | | V |
| | | Dropout voltage, I(LDOPM) = −12 mA | | 0.5 | | 0.7 | |
| | | Total accuracy | | −5% | | 5% | |
| I _{LKG(LDOPM)} | Leakage current | LDO off | | 1 | | | μA |

7.10 Electrical Characteristics – Switched-Mode SM1 Step-Down Converter

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), $V_{O(\text{SM1})} = 1.24\text{ V}$, application circuit [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------------|--------------------------------|--|--|------|------|------|-----|
| I _{Q(SM1)} | Quiescent current for SM1 | I _{Q(SM1)} = I(VIN_ SM1), no output load, not switching | 10 | | | μA | |
| | | SM1 OFF, set through I ² C | 0.1 | | | | |
| I _{O(SM1)} | Output current range | Vin = 4.2 V, Vout = 1.24 V (TPS65810) | 600 | | | mA | |
| | | Vin = 4.2 V, Vout = 1.24 V (TPS65811) | 750 | | | | |
| V _{O(SM1)} | Output voltage, PWM mode | Output voltage, selectable through I ² C, Standby OFF | Available output voltages: V _{O(SM1)TYP} = 0.6 V to 1.8 V, adjustable in 40-mV steps | | | V | |
| | | V _{O(SM1)} = V _{SBY(SM1)} , Output voltage range, Standby ON | Available output voltages: V _{SBY(SM1)} = 0.6 V to 1.8 V, adjustable in 40-mV steps | | | | |
| | | Total accuracy, V _{O(SM1)TYP} = V _{SBY(SM1)} = 1.24 V, V(VIN_ SM1) = 3.0 V to 4.7 V; 0 mA ≤ I _{O(SM1)} ≤ 600 mA | –3% | | 3% | | |
| | | Line Regulation, V(VIN_ SM1): 3.0 → 4.70 V, I _{O(SM1)} = 10 mA | 0.027 | | | | %/V |
| | | Load Regulation, V(VIN_ SM1) = 4.7 V, I _{O(SM1)} : 60 mA → 540 mA | 0.139 | | | | %/A |
| R _{DS(ON)(PSM1)} | P-channel MOSFET ON-resistance | V(VIN_ SM1) = 3.6 V, 100% duty cycle set | 310 | 500 | | mΩ | |
| I _{LKG(PSM1)} | P-channel leakage current | | 0.1 | | | μA | |
| R _{DS(ON)(NSM1)} | N-channel MOSFET ON-resistance | V(VIN_ SM1) = 3.6 V, 0% duty cycle set | 220 | 330 | | mΩ | |
| I _{LKG(PSM1)} | N-channel leakage current | | 5 | | | μA | |
| I _{LIM(SM1)} | P- and N-channel current limit | 3 V < V(VIN_ SM1) < 4.7 V (TPS65810) | 900 | 1050 | 1200 | mA | |
| | | 3 V < V(VIN_ SM1) < 4.7 V (TPS65811) | 1000 | 1200 | 1400 | | |
| f _{S(SM1)} | Oscillator frequency | PWM mode set | 1.3 | 1.5 | 1.7 | MHz | |
| EFF _(SM1) | Efficiency | V(VIN_ SM1) = 4.2 V, PWM mode, I _{O(SM1)} = 300 mA, V _{O(SM1)} = 3 V | 90% | | | | |
| t _{SS(SM1)} | Soft-start ramp time | Converter OFF→ON, V _{O(SM1)} : 5% → 95% of target value | 750 | | | μs | |
| t _{DLY(SM1)} | Converter turnon delay | GPIO1 pin programmed as SM1 converter enable control. Measured from V(GPIO1): LO → HI | 170 | | | μs | |

7.11 Electrical Characteristics – Switched-Mode SM2 Step-Down Converter

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), $V_{O(\text{SM}1)} = 1.24\text{ V}$, application circuit [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|--------------------------------|---|--|------|------|------|
| I _Q (SM2) | Quiescent current for SM2 | I _Q (SM2) = I(VIN_ SM2), no output load, not switching | 10 | | | μA |
| | | SM2 OFF, set through I ² C | 0.1 | | | |
| I _O (SM2) | Output current range | V _{in} = 4.2 V, V _{out} = 1.24 V (TPS65810) | 600 | | | mA |
| | | V _{in} = 4.2 V, V _{out} = 1.24 V (TPS65811) | 750 | | | |
| V _O (SM2) | Output voltage | Output voltage, selectable through I ² C, stand-by OFF | Available output voltages: V _O (SM2)TYP = 1 V to 3.4 V, adjustable in 80-mV steps | | | V |
| | | V _O (SM2) = V _{SBY} (SM2), Output voltage range, stand-by ON | Available output voltages: V _{SBY} (SM2) = 1 V to 3.4 V, adjustable in 80-mV steps | | | |
| | | Total accuracy, V _O (SM2)TYP = V _{SM2} (SBY) = 1.8 V, V(VIN_ SM2) = greater of [3.0 V or (V _O (SM2) + 0.3 V)] to 4.7 V; 0 mA ≤ I _O (SM2) ≤ 600 mA | −3%3% | | | |
| | | Line regulation, V(VIN_ SM2) = greater of [3 V or (V _O (SM2) + 0.3 V)] to 4.7 V; 0 mA ≤ I _O (SM2) ≤ 600 mA | 0.027 | | | %/V |
| | | Load regulation, V(VIN_ SM2) = 4.7 V, I _O (SM2): 60 mA → 540 mA | 0.139 | | | %/A |
| R _{DSON} (PSM2) | P-channel MOSFET ON-resistance | V(VIN_ SM2) = 3.6 V, 100% duty cycle set | 310 | 500 | | mΩ |
| I _{LKG} (PSM2) | P-channel leakage current | | 0.1 | | | μA |
| R _{DSON} (NSM2) | N-channel MOSFET ON-resistance | V(VIN_ SM2) = 3.6 V, 0% duty cycle set | 220 | 330 | | mΩ |
| I _{LKG} (PSM2) | N-channel leakage current | | 5 | | | μA |
| I _{LIM} (SM2) | P- and N-channel current limit | 3 V < V(VIN_ SM2) < 4.7 V (TPS65810) | 900 | 1050 | 1200 | mA |
| | | 3 V < V(VIN_ SM2) < 4.7 V (TPS65811) | 1000 | 1200 | 1400 | |
| f _S (SM2) | Oscillator frequency | PWM mode set | 1.3 | 1.5 | 1.7 | MHz |
| EFF _(SM2) | Efficiency | V(VIN_ SM2) = 4.2 V, I _O (SM2) = 300 mA, V _O (SM2) = 3 V | 90% | | | |
| t _{SS} (SM2) | Soft-start ramp time | Converter OFF→ON, V _O (SM2) : 5% → 95% of target value | 750 | | | μs |
| t _{DLY} (SM2) | Converter turnon delay | GPIO2 pin programmed as SM2 converter enable control. Measured from V(GPIO2): LO → HI | 170 | | | μs |

7.12 Electrical Characteristics – GPIOs

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|-----|-----|-----|---------------|
| GPIO1–3 | | | | | |
| V_{OL} Low level output voltage GPIO0 | $I_{\text{OL}} = 20\text{ mA}$ | | | 0.5 | V |
| I_{OGPIO} Low level sink current into GPIO1,2,3 | $V(\text{GPIO}n) = V(\text{OUT})$ | 20 | | | mA |
| V_{IL} Low level input voltage | | | | 0.4 | V |
| $I_{\text{LKG}(\text{GPIO})}$ Input leakage current | $V(\text{GPIO}n) = V(\text{OUT})$ | | 1 | | μA |

7.13 Electrical Characteristics – ADC

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), $V(\text{ADC_REF}) = 2.535\text{ V}$ if external reference voltage is used, application circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|----|------------------------|-------------------------------|------|--------|
| ANALOG INPUTS | | | | | | | |
| V _{RNG(CH1_5)} | Full scale input range Ch1 to Ch5 | Positive inputs (active clamp) Full scale ~ 2.535 V | | 0 | V(ADC_REF) | | V |
| V _{RNG(CH6_8)} | Full scale input range Ch6 to Ch8 | Positive inputs (active clamp), full scale ~4.7 V | | 0 | V _{INTREF} x1.854 | | V |
| C _{IN(ADC)} | Input capacitance (all channels) | | | 15 | | | pF |
| R _{INADC(CH1_5)} | Input resistance | (Ch1 to Ch5) | | 1 | | | MΩ |
| I _{LKGADC(CH1_5)} | Leakage current | (Ch1 to Ch5) | | | | 100 | nA |
| R _{INADC(CH6_8)} | Input resistance | (Ch6 to Ch8) | | 430 | 540 | | kΩ |
| I _{LKGADC(CH6_8)} | Leakage current | (Ch6 to Ch8) | | | | 10 | μA |
| V _{CH5(ADC)} | Internal voltage proportional to junction temperature | T _J = 25°C, ADC channel 5 input voltage | | 1.895 | | | V |
| | | Temperature coefficient | | 6.5 | | | mV/ °C |
| DC ACCURACY | | | | | | | |
| RES _(ADC) | Resolution | SAR ADC | | 10 | | | Bits |
| MCD _(ADC) | No missing codes | | | SPECIFIED | | | |
| INL _(ADC) | Integral linearity error | | | ±3 | | | LSB |
| DNL _(ADC) | Differential non-linearity error | | | ±1 | | | LSB |
| OFF _{ZERO(ADC)} | Offset error | Difference between the first code transition (00...00 to 00...01) and the ideal AGND + 1 LSB | | | | 5 | LSB |
| OFF _{CH(ADC)} | Offset error match between channels | | | | | 5 | LSB |
| GAIN _{ADC} | Gain error | Deviation in code from the ideal full scale code (11...111) for the full scale voltage | | ±8 | | | LSB |
| GAIN _{CH(ADC)} | Gain error match | Any two channels | | 2 | | | LSB |
| THROUGHPUT SPEED | | | | | | | |
| ADC _{CLK} | Sampling clock | | | 600 | 750 | 900 | kHz |
| ADC _{TCONV} | Conversion time | Sampling, conversion and setting R _s ≤ 200 K for CH1,CH2,CH3; R _s ≤ 500 Ω for CH6, CH7, CH8 | | 44 | 59 | 68 | μs |
| REFERENCE VOLTAGES | | | | | | | |
| V _{INTREF} | Internal ADC reference voltage | T _A = 25°C, V(ADC_REF)=V _{INTREF} when internal ADC reference is selected | | 2.53 | 2.535 | 2.54 | V |
| I _{SHRT(INTREF)} | Internal reference short circuit limit | V(ADC_REF)= AGND1, internal reference enabled through I ² C | | 6 | | | mA |
| V _{REF(DRIFT)} | ADC internal reference temperature drift | | | 50 | | 100 | ppm/°C |
| I _{Q(ADC)} | ADC Internal reference quiescent current | Measured at OUT pin (internal reference) or ADC_REF pin (external reference) | | 40 | | | μA |
| I _(ANLG2) | ANLG2 pin internal pullup current source | ADC channel 2 bias current, set through I ² C register ADC_WAIT bits (ADC_CH2I_D1_1, ADC_CH2I_D2) | 00 | 0 | | μA | |
| | | | 01 | 10 | | | |
| | | | 10 | 50 | | | |
| | | | 11 | 60 | | | |
| | | Total accuracy, relative to selected value | | -25% | | 25% | |
| I _(ANLG1) | ANLG1 pin internal pullup current source | ADC channel 1 bias current, set through I ² C register ADC_WAIT bits (BATIDI_D1, BATIDI_D2) | 00 | V(OUT) – 1.2 500 kΩ | | μA | |
| | | | 01 | 10 | | | |
| | | | 10 | 50 | | | |
| | | | 11 | 60 | | | |
| | | Total accuracy | | 10% | | 10% | |
| INTERNAL REFERENCE POWER CONSUMPTION | | | | | | | |
| PD _{ACTIVE} | Power dissipation | Conversion active | | 2.3 | | | mW |
| PD _{ARMED} | Power dissipation | Not converting | | 0.43 | | | mW |

7.14 Electrical Characteristics – LED and PWM Drivers

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|---|--|----------------|--|-----|-----|------|
| SM3 BOOST CONVERTER, WHITE LED CONSTANT CURRENT DRIVER | | | | | | | |
| V _{VIN(SM3)} | Input voltage range | V(OUT) = 3.3 V | | 3 | | 4.7 | V |
| V _{OVP3} | Output overvoltage trip | OVP detected at V(SM3) > V _{OVP3} | | 26.5 | 29 | 30 | V |
| V _{HYS(OVP3)} | Output overvoltage hysteresis | OVP not detected at V(SM3) < V _{OVP3} – V _{HYS(OVP3)} | | | 1.8 | | V |
| V _{SM3REF} | LED current-sense threshold | LED current below regulation point at V(FB3) < V _{SM3REF} | | 244 | 252 | 260 | mV |
| I _{O(SM3)} | LED current | $I_{O(SM3)} = \frac{V(SM3REF)}{R_{FB3}}$ | | 0 | | 25 | mA |
| | | Current range, V _{in} = 3.3 V, Total accuracy, I _{O(SM3)} = 10 mA | | –10%10% | | | |
| D _{SM3SW} | LED-switch duty cycle | Duty cycle range | | D _{SM3SW} = 0% to 99.6%, set through I ² C, 256 steps, 0.4% minimum step | | | |
| F _{REP_SM3} | LED-switch duty cycle pattern repetition rate | 256 pulses within repetition rate time | SM3_LF_OSC = 0 | 122 | | | Hz |
| | | | SM3_LF_OSC = 1 | 183 | | | |
| R _{DS(on)(SM3SW)} | LED switch MOSFET ON-resistance | V(OUT) = 3.6 V; I(SM3SW) = 20 mA | | | 1 | 2 | Ω |
| I _{LKG(SM3SW)} | LED switch MOSFET leakage | | | | 1 | | μA |
| R _{DS(on)(L3)} | Power stage MOSFET ON-resistance | V(OUT) = 3.6 V; I(L3) = 200 mA | | | 300 | 600 | mΩ |
| I _{LKG(L3)} | Power stage MOSFET leakage | | | | 1 | | μA |
| I _{MAX(L3)} | Power stage MOSFET current limit | 3 V < V(OUT) < 4.7 V | | 400 | 500 | 600 | mA |
| PWM DRIVER, PWM OPEN-DRAIN OUTPUT | | | | | | | |
| V _{OL(PWM)} | Low level output voltage | I(PWM) = 150 mA | | | | 0.5 | V |
| F _{PWM} | PWM driver frequency | Frequency range | | Set through I ² C, F _{PWM} = 0.5 / 1 / 1.5 / 2 / 3 / 4.5 / 7.8 / 15.6 | | | Hz |
| | | Total accuracy, relative to selected value | | –20%20% | | | |
| D _{PWM} | PWM driver duty cycle | Duty cycle range | | D _{PWM} = 6.25% to 100%, set through I ² C, 6.25% minimum step | | | |
| LED_PWM DRIVER, LED_PWM OPEN-DRAIN OUTPUT | | | | | | | |
| D _{LEDPWM} | LED_PWM driver duty cycle | Duty cycle range | | D _{LEDPWM} = 0% to 99.6%, set through I ² C, 256 steps 0.4% minimum step | | | |
| F _{REP(LEDPWM)} | LED_PWM driver duty cycle pattern repetition rate | 256 pulses within repetition rate time | SM3_LF_OSC = 0 | 122 | | | Hz |
| | | | SM3_LF_OSC = 1 | 180 | | | |
| V _{OL(LEDPWM)} | Low level output voltage | I(LED_PWM) = 150 mA | | | | 0.5 | V |
| V _{OH(LEDPWM)} | High level output voltage | | | | | 6 | V |

Electrical Characteristics – LED and PWM Drivers (continued)

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|----------------------------|---|--------------------------|--|-----|------|------|
| RGB DRIVER, RED, GREEN, AND BLUE OPEN-DRAIN OUTPUT | | | | | | | |
| t _{FLASH(RGB)} | Flashing period | Flashing period range | | t _{FLASH(RGB)} = 1 to 8 sec, set through I ² C, 0.5 s minimum step, 8 steps | | | s |
| | | Total accuracy | | −20% 20% | | | |
| t _{FLASH(ON)} | Flash on time | Flash on time range, value selectable by I ² C | | Set through I ² C, t _{FLASH(ON)} = 0.1 / 0.15 / 0.2 / 0.25 / 0.3 / 0.4 / 0.5 / 0.6 | | | s |
| | | Total accuracy relative to selected value | | −20% 20% | | | |
| D _{RGB} | Duty cycle | Duty cycle range, value selectable through I ² C | | D _{RGB} = 0% to 99.98%, set through I ² C, 3.23% minimum step | | | |
| I _{SINK(RGB)} | RGB output sink current | V(RED) = V(GREEN) = V(BLUE) = 2 V, set through I ² C RGB_ISET1,0 | 00 = (Driver set to OFF) | | | | mA |
| | | | 01 | 2.4 | 4 | 5.6 | |
| | | | 10 | 4.8 | 8 | 11.2 | |
| | | | 11 | 7 | 12 | 16.6 | |
| V _{OL(RGB)} | Low-level output voltage | Output low voltage, 8-mA load, RED/GREEN/BLUE PINS | | 0.3 | | | V |
| I _{LKG(RGB)} | Output off leakage current | V(RED) = V(GREEN) = V(BLUE) = 4.7 V, all drivers disabled | | 1 | | | μA |

7.15 Electrical Characteristics – I²C Interface

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------|-----------------|------|-----|-----|---------------|
| I²C INTERFACE LOGIC LEVELS | | | | | | |
| V_{IH} | High level input voltage | | 1.3 | | 6 | V |
| V_{IL} | Low level input voltage | | 0 | | 0.6 | V |
| I_{H} | Input bias current | | 0.01 | | | μA |

7.16 Timing Requirements – I²C Interface

over recommended operating conditions (typical values at $T_J = 25^\circ\text{C}$), application circuit as in [Figure 51](#) (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|--|-----|-----|---------------|
| I²C TIMING CHARACTERISTICS | | | | |
| t_{R} | SCLK/SDATA rise time | | 300 | ns |
| t_{F} | SCLK/SDATA fall time | | 300 | ns |
| $t_{\text{W(H)}}$ | SCLK pulse width, high | 600 | | ns |
| $t_{\text{W(L)}}$ | SCLK pulse width, low | 1.3 | | μs |
| $t_{\text{SU(STA)}}$ | Setup time for START condition | 600 | | ns |
| $t_{\text{H(STA)}}$ | START condition hold time after which first clock pulse is generated | 600 | | ns |
| $t_{\text{SU(DAT)}}$ | Data setup time | 100 | | ns |
| $t_{\text{H(DAT)}}$ | Data hold time | 0 | | ns |
| $t_{\text{SU(STOP)}}$ | Setup time for STOP condition | 600 | | ns |
| $t_{\text{(BUF)}}$ | Bus free time between START and STOP condition | 1.3 | | μs |
| FSC | Clock Frequency | | 400 | kHz |

7.17 Trigger Timing Characteristics

| | | | MIN | NOM | MAX | UNIT |
|-------------------------|--|---|------|-----|-------|------|
| $t_{\text{DELAY(TRG)}}$ | Trigger delay time accuracy | Time range, set through I ² C register ADC_DELAY | 0 | | 750 | μs |
| | Relative to typical value set through I ² C | | -20% | | 20% | |
| $t_{\text{WAIT(TRG)}}$ | Trigger wait time accuracy | Time range, set through I ² C register ADC_WAIT | 0 | | 20.48 | ms |
| | Relative to typical value set through I ² C | | -20% | | 20% | |

7.18 Dissipation Ratings

| PACKAGE | θ_{JA} | $T_{\text{A}} \leq 55^{\circ}\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_{\text{A}} = 55^{\circ}\text{C}$ |
|-------------|----------------------|--|--|
| RTQ (1) (2) | 21.7°C/W | 3.22 W | 0.046 W/°C |

- (1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a via matrix.
 (2) The RTQ package MSL level: HIR3 at 260°C

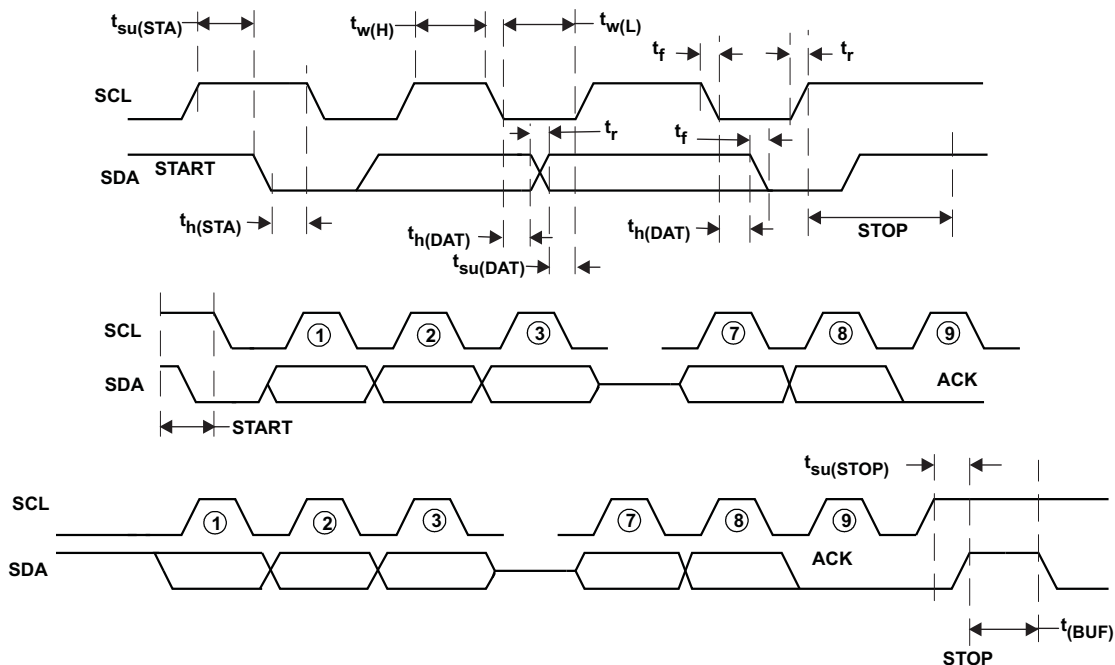
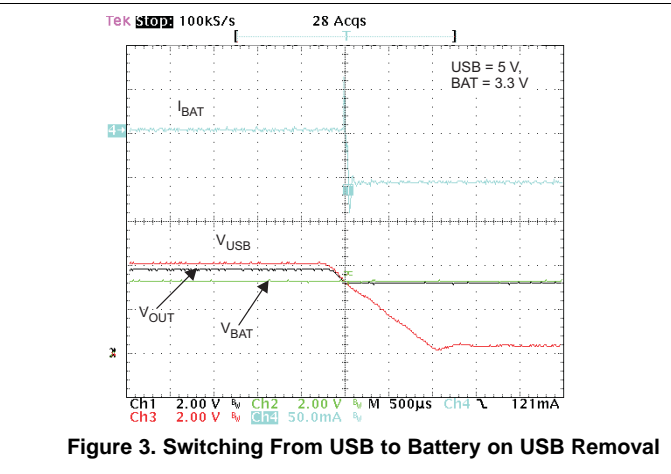
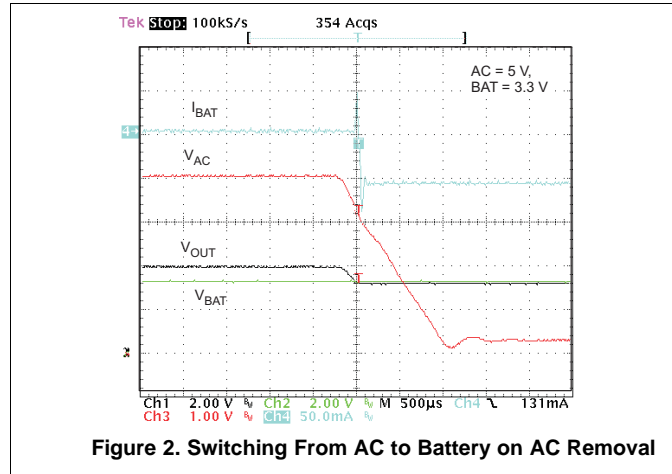


Figure 1. I²C Timing

7.19 Typical Characteristics

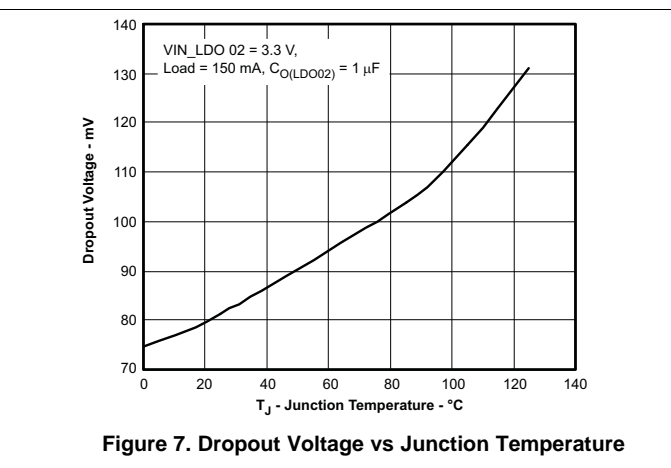
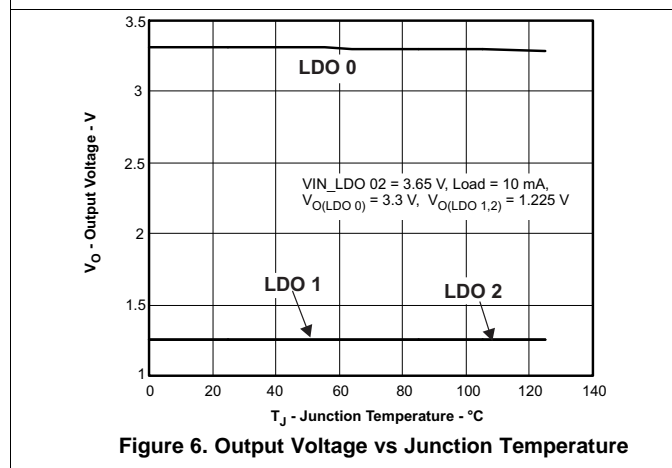
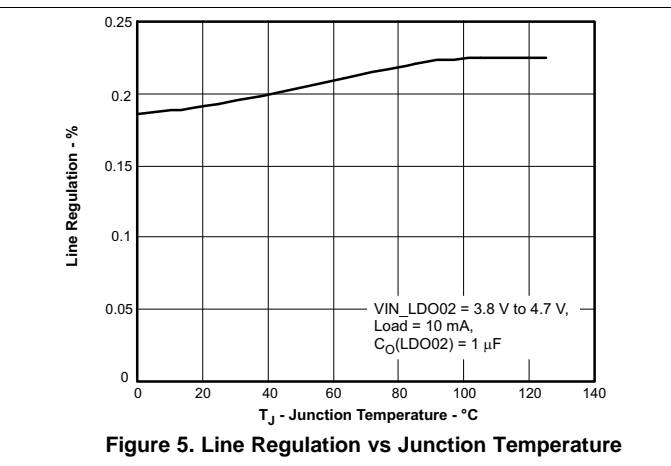
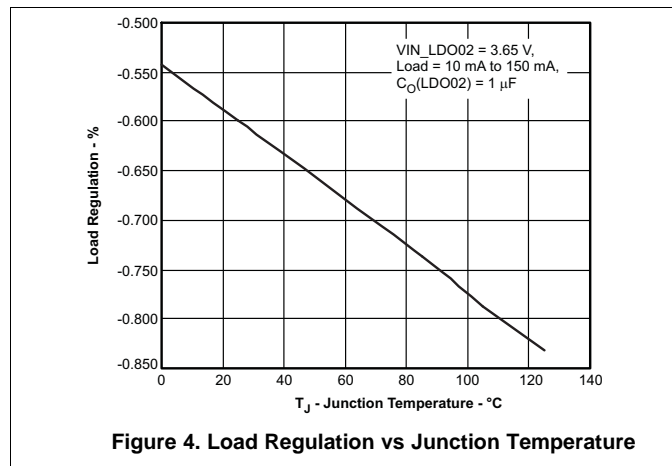
7.19.1 Power Path Management

These curves were measured with application circuit shown in [Figure 51](#) (unless otherwise noted).



7.19.2 Linear Regulators 0, 1, 2

These curves were measured with the application circuit shown in [Figure 51](#) (unless otherwise noted).



7.19.3 Linear Regulators 3, 4, 5

These curves were measured with the application circuit shown in Figure 51 (unless otherwise noted).

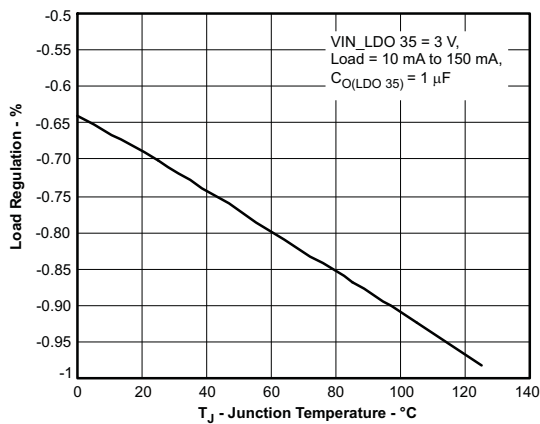


Figure 8. Load Regulation vs Junction Temperature

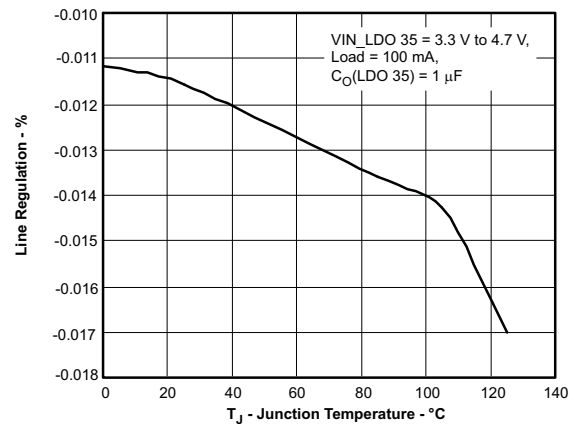


Figure 9. Line Regulation vs Junction Temperature

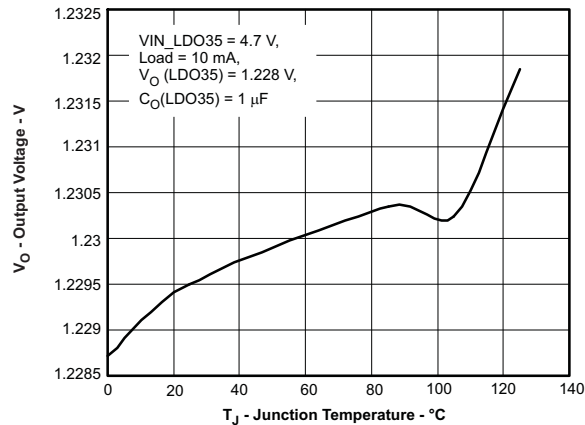


Figure 10. Output Voltage vs Junction Temperature

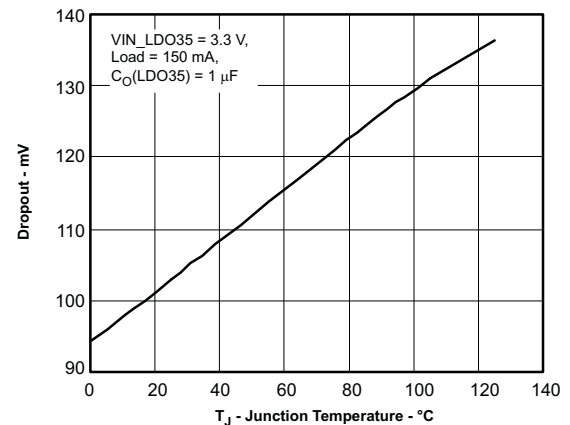


Figure 11. Dropout Voltage vs Junction Temperature

7.19.4 SM1 and SM2 Buck Converters

These curves were measured with the application circuit shown in Figure 51 (unless otherwise noted).

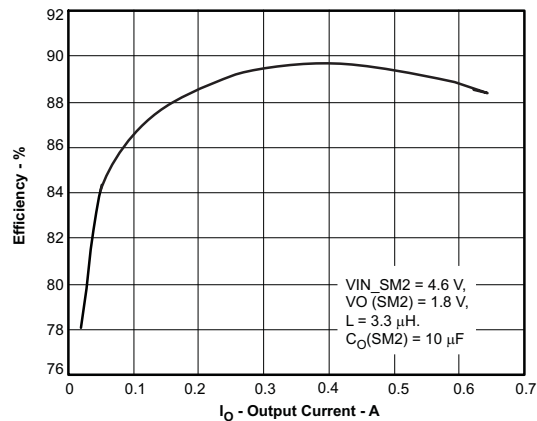


Figure 12. Efficiency in Automatic PWM/PFM Mode

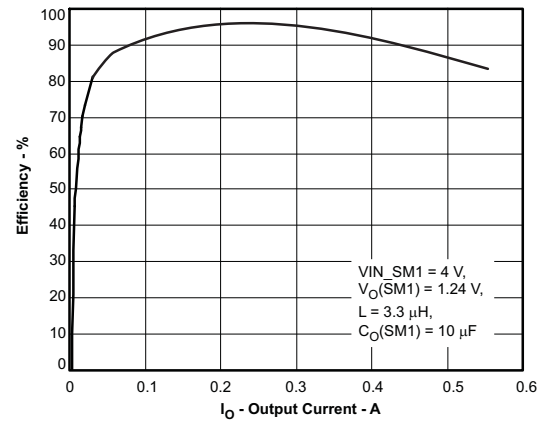
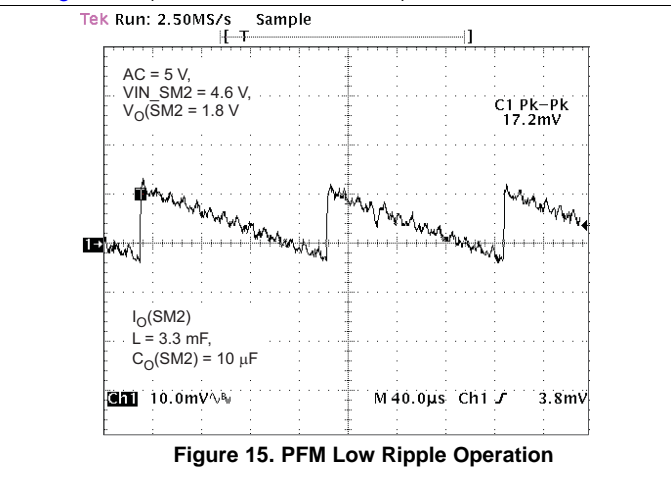
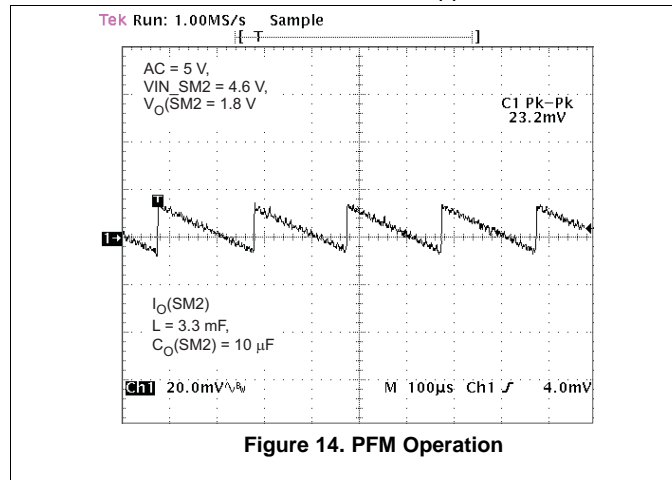


Figure 13. PWM Mode Efficiency vs Output Current

SM1 and SM2 Buck Converters (continued)

These curves were measured with the application circuit shown in [Figure 51](#) (unless otherwise noted).

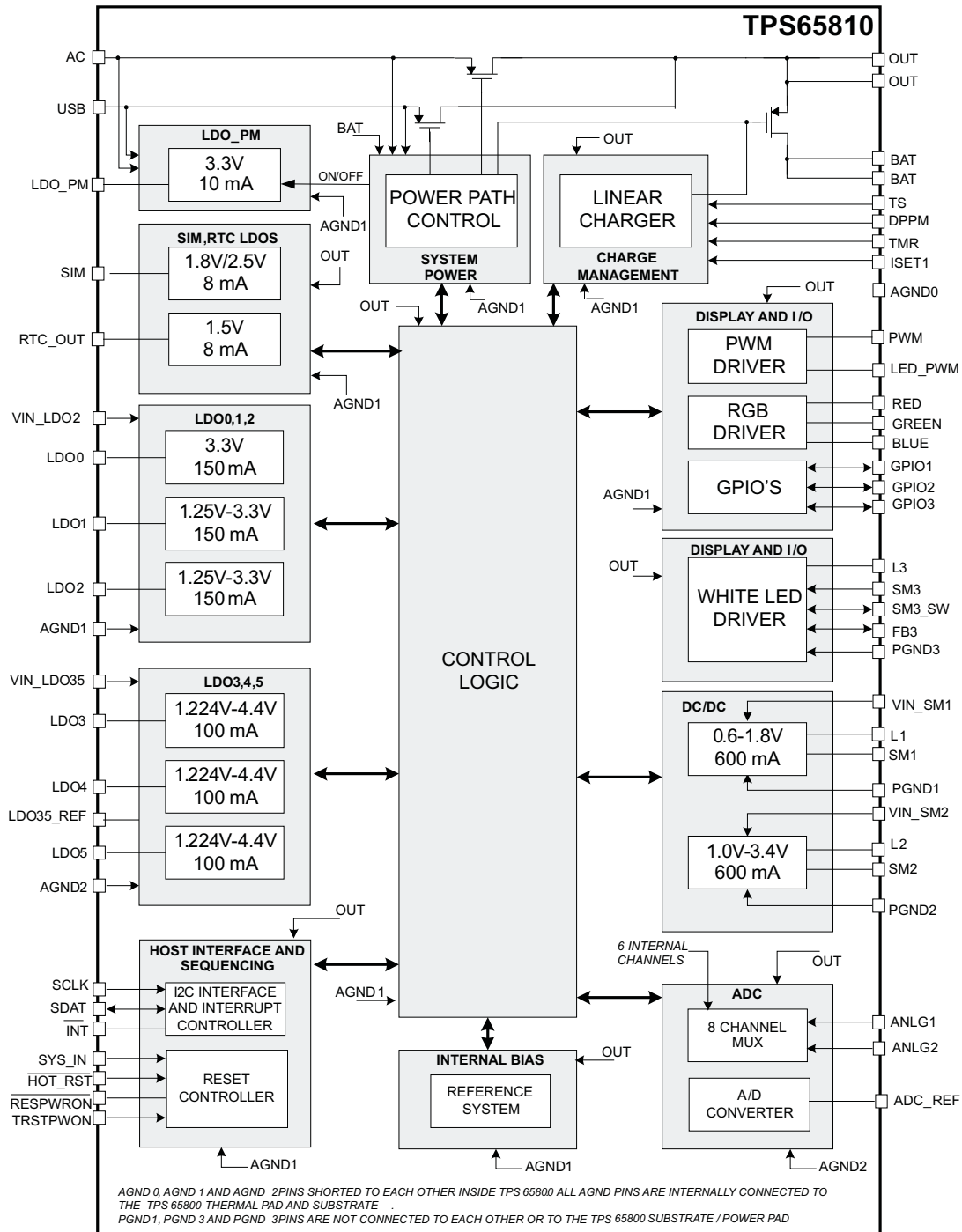


8 Detailed Description

8.1 Overview

This power management IC (PMIC) integrates a battery charger, nine LDOs, two buck converters, a white LED driver, and an RGB driver in a 56-pin QFN package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Interrupt Controller and System Sequencing

8.3.1.1 Overview

The TPS65810 has two dedicated internal controllers that execute the host interface and system sequencing tasks: a sequencing controller and an interrupt controller.

The sequencing controller monitors internal and system parameters and defines the sequencing of the internal power supplies during power-up, power-down, or power fault events, and executes specific internal power supply reset operations under external hardware control or host software commands.

The following parameters are monitored by the sequencing controller:

- System power bus voltage (at SYS_IN pin), input supply voltage, battery pack voltage
- TPS65810 thermal fault status
- Integrated supply status

The interrupt controller monitors multiple system status parameters and signals to the host when one of the monitored parameters toggled, as a result of a system status change. The interrupt controller inputs include all the parameters monitored by the sequencing controller plus:

- Charger status
- Battery pack status
- ADC status

Internal I²C registers enable masking of all the monitored parameters. Using those registers, the host can select which parameters trigger an interrupt or a power-good fault. Power-good faults trigger a change in the TPS65810 operating mode, as detailed in the next sections.

Figure 16 shows a simplified block diagram for the TPS65810 sections that interface to the external host.

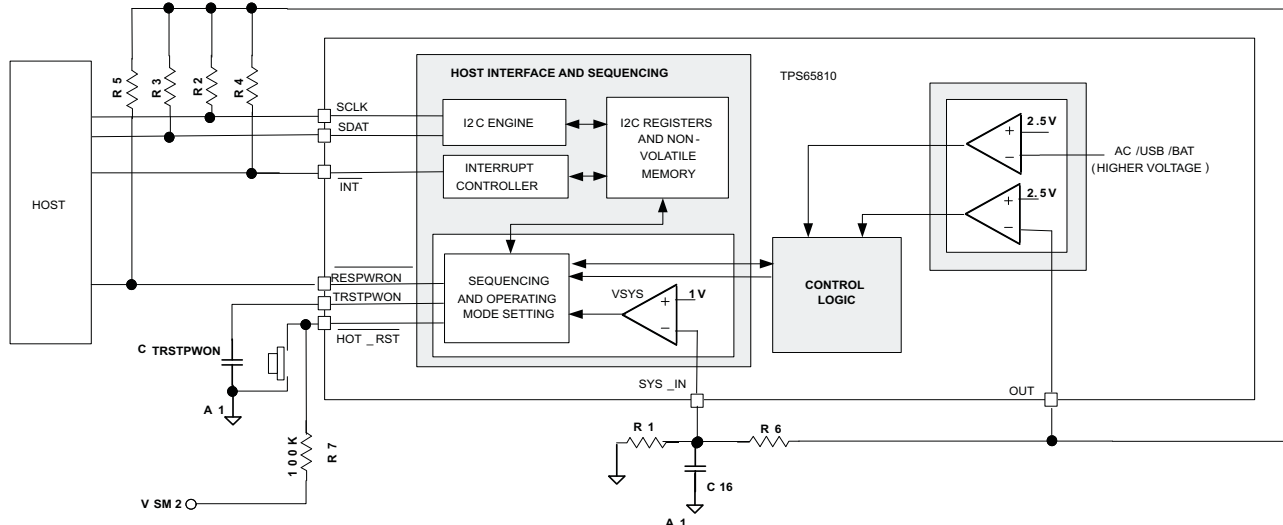


Figure 16. Simplified Block Diagram

Feature Description (continued)

8.3.1.2 Interrupt Controller

The TPS65810 has internal block and overall system status information stored in I²C status registers. The following subsystems and system parameters are monitored:

- External power supply status: AC or USB supply detected, AC or USB connected to system, AC/USB OVP
- Charger status: on, off, or suspend, fast charge or precharge, termination detected, DPPM on, thermal loop ON
- Battery pack status: temperature, discharge on and off
- TPS65810 thermal shutdown
- ADC status: conversion status, input out of range, ANLG1 high impedance detection
- Integrated supplies status: output out of regulation (power-good fault)

The GPIO1 and GPIO2 pins can be configured as inputs, generating an interrupt request to the host ($\overline{\text{INT}}\text{:HI}\rightarrow\text{LO}$) at the GPIO rising or falling edge. The host can use internal the INT_MASK I²C registers to define which of the monitored status variables triggers an interrupt. When a non-masked system status bit toggles state, the interrupt controller issues an interrupt, following the steps below:

1. System status bits that caused the interruption are set to HI in registers INT_ACK1 and INT_ACK2
2. An interrupt is sent to the host ($\overline{\text{INT}}\text{:HI}\rightarrow\text{LO}$)

When an interrupt is sent to the host, $\overline{\text{INT}}$ is kept in the LO state and the INT_ACK register contents are latched, holding the system status that generated the currently issued interrupt request. When an interrupt request is active ($\overline{\text{INT}} = \text{LO}$) additional changes in non-masked status registers and control signals are ignored, and the INT_ACK registers are not updated.

The host must write a 0 to the INT_ACK register bit that generated the interrupt to set $\overline{\text{INT}} = \text{HI}$ and enable new updates to the INT_ACK registers. If the host stops in the middle of a WRITE or READ operation, the $\overline{\text{INT}}$ pin stays at the LO level. The TPS65810 has no reset timeout; assume that the host does not leave $\overline{\text{INT}} = \text{LO}$ and the status registers unread for a long time.

The non-masked I²C register bits and internal control signals generate a new interrupt only after $\overline{\text{INT}}$ is set to HI. The non-masked power-good fault register bits generate a power-good fault when any of the non-masked bits detects that the monitored output voltage is out of regulation, independently of the $\overline{\text{INT}}$ pin level.

Feature Description (continued)

8.3.1.3 System Sequencing and TPS65810 Operating Modes

The TPS65810 has a state machine that controls the device power-up and power-down sequencing. Figure 17 is a state diagram which shows the main operating modes.

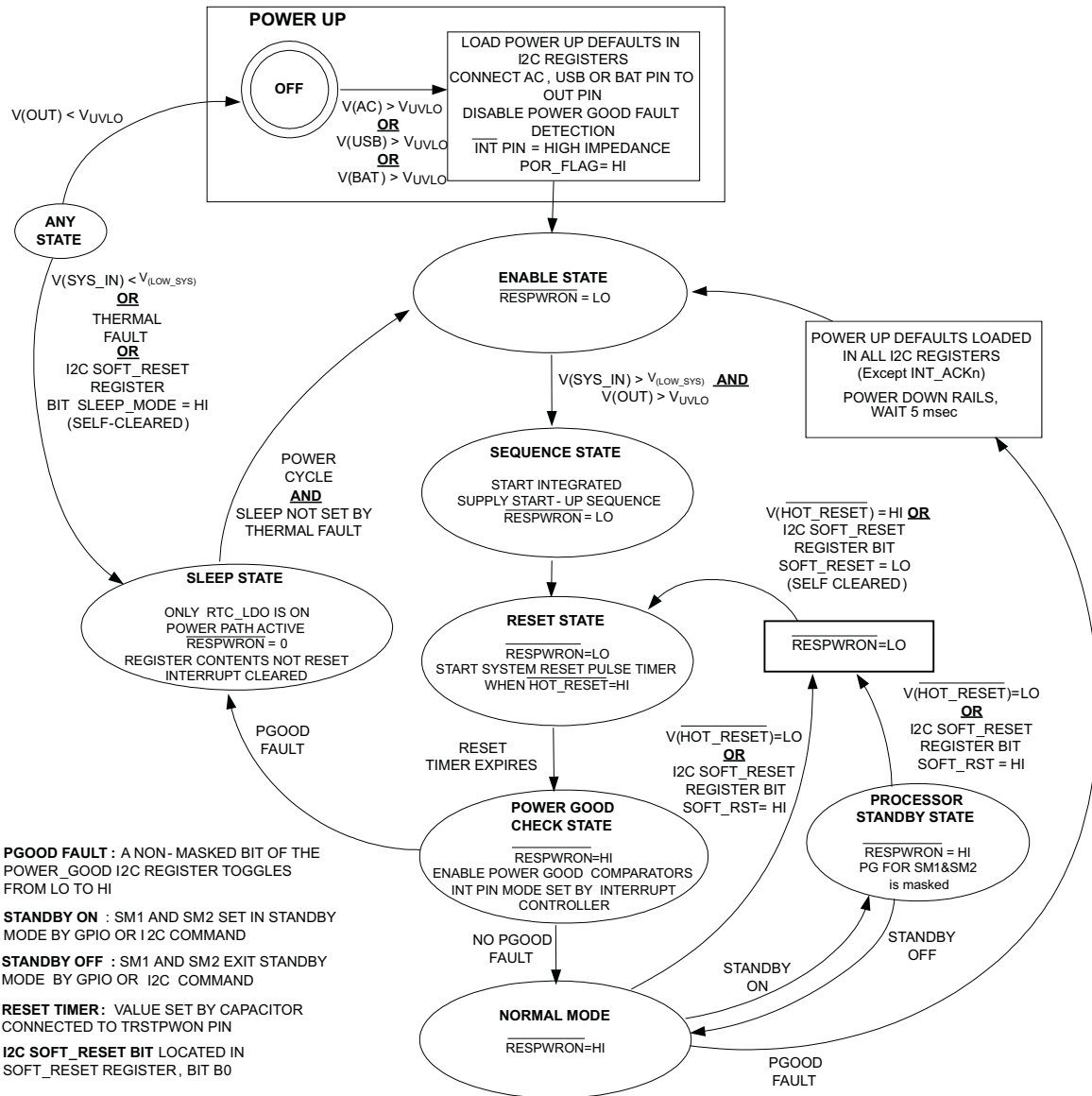


Figure 17. TPS65810 State Diagram

8.3.1.3.1 Power Up

If the AC, USB and BAT pin voltages are below the internal UVLO threshold V_{UVLO} (2.5 V typical) all IC blocks are disabled and the TPS65810 is not operational, with all functions OFF. When an external power source or battery with voltage greater than the V_{UVLO} voltage threshold is applied to AC/USB or BAT pins the internal TPS65810 references are powered up, biasing internal circuits. When all the main internal supply rails are active the TPS65810 I²C registers are set to the power-up default values, shown in [Table 1](#).

Feature Description (continued)

Table 1. Integrated Supply and Drivers I²C Registers Power-Up Defaults

| SUPPLY | POWER-UP DEFAULT | OTHER BLOCKS | POWER-UP DEFAULT |
|---------|--------------------------|-----------------|---------------------------|
| LDO0 | OFF, 3.3 V | POWER PATH | INPUT TO SYSTEM |
| LDO1 | 1.25V, OFF | PWM | OFF |
| LDO2 | 3.3 V, OFF | PWM_LED | OFF |
| LDO3 | 1.505 V, OFF | GPIO1 | INPUT, SM1 ON/OFF CONTROL |
| LDO4 | 1.811 V, OFF | GPIO2 | INPUT, SM2 ON/OFF CONTROL |
| LDO5 | 3.111 V, ON | GPIO3 | INPUT |
| SIM | 2.5 V, ON | ADC | OFF |
| RTC_OUT | ON, 1.5 V | SM3 (WHITE LED) | OFF |
| LDO_PM | 3.3 V, ON at OUT POWERED | RGB DRIVER | OFF |
| SM1 | OFF, 1.24 V | INTERRUPT MASK | NONE MASKED |
| SM2 | OFF, 3.32 V | POWER-GOOD MASK | ALL MASKED |
| CHARGER | OFF | | |

After the internal I²C register power-up defaults are loaded the power path control logic is enabled, connecting the external power source to the OUT pin. A status flag (nRAMLOAD) is set to LO in the SOFT_RESET register, indicating that the I²C registers were loaded with the power-up defaults, and the TPS65810 enters the ENABLE state.

8.3.1.3.2 Enable

In the ENABLE mode the $\overline{\text{RESPWRON}}$ output is set to the LO level, the $\overline{\text{INT}}$ pin mode is set to high impedance and all the power-good comparators that monitor the integrated supply outputs are disabled. The ENABLE mode is used by the TPS65810 to detect when the main system power rail (OUT pin) is powered and ready to be used on the internal supply power-up. The OUT pin voltage is sensed by an internal low-system-voltage comparator which holds the IC in the ENABLE mode until the system power-bus voltage (OUT pin) has reached a minimum operating voltage, defined by the user. The internal comparator senses the system voltage at pin SYS_IN, and the threshold for the minimum system operating voltage at the OUT pin is set by the external divider connected from OUT pin to SYS_IN pin. The threshold voltage is calculated in [Equation 1](#).

$$V(\text{OUT}) = V_{(\text{LOW_SYS})} \times \left(1 + \frac{R6}{R1} \right)$$

where

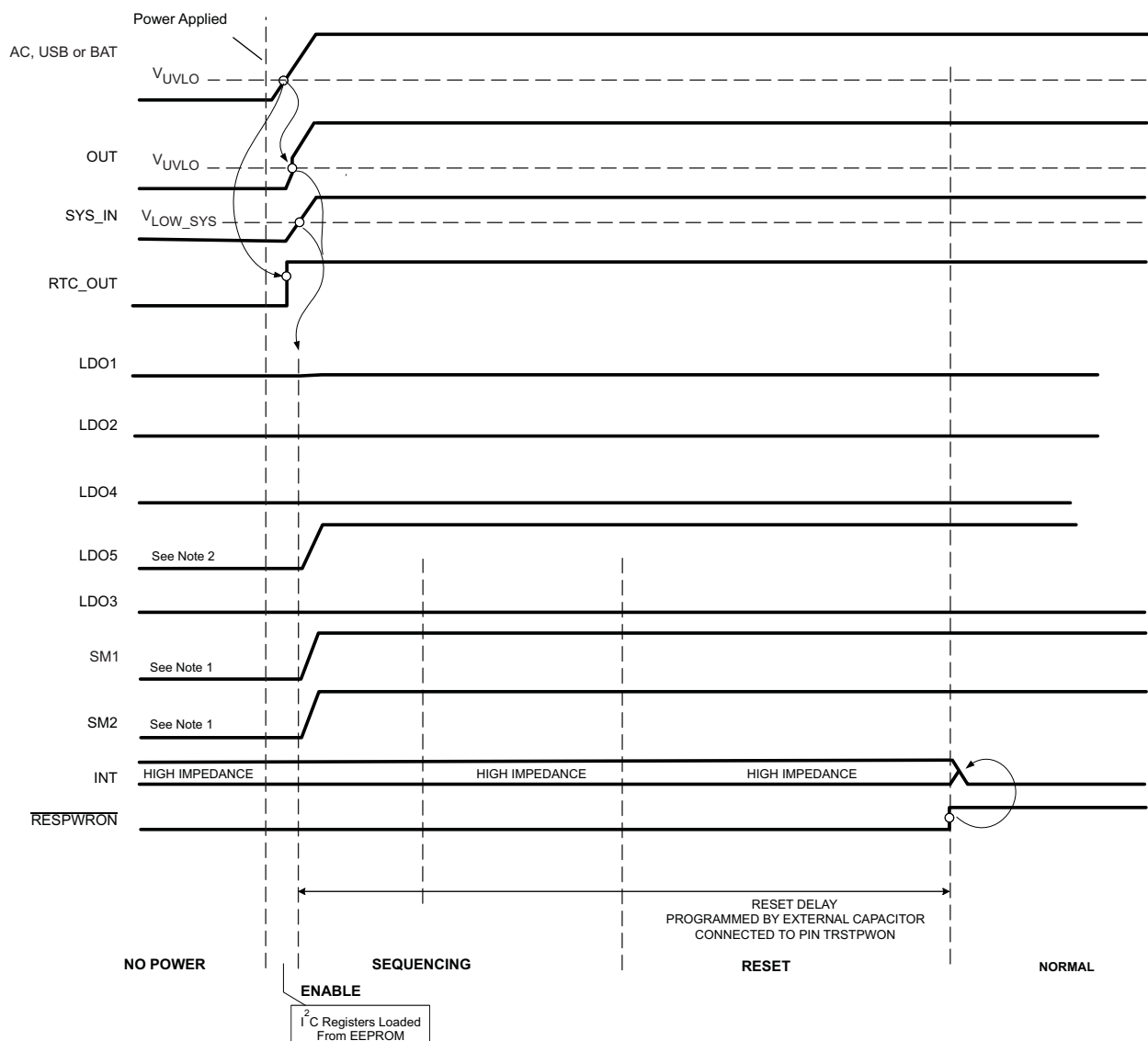
- R6 and R1 are external resistors
 - $V_{(\text{LOW_SYS})} = 1 \text{ V}$ (typical)
- (1)

The minimum system operating voltage must always be set above the internal UVLO threshold V_{UVLO} . In normal application conditions the minimum system operating voltage is usually set to a value that assures that the TPS65810 integrated regulators are not operating in the dropout region.

When the voltage at the SYS_IN pin exceeds the internal threshold $V_{(\text{LOW_SYS})}$ the TPS65810 device is ready to start the system power sequencing, and the SEQUENCING mode is entered.

8.3.1.3.3 Sequencing

The sequencing state starts immediately after the enable state. In this mode of operation the integrated supplies are turned ON. The TPS65810 sequencing timing diagram shown in [Figure 18](#) details the internal timing delays and supply sequencing. At the end of the sequencing state the user-programmable reset timer is started, and the TPS65810 enters the reset state.



- (1) SM1 and SM2 are externally enabled by GPIO1 and GPIO2. This waveform represents the earliest time that SM1 and SM2 are enabled if GPIO1 and GPIO2 are tied high.
- (2) LDO5, SM1, and SM2 are all enabled at the same time. This waveform represents the earliest time that LDO5 is enabled if VIN_LDO35 is connected to OUT. LDO5 power up can be synchronized to SM1 or SM2 by connecting VIN_LDO35 to the SM1 or SM2 output, respectively.

Figure 18. TPS65810 Supply Sequencing Timing

8.3.1.3.4 Reset

When the reset state starts the $\overline{\text{RESPWRON}}$ output is LO. The user can program the reset timer value by selecting the value of the external capacitor connected to pin TRSTPWON, as shown in [Equation 2](#).

$$T_{(\text{RESET})} = K_{\text{RESET}} \cdot C_{\text{TRSTPWON}}$$

where

- K_{RESET} is the reset timer constant (1 ms/nF typical) (2)

The **TPS65810** **RESPWRON** pin must be used to reset the external host. During the external host reset (**RESPWRON** = LO) the I²C SDA and SCL pins are not used to access **TPS65810** internal registers. If a non-standard configuration is used to reset the system the SDA and SCL lines must not be used to communicate with the **TPS65810** until **RESPWRON** = HI, to avoid overwriting the integrated power supply internal power-up settings during the sequencing mode.

The power-good comparators are masked during the reset mode. The reset mode ends when the reset timer expires, and the **TPS65810** goes into the power-good check mode.

The **RESPWRON** signal set to a high level is the proper signal to use as an indicator that the device has transitioned out of the reset state. During the power-up sequence the **RESPWRON** pin is asserted LOW until the RESET TIMER expires. The RESET TIME ($t_{\text{reset}} = 1\text{ms/nF} \times \text{CTRSTPWON}$) can be programmed through a capacitor between the **TRSTPWON** pin and ground.

When the **RESPWRON** signal is LO, all internal and external interrupts are ignored. As a result, the open-drain output that asserts the INT pin LO during a NORMAL MODE interrupt request is disabled. The INT pin is then asserted HI through a pullup resistor that is typically connected to VOUT. After the **RESPWRON** signal goes HI, the interrupt controller is given control of the INT pin. Finally, the rising edge of the **RESPWRON** pin must be used to indicate the PMIC has transitioned from the RESET STATE to the POWER-GOOD CHECK STATE. At that point, the interrupt controller asserts an interrupt if necessary.

8.3.1.3.5 Power-Good Check

In the power-good check mode the power-good comparators are enabled, providing status on the integrated supplies output voltages. An output voltage is considered as out of regulation and generates a fault condition if the output voltage is below 90% of the target output voltage regulation value. If a power-good fault is detected the SLEEP mode is set, if a power-good fault is not detected the NORMAL mode is set.

The individual supply power-good status can be masked through an I²C register PGOODFAULT_MASK. Supplies that have their power-good fault status masked do not generate a power-good fault. However, the status bit for the supply indicates that the output voltage is out of regulation.

The power-good mask register bits default to masked upon power up.

8.3.1.3.6 Sleep Mode

The SLEEP mode is set when a thermal fault or system low voltage fault is detected, under NORMAL operation mode set. This operation mode is also set when a power-good fault is detected during the power-good check state or the I²C bit SLEEP_MODE. In the SLEEP mode the **RESPWRON** output is set to LO, and the I²C registers keep the same contents as in the state preceding SLEEP mode, with the exception of the following control bits, which are reset to the default power-up values:

1. LDO1,2,3,4,5 and RTC_OUT are enabled, SIM LDO is disabled: EN_LDO register set to default values
2. LDO0 disabled, all GPIOs with no control function assigned: GPIO12, GPIO3 registers set to default values
3. White LED driver is set to OFF: SM3_SET register has all bits set to LO
4. RGB drivers are set to OFF: RGB_FLASH, RGB_RED, RGB_GREEN, RGB_BLUE registers are set to default values
5. PWM, PWM_LED drivers OFF: PWM, LED_PWM registers are set to default values
6. ADC engine reset to power-up default: ADC_SET, ADC_DELAY, ADC_WAIT registers are set to default values

NOTE

In SLEEP mode the power path and main internal blocks are still active, but the internal integrated supply sequencing is disabled. As a result of that, during SLEEP mode ALL integrated supplies (ALL LDO's, ALL buck Converters) are disabled.

At the end of the SLEEP mode, the sequencer block uses the I²C control register values (which were reset to the default power-up values) to sequence the integrated power supplies. The SLEEP mode ends when one of the three following events occurs:

1. *If SLEEP was set by thermal fault:* The SLEEP mode ends only when all external input supplies and battery pack are removed and a UVLO condition is detected by the **TPS65810**, setting the NO POWER mode.

2. If *SLEEP* was set by a system low voltage detection, or *I²C* bit *SLEEP_MODE*, only with battery present: Input power must be connected, setting the TPS65810 in the *ENABLE* mode. If no input power is inserted, the battery discharges until the TPS65810 detects a *UVLO* condition and enters the *NO POWER* mode.
3. If *sleep* was set by a system low voltage detection, power-good fault or *SLEEP_MODE*, with battery and input power present: all external input supplies connected to *AC* and *USB* pins must be removed, and then at least one of them reconnected to the system. The input power cycling triggers a transition from *SLEEP* mode to the *ENABLE* mode.

8.3.1.3.7 Normal Mode

If a power-good fault is not present at the end of the power-good check mode the *NORMAL* mode starts. In this mode of operation the *I²C* registers define the TPS65810 operation, and the host has full control on operation modes, parameter settings, and so forth. The normal state operation ends if a thermal fault, system low voltage fault ($V(\text{SYS_IN}) < V_{\text{LOW_SYS}}$) or power-good fault is detected. A thermal fault or system low voltage fault sets the *SLEEP* mode operation, a power-good fault sets the *NO POWER* operation mode. From the normal mode the converters *SM1* and *SM2* can be set in the *STANDBY* mode, with reduced output voltages. In *NORMAL* mode either an *I²C* register bit (*SOFT_RESET* register bit *SOFT_RST*) or a hardware input (*HOT_RESET* pin set to *LO*) can trigger a transition to the *RESET* state, enabling implementation of a host reset function. In *NORMAL* mode an *I²C* register bit (*SOFT_RESET* register bit *SLEEP_MODE*) can trigger a transition to *SLEEP* mode.

8.3.1.3.8 Processor Standby State

This state is set using an *I²C* register or a *GPIO* configured as *SM1* and *SM2* stand-by control. In stand-by mode operation, the *SM1* and *SM2* voltages are set to value distinct than the normal mode output voltage, and *SM1/SM2* are set to *PFM* mode. The stand-by output voltage is defined in *I²C* registers *SM1_STANDBY* and *SM2_STANDBY*.

8.3.1.4 TPS65810 Operating Mode Controls

The three operating mode controls are defined as follows:

HARDWARE RESET A dedicated control pin, *HOT_RESET*, enables implementation of a hardware reset function. The system reset pin *RESPWRON* is set to *LO* when *HOT_RESET* = *LO* for a period longer than the internal deglitch (5 ms typical). The *RESET* mode is started when the *HOT_RESET* pin transitions from *LO* to *HI*, as shown in the state diagram. When *HOT_RESET* = *LO* all *I²C* registers are reset to the default power-up values.

SOFTWARE RESET The external host can set the TPS65810 device in *RESET* mode using the *I²C* register *SOFT_RESET*, bit *B0* (*SOFT_RST*).

SOFTWARE SLEEP The external host can set the TPS65810 in *SLEEP* mode using the *I²C* register *SOFT_RESET*, bit *B6* (*SLEEP_MODE*).

A software reset does not affect the contents of the *I²C* registers.

8.3.1.5 Functionality Reference Guide – Host Interface and System Sequencing

Table 2. Interrupt Controller, Open-Drain Output (INT)

| SYSTEM PARAMETERS MONITORED BY THE INTERRUPT CONTROLLER | | | | | POWER UP DEFAULT |
|---|---|---|--|--|---|
| SUPPLY OUTPUT POWER-GOOD FAULT DETECTION ⁽¹⁾ | SYSTEM STATUS MODIFICATION | ADC STATUS | CHARGER STATUS TRANSITION | INPUT AND OUTPUT POWER TRANSITION | |
| SM1, SM2, SM3, LDO1, LDO2, LDO3, LDO4, LDO5 | Thermal Fault or GPIO 1,2 configured as external interrupt request | ADC conversion end ADC Input out of range External resistive load connected to ANLG1 | Charge: Pre↔ Fast ↔Done DPPM:on ↔ off Charge Suspend: on ↔ off Thermal Foldback: on ↔ off | AC detected: yes ↔ no USB detected: yes ↔ no Input OVP: yes ↔ no System Power: AC ↔ USB | All interrupt controller inputs set to non-masked |
| Can be masked Individually through I ² C. Blanked during initial power up | Can be masked Individually through I ² C | | Can be masked as a group through a single I ² C mask register bit | | |

- (1) For all supplies (except) for *SM3* an output fault is detected if the output voltage is below 90% of the programmed regulation voltage. In the *SM3* converter an output fault indicates that the output *OVP* threshold was reached.

Table 3. Events Triggering TPS65810 Operating Mode Changes

| EVENT | POWER-GOOD FAULT DETECTION ⁽¹⁾ | THERMAL FAULT | HARDWARE RESET | SOFTWARE RESET |
|-----------------------------|---|--|--|--|
| How transition is triggered | Integrated regulator output voltage below target value: SM1, SM2, SM3, LDO1, LDO2, LDO3, LDO4, LDO5 | Internal IC junction temperature | Using $\overline{\text{HOT_RST}}$ control pin | I ² C register control bit |
| Operating mode change | Sets Sleep mode or starts a new power-up cycle when power-good fault is detected (see state machine diagram). | Sets Sleep mode when thermal fault is detected | Generates external host reset pulse at pin $\overline{\text{RESPWON}}$ when $\overline{\text{HOT_RST}} = \text{LO}$. | Generates external host reset pulse at pin $\overline{\text{RESPWON}}$ when I ² C control bit is set. |
| | Power-good fault detection comparators are blanked during initial power-up. | Input and Battery power cycling required to exit sleep | Pulse duration set by external capacitor. | Pulse duration set by external capacitor. |
| Controls | Can be masked Individually through I ² C. | Fixed Internal Threshold | External Input | Set through I ² C |

(1) For all supplies (except) for SM3 an output fault is detected if the output voltage is below 90% of the programmed regulation voltage. In the SM3 converter an output fault indicates that the output OVP threshold was reached.

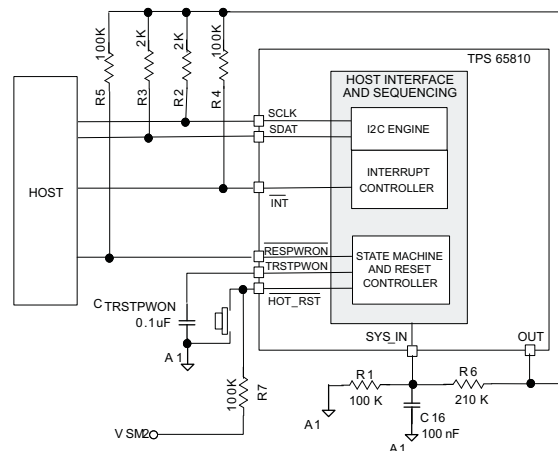


Figure 19. Required External Components, Recommended Values, External Connections

8.3.2 Power Path and Charge Management

8.3.2.1 Overview

The TPS65810 has an integrated charger with power path integrated MOSFETs. This topology, shown in Figure 20, enables using an external input power to run the system and charge the battery simultaneously. The power path has dual inputs that can be used to select either an external AC_DC adapter (AC pin) or an USB port power (USB pin) to power the end equipment main power rail (OUT pin, also referred to as the system power bus) and charge the battery pack (connected to BAT pin).

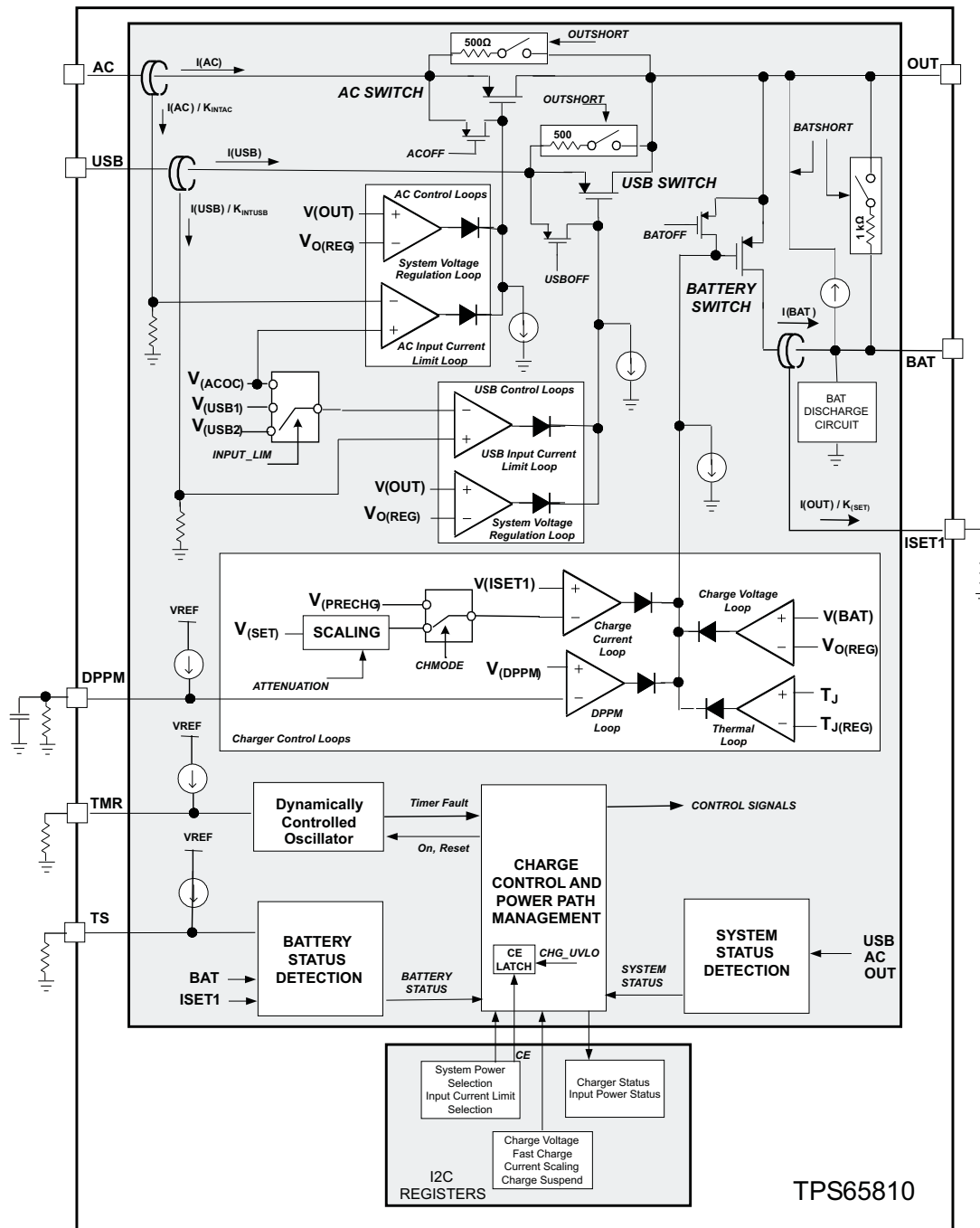


Figure 20. TPS65810 Charger and Power Path Section Simplified Block Diagram

The power path has three integrated power MOSFETs: the battery to system MOSFET (battery switch), the AC input to system MOSFET (AC switch) and the USB input to system MOSFET (USB switch). Each of those power MOSFETs can be operated either as an ON/OFF switch or as a linear pass element under distinct operating conditions, as defined by the control circuits that set the power MOSFET gate voltage.

The TPS65810 regulates the voltage at the OUT pin to 4.6 V when one of the external supplies connected to pins AC or USB is powering the OUT pin. The selected input (AC or USB pin) current is limited to a value defined by I²C register settings. The input current limit function assures compatibility with USB standard requirements, and also implements a protection function by limiting the maximum current supplied by an external AC_DC adapter or USB port power terminal.

The AC power MOSFET and USB power MOSFET operating modes are set by integrated control loops. Each of the power MOSFETs is controlled by two loops: one system voltage regulation loop and one input current limiting loop. The integrated loops modulate the AC or USB power MOSFETs drain to source resistance to regulate either the OUT pin voltage or to limit the input current. If no input power is present (AC and USB input power not detected) the AC and USB power MOSFETs are turned OFF, and the battery MOSFET is turned ON, connecting the BAT pin to the OUT pin.

The battery switch is turned ON when the AC or USB input power is detected and the charger function is enabled, charging the battery pack. During charge the battery MOSFET switch operation mode is defined by the charger control loops. The battery MOSFET switch drain-to-source resistance is modulated by the charge current loop and charge voltage loop to implement the battery charging algorithm. In addition to that multiple safety functions are activated (thermal shutdown, safety timers, short-circuit recovery), and additional functions (thermal loop and DPPM loop) optimize the charging process.

8.3.2.2 Power Path Management Function

8.3.2.2.1 Detecting the System Status

The power path and charge management block operate independently of the other TPS65810 circuits. Internal circuits check battery parameters (pack temperature, battery voltage, charge current) and system parameters (AC and USB voltage, battery voltage detection), setting the power path MOSFETs operating modes automatically. The TPS65810 has integrated comparators that monitor the battery voltage, AC pin voltage, USB pin voltage and the OUT pin voltage. The data generated by those comparators is used by the power path control logic to define which of the integrated power path switches are active. Figure 21 shows a simplified block diagram for the system status detection.

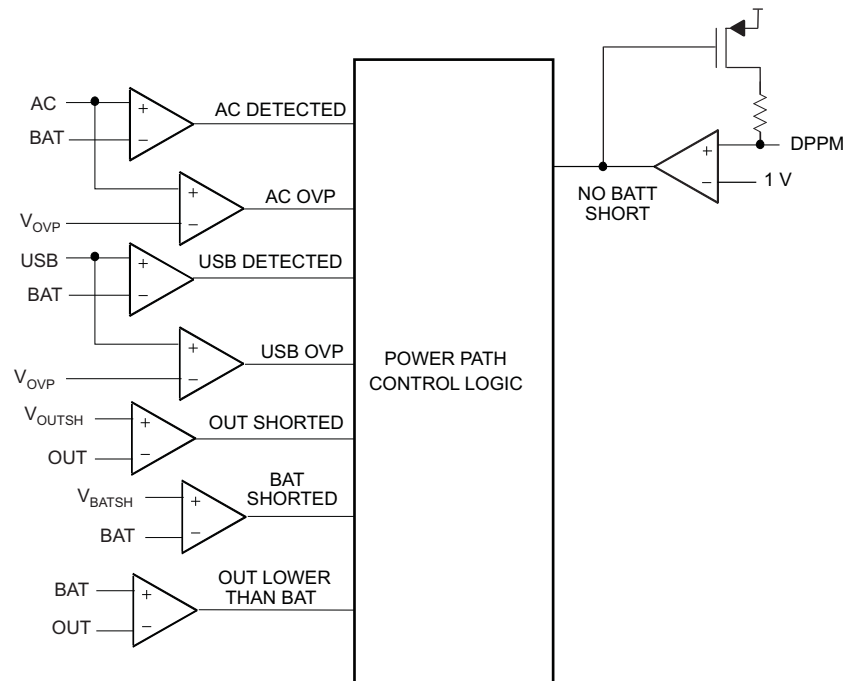


Figure 21. TPS65810 Systems Status Detection, Charger and Power Path Section

Table 4 lists the system power detection conditions. $V_{IN(DT)}$, V_{OUTSH} , V_{BATSH} , V_{OVP} are the TPS65810 internal references, refer to the electrical characteristics in the [Specifications](#) section for additional details.

Table 4. System Status Detection, Charger and Power Path Section

| SYSTEM STATUS DETECTION | CONDITION |
|--|----------------------------------|
| AC input voltage detected | $V(AC) - V(BAT) > V_{IN(DT)}$ |
| USB input voltage detected | $V(USB) - V(BAT) > V_{IN(DT)}$ |
| AC overvoltage detected | $V(AC) > V_{OVP}$ |
| USB overvoltage detected | $V(USB) > V_{OVP}$ |
| AC PIN TO OUT pin OR USB TO OUT PIN short detected | $V(OUT) < V_{INOUTSH}$ |
| BAT pin to OUT pin short detected | $V(BAT) - V(OUT) > V_{BATOUTSH}$ |
| Battery supplement mode need detected | $V(BAT) - V(OUT) > V_{SUP}$ |
| Blank BAT to OUT short circuit detection | $V(DPPM) < 1V$ |

8.3.2.2.2 Power Path Logic: Priority Algorithm

The system power bus supply is automatically selected by the power path control logic, following an internal algorithm. The power path function detects an external input power connection when the input voltage exceeds the battery pack voltage. It also detects a supplement mode need (battery switch must be turned ON) when the system voltage (OUT pin) is below the battery voltage. A connected and non-selected external supply or the battery is automatically switched to the system bus, following the priority algorithm, when the external supply currently selected is disconnected from the system.

The input power priority is hard-wired internally, with the AC input having the higher priority, followed by the USB input (2nd) and the battery pack (3rd). Using the I²C CHG_CONFIG register control bit CE the user can override the power path algorithm, connecting the battery to the system power bus. Take care when using the battery-to-system connection option, as the system power bus **is not** connected back to the AC or USB inputs (even if those are detected) when the battery is removed. [Table 5](#) describes the priority algorithm.

Table 5. Power Path Control Logic Priority Algorithm

| CE BIT (I ² C CHG_CONFIG Register) | EXTERNAL SUPPLY DETECTED | | SWITCH MODE | | | SYSTEM POWER SOURCE |
|--|-----------------------------|-----|-------------|-----|---|------------------------|
| | AC | USB | AC | USB | BATTERY | |
| HI | YES | NO | ON | OFF | ON if Supplement mode is required, OFF otherwise | AC |
| | NO | YES | OFF | ON | | USB |
| | YES | YES | ON | OFF | | AC |
| | NO | NO | OFF | OFF | | BATTERY |
| LO | XX | XX | OFF | OFF | ON | BATTERY |

The power path status is stored in register CHG_STAT.

8.3.2.2.3 Input Current Limit

The USB input current is limited to the maximum value programmed by the host, using the I²C interface. If the system current requirements exceed the input current limit, the output voltage collapses, the charge current is reduced, and finally, the supplement mode is set. The input current limit value is set with the I²C charge control register bits PSEL and ISET2, and it is applied to the USB input ONLY. The AC input current limit is fixed to the internal short circuit limit value.

Table 6. Charge-Current Scaling Through I²C

| PSEL (I ² C) | ISET2 (I ² C) | INPUT CURRENT LIMIT | |
|-------------------------|--------------------------|---------------------|--------|
| | | USB | AC |
| LO | LO | 100 mA | 2.75 A |
| LO | HI | 500 mA | 2.75 A |
| HI | LO | 2.75 A | 2.75 A |
| HI | HI | 2.75 A | 2.75 A |

8.3.2.2.4 System Voltage Regulation

The system voltage is regulated to a fixed voltage when one of the input power supplies is connected to the system. The system voltage regulation is implemented by a control loop that modulates the selected switch Rds(on).

The typical system regulation voltage is 4.6 V.

8.3.2.2.5 Input Overvoltage Detection

The AC and USB input voltages are monitored by voltage comparators that identify an overvoltage condition. If an overvoltage condition is detected a status register bit is set, indicating a potential fault condition.

When an overvoltage condition is detected, the AC or USB switches state is not modified. If any of those switches was ON, it is kept in the ON state. During overvoltage conditions, the system voltage is still regulated, and no major safety issues are observed when not modifying the input switch state.

If the input overvoltage condition results in excessive power dissipation, the thermal shutdown circuit is activated, the AC and USB switches are turned OFF, and the BAT switch is turned ON.

8.3.2.2.6 Output Short-Circuit Detection

If the OUT pin voltage falls below an internal threshold V_{INOUTSH} the AC and USB switches are turned off and internal pullup resistors are connected from AC pin to OUT pin and USB pin to OUT pin. When the short circuit is removed those resistors enable the OUT pin voltage to rise above the V_{INOUTSH} threshold, returning the system to normal operation.

8.3.2.2.7 Battery Short-Circuit Detection

If the OUT pin voltage falls below the BAT pin voltage by more than an internal threshold V_{BATOUTSH} the battery switch is turned off and internal pullup resistor is connected between the OUT pin and the BAT pin. This resistor enables detection of the short removal, returning the system to normal operation.

8.3.2.2.8 Initial Power Path Operation

During the initial TPS65810 power-up the contents of the ISET2, CE and SUSPEND bits on the control register are immediately implemented. The charger is disabled (SUSPEND=LO) and the selected input current limit is set internally to 500 mA max.

8.3.2.2.9 No-Battery Detection Circuit

The ANLG1 pin may be used to detect the connection of an external resistor that is embedded in a battery pack and is used as a pack ID function. The ANLG1 pin has an internal current source connected between OUT and ANLG1, which is automatically enabled when the TPS65810 is not in SLEEP mode. The current levels for ANLG1 pin can be programmed through I²C register ADC_WAIT, bits BATID_n, as shown in Figure 22.

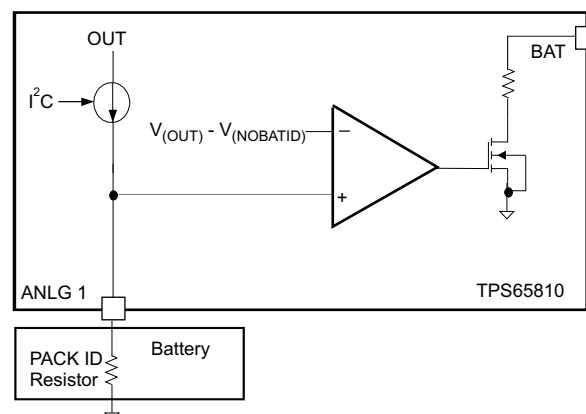


Figure 22. Battery Removal Detection, ANLG1 Pin

An internal comparator with a fixed deglitch time, $t_{DGL(NO\text{BAT})}$ monitors the ANLG1 pin voltage, if $V(\text{ANLG1}) > V(\text{OUT}) - V_{\text{NOBATID}}$, a battery removed condition is detected and an internal discharge switch is activated, connecting an internal resistor from BAT pin to AGND1. Note that ANLG1 can also be used as an analog input for the ADC converter, in this case the voltage at pin ANLG1 must never exceed the $V(\text{OUT}) - V_{\text{NOBATID}}$ threshold to avoid undesired battery discharge.

8.3.2.2.10 Using the Input Power to Run the System and Charge the Battery Pack

The external supply connected to AC or USB pins must be capable of supplying the system power and the charger current. If the external supply power is not sufficient to run the system and charge the battery pack the TPS65810 executes a two-stage algorithm that prevents a low voltage condition at the system power bus:

1. The charge current is reduced, until the total (charger + system current) is at a level that can be supplied by the external input supply. This function is implemented by a dedicated charger control loop (see [Dynamic Power Path Management](#) for additional details).
2. The battery switch is turned ON if the charge current is reduced to zero and the input current is not enough to run the system. In this mode of operation both the battery and the external input power supply the system power (supplement operation mode).

The supplement operation mode is automatically set by the TPS65810 when the input power is switched to the OUT pin, and the OUT pin voltage falls below the battery voltage.

8.3.2.3 Battery Charge Management Function

8.3.2.3.1 Operating Modes

The TPS65810 supports charging of single-cell Li-Ion or Li-Pol battery packs. The charge process is executed in three phases: precharge (or preconditioning), constant current and constant voltage.

The charge parameters are selectable through I^2C interface and using external components. The charge process starts when an external input power is connected to the system, the charger is enabled by the I^2C register CHG_CONFIG bits CE = HI and CHGON = HI, and the battery voltage is below the recharge threshold, $V(\text{BAT}) < V_{\text{RCH}}$. When the charge cycle starts a safety timer is activated. The safety timer timeout value is set by an external resistor connected to the TMR pin.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If $V(\text{BAT}) < 3\text{ V}$ (typical) the BAT pin current is internally set to 10% of the programmed charge current value. [Figure 23](#) shows a typical charge profile for an operation condition that does not cause the IC junction temperature to exceed 125°C (typical).

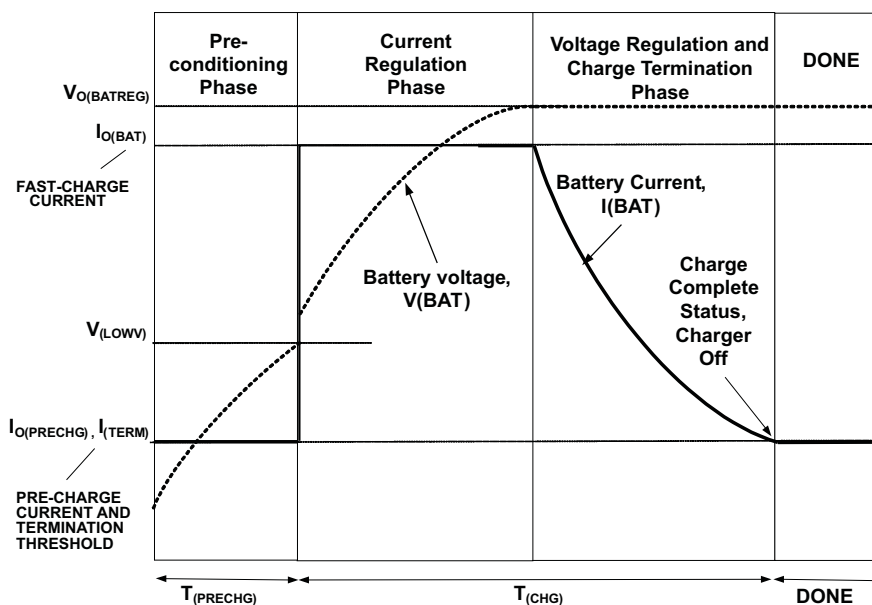


Figure 23. Typical Charge Cycle, Thermal Loop not Active

If the operating conditions cause the IC junction temperature to exceed 125°C the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to 125°C, effectively regulating the IC junction temperature.

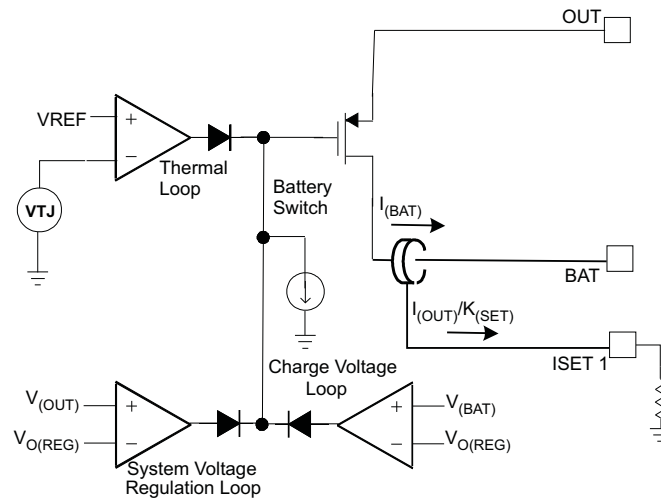


Figure 24 shows a modified charge cycle, with the thermal loop active.

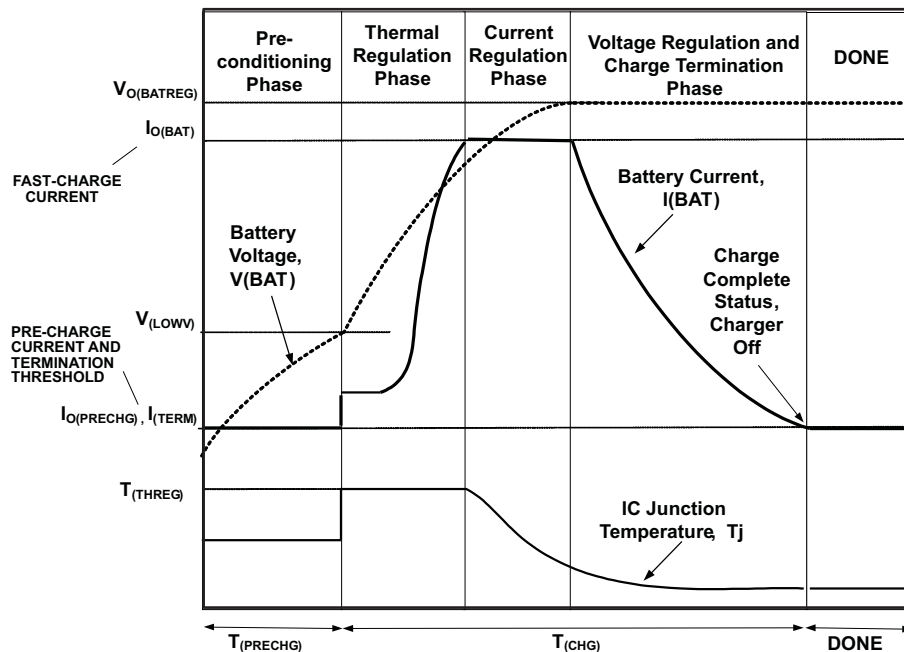


Figure 24. Typical Charge Cycle, Thermal Loop Active

8.3.2.3.2 Battery Preconditioning

The TPS65810 applies a precharge current $I_{O(PRECHG)}$ to the battery if the battery voltage is below the $V_{(LOWV)}$ threshold, preconditioning deeply discharged cells. The charge current loop regulates the ISET1 pin voltage to an internal reference value, $V_{(PRECHG)}$. The resistor connected between the ISET1 and AGND pins, R_{SET} , determines the precharge rate.

The precharge rate programmed by R_{SET} is always applied to a deeply discharged battery pack, independently of the input power selection (AC or USB). Use Equation 3 to calculate the precharge current.

$$I_{O(PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}}$$

where

- $K_{(SET)}$ is the charge current scaling factor
- $V_{(PRECHG)}$ is the precharge set voltage

(3)

8.3.2.3.3 Constant Current Charging

The constant charge current mode (fast charge) is set when the battery voltage is higher than the precharge voltage threshold. The charge current loop regulates the ISET1 pin voltage to an internal reference value, $V_{(SET)}$. The fast charge current regulation point is defined by the external resistor connected to the ISET1 pin, R_{SET} , as shown in the following:

$$I_{O(BAT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}}$$

where

- $V_{(SET)}$ (2.5 V typical) is the voltage at ISET1 pin during charge current regulation
- $K_{(SET)}$ = charge- current scaling factor

(4)

The reference voltage $V_{(SET)}$ can be reduced through I²C register CHG_CONFIG bits ISET1_1 and ISET1_0. $V_{(SET)}$ can be selected as a percentage (75%, 50% or 25%) of the original 2.5 V typ, non-attenuated $V_{(SET)}$ value, effectively scaling down the charge current.

The ISET1 resistor always sets the maximum charge current if the AC input is selected. When the USB input is selected, the maximum charge current is defined by the USB input current limit and the programmed charge current. If the USB input current limit is lower than the $I_{O(OUT)}$ value, the battery switch is set in the dropout region and the charge current is defined by the input current limit value and system load, as shown in Figure 25.

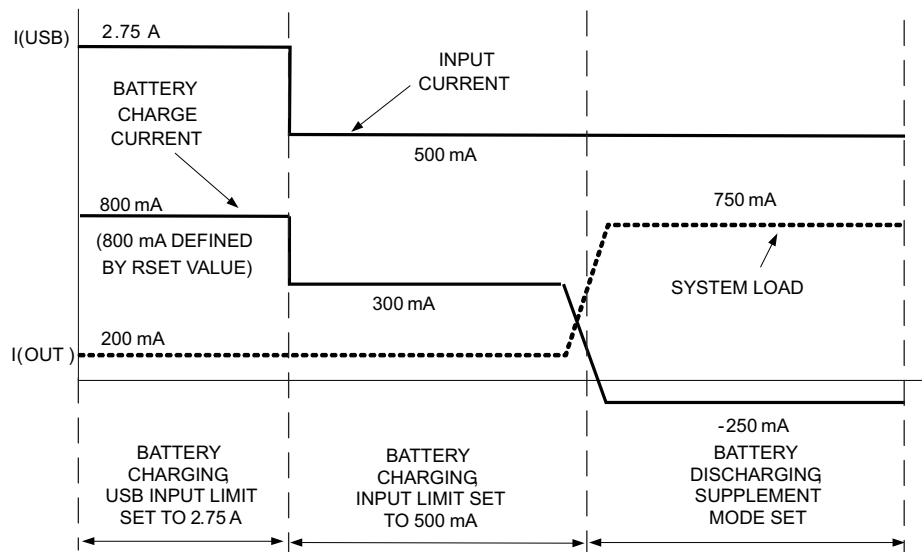


Figure 25. Input Current Limit Impact on Effective Charge Current

8.3.2.3.4 Charge Termination and Recharge

The TPS65810 monitors the charging current during the voltage regulation phase. Charge is terminated when the charge current is lower than an internal threshold, set to 10% (typical) of the fast charge current rate. The termination point applies to both AC and USB charging. Use Equation 5 to calculate the termination point, $I_{(TERM)}$.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}}$$

where

- $V_{(TERM)}$ is the termination detection voltage reference (5)

The voltage at ISET1 pin is monitored to detect termination, and termination is detected when $V_{(SET1)} < V_{(TERM)}$ (0.25 V typical). The voltage reference $V_{(TERM)}$ is internally set to 10% of the $V_{(SET)}$ reference voltage, and it is modified if the reference voltage $V_{(SET)}$ is scaled through I²C register CHG_CONFIG bits ISET1_1 and ISET1_0. $V_{(TERM)}$ is reduced by the same percentage used to scale down $V_{(SET)}$.

Table 7 lists the charge current and termination thresholds for a 1-A charge current set (1-kΩ resistor connected to ISET1 pin), with the selected input current limit set to a value higher than the programmed charge current. The termination current is scaled for all charge current modes (AC or USB), as it is always set by the ISET1 pin external resistor value.

Table 7. Charge Current and Termination Threshold Selection Example

| CHARGE CONTROL REGISTER BITS | | CHARGE CURRENT, (% OF TYPICAL VALUE PROGRAMMED BY ISET1 RESISTOR) | $V_{(SET)}$ (V) | $V_{(TERM)}$ (mV) | CHARGE CURRENT (A) | TERMINATION CURRENT (mA) |
|------------------------------|---------|---|-----------------|-------------------|--------------------|--------------------------|
| ISET1_1 | ISET1_0 | | | | | |
| 0 | 0 | 25% | 0.6 | 60 | 0.24 | 20 |
| 0 | 1 | 50% | 1.25 | 115 | 0.5 | 40 |
| 1 | 0 | 75% | 1.9 | 160 | 0.78 | 60 |
| 1 | 1 | 100% | 2.5 | 250 | 1 | 100 |

When the termination is detected, a new charge cycle starts if the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. A new charge start is also triggered if the charger is enabled, disabled, or re-enabled through I²C (CHG_CONFIG register bits CE or CHGON), or if both AC and USB input power are removed and then at least one of them is re-inserted.

The termination is disabled when the thermal loop OR DPPM loop are active, and during supplement mode.

8.3.2.3.5 Battery Voltage Regulation, Charge Voltage

The voltage regulation feedback is implemented by sensing the BAT pin voltage, which is connected to the positive side of the battery pack. The TPS65810 monitors the battery-pack voltage between the BAT and AGND1 pins, when the battery voltage rises to the $V_{O(REG)}$ threshold the voltage regulation phase begins and the charging current tapers down.

The charging voltage can be selected as 4.2 V or 4.365 V (typical). The default power-up voltage is 4.2 V. As a safety measure the 4.365 V charge voltage is programmed only if two distinct bits are set through I²C: VCHG=HI in the CHG_CONFIG, and CHG_VLTG=LO in the GPIO3 register.

8.3.2.3.6 Temperature Qualification

The TPS65810 charger section does not monitor the battery temperature. This function may be implemented by an external host, which can measure the pack temperature by monitoring the ADC channel connected to the TS pin. An external pullup resistor must be connected to the TS pin to bias the pack thermistor, as the TPS65810 device has no internal current source connected to the TS pin.

8.3.2.3.7 Dynamic Power Path Management

Under normal operating conditions, the OUT pin voltage is regulated when the AC or USB pin is powering the OUT pin and the battery pack is being charged. If the total (system + charge current) exceeds the available input current, the system voltage drops below the regulation value.

The dynamic power path management function monitors the system output voltage. A condition where the external input supply rating has been exceeded or the input current limit has been reached is detected when the OUT pin voltage drops below an user-defined threshold, V_{DPPM} . Use Equation 6 to calculate the value of V_{DPPM} .

$$V_{DPPM} = R_{DPPM} \times K_{DPPM} \times I_{DPPM}$$

where

- R_{DPPM} = external resistor connected to DPPM pin
- K_{DPPM} = DPPM scaling factor
- I_{DPPM} = DPPM pin internal current source

(6)

To correct this situation the DPPM loop reduces the charge current, regulating the OUT pin voltage to the user-defined V_{DPPM} threshold. The DPPM loop effectively identifies the maximum current that can be delivered by the selected input and dynamically adjusts the charge current to guarantee that the end equipment is always powered. To minimize OUT voltage ripple during DPPM operation the V_{DPPM} threshold must be set just below the system regulation voltage.

If the charge current is reduced to zero by the DPPM and the input current is still lower than the OUT pin load, the output voltage falls below the DPPM threshold, decreasing until the battery supplement mode is set [$V(OUT) = V(BAT) - V_{SUP(DT)}$].

8.3.2.3.8 Charger Off Mode

The TPS65810 charger circuitry enters the low-power OFF mode if both AC and USB power are not detected. This feature prevents draining the battery during the absence of input supply.

8.3.2.3.9 Precharge Safety Timer

The TPS65810 device activates an internal safety timer during the battery preconditioning phase. The precharge safety timer time-out value is set by the external resistor connected to TMR pin, RTMR, and the timeout constants K_{PRE} and K_{TMR} . Use Equation 7 to calculate the timeout value of the precharge safety timer.

$$T_{PRECHG} = K_{PRE} \times R_{TMR} \times K_{TMR}$$

(7)

The K_{PRE} constant typical value is 0.1, setting the precharge timer value to 10% of the charge safety timer value.

When the charger is in suspend mode, set through I²C register CHG_CONFIG bit CHGON or set by a pack temperature fault, the precharge safety timer is put on hold (that is, charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If $V(BAT)$ does not reach the internal voltage threshold V_{PRECHG} within the precharge timer period a fault condition is detected and the charger is turned off.

If the TMR pin is left floating, an internal resistor of 50 K Ω (typical) is used to generate the time base used to set the precharge timeout value. The typical precharge timeout value can be then calculated using Equation 8.

$$T_{PRECHG} = K_{PRE} \times 50K \times K_{TMR}$$

(8)

8.3.2.3.10 Charge Safety Timer

As a safety mechanism the TPS65810 has a user-programmable timer that measures the total fast charge time. This timer (charge safety timer) is started at the end of the preconditioning period. The safety charge timeout value is set by the value of an external resistor connected to the TMR pin R_{TMR} . Use Equation 9 to calculate the charge safety timer time-out value.

$$T_{CHG} = K_{TMR} \times R_{TMR}$$

(9)

When the charger is in suspend mode, set through I²C register CHG_CONFIG bit CHGON or set by a pack temperature fault, the charge safety timer is put on hold (that is, charge safety timer is not reset). Normal operation resumes when the charger exits the suspend mode. If charge termination is not reached within the timer period a fault condition is detected, and the charger is turned off.

The charge safety timer is held in reset if the TMR pin is left floating. Under this mode of operation an internal resistor, 50 k Ω typical, sets the internal charger and power path deglitch and delay times, as well as the precharge safety timer timeout value.

8.3.2.3.11 Timer Fault Recovery

The TPS65810 provides a recovery method to deal with timer fault conditions. The following summarizes this method:

- Condition 1: Charge voltage above recharge threshold, $V_{(RCH)}$, and timeout fault occurs.

Recovery method The IC waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. When the battery falls below the recharge threshold, the IC clears the fault and starts a new charge cycle.

- Condition 2: Charge voltage below recharge threshold, $V_{(RCH)}$, and timeout fault occurs.

Recovery method Under this scenario, the IC connects an internal pullup resistor from OUT pin to BAT pin. This pullup resistor is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the IC disables the pullup resistor connection and executes the recovery method described for condition 1.

All timers are reset and all timer fault conditions are cleared when a new charge cycle is started either through I²C (toggling CHG_CONFIG bits CE, CHGON) or by cycling the input power. All timers are reset and all timer fault conditions are cleared when the TPS65810 enters the UVLO mode.

8.3.2.3.12 Dynamic Timer Function

The charge and precharge safety timers are programmed by the user to detect a fault condition if the charge cycle duration exceeds the total time expected under normal conditions. The expected total charge time is usually calculated based on the fast charge current rate.

When the thermal loop or the DPPM loops are activated the charge current is reduced, and a false safety timer fault can be observed if this mode of operation is active for a long periods. To avoid this undesirable fault condition the TPS65810 activates the dynamic timer function when the DPPM and thermal loops are active. The dynamic timer function slows down the safety timers clock, effectively adding an extra time to the programmed timeout value as follows:

- If the battery voltage is below the battery depleted threshold: the precharge timer value is modified while the thermal loop or the DPPM loop are active
- If the battery voltage is above the precharge threshold: the safety timer value is modified if the DPPM or the thermal loop are active AND the battery voltage is below the recharge threshold.

The TPS65810 dynamic timer function circuit monitors the voltage at pin ISET1 during precharge and fast charge. When the charger is regulating the charge current, the voltage at pin ISET1 is regulated by the control loops to either $V_{(SET)}$ or $V_{(PRECHG)}$. If the thermal loop or DPPM loops are active, the voltage at pin ISET1 is lower than $V_{(SET)}$ or $V_{(PRECHG)}$, and the dynamic timer control circuit changes the safety timers clock period based on the $V_{(SET)}/V(ISET1)$ ratio (fast charge) or $V_{(PRECHG)}/V(ISET1)$ ratio (precharge).

The maximum *clock period* is internally limited to twice the value of the programmed clock period, which is defined by the resistor connected to TMR pin, as shown in Figure 26.

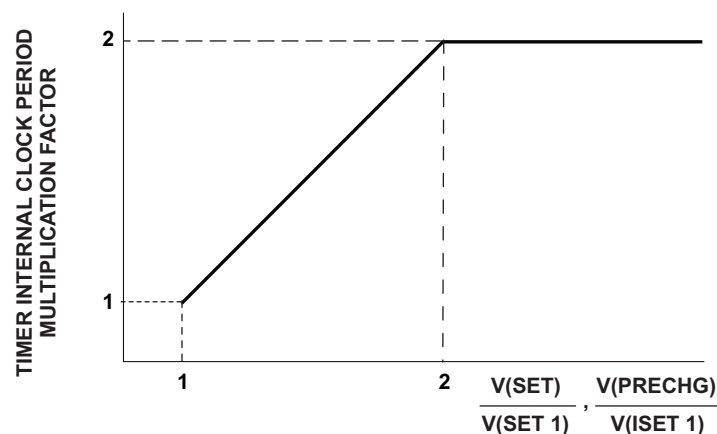


Figure 26. Safety Timer Internal Clock Slowdown

The effective charge safety timer value can then be expressed as follows:

$$\text{Effective precharge timeout} = t_{(\text{PRECHG})} + t_{(\text{PCHGADD})}$$

$$\text{Effective charge safety timeout} = t_{(\text{CHG})} + t_{(\text{CHGADD})}$$

The *added* timeout values, $t_{(\text{PCHGADD})}$, $t_{(\text{CHGADD})}$, are equal to the sum of all time periods when either the thermal loop or DPPM loops were active. The *maximum added* timeout value is internally limited to $2 \times t_{(\text{CHG})}$ or $2 \times t_{(\text{PRECHG})}$

8.3.2.4 Functionality Guide — System Power and Charge Management

Table 8. Charge Management

| FAST CHARGE ⁽¹⁾ | | PRECHARGE CURRENT | TERMINATION | | CHARGE VOLTAGE | PRECHARGE VOLTAGE | SAFETYTIMER TIMEOUT | POWER UP DEFAULT |
|---|--|----------------------------|--|--|------------------------------|-------------------|-------------------------------|------------------|
| CHARGE CURRENT VALUE | CHARGE CURRENT SCALING | | CURRENT | CURRENT SCALING | | | | |
| $I_{O(\text{BAT})}$, Programmable, 1.5 A (maximum) | 25%, 50%, 75%, 100% of $I_{O(\text{BAT})}$ | 10% of $I_{O(\text{BAT})}$ | $I_{(\text{TERM})}$, 10% of $I_{O(\text{BAT})}$ | 25%, 50%, 75%, 100% of $I_{(\text{TERM})}$ value | 4.2 V or 4.36 V | 3 V | Programmable | Charger OFF |
| Set through external resistor | Set through I ² C | Fixed ratio | Fixed ratio | Set through I ² C | Set through I ² C | Fixed | Set through external resistor | |

- (1) The input current limit (see [Table 9](#)) regulates the input current, effectively limiting the charge current if the input current limit is lower than the fast charge current value programmed.

Table 9. Power Path Management

| INPUT CURRENT LIMIT | | INPUT CONNECTED TO OUT PIN | | POWER UP DEFAULT |
|------------------------------|---|---|---|--|
| AC PIN | USB PIN | INPUT POWER TO SYSTEM | BATTERY TO SYSTEM | |
| 2.5 A typical | 100 mA maximum or 500 mA maximum or 2.5 A typical | #1 – AC #2 – USB #3 – Battery (when AC pin power and USB pin power are not detected) | Battery connected to system, independently of battery voltage | Input Power to System, USB mode selected, 100 mA max |
| Internal fixed current limit | Set through I ² C | Automatic internal algorithm | Set through I ² C, overrides internal algorithm | |

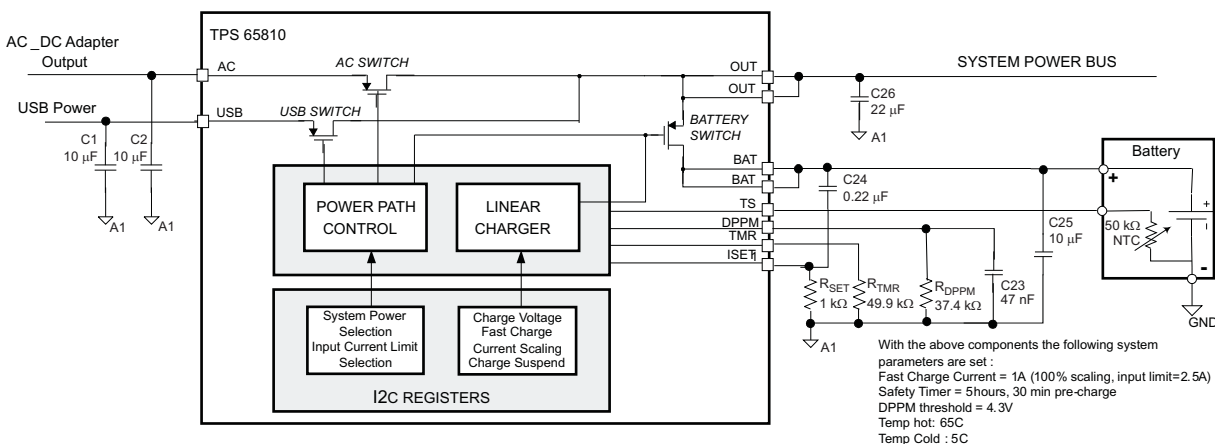


Figure 27. Required External Components, Recommended Values, External Connections

8.3.3 Linear Regulators

The TPS65810 offers nine integrated linear regulators, designed to be stable over the operating load range with use of external ceramic capacitors, as long as the recommended filter capacitor values (see [Figure 51](#) and the [Pin Configuration and Functions](#) section) are used. The output voltage can be programmed through I²C (LDO0-2, LDO3-5) or have a fixed output voltage.

8.3.3.1 Simplified Block Diagram

Figure 28 shows a simplified block diagram for the LDOs.

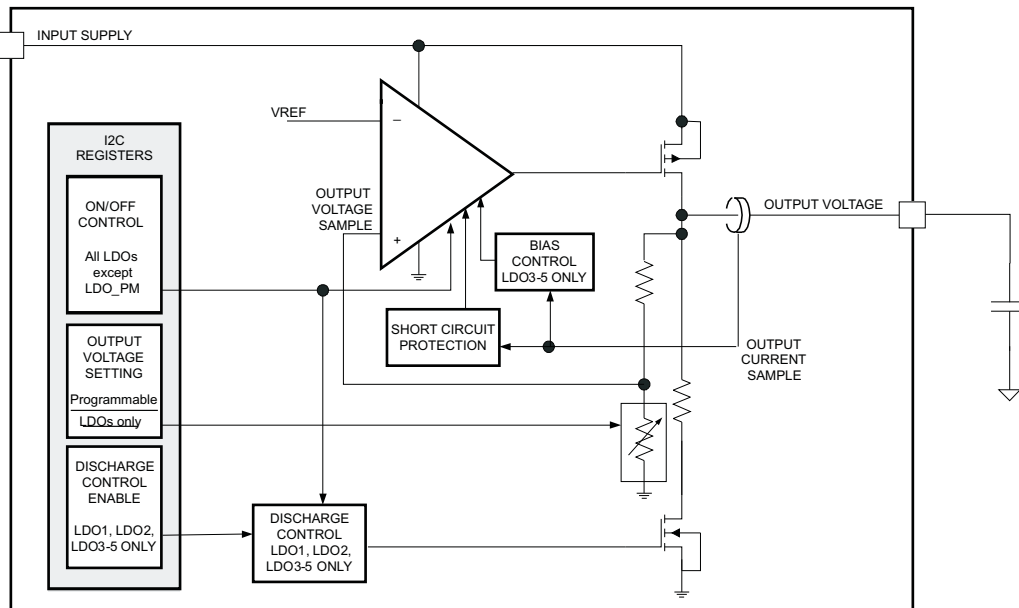


Figure 28. Simplified Block Diagram

8.3.3.2 Connecting the LDO Input Supply

Both LDO1-2 and LDO3-5 have uncommitted input power supply pins (VIN_LDO12, VIN_LDO35), which must be externally connected to the OUT pin. Optionally the LDO0-2 and LDO3-5 input supplies can be connected to the output of the available buck converters SM1 or SM2, as long as the resulting overall power-up sequence meets the system requirements.

The RTC_OUT, SIM, LDO0 and LDO_PM linear regulators are internally connected to the OUT pin.

8.3.3.3 ON/OFF Control

All the LDOs, with exception of LDO_PM LDO, have a ON and OFF control which can be set through I²C commands, facilitating host management of the distinct system power rails. The LDO_PM LDO ON and OFF control is internally hard-wired, and it is set to ON when either the AC or USB input power is detected.

8.3.3.4 Output Discharge Switch

LDO1, LDO2 AND LDO3-5 have integrated switches that discharge each output to ground when the LDO is set to OFF by an I²C command. The output discharge switch function can be disabled by using I²C register control bits. The discharge switches are enabled after the initial power-up

8.3.3.5 Special Functions

The RTC_OUT, SIM (Subscriber line interface module) and LDO_PM linear regulators are designed to support lower load currents. The SIM and RTC_LDO have low leakage in OFF mode, with the input pin voltage above or below the output pin voltage. The LDO_PM can be used for USB enumeration, or a status indication of input power connection.

8.3.3.6 Output Voltage Monitoring

Internal power-good comparators monitor the LDO outputs and detect when the output voltage is below 90% of the programmed value. This information is used by the TPS65810 to generate interrupts or to trigger distinct operating modes, depending on specific I²C register settings. See the [Interrupt Controller and System Sequencing](#) section for additional details.

8.3.3.7 Functionality Guide — Linear Regulators

Table 10. Selectable Output Voltage LDO

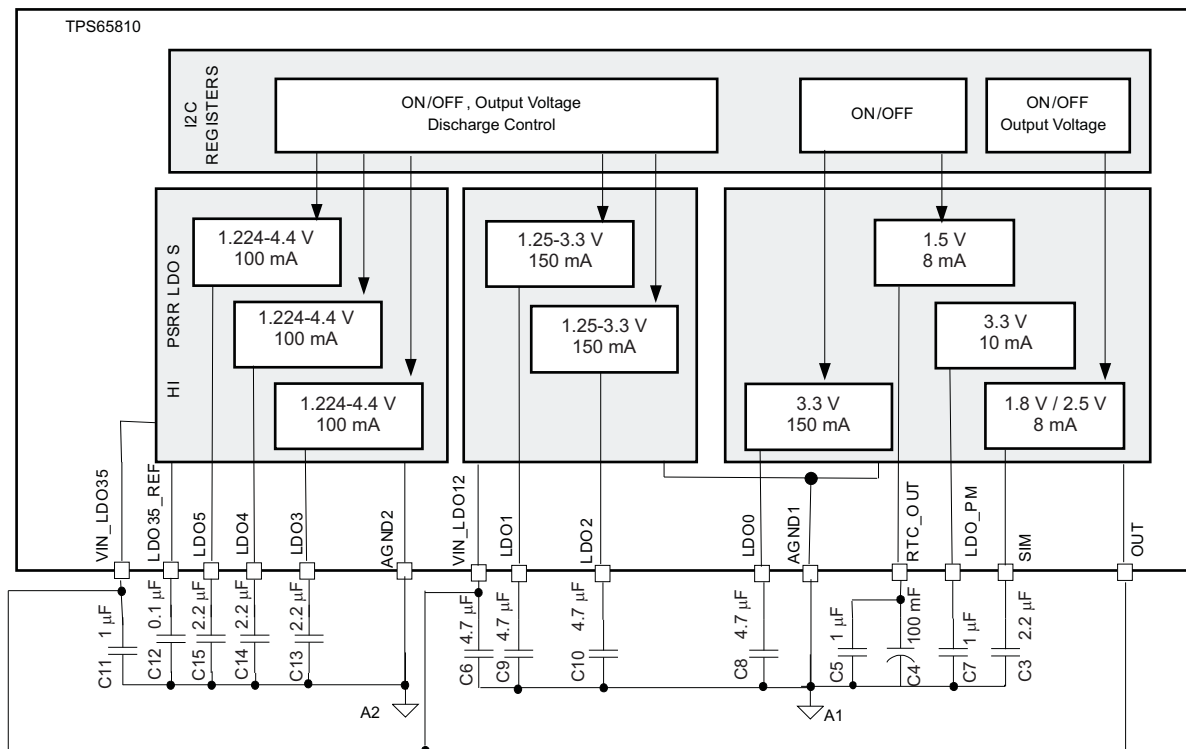
| SUPPLY | ON/OFF CONTROL | OUTPUT DISCHARGE SWITCH | OUTPUT VOLTAGE (V), SET THROUGH I ² C | | IO MAX (mA) | ACCURACY % | POWER UP DEFAULT |
|--------|-----------------------------------|---------------------------------------|--|-------------------------------|-------------|------------|------------------|
| | | | NUMBER OF STEPS | AVAILABLE VALUES (V) | | | |
| LDO1 | Yes, set through I ² C | Yes, enabled through I ² C | 8 | 1.25/1.5/1.8/2.5/2.85/3.2/3.3 | 150 | 3 | OFF, 1.25 V |
| LDO2 | Yes, set through I ² C | Yes, enabled through I ² C | 8 | 1.25/1.5/1.8/2.5/2.85/3.2/3.3 | 150 | 3 | OFF, 3.3 V |
| SIM | Yes, set through I ² C | no | 2 | 1.8 / 2.5 | 8 | 2 | ON, 2.5 V |

Table 11. Programmable Output Voltage LDO

| SUPPLY | ON/OFF CONTROL | OUTPUT DISCHARGE SWITCH | OUTPUT VOLTAGE (V), SET THROUGH I ² C | | | IO MAX (mA) | ACCURACY % | POWER UP DEFAULT |
|--------|-----------------------------------|---------------------------------------|--|-----------------|--------------|-------------|------------|------------------|
| | | | RANGE | NUMBER OF STEPS | MINIMUM STEP | | | |
| LDO3 | Yes, set through I ² C | Yes, enabled through I ² C | 1.224 to 4.46 | 128 | 25 mV | 100 | 3 | OFF, 1.505 V |
| LDO4 | Yes, set through I ² C | Yes, enabled through I ² C | 1.224 to 4.46 | 128 | 25 mV | 100 | 3 | OFF, 1.811 V |
| LDO5 | Yes, set through I ² C | Yes, enabled through I ² C | 1.224 to 4.46 | 128 | 25 mV | 100 | 3 | ON, 3.111 V |

Table 12. Fixed-Output Voltage LDOs

| SUPPLY | ON/OFF CONTROL | OUTPUT VOLTAGE (V) | IO MAX (mA) | ACCURACY % | POWER UP DEFAULT |
|---------|-------------------------------|--------------------|-------------|------------|--------------------------------|
| RTC_OUT | Yes, through I ² C | 1.5, fixed | 8 | 5 | ON |
| LDC0 | | 3.3, fixed | 150 | 3 | OFF |
| LDO_PM | NO, enabled internally | 3.3, fixed | 20 | 5 | ON if AC or USB power detected |


Figure 29. Required External Components, Recommended Values, External Connections

8.3.4 Step-Down Switched-Mode Converters: SM1 and SM2

The TPS65810 device has two high-efficiency, step-down, synchronous converters. The integration of the power stage switching MOSFETs reduces the external component count, and only the external output inductor and filter capacitor are required. The integrated power stage supports 100% duty cycle operation. Multiple operation modes are available, enabling optimization of the overall system performance under distinct load conditions.

The converters have two modes of operation: a 1.5-MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy loads, and a pulse frequency modulation (PFM) mode at light loads. The converter output voltage is programmable through I²C registers SM1_SET1 and SM2_SET1.

When the SM1/SM2 converters are disabled an integrated switch automatically discharges the converter output capacitor. The discharge switch function can be disabled by setting the control bits DISCHSM1 and DISCHSM2 to LO, in I²C registers SM1_SET2 and SM2_SET2.

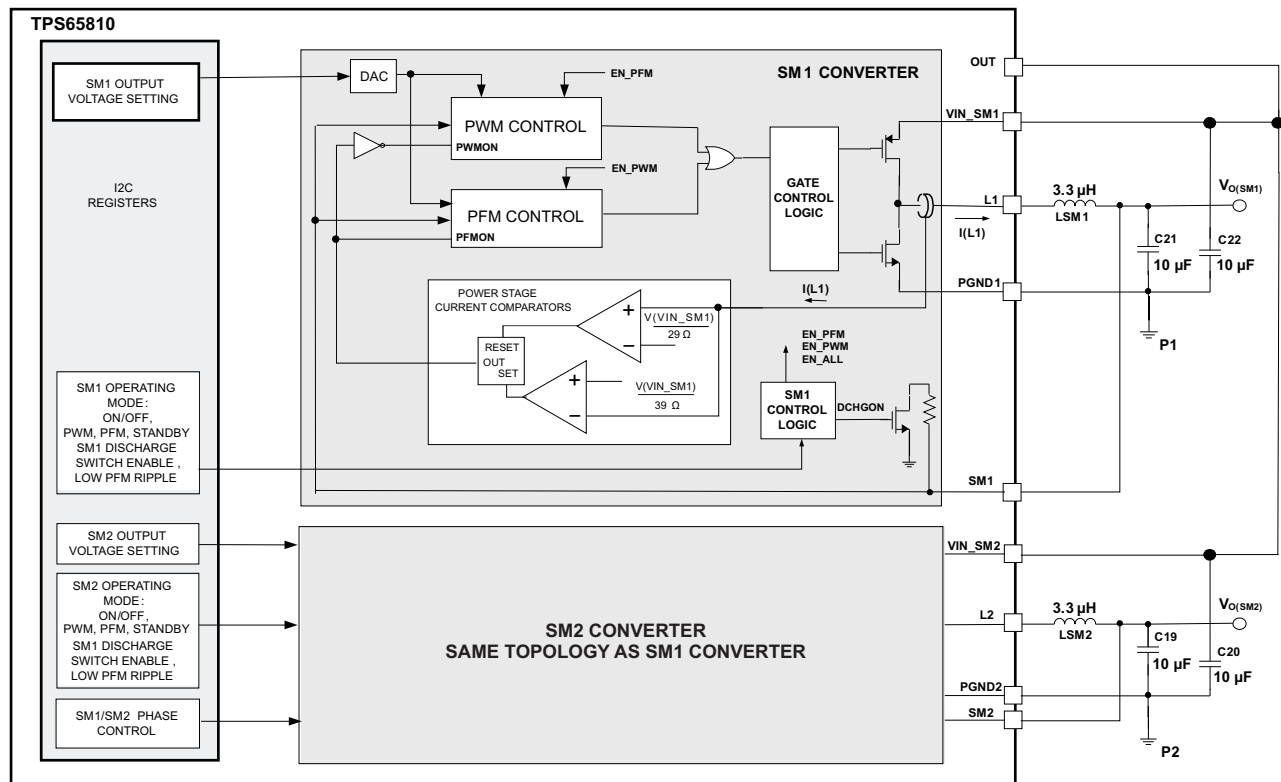


Figure 30. SM1 and SM2 Converter

The TPS65810 SM1 and SM2 buck converters can be set to operate only in PWM mode or to switch automatically between PFM and PWM modes. The average load current is monitored, and the PFM mode is set if the average load current is below the threshold $I_{PFM(ENTER)}$. When in PFM mode the load current is also monitored, and the PWM mode is set when the load current exceeds the threshold $I_{PFM(LEAVE)}$. Use Equation 10 to calculate the thresholds for automatic PFM/PWM switching for the SM1 converter. The same thresholds apply to the SM2 converter by replacing VIN_SM1 by VIN_SM2.

$$I_{PFM(LEAVE)} = \frac{V(VIN_SM3)}{29\ \Omega}, \quad I_{PFM(ENTER)} = \frac{V(VIN_SM3)}{39\ \Omega} \quad (10)$$

The automatic switching mode is enabled through the control bits PFM_SM1 and PFM_SM2 on I²C registers SM1_SET1 and SM2_SET1.

8.3.4.1 Output Voltage Slew Rate

I²C registers enable setting the output voltage slew rate, when transitioning from one programmed voltage to a new programmed voltage value. These events can be triggered by a new output voltage selection or by switching from a low-power mode (stand-by) to a normal operating mode. During a transition, the output voltage is stepped from the currently programmed voltage to the new target voltage. The slew rate from the initial voltage to the final voltage can be selected using I²C registers, SM1_SET2 and SM2_SET2, ranging from 0.24 mV/μs to 15.36 mV/μs for the SM1 converter and 0.48 to 30.72 mV/μs for the SM2 converter. If the slew rate is set to OFF the output voltage goes from the current value to the programmed value in a single step.

During the transition to stand-by mode the power-good comparators are disabled.

8.3.4.2 Soft-Start

SM1 and SM2 have an internal soft-start circuit that limits the inrush current during start-up. An initial delay (170 μs typical) from the converter enabled command to the converter effectively being operational is required, to assure that the internal circuits of the converter are properly biased. At the end of that initial delay the soft-start is initiated, and the internal compensation capacitor is charged with a low value current source. The soft-start time is typically 750 μs, with the output voltage ramping from 5% to 95% of the final target value.

8.3.4.3 Dropout Operation at 100% Duty Cycle

The TPS65810 buck converters offer a low input to output voltage difference while still maintaining operation when the duty cycle is set to 100%. In this mode of operation the P-channel switch is constantly turned on, enabling operation with a low input voltage. The dropout operation begins if Equation 11 is true:

$$V(VIN_SM1) \leq V(SM1) + I(L1)(R_{DS(on)(PSM1)} + R_L)$$

where

- I(L1) = Output current plus inductor ripple current
- R_L = DC resistance of the inductor

(11)

Equation 11 can be also used for the SM2 converter, replacing SM1 by SM2 and L1 by L2.

8.3.4.4 Output Voltage Monitoring

The output voltage of converters SM1 and SM2 is monitored by internal comparators, and an output low voltage condition is detected when the output voltage is below 90% of the programmed value. The power-good status for SM1 and SM2 is accessible through I²C, see interrupt controller section for more details.

The power-good comparators for SM1 and SM2 are disabled during the transition to stand-by mode operation. They are enabled when the transition to stand-by mode is complete.

8.3.4.5 Stand-by Mode

Using the I²C SM1 and SM2 can be set in stand-by mode. In stand-by mode the PFM operation mode is set and the output voltage is defined by I²C registers SM1_STANDBY and SM2_STANDBY, and it can be set to a value different than the normal mode output regulation voltage. The stand-by mode can also be set by the GPIO pins, if those are configured as control pins that define the SM1 and SM2 operating modes.

8.3.4.6 PWM Operation

During PWM operation the converters use a fast response voltage mode controller scheme with input voltage feed-forward, enabling the use of small ceramic input and output capacitors. At the beginning of each clock cycle the P-channel MOSFET switch is turned on, and the oscillator starts the voltage ramp. The inductor current ramps up until the ramp voltage reaches the error amplifier output voltage, when the comparator trips and the P-channel MOSFET switch is turned off. Internal adaptive break-before-make circuits turn on the integrated N-channel MOSFET switch after an internal, fixed dead-time delay, and the inductor current ramps down, until the next cycle is started. When the next cycle starts the ramp voltage is reset to its low value and the P-channel MOSFET switch is turned on again.

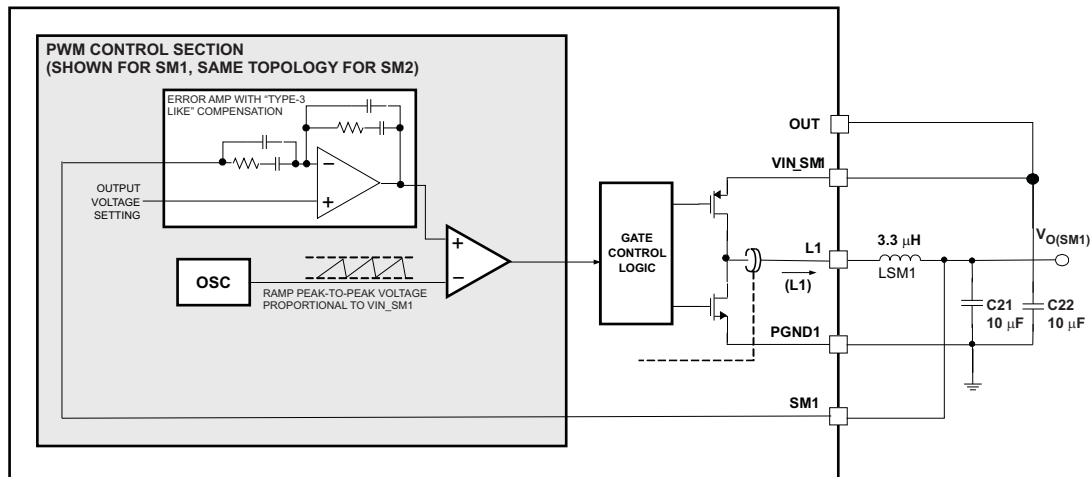


Figure 31. PWM Operation

The integrated power MOSFETs current is monitored at all times and the power MOSFET is turned off if the internal short circuit current limit is reached.

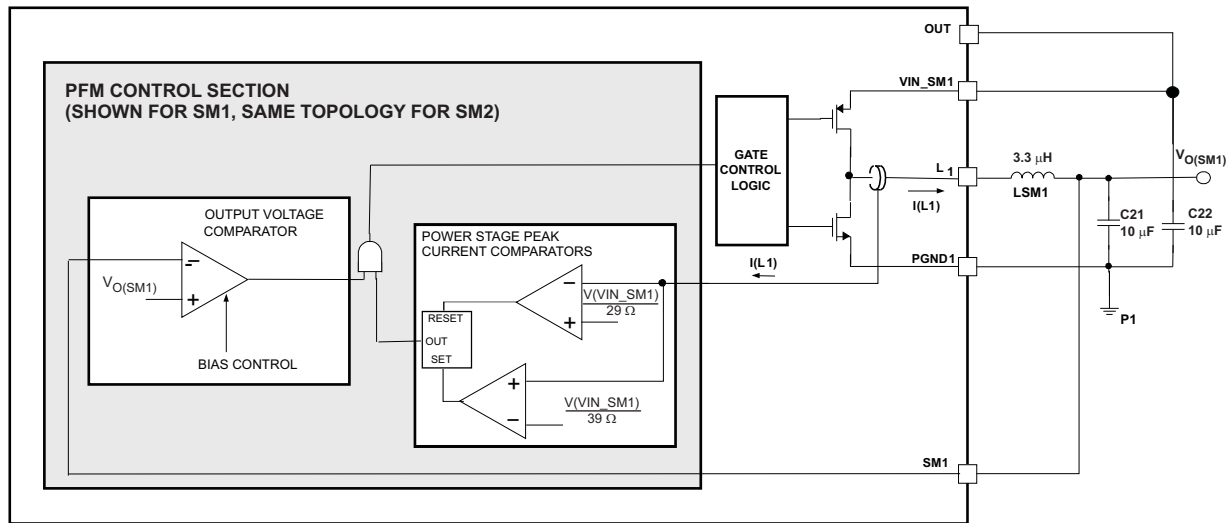
8.3.4.7 Phase Control in PWM Mode

The SM1 and SM2 converters operate synchronized to each other when both are in PWM mode, with converter SM1 as the master. I²C control register bits S1S2PHASE in register SM1_SET2 enables delaying the SM2 PWM clock with respect to SM1 PWM clock, selecting a phase shift from 0 to 270 degrees. The out-of-phase operation reduces the average current at the input node, enabling use of smaller input filter capacitors when both converters are connected to the same input supply.

8.3.4.8 PFM Mode Operation

Using the I²C interface the SM1 and SM2 converters can have the automatic power saving PFM mode enabled. When the PFM mode is set the switching frequency is reduced and the internal bias currents are decreased, optimizing the converter efficiency under light load conditions.

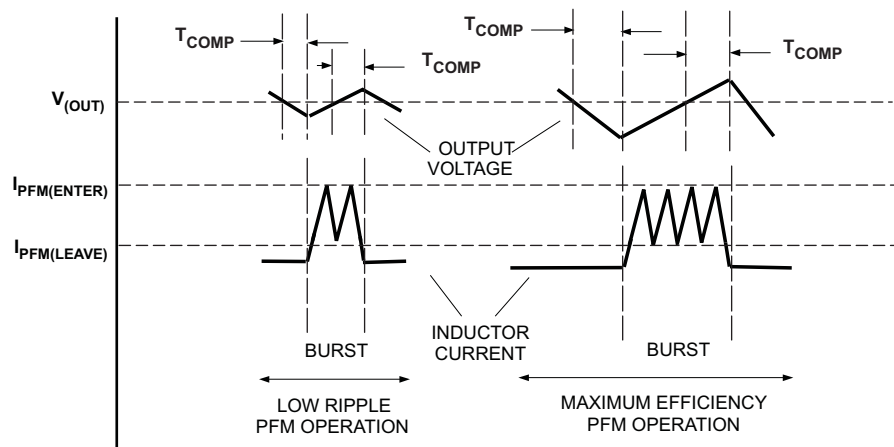
In PFM mode, the output voltage is monitored by a voltage comparator, which regulates the output voltage to the programmed value, $V_{O(SM1)}$. If the output voltage is below $V_{O(SM1)}$, the PFM control circuit turns on the power stage, applying a burst of pulses to increase the output voltage. When the output voltage exceeds the target regulation voltage, $V_{O(SM1)}$, the power stage is disabled, and the output voltage drops until it is below the regulation voltage target, when the power stage is enabled again.


Figure 32. PFM Mode Operation

During burst operation two current comparators control the power stage integrated MOSFETs. These comparators monitor the instantaneous inductor current and compare it to the internal thresholds $I_{PFM(ENTER)}$ and $I_{PFM(LEAVE)}$, turning the P-channel switch on if the inductor current is less than $I_{PFM(LEAVE)}$ and turning it off if the inductor current exceeds $I_{PFM(ENTER)}$. The N-channel switch is turned on when the P-channel MOSFET is off.

The PFM output voltage comparator quiescent current may be reduced using the I²C register bits PFM_RPL1 and PFM_RPL2 in registers SM1_SET and SM2_SET. The voltage comparator quiescent current is reduced if PFM_RPL1 and PFM_RPL2 bits are set to LO, and the comparator response time (t_{COMP} , see Figure 33) increases. A reduction in quiescent current increases the converter efficiency at light loads, at the expense of a larger output voltage ripple when in PFM mode.

The ripple is minimized if PFM_RPL1 and PFM_RPL2 bits are set to HI, at the expense of reduced efficiency under light loads. The operation under low and high ripple settings is described in Figure 33.


Figure 33. PFM Mode Operation Waveforms

When a burst of pulses is generated, the PFM current comparators control the power-stage MOSFETs to limit the inductor current to a value between the thresholds $I_{PFM(LEAVE)}$ and $I_{PFM(ENTER)}$. The number of pulses in a burst cycle is proportional to the load current, and the average current is always below $I_{PFM(LEAVE)}$ once PFM operation is set. The typical burst operation in PFM mode is shown in Figure 34.

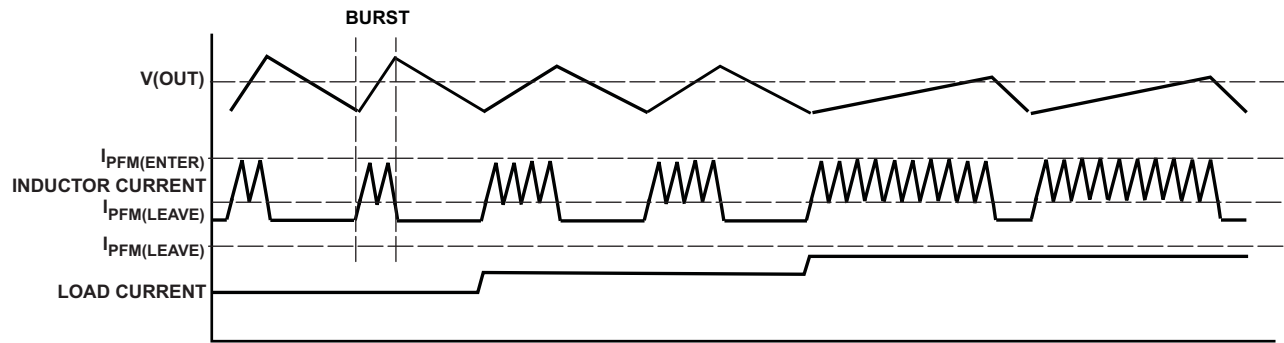


Figure 34. Typical Burst Operation in PFM Mode

The PFM operation is disabled and PWM operation set if one of the following events occur during PFM operation:

- The total burst operation time exceeds 10 μ s (typical).
- The output voltage falls below 2% of the target regulation voltage.

The PFM mode can be disabled through the serial interface to force the individual converters to stay in fixed frequency PWM mode.

8.3.4.9 Functionality Guide — Switched-Mode Step-Down Converters

Table 13. Buck Converters, I²C Programmable Output Voltage

| SUPPLY | PFM MODE | STANDBY MODE | OUTPUT VOLTAGE (V), SET THROUGH I ² C, SEPARATE SETTINGS FOR NORMAL OR STANDBY MODE | | | | I _O MAX (mA) | PWM FREQUENCY AND PHASE | SLEW RATE, mV/ μ s, SET THROUGH I ² C | | | POWER UP DEFAULT |
|--------|--|--|--|-----------------|----------|----------|-------------------------|---|--|--------------|----------|--|
| | | | RANGE | NUMBER OF STEPS | MIN STEP | ACC. (%) | | | RANGE | NO. OF STEPS | MIN STEP | |
| SM1 | PFM/PWM with automatic mode selection or PWM only. | Standby mode with distinct voltage available. | 0.6 to 1.8 | 32 | 40 mV | 3 | 600 | 1.5 MHz, 0° | 0, 0.24 to 15.36 | 8 | 0.24 | OFF, skip mode off, PWM only, 1.24 V (on/sby), 15.36 mV/ μ s |
| SM2 | Mode of operation set through I ² C | Standby mode set through I ² C or with GPIO pin | 1 to 3.4 | 32 | 80 mV | 3 | 600 | 1.5 MHz, 0/90/180 270°, with respect to SM1, set through I ² C | 0, 0.48 to 30.72 | 8 | 0.48 | OFF, skip mode on, PWM/PFM, 3.32 V (on/sby), 180°, 30.72 mV/ μ s |

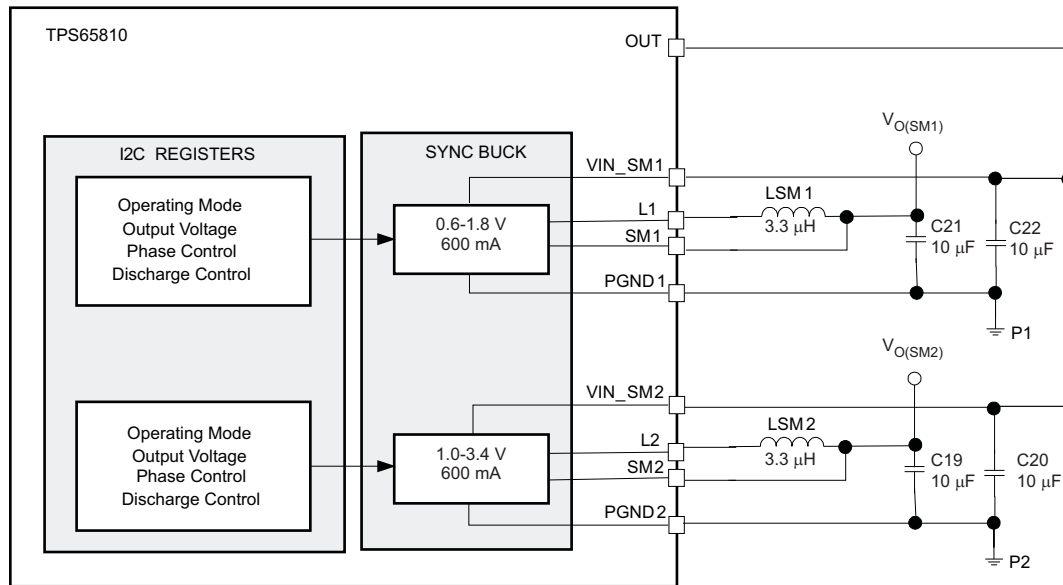


Figure 35. Required External Components, Recommended Values, External Connections

8.3.5 Analog-to-Digital Converter

8.3.5.1 Overview

The TPS65810 has a 10-bit integrated successive approximation A/D, capable of running A/D conversions on eight distinct channels in a variety of modes. Two of the eight channels are connected to uncommitted pins ANLG1 and ANLG2, and can be used to convert external voltages. The other six channels monitor system parameters which are critical to the overall system monitoring. The channel selection is set through I²C.

A dedicated set of I²C registers enables configuration of the ADC to perform a conversion cycle with either a single conversion or a multiple conversions. The ALU generates a data set containing maximum value detection, minimum value detection and average value calculation for each conversion cycle. Each cycle can be performed a single time or multiple times.

8.3.5.2 Input Channels

The channels listed in [Table 14](#) are available for selection through the I²C register ADC_SET bits CHSEL_SET bits.

Table 14. ADC Input Channel Overview

| CHANNEL | CONNECTION | PARAMETER SAMPLED | VOLTAGE RANGE UNDER NORMAL OPERATING CONDITIONS | SPECIAL FEATURES | FULL SCALE READING (INTERNAL REFERENCE SELECTED) | LSB VALUE |
|---------|-------------------------------|---|---|---|--|--------------------------------|
| CH1 | ANLG1 pin | User defined | User defined | Internal pullup current source programmable through I ² C: 0/ 10/50/60 μ A | 2.535 V | Full scale reading \div 1023 |
| CH2 | ANLG2 pin | | | | 2.535 V | |
| CH3 | ISET1 pin | Voltage proportional to charge current | 0 V (charger off) to 2.525 V (fast charge) | — | 2.535 V | |
| CH4 | TS pin | Voltage proportional to pack temperature | 0 V (short) to 4.7V (no thermistor) | No internal pullup current, use external pullup resistor to bias pack thermistor | 2.535 V | |
| CH5 | Internal junction temperature | Voltage proportional to IC junction temperature | 1.85 V at T _J = 25°C, –6.5 mV/°C slope typ | — | 2.535 V | |
| CH6 | RTC_OUT pin | Internal LDO output voltage | 0 V to 3.3 V | — | 4.7 V | |
| CH7 | OUT pin | System power bus voltage | 0 V to 4.4 V | — | 4.7 V | |
| CH8 | BAT pin | Battery pack positive terminal voltage | 0 V to 4.4 V | — | 4.7 V | |

8.3.5.3 Functional Overview

The TPS65810 ADC can be subdivided in four sections which are defined as follows:

Input Selection The input selection section has two major blocks, the input bias control and an 8 channel MUX. The input bias control provides the bias currents that are applied to pins ANLG1 and ANLG2. The bias currents for pins ANLG1 and ANLG2 are set on I²C register ADC_WAIT.

The ANLG1 pin current source is automatically enabled when the input power is detected, providing the required setup to measure a battery ID resistor (ANLG1 pin). ANLG1 and ANLG2 can be used to measure external resistive loads or analog voltages. The bias current sources are always connected to the OUT pin internally.

The internal MUX connects one of the monitored analog inputs to the ADC engine, following the selection defined on register ADC_SET.

ADC Engine The ADC engine uses an internal or external voltage reference, as defined by the ADC_REF bit on the ADC_SET control register. If the internal reference is selected ADC_REF is connected to an internal LDO that regulates the ADC_REF pin voltage to generate the ADC supply and internal voltage reference. The internal LDO maximum output current is 6 mA typical, and a conversion must be started only after the external capacitor is fully charged.

If an external reference is used it must be connected to the ADC_REF pin. When an external reference is selected the internal LDO connected to ADC_REF is disabled. Care must be taken when selecting an external reference as the ADC reference voltage, as it affects the ADC LSB absolute value.

Trigger Control and Synchronization The ADC engine starts a conversion of the selected input when the trigger control circuit sends a start command. The trigger control circuit starts the ADC conversion and transfers the ADC output data to the arithmetic logic unit (ALU) at the end of the conversion. It also synchronizes the data transfer from the ALU to the I²C ADC_READING register at the end of a conversion cycle, and generates the ADC status information sent to the ADC registers.

An ADC engine conversion is triggered by the TPS65810 trigger control circuit using either an internal trigger or an external trigger. The internal trigger is automatically generated by the TPS65810 at the end of each ADC engine conversion, following the timing parameters set on I²C registers ADC_SET, ADC_DELAY and ADC_WAIT.

The GPIO3 pin can be used as an external trigger if the bit ADC_TRG_GPIO3 is set HI, in the I²C register ADC_DELAY. In the external trigger mode a new conversion is started after the GPIO3 pin has an edge transition, following the timing parameters set on I²C registers ADC_SET, ADC_DELAY and ADC_WAIT.

Arithmetic Logic Unit (ALU) The ALU performs mathematical operations on the ADC output data as defined by the I²C ADC_READING registers. It executes average calculations or minimum /maximum detection. The result of the calculations is stored in a 11 bit accumulator register (1 bit allocated for carry-over). The accumulator value is transferred to the I²C data register at the end of a conversion cycle.

Figure 36 shows a simplified block diagram for the ADC.

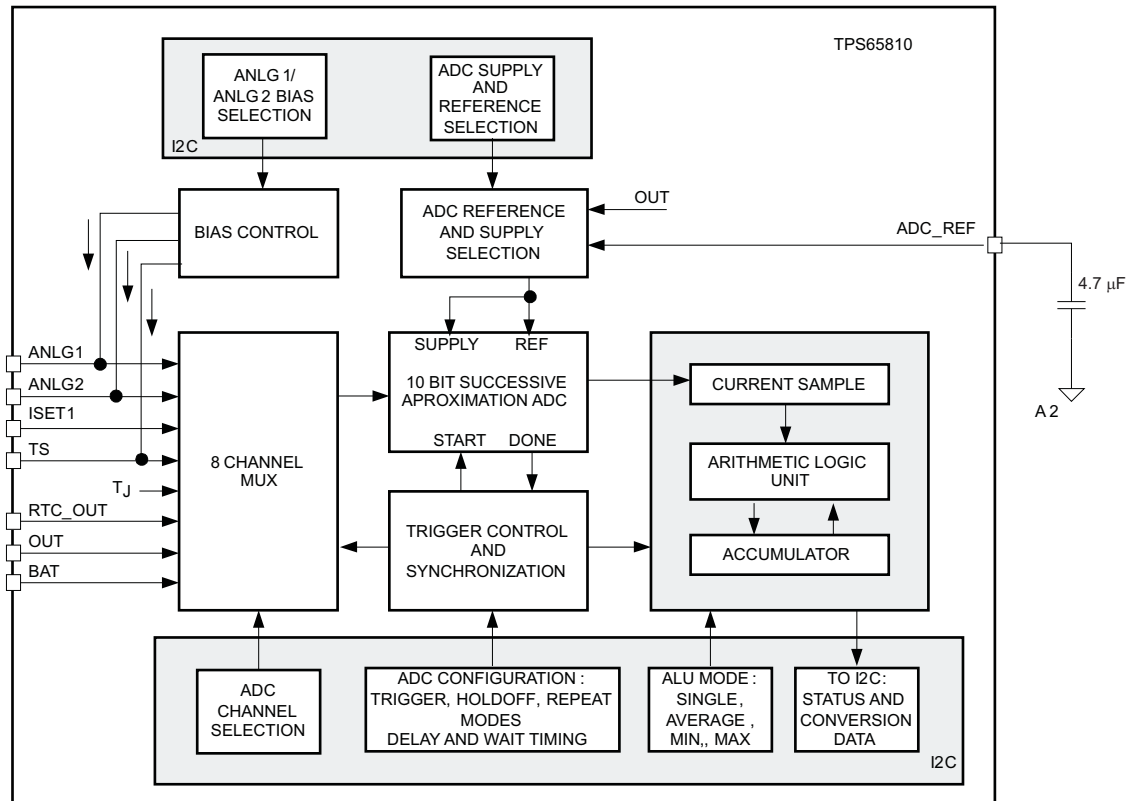


Figure 36. ADC Simplified Block Diagram

8.3.5.3.1 ADC Conversion Cycle

A conversion cycle includes all the steps required to successfully sample the selected input signal and transfer the converted data to the I²C, generating an interrupt request to the host (pin: HI→LO). The number of individual conversions (samples) in a conversion cycle is defined by the I²C ADC_SET register bits READ_MODE settings, and can range from a single sample to 256 samples. The conversion cycle settings for the ALU is defined by register ADC_READING and it can be set to average, maximum value detection, minimum value detection or no processing (ADC engine output loaded in the accumulator directly).

The conversion cycle begins with the first sampling and ends when the following occurs:

- The required ALU operations are performed on the final sample, and
- The ALU accumulator data is transferred to the I²C ADC_READING register, and
- The register bit ADC_STATUS in the ADC_READING register is set to LO.

A conversion cycle is always started by the external host when the ADC_EN bit in the ADC_SET register is toggled from LO to HI by a I²C write operation. Resetting the ADC_EN bit to LO before the current conversion cycle ends (INT: LO → HI, ADC_STATUS bit set to LO) is not recommended, as the ADC keeps its current configuration until the current conversion cycle ends.

At the end of a conversion cycle the output data is stored at registers in the ALU block. The ADC_STATUS bit is set to LO (DONE) and an interrupt is generated (INT pin: HI→LO) if the ADC_STATUS bit is unmasked, at the interrupt masking registers INT_MASK. It must be noted that the minimum, maximum and average values are ALWAYS calculated by the ALU for each conversion cycle.

The value loaded in the I²C registers ADC_READING_HI and ADC_READING_LO at the end of a conversion cycle is defined by control bits ADC_READ0 and ADC_READ1 in register ADC_READING_HI. The average, minimum, maximum, and last-sample values for a conversion cycle can be read if the external host executes an I²C write operation, changing the values of bits ADC_READ0 and ADC_READ1, followed by an I²C read operation on registers ADC_READING_HI and ADC_READING_LO. The minimum, maximum, average, and last values have the same value if a conversion cycle with only one sample is executed.

The ADC_READ0 and ADC_READ1 bits *can not be modified* during the execution of a conversion cycle. A new conversion cycle must be started *only after* the current conversion cycle is completed, by toggling the ADC_EN bit from HI to LO and HI again.

8.3.5.3.2 External Trigger Operation

The trigger control circuit can be programmed to use an external signal to start a conversion. The TPS65810 GPIO3 input is configurable as an ADC trigger, with ADC conversion starting on either a rising edge or falling edge. When using an external trigger the trigger delay, trigger wait time delay and trigger hold-off mode can be programmed using I²C registers.

The procedure to start an externally-triggered conversion cycle has the following steps:

1. Verify that the current conversion cycle has ended (ADC_STATUS = LO, I²C register ADC_READING_HI)
2. Set ADC_EN = LO
3. Configure ADC sampling mode, ALU mode, trigger parameters, and so forth
4. Set ADC_EN = HI

After step 4 the ADC is armed, waiting for an external trigger detection to start a conversion cycle. Similarly to the non-triggered mode, the ADC configuration *must not be modified until the current conversion cycle ends*. Note that in the external trigger mode the current cycle does not end if the converter is armed and an external trigger is not detected.

8.3.5.3.3 Detecting an External Trigger Event

An external trigger event is detected when the GPIO3 input has an edge that matches the edge detection programmed in the EDGE bit, at the I²C register ADC_DELAY. The internal ADC trigger can be delayed with respect to the external trigger signal edge. The delay time value is set by the ADC_DELAY register bits DELAY_n, and can range from 0 μs (no delay) to 750 μs. A conversion is started only if the external trigger remains at its active level when the delay time expires, as shown in [Figure 37](#). In a positive-edge detection the active trigger level is HI; in a negative-edge detection the active trigger level is LO.

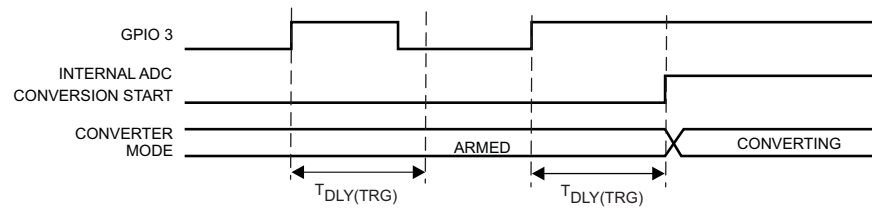


Figure 37. ADC Conversion Triggered by GPIO3 Positive Edge Triggered Active Level Hi

8.3.5.3.4 Executing Multiple-Sample Cycles With an External Trigger

When executing conversion cycles that require multiple samples it may be desirable to synchronize the input signal conversion using either an external trigger that has a periodic repetition rate or an external asynchronous trigger that indicates when the external input signal being converted is valid. The TPS65810 has additional operating modes and timing parameters that can be programmed using the I²C to configure multiple sample conversion cycles.

In multiple sample cycles the host can select the wait time between samples using the bits WAITn in the ADC_WAIT register to set the wait time between samples. The wait time is measured between the end of a conversion and the start of a new conversion.

With the default power-up settings (HOLDOFF=LO, ADC_DELAY register), the TPS65810 executes a multiple-sample conversion cycle if the first sample is taken when the trigger is at its active level. Subsequent samples are converted at the end of the wait time, even if the trigger returns to the non-active level. The external trigger level edge is ignored until the current conversion cycle ends.

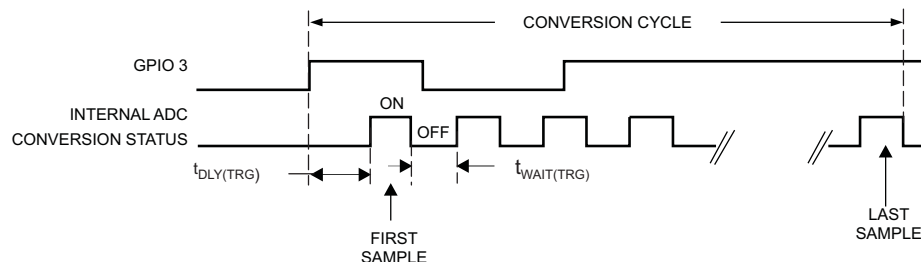


Figure 38. ADC Conversion Triggered by GPIO3 Positive Edge Triggered Active Level Hi, Holdoff = LC

If the sample conversion needs to be synchronized with an external trigger, during multiple sample conversion cycles, the control bit HOLDOFF must be set to HI. When the holdoff mode is active, the internal trigger starts a sample conversion only if the external trigger was detected and is at its active level at the end of the wait time, as shown in [Figure 39](#).

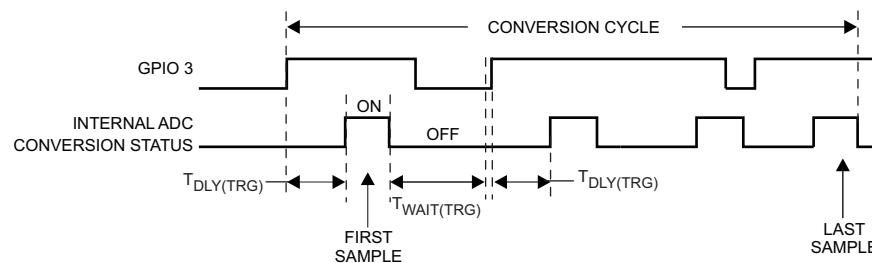


Figure 39. ADC Conversion Triggered by GPIO3 Positive Edge Triggered Active Level HI, Holdoff = HI, Four Sample Cycles

When the multiple sample cycles are executed the host must configure the maximum and minimum limits for the ADC output using registers DLOLIM1, DLOLIM2, DHILIM1 and DHILIM2. A conversion cycle ends if any individual conversion result exceeds the maximum limit value or is below the minimum limit value. When an out of limit conversion is detected an interrupt is sent to the host, and the ADC_STATUS bit on register ADC_READING_HI is set to DONE.

8.3.5.3.5 Continuous Conversion Operation (Repeat Mode)

The TPS65810 ADC can be set to operate in a continuous conversion mode, with back-to-back conversion cycles executed. The REPEAT mode is targeted at applications where an input is continuously monitored for a period of time, and the host must be informed if the monitored input is out of the range set by I²C registers DLOLIM1, DLOLIM2, DHILIM1 and DHILIM2. In REPEAT mode each conversion is started when the ADC trigger (internal or external) is detected, and a new conversion cycle is started when the current conversion cycle ends. All the trigger and sampling modes available for normal conversion cycles are available in repeat mode. Executing I²C read operations to get the ADC readings for average, minimum, maximum and last sample values is possible in REPEAT mode. However, TI does not recommend this operation, as the REPEAT mode does not generate a DONE status flag making it difficult to synchronize the ADC data reading to the end of a conversion cycle.

TI recommends using these steps for the REPEAT mode:

1. Configure the ADC conversion cycle: trigger mode, sample mode, select input signal, or others.
2. Configure the HI and LO limits for the ADC readings
3. Set the ADC_DELAY register bit REPEAT to HI
4. Toggle ADC_DELAY register bit ADC_EN bit from LO to HI
5. Monitor the INT pin. An interrupt triggered by ADC_STATUS = LO indicates that the selected input signal is out of range

To exit the continuous mode the host must follow the steps below, if external trigger mode was set:

1. Exit external trigger mode
2. Set REPEAT bit to LO, effectively terminating the repeat mode. This generates an additional conversion; at the end of this conversion the ADC is ready for a new configuration.
3. Set ADC_EN to LO after on-going conversion ends.

To exit the continuous mode the host must follow the steps below, if internal trigger mode was set:

1. Set REPEAT bit to LO, effectively terminating the repeat mode.
2. Set ADC_EN to LO, after on-going conversion ends

8.3.5.3.6 ADC Input Signal Range Setting

The registers DHILIMn and DLOLIMn can be used by the host to set maximum and minimum limits for the DAC engine output. At the end of each conversion the ADC output is checked for the maximum and minimum limits, and a status flag is set if the converted data exceeds the high limit or is under the low limit. In multiple sample operation the converted data range is checked when all programmed samples have been converted.

The host can mask or unmask interrupts caused by the ADC range status bits using the INT_MASKn registers.

8.3.5.3.7 ADC State Machine

Figure 40 shows the ADC state machine with all the trigger and operation modes.

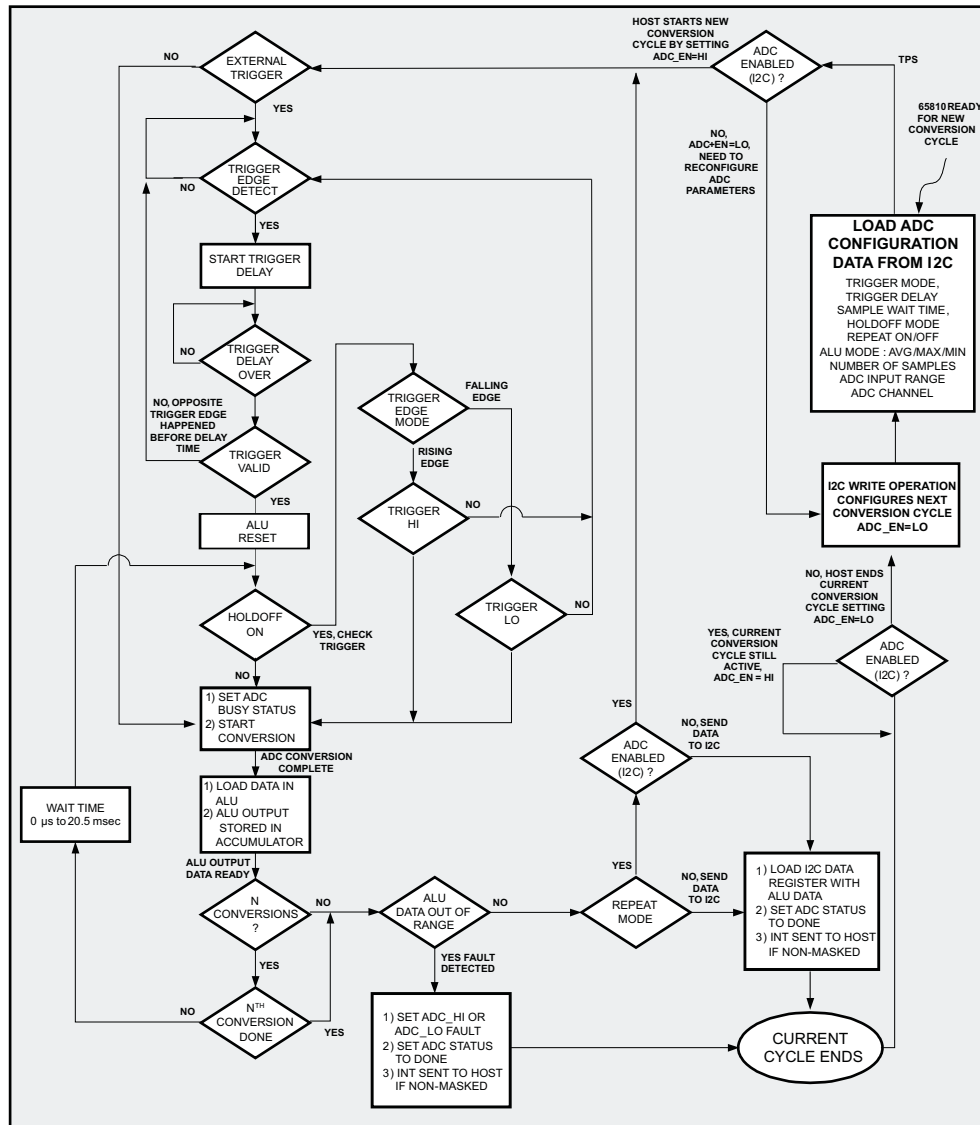


Figure 40. Trigger and Operation Modes for the ADC State Machine

8.3.5.4 Battery Detection Circuit

The ANLG1 pin has an internal current source connected between OUT and ANLG1, which is automatically turned on when the OUT pin voltage exceeds the minimum system voltage set by the SYS_IN pin external resistive divider. The current levels for ANLG1 pin can be programmed through I²C register ADC_WAIT, bits BATID_n. An integrated switch discharges the BAT pin to AGND1 when $V(\text{ANLG1}) > V(\text{OUT}) - V_{(\text{NOBATID})}$, enabling implementation of a battery removal function if an external pack resistor ID is connected between ANLG1 and ground.

The ANLG1 pin may be used to monitor other parameters than a pack ID resistor. When ANLG1 pin is used as a generic ADC analog input $V(\text{ANLG1})$ must never exceed $V(\text{OUT}) - V_{(\text{NOBATID})}$, to avoid undesired battery discharge caused by activation of the battery pin discharge circuit.

8.3.5.5 Functionality Guide – Analog to Digital Converter

Table 15. 10-Bit Successive Approximation ADC

| ADC INPUT CHANNELS | | TRIGGER MODE | CONVERSION COUNT | CONVERTER MODE | TRIGGER DELAY | | WAIT TIME, MULTIPLE CONVERSIONS | POWER UP DEFAULT |
|--|-------------------------------------|--|-------------------------------------|---|-------------------------------------|-------------------------------------|--|------------------|
| INTERNAL | EXTERNAL | | | | RANGE | MIN STEP | | |
| Charge Current, Thermistor temperature, IC junction temperature, RTC_OUT voltage, OUT voltage, Battery voltage | ANLG1 and ANLG2 voltages | GPIOB, I ² C driven, Repeat | 1, 4, 8, 16, 32, 64, 128, 256 | Single, Average, Find max value, Find min value | 0 to 750 μ s, 16 steps | 50 μ s | μ s: 20, 40, 60, 80, 160, 240, 320, 640 ms: 1.28, 1.92, 2.56, 5.12, 10.24, 15.36, 20.48 | ADC off |
| Fixed internally | Selectable through I ² C | Selectable through I ² C | Selectable through I ² C | Selectable through I ² C | Selectable through I ² C | Selectable through I ² C | Selectable through I ² C | |

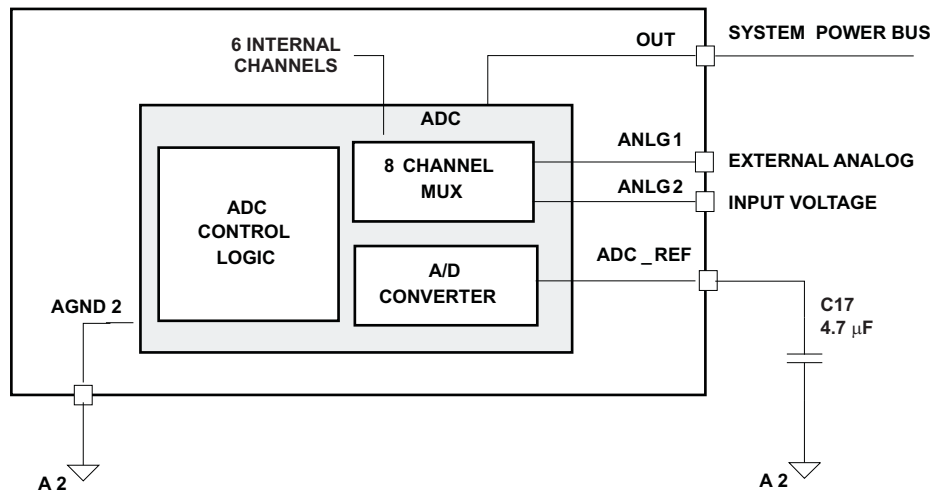


Figure 41. Required External Components, Recommended Values, External Connections

8.3.6 LED and Peripheral Drivers

8.3.6.1 White LED Constant Current Driver

The TPS65810 has an integrated boost converter (SM3) that is optimized to drive white LEDs connected in a series configuration. Up to six series white LEDs can be driven, with programmable current and duty cycle adjustable through a dedicated I²C register.

The SM3 boost converter (SM3) has a 30-V, 500-mA, low-side integrated power stage switch that drives the external inductor. Another integrated 30-V, 25-mA switch (LED switch) is used to modulate the brightness of the external white LEDs. [Figure 42](#) shows a simplified block diagram.

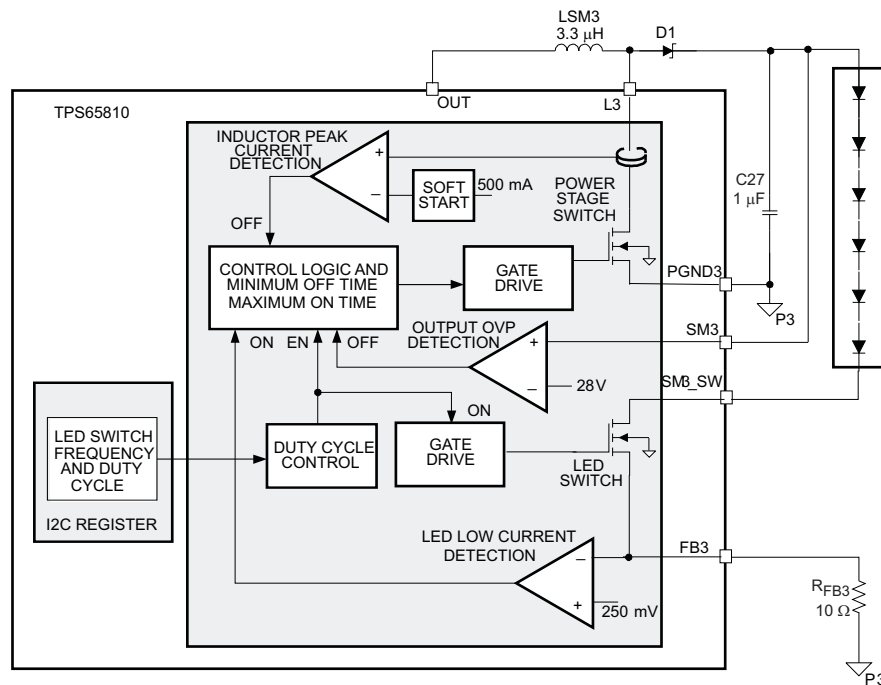


Figure 42. Simplified Block Diagram

The SM3 converter operates like a standard boost converter. The LED current is defined by the value of the external resistor R_{FB3} , connected from pin FB3 to AGND1. The integrated power stage switch control monitors the LED switch current (FB3) and the integrated power stage switch current, implementing a topology that effectively regulates the LED current independently of the input voltage and number of LEDs connected. The high voltage rating of the integrated switches enables driving up to six white LEDs, connected in a series configuration.

The internal LED switch, in series with the external LEDs, disconnects the LEDs from ground during shutdown. In addition, the LED switch is driven by a PWM signal that sets the duty cycle, enabling adjustment to the average LED current by modifying the settings of the I²C register SM3_SET. With this control method, the LED brightness depends on the LED-switch duty cycle only, and is independent of the PWM control signal.

The duty cycle control used in the SM3 converter LED switch is implemented by generating a burst of high frequency pulses, with a pattern that is repeated periodically. For a duty cycle of 50%, all of the high frequency pulses have a 50% duty cycle. The duty cycle control sets individual pulses to 100% duty cycle when increasing the LED_PWM output duty cycle; for decreasing LED_PWM output duty cycles, individual pulses are set to 0% duty cycle. An example of distinct duty cycles is shown in Figure 43, the sum of the individual pulses ON and OFF-time over the repetition period are equivalent to the duty cycle obtained with traditional single-pulse duty cycle circuits.

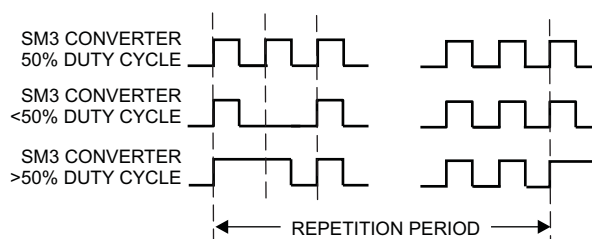


Figure 43. Example of Distinct Duty Cycles

The repetition period can be set using the register `SOFT_RESET` control bit `SM3_LF_OSC` to either 183 Hz (HI) or 122 Hz (LO). Each repetition period has a total of 256 pulses, enabling a resolution of 0.4% when programming the duty cycle.

8.3.6.1.1 SM3 Control Logic Overview

The SM3 boost converter operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and enables the use of small external components, as the switching frequency can reach up to 1 MHz depending on the load conditions. The LED current ripple is defined by the external inductor size.

The converter monitors the sense voltage at pin FB3, and turns on the integrated power stage switch when $V_{(FB3)}$ is below the 250-mV (typical) internal reference voltage and the LED Switch is ON, starting a new cycle. The integrated power switch turns off when the inductor current reaches the internal 500-mA (typical) peak current limit, or if the switch is on for a period longer than the maximum on-time of 6 μ s (typical). The integrated power switch also turns off when the LED switch is set to OFF. As the integrated power switch is turned off, the external Schottky diode is forward biased, delivering the stored inductor energy to the output. The main switch remains off until the FB3 pin voltage is below the internal 250-mV reference voltage and the LED switch is turned ON, when it is turned on again.

This PFM peak current control scheme sets the converter in discontinuous conduction mode (DCM), and the switching frequency depends on the inductor, input/output voltage and LED current. Lower LED currents reduce the switching frequency, with high efficiency over the entire LED current range. This regulation scheme is inherently stable, allowing a wide range for the selection of the inductor and output capacitor.

8.3.6.1.2 Peak Current Control (Boost Converter)

The SM3 integrated power stage switch is turned on until the inductor current reaches the DC current limit $I_{MAX(L3)}$ (500 mA, typical). Because of internal delays, typically around 100 ns, the actual current exceeds the DC current limit threshold by a small amount. Use [Equation 12](#) to calculate the typical peak current limit.

$$I_{P(typ)} = I_{MAX(L3)} + \frac{V(OUT)}{L} \times 100 \text{ ns}, \text{ or: } I_{P(typ)} = 500 \text{ mA} + \frac{V(OUT)}{L} \times 100 \text{ ns} \quad (12)$$

The current overshoot is directly proportional to the input voltage, and inversely proportional to the inductor value.

8.3.6.1.3 Soft-Start

All inductive step-up converters exhibit high in-rush current during start-up. If no special precautions are taken, voltage drops can be observed at the input supply rail during start-up, with unpredictable results in the overall system operation.

The SM3 boost converter limits the inrush current during start-up by increasing the current limit in the following three steps:

1. 125 mA (typical),
2. 250 mA (typical) and
3. 500 mA (typical)

The two initial steps (125 mA and 250 mA) are active for 256 power stage switching cycles.

8.3.6.1.4 Enabling the SM3 Converter

The `SM3_SET` I²C register controls the SM3 LED-switch duty cycle. If the register is set to all zeros SM3 is set to OFF mode. When the host writes a value other than 00 in `SM3_SET` the SM3 converter is enabled, entering the soft-start phase and then normal operation. The SM3 converter can operate with duty cycles varying from 0.4% to 99.6%, with LED switch frequencies of 122 Hz or 180 Hz. The LED switch operating frequency is set by bit `SM3_LF`, in the `SOFT_RESET` register.

8.3.6.1.5 Overvoltage Protection

The output voltage of the boost converter is sensed at pin SM3, and the integrated power stage switch is turned OFF when $V(SM3)$ exceeds the internal overvoltage threshold V_{OVP3} . The converter returns to normal operation when $V(SM3) < V_{OVP3} - V_{HYS(OVP3)}$.

8.3.6.1.6 Under Voltage Lockout Operation

When the TPS65810 device enters the UVLO mode, the SM3 converter is set to OFF mode with the power stage MOSFET switch and the LED switch open (off).

8.3.6.1.7 Thermal Shutdown Operation

When the TPS65810 device enters the thermal shutdown mode, the SM3 converter is set to OFF mode with the power stage MOSFET switch and the LED switch open (off).

8.3.6.2 PWM Drivers

8.3.6.2.1 PWM Pin Driver

The TPS65810 device offers one low-frequency, open-drain PWM driver, capable of driving up to 150 mA. The PWM frequency and duty cycle are defined by the PWM I²C register settings. The PWM parameters are set in I²C register PWM. Available frequency values range from 500 Hz to 15 kHz, with 8 frequency values and 16 duty cycle options (6.25% each).

8.3.6.2.2 LED_PWM Pin Driver

The TPS65810 has another PWM driver output (pin LED_PWM), which is optimized to drive a backlight LED. The LED_PWM driver controls the external LED current intensity using a pulse-width control method, with duty cycle being set by the I²C register LED_PWM.

The pulse width method implemented generates a burst of high frequency pulses, with a pattern that is repeated periodically. For a duty cycle of 50%, all of the high -frequency pulses have a 50% duty cycle. The duty cycle control sets individual pulses to 100% duty cycle when increasing the LED_PWM output duty cycle; for decreasing LED_PWM output duty cycles individual pulses are set to 0% duty cycle. An example of distinct duty cycles is shown in Figure 44; the sum of the individual pulses on/off time over the repetition period is equivalent to the duty cycle obtained with traditional single-pulse duty cycle circuits.

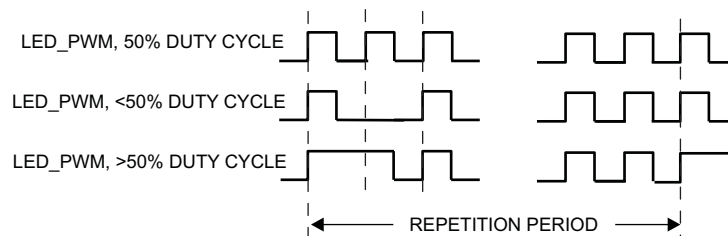


Figure 44. Example of Distinct Duty Cycles

The repetition period can be set using the register SOFT_RESET control bit SM3_LF_OSC to either 180 Hz (HI) or 122 Hz (LO). Each repetition period has a total of 256 pulses, enabling a resolution of 0.4% when programming the duty cycle. The LED_SET register enables control of the duty cycle through I²C, with duty cycle ranging from 0.4% to 99.6%. Setting the LED_SET register to all zeros forces the LED_PWM pin to 0% duty cycle (OFF).

8.3.6.2.3 RGB Driver

The TPS65810 has a dedicated driver for an RGB external LED. Three outputs are available (pins RED, GREEN, BLUE), with common settings for operation mode (flash on/off, flash period, flash on time), LED current and phase delay between outputs. The TPS65810 RGB driver continually flashes the external LEDs connected to the RED, GREEN and BLUE pins using the flash operation parameters defined in register RGB_FLASH.

The currents for the external LEDs can be programmed through I²C, and external resistors are not required to limit the LED current. However, they can be added to set the LED current if the available I²C values are not compatible with the current application, as shown in Figure 45.

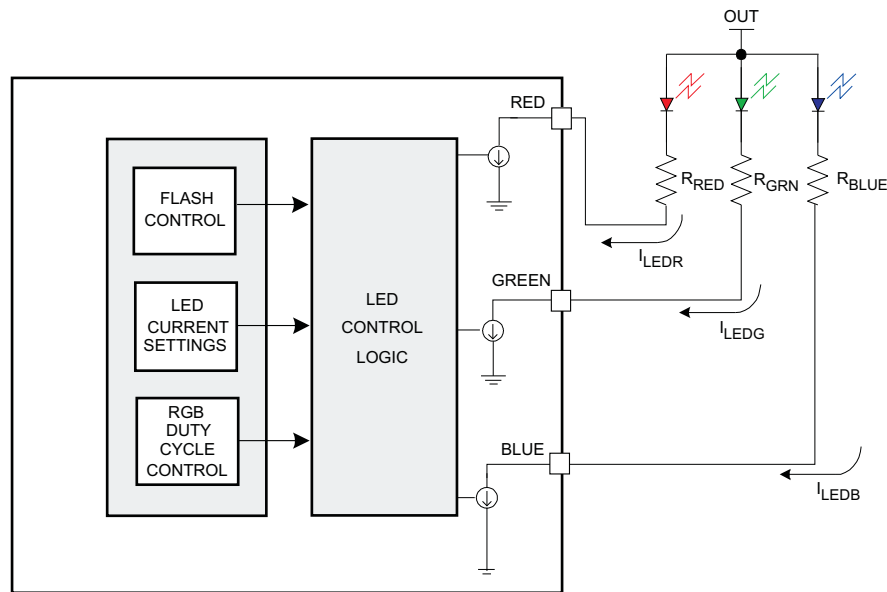


Figure 45. Limiting the External LED Current

The flashing-mode parameters defined in register RGB_FLASH enable setting the flashing period from 1 to 8 seconds in 0.5-sec steps, or to continuous operation. Flashing operation is enabled by setting the FLASH_EN bit in register RGB_FLASH to HI. This bit must be set HI to enable the RGB current-sink channels.

Each driver has an individual duty cycle control. The duty cycle modulation method used is similar to the PWM_LED duty cycle control, with high frequency pulses being generated when the driver (RED, GREEN, or BLUE pins) is ON. The repetition period for the RGB drivers has a total of 32 pulses, enabling a 3.125% resolution when programming the individual RED, GREEN and BLUE drivers duty cycles. The duty cycles for each driver can be set individually using control bits on registers RGB_RED, RGB_GREEN and RGB_BLUE.

The RGB drivers can be programmed to sink 4, 8, or 12 mA, with no external current limiting resistor.

8.3.6.3 *Functionality Guide — LED And Peripheral Drivers*

Table 16. White Led Constant Current Driver

| DRIVER | PWM | | OUTPUT VOLTAGE | LED CURRENT | | | EFFICIENCY (%) | POWER UP DEFAULT |
|--------|--|-----------------|----------------|--------------------------|-------|--------------|----------------|------------------|
| | DUTY CYCLE RANGE | NUMBER OF STEPS | | I _o (TYP) | MAX | ACCURACY (%) | | |
| SM3 | Off (0%), 0.4% to 99.6% Set through I ² C | 256 | 5 V to 25 V | Set by external resistor | 25 mA | 25 | 80 | Off (0%) |

Table 17. Open-Drain PWM Drivers

| DRIVER | PWM FREQUENCY (kHz) | PWM DUTY CYCLE | | | I _{O(MAX)} mA | POWER UP DEFAULT |
|---------|---|---|-----------------|----------|---------------------------|------------------|
| | | RANGE | NUMBER OF STEPS | MIN STEP | | |
| PWM | 0.5/1/1.5/2/3/ 4.5/7.8/15.6 Set through I ² C | Off (0%), 6.25% to 100 Set through I ² C | 8 | 6.25% | 150 | Off(0%) |
| LED_PWM | 15.625 or 23.4 , set through I ² C | Off(0%). 0.4% to 99.6% Set through I ² C | 256 | 0.4% | 150 | Off (0%) |

Table 18. RGB Open-Drain LED Driver

| DRIVER | FLASH PERIOD (SAME FOR RGB) | | | FLASH ON TIME (SAME FOR RGB) | | | BRIGHTNESS (INDIVIDUAL R/G/B CONTROL) | | | I _o mA | POWER UP DEFAULT |
|------------------------|---|-----------------------|----------|--|-----------------------|----------|---|------------------------|--------------|-------------------|---|
| | RANGE | NUMBER OF STEPS | MIN STEP | RANGE | NUMBER OF STEPS | MIN STEP | DUTY (%) | NUMBE R OF STEPS | MIN STEPS | | |
| RED, GREEN, BLUE | No flash, or 1 to 8 s Set through I ² C | 16 | 0.5 s | 0.1 to 0.6 s Set through I ² C | 8 | 0.1 s | Off (0%), 3.125 to 96.87 Set through I ² C | 32 | 3.125% | 0/4/8/12 | Flash Off, 0 mA, 0% brightness duty cycle |

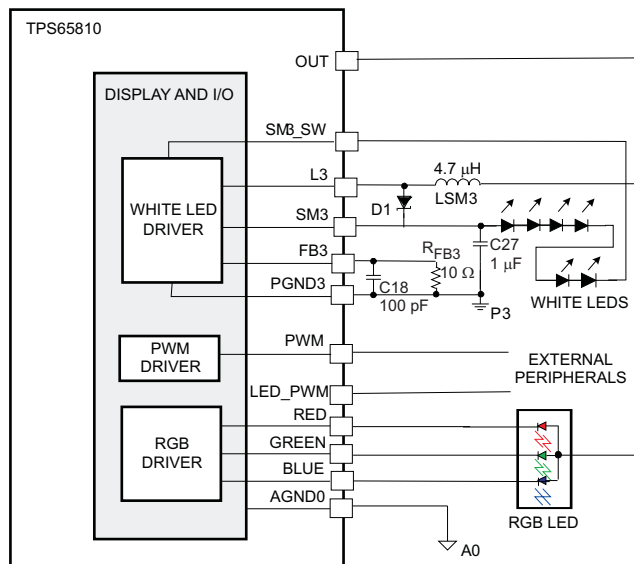


Figure 46. Required External Components, Recommended Values, External Connections

Table 19. SM3 Duty Cycle Settings

| DEC | B7-B0 | DCPU | DEC | B7-B0 | DCPU | DEC | B7-B0 | DCPU | DEC | B7-B0 | DCPU | DEC | B7-B0 | DCPU |
|-----|-----------|-------|-----|-----------|-------|-----|-----------|-------|-----|-----------|-------|-----|-----------|-------|
| 0 | 0000 0000 | – | 52 | 0011 0100 | 0.203 | 104 | 0110 1000 | 0.406 | 156 | 1001 1100 | 0.609 | 208 | 1101 0000 | 0.813 |
| 1 | 0000 0001 | 0.004 | 53 | 0011 0101 | 0.207 | 105 | 0110 1001 | 0.41 | 157 | 1001 1101 | 0.613 | 209 | 1101 0001 | 0.816 |
| 2 | 0000 0010 | 0.008 | 54 | 0011 0110 | 0.211 | 106 | 0110 1010 | 0.414 | 158 | 1001 1110 | 0.617 | 210 | 1101 0010 | 0.82 |
| 3 | 0000 0011 | 0.012 | 55 | 0011 0111 | 0.215 | 107 | 0110 1011 | 0.418 | 159 | 1001 1111 | 0.621 | 211 | 1101 0011 | 0.824 |
| 4 | 0000 0100 | 0.016 | 56 | 0011 1000 | 0.219 | 108 | 0110 1100 | 0.422 | 160 | 1010 0000 | 0.625 | 212 | 1101 0100 | 0.828 |
| 5 | 0000 0101 | 0.02 | 57 | 0011 1001 | 0.223 | 109 | 0110 1101 | 0.426 | 161 | 1010 0001 | 0.629 | 213 | 1101 0101 | 0.832 |
| 6 | 0000 0110 | 0.023 | 58 | 0011 1010 | 0.227 | 110 | 0110 1110 | 0.43 | 162 | 1010 0010 | 0.633 | 214 | 1101 0110 | 0.836 |
| 7 | 0000 0111 | 0.027 | 59 | 0011 1011 | 0.23 | 111 | 0110 1111 | 0.434 | 163 | 1010 0011 | 0.637 | 215 | 1101 0111 | 0.84 |
| 8 | 0000 1000 | 0.031 | 60 | 0011 1100 | 0.234 | 112 | 0111 0000 | 0.438 | 164 | 1010 0100 | 0.641 | 216 | 1101 1000 | 0.844 |
| 9 | 0000 1001 | 0.035 | 61 | 0011 1101 | 0.238 | 113 | 0111 0001 | 0.441 | 165 | 1010 0101 | 0.645 | 217 | 1101 1001 | 0.848 |
| 10 | 0000 1010 | 0.039 | 62 | 0011 1110 | 0.242 | 114 | 0111 0010 | 0.445 | 166 | 1010 0110 | 0.648 | 218 | 1101 1010 | 0.852 |
| 11 | 0000 1011 | 0.043 | 63 | 0011 1111 | 0.246 | 115 | 0111 0011 | 0.449 | 167 | 1010 0111 | 0.652 | 219 | 1101 1011 | 0.855 |
| 12 | 0000 1100 | 0.047 | 64 | 0100 0000 | 0.25 | 116 | 0111 0100 | 0.453 | 168 | 1010 1000 | 0.656 | 220 | 1101 1100 | 0.859 |
| 13 | 0000 1101 | 0.051 | 65 | 0100 0001 | 0.254 | 117 | 0111 0101 | 0.457 | 169 | 1010 1001 | 0.66 | 221 | 1101 1101 | 0.863 |
| 14 | 0000 1110 | 0.055 | 66 | 0100 0010 | 0.258 | 118 | 0111 0110 | 0.461 | 170 | 1010 1010 | 0.664 | 222 | 1101 1110 | 0.867 |
| 15 | 0000 1111 | 0.059 | 67 | 0100 0011 | 0.262 | 119 | 0111 0111 | 0.465 | 171 | 1010 1011 | 0.668 | 223 | 1101 1111 | 0.871 |
| 16 | 0001 0000 | 0.063 | 68 | 0100 0100 | 0.266 | 120 | 0111 1000 | 0.469 | 172 | 1010 1100 | 0.672 | 224 | 1110 0000 | 0.875 |
| 17 | 0001 0001 | 0.066 | 69 | 0100 0101 | 0.27 | 121 | 0111 1001 | 0.473 | 173 | 1010 1101 | 0.676 | 225 | 1110 0001 | 0.879 |
| 18 | 0001 0010 | 0.07 | 70 | 0100 0110 | 0.273 | 122 | 0111 1010 | 0.477 | 174 | 1010 1110 | 0.68 | 226 | 1110 0010 | 0.883 |
| 19 | 0001 0011 | 0.074 | 71 | 0100 0111 | 0.277 | 123 | 0111 1011 | 0.48 | 175 | 1010 1111 | 0.684 | 227 | 1110 0011 | 0.887 |
| 20 | 0001 0100 | 0.078 | 72 | 0100 1000 | 0.281 | 124 | 0111 1100 | 0.484 | 176 | 1011 0000 | 0.688 | 228 | 1110 0100 | 0.891 |
| 21 | 0001 0101 | 0.082 | 73 | 0100 1001 | 0.285 | 125 | 0111 1101 | 0.488 | 177 | 1011 0001 | 0.691 | 229 | 1110 0101 | 0.895 |
| 22 | 0001 0110 | 0.086 | 74 | 0100 1010 | 0.289 | 126 | 0111 1110 | 0.492 | 178 | 1011 0010 | 0.695 | 230 | 1110 0110 | 0.898 |
| 23 | 0001 0111 | 0.09 | 75 | 0100 1011 | 0.293 | 127 | 0111 1111 | 0.496 | 179 | 1011 0011 | 0.699 | 231 | 1110 0111 | 0.902 |
| 24 | 0001 1000 | 0.094 | 76 | 0100 1100 | 0.297 | 128 | 1000 0000 | 0.5 | 180 | 1011 0100 | 0.703 | 232 | 1110 1000 | 0.906 |
| 25 | 0001 1001 | 0.098 | 77 | 0100 1101 | 0.301 | 129 | 1000 0001 | 0.504 | 181 | 1011 0101 | 0.707 | 233 | 1110 1001 | 0.91 |
| 26 | 0001 1010 | 0.102 | 78 | 0100 1110 | 0.305 | 130 | 1000 0010 | 0.508 | 182 | 1011 0110 | 0.711 | 234 | 1110 1010 | 0.914 |
| 27 | 0001 1011 | 0.105 | 79 | 0100 1111 | 0.309 | 131 | 1000 0011 | 0.512 | 183 | 1011 0111 | 0.715 | 235 | 1110 1011 | 0.918 |
| 28 | 0001 1100 | 0.109 | 80 | 0101 0000 | 0.313 | 132 | 1000 0100 | 0.516 | 184 | 1011 1000 | 0.719 | 236 | 1110 1100 | 0.922 |
| 29 | 0001 1101 | 0.113 | 81 | 0101 0001 | 0.316 | 133 | 1000 0101 | 0.52 | 185 | 1011 1001 | 0.723 | 237 | 1110 1101 | 0.926 |
| 30 | 0001 1110 | 0.117 | 82 | 0101 0010 | 0.32 | 134 | 1000 0110 | 0.523 | 186 | 1011 1010 | 0.727 | 238 | 1110 1110 | 0.93 |
| 31 | 0001 1111 | 0.121 | 83 | 0101 0011 | 0.324 | 135 | 1000 0111 | 0.527 | 187 | 1011 1011 | 0.73 | 239 | 1110 1111 | 0.934 |
| 32 | 0010 0000 | 0.125 | 84 | 0101 0100 | 0.328 | 136 | 1000 1000 | 0.531 | 188 | 1011 1100 | 0.734 | 240 | 1111 0000 | 0.938 |
| 33 | 0010 0001 | 0.129 | 85 | 0101 0101 | 0.332 | 137 | 1000 1001 | 0.535 | 189 | 1011 1101 | 0.738 | 241 | 1111 0001 | 0.941 |
| 34 | 0010 0010 | 0.133 | 86 | 0101 0110 | 0.336 | 138 | 1000 1010 | 0.539 | 190 | 1011 1110 | 0.742 | 242 | 1111 0010 | 0.945 |
| 35 | 0010 0011 | 0.137 | 87 | 0101 0111 | 0.34 | 139 | 1000 1011 | 0.543 | 191 | 1011 1111 | 0.746 | 243 | 1111 0011 | 0.949 |
| 36 | 0010 0100 | 0.141 | 88 | 0101 1000 | 0.344 | 140 | 1000 1100 | 0.547 | 192 | 1100 0000 | 0.75 | 244 | 1111 0100 | 0.953 |
| 37 | 0010 0101 | 0.145 | 89 | 0101 1001 | 0.348 | 141 | 1000 1101 | 0.551 | 193 | 1100 0001 | 0.754 | 245 | 1111 0101 | 0.957 |
| 38 | 0010 0110 | 0.148 | 90 | 0101 1010 | 0.352 | 142 | 1000 1110 | 0.555 | 194 | 1100 0010 | 0.758 | 246 | 1111 0110 | 0.961 |
| 39 | 0010 0111 | 0.152 | 91 | 0101 1011 | 0.355 | 143 | 1000 1111 | 0.559 | 195 | 1100 0011 | 0.762 | 247 | 1111 0111 | 0.965 |
| 40 | 0010 1000 | 0.156 | 92 | 0101 1100 | 0.359 | 144 | 1001 0000 | 0.563 | 196 | 1100 0100 | 0.766 | 248 | 1111 1000 | 0.969 |
| 41 | 0010 1001 | 0.16 | 93 | 0101 1101 | 0.363 | 145 | 1001 0001 | 0.566 | 197 | 1100 0101 | 0.77 | 249 | 1111 1001 | 0.973 |
| 42 | 0010 1010 | 0.164 | 94 | 0101 1110 | 0.367 | 146 | 1001 0010 | 0.57 | 198 | 1100 0110 | 0.773 | 250 | 1111 1010 | 0.977 |
| 43 | 0010 1011 | 0.168 | 95 | 0101 1111 | 0.371 | 147 | 1001 0011 | 0.574 | 199 | 1100 0111 | 0.777 | 251 | 1111 1011 | 0.98 |
| 44 | 0010 1100 | 0.172 | 96 | 0110 0000 | 0.375 | 148 | 1001 0100 | 0.578 | 200 | 1100 1000 | 0.781 | 252 | 1111 1100 | 0.984 |
| 45 | 0010 1101 | 0.176 | 97 | 0110 0001 | 0.379 | 149 | 1001 0101 | 0.582 | 201 | 1100 1001 | 0.785 | 253 | 1111 1101 | 0.988 |
| 46 | 0010 1110 | 0.18 | 98 | 0110 0010 | 0.383 | 150 | 1001 0110 | 0.586 | 202 | 1100 1010 | 0.789 | 254 | 1111 1110 | 0.992 |
| 47 | 0010 1111 | 0.184 | 99 | 0110 0011 | 0.387 | 151 | 1001 0111 | 0.59 | 203 | 1100 1011 | 0.793 | 255 | 1111 1111 | 0.996 |
| 48 | 0011 0000 | 0.188 | 100 | 0110 0100 | 0.391 | 152 | 1001 1000 | 0.594 | 204 | 1100 1100 | 0.797 | | | |
| 49 | 0011 0001 | 0.191 | 101 | 0110 0101 | 0.395 | 153 | 1001 1001 | 0.598 | 205 | 1100 1101 | 0.801 | | | |
| 50 | 0011 0010 | 0.195 | 102 | 0110 0110 | 0.398 | 154 | 1001 1010 | 0.602 | 206 | 1100 1110 | 0.805 | | | |
| 51 | 0011 0011 | 0.199 | 103 | 0110 0111 | 0.402 | 155 | 1001 1011 | 0.605 | 207 | 1100 1111 | 0.809 | | | |

TPS65810, TPS65811

SLVS658C – MARCH 2006 – REVISED JANUARY 2016

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Table 20. RGB Duty Cycle Control Settings

| RGB_D4 | RGB_D3 | RGB_D2 | RGB_D1 | RGB_D0 | DC(%) | FLASH_PER3 | FLASH_PER2 | FLASH_PER1 | FLASH_PER0 | P(s) |
|--------|--------|--------|--------|--------|-------|------------|------------|------------|------------|-------------|
| 0 | 0 | 0 | 0 | 0 | 0.00 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 3.23 | 0 | 0 | 0 | 1 | 1.5 |
| 0 | 0 | 0 | 1 | 0 | 6.45 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 1 | 9.68 | 0 | 0 | 1 | 1 | 2.5 |
| 0 | 0 | 1 | 0 | 0 | 12.90 | 0 | 1 | 0 | 0 | 3 |
| 0 | 0 | 1 | 0 | 1 | 16.13 | 0 | 1 | 0 | 1 | 3.5 |
| 0 | 0 | 1 | 1 | 0 | 19.35 | 0 | 1 | 1 | 0 | 4 |
| 0 | 0 | 1 | 1 | 1 | 22.58 | 0 | 1 | 1 | 1 | 4.5 |
| 0 | 1 | 0 | 0 | 0 | 25.80 | 1 | 0 | 0 | 0 | 5 |
| 0 | 1 | 0 | 0 | 1 | 29.03 | 1 | 0 | 0 | 1 | 5.5 |
| 0 | 1 | 0 | 1 | 0 | 32.25 | 1 | 0 | 1 | 0 | 6 |
| 0 | 1 | 0 | 1 | 1 | 35.48 | 1 | 0 | 1 | 1 | 6.5 |
| 0 | 1 | 1 | 0 | 0 | 38.70 | 1 | 1 | 0 | 0 | 7 |
| 0 | 1 | 1 | 0 | 1 | 41.93 | 1 | 1 | 0 | 1 | 7.5 |
| 0 | 1 | 1 | 1 | 0 | 45.15 | 1 | 1 | 1 | 0 | 8 |
| 0 | 1 | 1 | 1 | 1 | 48.38 | 1 | 1 | 1 | 1 | Continuous |
| 1 | 0 | 0 | 0 | 0 | 51.60 | | | | | |
| 1 | 0 | 0 | 0 | 1 | 54.83 | | | | | |
| 1 | 0 | 0 | 1 | 0 | 58.05 | | FLASH_ON2 | FLASH_ON1 | FLASH_ON0 | ON_TIME (s) |
| 1 | 0 | 0 | 1 | 1 | 61.23 | | 0 | 0 | 0 | 0.1 |
| 1 | 0 | 1 | 0 | 0 | 64.50 | | 0 | 0 | 1 | 0.15 |
| 1 | 0 | 1 | 0 | 1 | 67.73 | | 0 | 1 | 0 | 0.2 |
| 1 | 0 | 1 | 1 | 0 | 70.95 | | 0 | 1 | 1 | 0.25 |
| 1 | 0 | 1 | 1 | 1 | 74.18 | | 1 | 0 | 0 | 0.3 |
| 1 | 1 | 0 | 0 | 0 | 77.40 | | 1 | 0 | 1 | 0.4 |
| 1 | 1 | 0 | 0 | 1 | 80.63 | | 1 | 1 | 0 | 0.5 |
| 1 | 1 | 0 | 1 | 0 | 83.85 | | 1 | 1 | 1 | 0.6 |
| 1 | 1 | 0 | 1 | 1 | 87.08 | | | | | |
| 1 | 1 | 1 | 0 | 0 | 90.30 | | | | | |
| 1 | 1 | 1 | 0 | 1 | 93.53 | | | | | |
| 1 | 1 | 1 | 1 | 0 | 96.75 | | | | | |
| 1 | 1 | 1 | 1 | 1 | 99.98 | | | | | |

Table 21. PWM Frequency and Duty Cycle Settings

| PWM FREQUENCY TABLE | | | | PWM_D DUTY CYCLE | | | | |
|---------------------|--------|--------|--------|------------------|---------|---------|---------|--------------|
| PWM_F2 | PWM_F1 | PWM_F0 | F (Hz) | PWM2_D3 | PWM2_D2 | PWM2_D1 | PWM2_D0 | D_cycle (pu) |
| 0 | 0 | 0 | 15600 | 0 | 0 | 0 | 0 | 0.0625 |
| 0 | 0 | 1 | 7800 | 0 | 0 | 0 | 1 | 0.125 |
| 0 | 1 | 0 | 4500 | 0 | 0 | 1 | 0 | 0.1875 |
| 0 | 1 | 1 | 3000 | 0 | 0 | 1 | 1 | 0.25 |
| 1 | 0 | 0 | 2000 | 0 | 1 | 0 | 0 | 0.3125 |
| 1 | 0 | 1 | 1500 | 0 | 1 | 0 | 1 | 0.375 |
| 1 | 1 | 0 | 1000 | 0 | 1 | 1 | 0 | 0.4375 |
| 1 | 1 | 1 | 500 | 0 | 1 | 1 | 1 | 0.5 |
| | | | | 1 | 0 | 0 | 0 | 0.5625 |
| | | | | 1 | 0 | 0 | 1 | 0.625 |
| | | | | 1 | 0 | 1 | 0 | 0.6875 |
| | | | | 1 | 0 | 1 | 1 | 0.75 |
| | | | | 1 | 1 | 0 | 0 | 0.8125 |
| | | | | 1 | 1 | 0 | 1 | 0.875 |
| | | | | 1 | 1 | 1 | 0 | 0.9375 |
| | | | | 1 | 1 | 1 | 1 | 1 |

8.3.7 General-Purpose I/Os — GPIO 1, 2, 3

The TPS65810 device integrates 3 general-purpose, open-drain ports (GPIOs) that can be configured as selectable inputs or outputs. When configured as outputs the output level can be set to LO or HI through I²C commands. When the GPIOs are configured as inputs the action to be taken when a transition or HI/LO level is detected at the GPIO pin is selectable through I²C.

When configured as inputs the GPIOs can be set in the following modes which are defined as follows:

Interrupt request In this mode of operation, a transition at the GPIO pin generates an interrupt request at the interrupt controller. The GPIO interrupt request can be masked at the INT_MASK register. This operation mode is available for GPIOs 1 and 2.

SM1 and SM2 control The GPIOs can be used to turn the converters SM1 and SM2 ON/OFF, as well as setting them in stand-by mode. This control mode is available for GPIO1 (SM1 on/off and SM1/SM2 stand-by) and GPIO2 (SM2 on/off control).

ADC trigger GPIO3 can be configured as an external ADC trigger. The GPIO3 trigger configuration bit is located at the ADC register ADC_DELAY.

8.3.7.1 GPIOs Input Level Configuration

When using I²C commands, the GPIO1 and GPIO2 pins can be configured as logic output signals or as level-controlled inputs which enables (or disables) the switch mode converters SM1 and/or SM2. These pins may also be configured as rising- or falling-edge-triggered inputs to externally control the generation of an interrupt signal (INT), if desired.

The GPIO3 pin may be used as an external trigger source to start an A/D conversion cycle or as a logic output.

See [Figure 47](#) for a description of the logic used for GPIO1 and GPIO2 inputs when configured for edge-triggered interrupt generation. The signal from the GPIO pin input is double-latched before being sent to the interrupt controller logic. The inversion of the Q output from the first flip-flop must be HI to allow the output latch to be cleared when a READ command occurs. On the initial edge of the GPIO signal, the Q output of the flip-flop is set (HI). The INT line is asserted (LO) after the initial selected edge from the GPIO pin. On the next falling (or rising) edge of the GPIO pin, the interrupt can again be cleared (which allows the INT pin to go back high). The INT signal is cleared (set back HI) after an I²C READ operation is performed.

Thus, two successive edges of the GPIO signal, followed by an I²C READ command, are required to clear the INT pin output. If no I²C READ commands occur, repeatedly applying edges to the GPIO pin does not toggle the state of the INT pin output.

In addition to an I²C READ command after two GPIO edges, a UVLO event or reconfiguration of the GPIO pins as outputs also deasserts the INT signal.

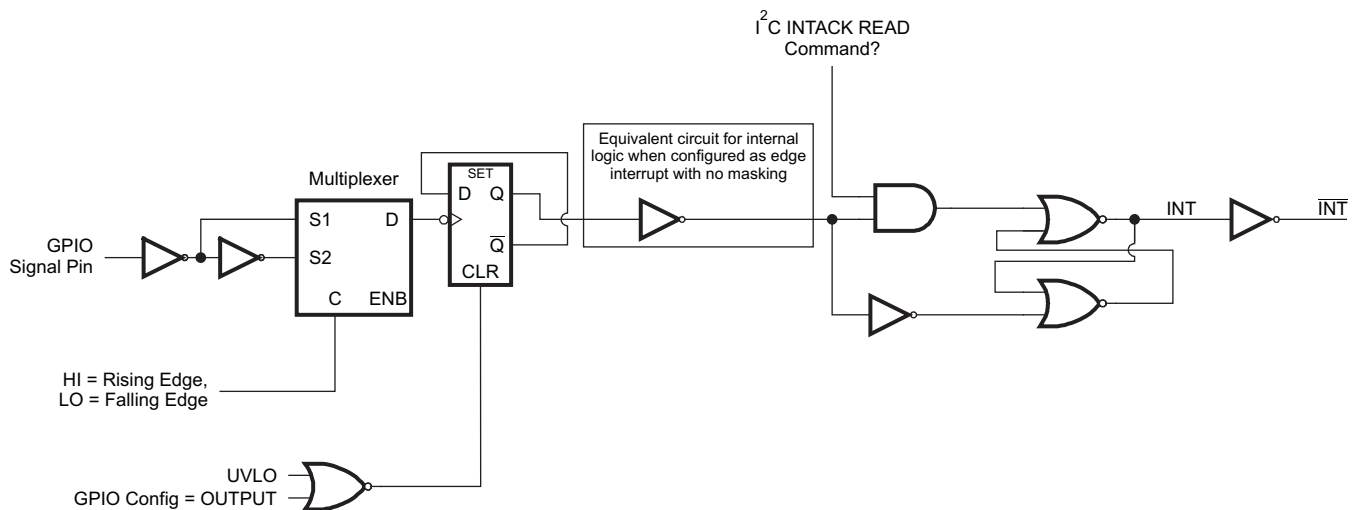


Figure 47. GPIO 1 or GPIO2 Configured as an Interrupt Request Input

8.3.7.2 Function Implementation: I²C Commands Versus GPIO Commands

Some of the GPIO SM1/SM2 control functions overlap I²C register control functions. [Table 22](#) lists the TPS65810 action when the command of the GPIOs and I²C registers commands are not compatible with each other.

Table 22. GPIO Commands and I²C Registers Commands

| SM1 AND SM2 I ² C COMMAND | GPIO COMMAND | SM1 OR SM2 MODE SET |
|--------------------------------------|--------------------|---------------------|
| ON/OFF | | |
| CONVERTER DISABLED | CONVERTER DISABLED | DISABLED |
| CONVERTER ENABLED | DON'T CARE | ENABLED |
| DON'T CARE | CONVERTER ENABLED | ENABLED |
| STANDBY | | |
| DO NOT SET STANDBY | DON'T CARE | NORMAL |
| SET STANDBY | SET STANDBY | STANDBY |
| DON'T CARE | DO NOT SET STANDBY | NORMAL |

8.3.7.2.1 GPIO Configuration Table

[Table 23](#) lists the I²C register settings required to program the available GPIO modes. The GPIO pins logic level is available at register SM1_STANDBY, bits B5, B6 and B7.

Table 23. Recommended GPIO Configuration Procedure

| GPIO MODE | I ² C REGISTERS | I ² C REGISTER BIT SETTING | ADDITIONAL DETAILS |
|---|----------------------------|---|---|
| GPIO3 = OUTPUT | GPIO3 | GPIO3/O=HI AND GPIO3OUT = HI | GPIO3 PIN SET TO HIGH IMPEDANCE MODE |
| | | GPIO3/O=HI AND GPIO3OUT = LO | V(GPIO3) = V _{OL} |
| GPIO3 =INPUT ADC CONVERSION START TRIGGER | GPIO3 AND ADC_DELAY | GPIO3/O=LO AND ADC_TRG_GPIO3 = HI AND EDGE_GPIO3 = HI | GPIO3 pin rising edge triggers ADC conversion |
| | | GPIO3/O=LO AND ADC_TRG_GPIO3 = HI AND EDGE_GPIO3=LO | GPIO3 pin falling edge triggers ADC conversion |
| GPIO2 = OUTPUT | GPIO12 | GPIO2/O=HI AND GPIO2OUT = HI | GPIO2 PIN SET TO HIGH IMPEDANCE MODE |
| | | GPIO2/O=HI AND GPIO2OUT = LO | V(GPIO2) = V _{OL} |
| GPIO2=INPUT, HOST INTERRUPT REQUEST | GPIO12 AND GPIO3 | GPIO2/O=LO AND GPIO2INT = HI AND GPIO2LVL=HI AND GPIO2SM2=LO | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO2) falling edge |
| | | GPIO2/O=LO AND GPIO2INT = HI AND GPIO2LVL=HI AND GPIO2SM2=LO | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO2) rising edge |
| GPIO2=INPUT, SM2 ENABLE | GPIO12 AND GPIO3 | GPIO2/O=LO AND GPIO2INT = LO AND GPIO2LVL=HI AND GPIO2SM2 = HI | SM2 converter ON at V(GPIO2) = HI |
| | | GPIO2/O=LO AND GPIO2INT = LO AND GPIO2LVL=LO AND GPIO2SM2 = HI | SM2 converter ON at V(GPIO2) = LO |
| GPIO1 = OUTPUT | GPIO12 | GPIO1/O=HI AND GPIO1OUT = HI | GPIO1 PIN SET TO HIGH IMPEDANCE MODE |
| | | GPIO1/O=HI AND GPIO1OUT = LO | V(GPIO1) = V _{OL} |
| GPIO1=INPUT, HOST INTERRUPT REQUEST | GPIO12 AND GPIO3 | GPIO1/O=LO AND GPIO1INT = HI AND GPIO1LVL=HI AND GPIO1SM1=LO AND GPIO1SMSBY = LO | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO1) falling edge |
| | | GPIO1/O=LO AND GPIO1INT = HI AND GPIO1LVL=LO AND GPIO1SM1=LO AND GPIO1SMSBY = LO | $\overline{\text{INT}}$ pin HI→LO→HI at V(GPIO1) rising edge |
| GPIO1=INPUT, SM1 ENABLE | GPIO12 AND GPIO3 | GPIO1/O=LO AND GPIO1INT = LO AND GPIO1LVL=HI AND GPIO1SM1 = HI AND GPIO1SMSBY = LO | SM1 converter ON at V(GPIO1) = HI |
| | | GPIO1/O=LO AND GPIO1INT = LO AND GPIO1LVL=LO AND GPIO1SM1 = HI AND GPIO1SMSBY = LO | SM1 converter ON at V(GPIO1) = LO |
| GPIO1=INPUT, SM1/SM2 STANDBY CONTROL | GPIO12 AND GPIO3 | GPIO1/O=LO AND GPIO1INT = LO AND GPIO1LVL=HI AND GPIO1SM1=LO AND GPIO1SMSBY = HI | SM1/SM2 converter stand-by set at V(GPIO1) = HI |
| | | GPIO1/O=LO AND GPIO1INT = LO AND GPIO1LVL=LO AND GPIO1SM1=LO AND GPIO1SMSBY = HI | SM1/SM2 converter stand-by set at V(GPIO1) = LO |

8.3.7.3 Functionality Guide – General-Purpose Inputs and Outputs

Table 24. GPIO3 Functions

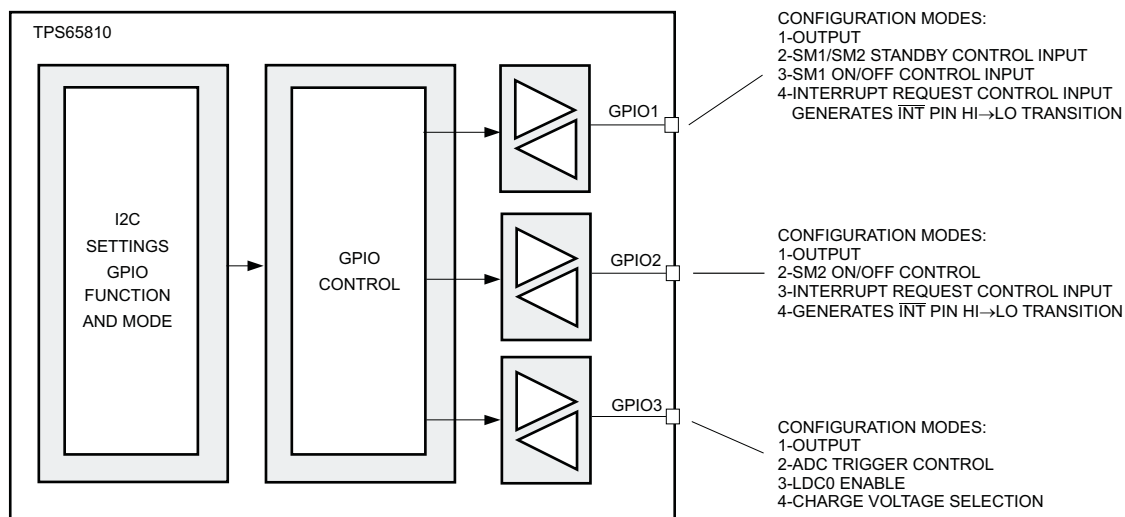
| CONFIGURED AS OUTPUT | | CONFIGURED AS INPUT | POWER-UP DEFAULT |
|---|------------------------|--|-------------------------|
| OUTPUT LEVEL | I _{O(MAX)} mA | A/D CONVERSION START TRIGGER | |
| HI or LO at output set through I ² C | 5 | Falling or rising edge selected through I ² C | Input, no mode selected |

Table 25. GPIO2 Functions

| CONFIGURED AS OUTPUT | | CONFIGURED AS INPUT | | POWER-UP DEFAULT |
|---|------------------------|--|--|--|
| OUTPUT LEVEL | I _{O(MAX)} mA | HOST INTERRUPT REQUEST | SM2 ENABLE | |
| HI or LO at output set through I ² C | 5 | Set $\overline{\text{INT}}$ pin to LO through I ² C when GPIO2 pin edge is detected. Rising or falling edge detection selected through I ² C | GPIO2 level sets SM2 converter ON/OFF operation. GPIO2 pin level (HI or LO) for ON operation selected through I ² C | Input, SM2 enable, SM2 ONat GPIO2 = HI |
| | | The host interrupt request and SM2 enable GPIO2 functions are mutually exclusive, and they must NOT be configured simultaneously | | |

Table 26. GPIO1 Functions

| CONFIGURED AS OUTPUT | | CONFIGURED AS INPUT | | | POWER-UP DEFAULT |
|---|------------------------|---|---|--|--|
| OUTPUT LEVEL | I _{O(MAX)} mA | HOST INTERRUPT REQUEST | SM1 ENABLE | SM1 AND SM2 STANDBY CONTROL | |
| HI or LO at output set through I ² C | 5 | Set $\overline{\text{INT}}$ pin to LO through I ² C when GPIO1 pin edge is detected. Rising or falling edge detection set through I ² C | GPIO1 level sets SM1 converter ON/OFF operation. GPIO2 pin level (HI or LO) for ON operation set through I ² C | GPIO1 level sets SM2 and SM1 converters in stand-by mode. GPIO1 pin level (HI or LO) for stand-by mode set selected through I ² C | Input, SM1 enable, SM1 ONat GPIO1 = HI |
| | | The host interrupt request, SM1 enable and SM1/SM2 stand-by control GPIO1 functions are mutually exclusive, and they must NOT be configured simultaneously. | | | |


Figure 48. Required External Components, Recommended Values, External Connections

8.4 Device Functional Modes

8.4.1 Sleep Mode

The device enters the *Sleep* mode if a thermal fault or a system low voltage fault is detected. For a detailed description of which registers are reset to their default state and which registers keep their state, reference the section on [System Sequencing and TPS65810 Operating Modes](#).

8.4.2 Normal Mode

The device enters the *Normal* mode after all power-good checks pass. In this mode, the I²C registers define the operation of the device.

8.5 Programming

8.5.1 Serial Interface

8.5.1.1 Overview

The TPS65810 device is compatible with a host-controlled environment, with internal parameters and status information accessible through an I²C interface. An I²C communication port provides a simple way for an I²C-compatible host to access system status information and reset fault modes, functioning as a SLAVE port enabling I²C-compatible hosts to WRITE to or to READ from internal registers. The TPS65810 I²C port is a 2-wire bidirectional interface using SCL (clock) and SDA (data) pins; the SDA pin is open-drain and requires an external pullup. The I²C is designed to operate at SCL frequencies up to 400 kHz. The standard 8-bit command is supported, the CMD part of the sequence is the 8-bit register address to READ from or to WRITE to.

8.5.1.2 Register Default Values

The internal TPS65810 registers are loaded during the initial power-up from an internal, non-volatile memory bank. The power-up default values are described in the sections detailing the registers functionality.

The register contents remain intact as long as OUT pin voltage remains above the internal UVLO threshold, V_{UVLO}. All register bits are reset to the internal power up default when the OUT pin voltage falls below the V_{UVLO} threshold or if the `HOT_RESET` pin is set to LO.

8.5.1.3 I²C Address

The I²C specification contains several global addresses, which the slaves on the bus are required to respond to. The TPS65810 only responds (ACK) to addresses: 0x90 and 0x91 and does not respond (NACK) to any other address.

Table 27. TPS65810 I²C Read and Write Address

| BYTE | BIT | | | | | | | |
|---|-----|----|----|----|----|----|----|-----|
| | MSB | 6 | 5 | 4 | 3 | 2 | 1 | LSB |
| TPS65810 I ² C WRITE ADDRESS | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| TPS65810 I ² C READ ADDRESS | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| I/O DATA BUS | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

8.5.1.4 Incremental Read

The TPS65810 does not support incremental read operations. Each register must be accessed in a single read operation.

8.5.1.5 I²C Bus Release

The TPS65810 I²C engine does not create START or STOP states on the I²C bus during normal operation.

8.5.1.6 Sleep Mode Operation

When the sleep mode is set SDAT is held LO by the TPS65810. The overall system operation is not affected, as in sleep mode all TPS65810 integrated supplies are disabled and no power is available for any external devices connected to the TPS65810 SDAT pin. When sleep mode ends the SDAT pin is released before the TPS65810 integrated regulated supplies are enabled. See section on [System Sequencing and TPS65810 Operating Modes](#) for additional details on sleep mode operation.

8.5.1.7 I²C Communication Protocol

Table 28 lists the conventions used when describing the communication protocol.

Table 28. I²C Naming Conventions Used

| CONDITION | CODE |
|---|--------|
| START sent from host | S |
| STOP sent from host | P |
| TPS65810 I ² C slave address sent from host, bus direction set from host to TPS65810 (WRITE) | hA0 |
| TPS65810 register address sent from TPS65810, bus direction is from TPS65810 to host (READ) | hA1 |
| Non-valid I ² C slave address sent from host | hA_N |
| Valid TPS65810 register address sent from host | HCMD |
| Non-valid TPS65810 register address sent from host | HCMD_N |
| I/O data byte (8 bits) sent from host to TPS65810 | hDATA |
| I/O data byte (8 bits) sent from TPS65810 to host | bqDATA |
| Acknowledge (ACK) from host | hA |
| Not acknowledge (NACK) from host | hN |
| Acknowledge (ACK) from TPS65810 | bqA |
| Not acknowledge (NACK) from TPS65810 | bqN |

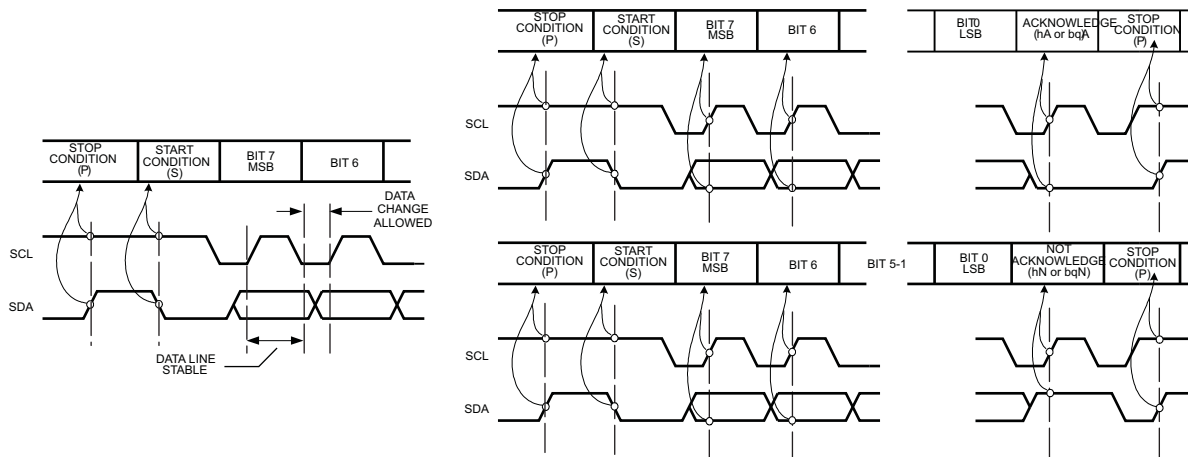


Figure 49. I²C operation waveforms

For normal data transfers, SDA is allowed to change only when SCL is low, and one clock pulse is used per bit of data. The SDA line must remain stable whenever the SCL line is high, as SDA changes when SCL is high are reserved for indicating the start and stop conditions. Each data transfer is initiated with a start condition and terminated with a stop condition.

When addressed, the TPS65810 device generates an acknowledge bit after the reception of each byte by pulling the SDA line Low. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. After the acknowledge or not acknowledge bit, the TPS65810 device leaves the data line high, enabling a STOP condition generation.

8.5.1.8 I²C Read and Write Operations

The TPS65810 device supports the standard I²C one-byte Write. The basic I²C read protocol has the following steps:

- Host sends a start and sets TPS65810 I²C slave address in write mode
- The TPS65810 device acknowledges (ACKs) that this is a valid I²C address and that the bus is configured for write
- Host sends TPS65810 register address
- The TPS65810 device acknowledges (ACKs) that this is a valid register and stores the register address to be read
- Host sends a repeated start and TPS65810 I²C slave address, reconfiguring the bus for read
- The TPS65810 device acknowledges (ACKs) that this is a valid address and that bus is reconfigured
- Bus is in read mode, TPS65810 device begins sending data from selected register

The I²C write protocol is similar to the read, without the need for a repeated start and bus being set in write mode. In a WRITE, it is not necessary to end each 1-byte WRITE command with a STOP; a START has the same effect (repeated start).

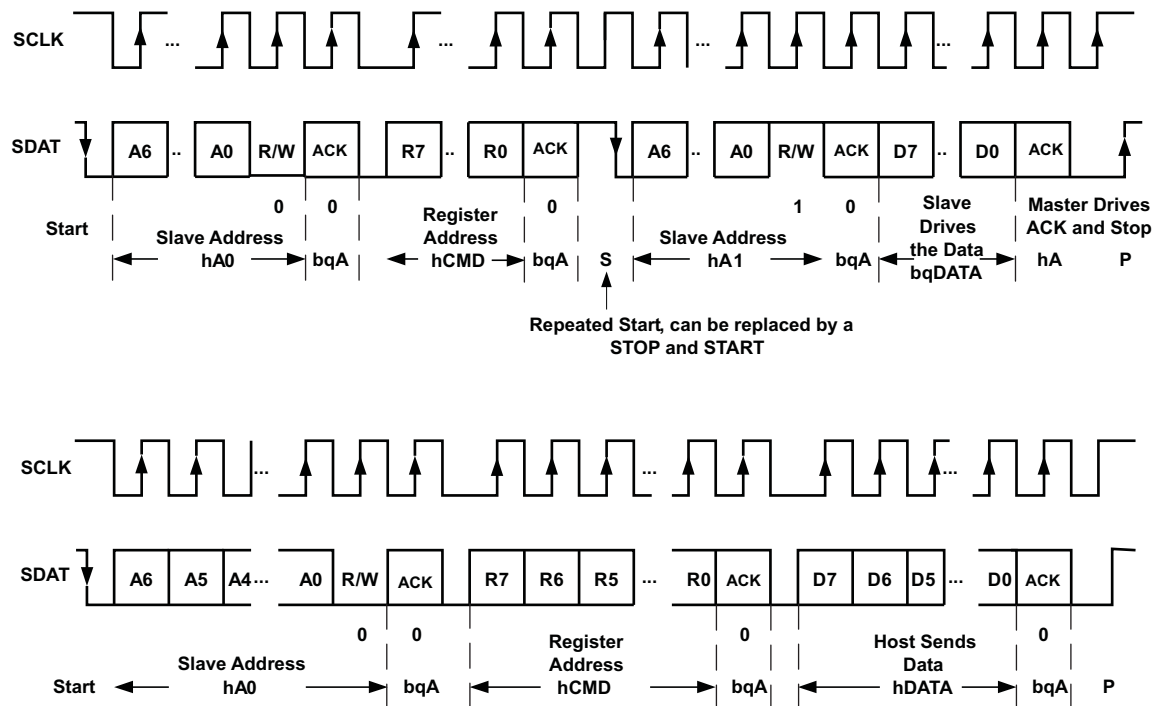


Figure 50. I²C read and write operations

The host can complete a READ or a WRITE sequence with either a STOP or a START.

8.5.1.9 Valid Write Sequences

The TPS65810 device always ACKs its own address. If the CMD points to an allowable READ or WRITE address, bq writes the address into its RAM address register and sends an ACK. If the CMD points to a non-allowed address, bq does NOT write the address into its RAM address register and sends a NACK.

Table 29. Valid Write Sequence Address Registers

| | | | | |
|---|-----|-----|--------|-----|
| S | hA0 | bqA | | |
| S | hA0 | bqA | hCMD | bqA |
| S | hA0 | bqA | hCMD_N | bqN |

8.5.1.10 One-Byte Write

The data is written to the addressed register when the bq ACK ending the one byte write sequence is received. The host can cancel a WRITE by sending a STOP or START before the trailing edge of the bq ACK clock pulse.

Table 30. One-Byte Write Address Register

| | | | | | | |
|---|-----|-----|------|-----|-------|-----|
| S | hA0 | bqA | hCMD | bqA | hDATA | bqA |
|---|-----|-----|------|-----|-------|-----|

8.5.1.11 Valid Read Sequences

The TPS65810 always ACKs its own address.

Table 31. Valid Read Sequence ACK Register

| | | |
|---|-----|-----|
| S | hA1 | bqA |
|---|-----|-----|

Upon receiving hA1, TPS65810 starts at wherever the RAM address register is pointing. The START and the STOP both act as priority interrupts. If the host has been interrupted and is not sure where it left off it can send a STOP and reset the TPS65810 state machine to the WAIT state; once in WAIT state, the TPS65810 ignores all activity on the SCL and SDA lines until it receives a START. A repeated START and START in the I²C specification are both treated as a START.

Table 32. Valid Read Sequence Address Registers

| | | | | | | | | | | |
|---|-----|-----|--------|-----|---|-----|-----|--------|----|---|
| S | hA0 | bqA | hCMD | bqA | P | | | | | |
| S | hA0 | bqA | hCMD | bqA | S | hA1 | bqA | bqDATA | hN | P |
| S | hA1 | bqA | bqDATA | hN | P | | | | | |

8.5.1.12 Non-Valid Sequences

Table 33. Incremental Read Sequences

| | | | | | | | | | | | | | | |
|---|-----|-----|--------|----|--------|----|--------|----|--------|----|-----|--------|----|---|
| S | hA1 | bqA | bqDATA | hA | bqDATA | hA | bqDATA | hA | bqDATA | hA | ... | bqDATA | hA | P |
|---|-----|-----|--------|----|--------|----|--------|----|--------|----|-----|--------|----|---|

A START followed by an address which is not bqA0 or bqA1 is NACKED.

Table 34. START and Non-hA0 or Non-hA1 Address

| | | |
|---|------|-----|
| S | hA_N | bqN |
|---|------|-----|

If the CMD points to a non-allowed READ address (reserved registers), bq sends a NACK back to the host, and it does not load the address in the RAM address register. Note that TPS65810 NACKS whether a stop is sent or not.

Table 35. Attempt to Specify Non-Allowed READ Address

| | | | | | |
|---|-----|-----|--------|-----|---|
| S | hA0 | bqA | hCMD_N | bqN | P |
| S | hA0 | bqA | hCMD_N | bqN | |

If the host attempts to WRITE to a READ-ONLY or non-accessible address TPS65810 ACKS the CMD containing the allowed READ address, loads the address into the address register and NACKS after the host sends the next data byte. After issuing the NACK TPS65810 returns to WAIT state. A subsequent hA1 READ could read this address.

Table 36. Attempt to Specify Non-Allowed WRITE Address

| | | | | | | |
|---|-----|-----|------|-----|-------|----|
| S | hA0 | bqA | hCMD | bqA | hDATA | bN |
|---|-----|-----|------|-----|-------|----|

8.6 Register Maps

Table 37. TPS65810 Internal Register Map

| Hex | Name | Description | Additional Details |
|-----|-----------------|---|--------------------|
| 0 | RESERVED_01 | RESERVED | FACTORY ONLY |
| 1 | RESERVED_02 | RESERVED | FACTORY ONLY |
| 2 | PGOOD | Output voltage status for linear regulators and DC–DC buck converters | |
| 3 | INTMASK1 | Interrupt request masking settings | |
| 4 | INTMASK2 | Interrupt request masking settings | |
| 5 | INT_ACK1 | Masked interrupt request register, latched | |
| 6 | INT_ACK2 | Masked interrupt request register, latched | |
| 7 | PGOODFAULT_MASK | System Reset masking settings | |
| 8 | SOFT_RESET | Generates a software reset | |
| 9 | CHG_CONFIG | Battery charger configuration | |
| A | CHG_STAT | Battery charger status | |
| B | EN_LDO | Linear regulator ON/OFF control | |
| C | LDO12 | LDO1 and LDO2 output voltage setting | |
| D | LDO3 | LDO3 output voltage settings | |
| E | LDO4 | LDO4 output voltage settings | |
| F | LDO5 | LDO5 output voltage settings | |
| 10 | SM1_SET1 | SM1 Buck converter ON/OFF control and output voltage setting, normal mode | |
| 11 | SM1_SET2 | SM1 Buck converter configuration | |
| 12 | SM1_STANDBY | SM1 Buck converter stand-by mode ON/OFF and stand-by output voltage setting | |
| 13 | SM2_SET1 | SM2 Buck converter ON/OFF control and output voltage setting, normal mode | |
| 14 | SM2_SET2 | SM2 Buck converter configuration | |
| 15 | SM2_STANDBY | SM2 Buck converter stand-by mode ON/OFF and stand-by output voltage setting | |
| 16 | SM3_SET | SM3 White LED driver ON/OFF control and settings | |
| 17 | RGB_FLASH | Overall RGB driver timing settings | |
| 18 | RGB_RED | RGB driver: RED duty cycle and output current setting | |
| 19 | RGB_GREEN | RGB driver: GREEN duty cycle and output current setting | |
| 1A | RGB_BLUE | RGB driver: BLUE duty cycle and output current setting | |
| 1B | GPIO12 | GPIO1 and GPIO2 configuration | |
| 1C | GPIO3 | GPIO2 and GPIO3 configuration, battery charge voltage selection | |
| 1D | PWM | PWM output configuration | |
| 1E | ADC_SET | ADC On/OFF control, ADC configuration | |
| 1F | ADC_reading_hi | ADC data output | |
| 20 | ADC_reading_lo | ADC data output | |
| 21 | DHILIM1 | ADC Maximum threshold setting | |
| 22 | DHILIM2 | ADC Maximum threshold setting | |
| 23 | DLOLIM1 | ADC Minimum threshold setting | |
| 24 | DLOLIM2 | ADC Minimum threshold setting | |
| 25 | ADC_DELAY | ADC configuration: conversion delay | |
| 26 | ADC_WAIT | ADC configuration: wait and repeat operation | |
| 27 | LED_PWM | LED_PWM configuration | |
| 2E | RESERVED_03 | RESERVED | FACTORY ONLY |

8.6.1 Sequencing and Operating Modes – I²C Registers

The I²C registers that control sequencing-related functions are shown in Table 38. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

Table 38. I²C Registers – Sequencing and Operating Modes

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|-----------------------------------|---|----------|----------|--|----------|-------------------------|---|
| Soft_reset, Address = 08, All Bits R/W, Bits B7/B6/B1/B0 Apply to Sequencing. | | | | | | | | |
| Bit Name | STBY MODE | SLEEP MODE | NOT USED | NOT USED | SM3_LF_OSc | NOT USED | nRAMLOAD | SOFT RST |
| Function | SET SM1 AND SM2 IN STANDBY MODE | SET TPS65810 IN SLEEP MODE | NOT USED | NOT USED | NOT RELATED TO SEQUENCING See SM3 SECTION | NOT USED | RAM RESET FLAG | SOFTWARE RESET CONTROL |
| When 0 | NOT ACTIVE | NOT ACTIVE | NOT USED | NOT USED | | NOT USED | RAM DEFAULTS LOADED | NOT ACTIVE |
| When 1 | When 1 SET SM1 AND SM2 IN STANDBY | SET SLEEP MODE (reset to LO internally) | NOT USED | NOT USED | | NOT USED | RAM DEFAULTS NOT LOADED | SET RESET MODE (reset to LO internally) |

Some host algorithms need to identify when the power-up defaults are loaded in the RAM, to start routines that initialize specific RAM registers. If that functionality is required the nRAMLOAD bit must be set to HI by the host when entering the NORMAL operation mode. The nRAMLOAD bit is reset to LO by the TPS65810 when the power-up defaults are loaded in the I²C registers ($V(OUT) < V_{UVLO}$ OR $V(HOT_RESET) = LO$), enabling the host algorithm to detect that the RAM registers need to be initialized.

The integrated supplies status is available in a dedicated register, shown below. The host can select which integrated supply outputs trigger a power-good fault condition using the PGOODFAULT_MASK register. When a non-masked power-good status register bit toggles state, the sequence controller generates a transition in the TPS65810 state machine, indicated as a PGOOD FAULT in TPS65810 state diagram. The power-good status register and mask register are shown below:

Table 39. System Status Monitored By Sequencing Controller

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|-------------------------|-------------------------|-------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| PGOOD, Address = 02, All Bits Read Only - Power Up Defaults Show System Status When Exiting Power Down | | | | | | | | |
| Bit name | PGOOD SM1 | PGOOD SM2 | PGOOD SM3 | PGOOD LDO1 | PGOOD LDO2 | PGOOD LDO3 | PGOOD LDO4 | PGOOD LDO5 |
| Function | SM1 OUTPUT STATUS | SM2 OUTPUT STATUS | SM3 OVP STATUS | LDO1 OUTPUT STATUS | LDO2 OUTPUT STATUS | LDO3 OUTPUT STATUS | LDO4 OUTPUT STATUS | LDO5 OUTPUT STATUS |
| When 0 | OK | OK | OK | OK | OK | OK | OK | OK |
| When 1 | FAULT | FAULT | FAULT | FAULT | FAULT | FAULT | FAULT | FAULT |
| PGOODFAULT_MASK, Address = 07, All Bits R/W | | | | | | | | |
| Bit name | MASK_PSM1 | MASK_PSM2 | MASK_PSM3 | MASK_PLDO1 | MASK_PLDO2 | MASK_PLDO3 | MASK_PLDO4 | MASK_PLDO5 |
| Function | MASK PGOOD FAULT BY SM1 | MASK PGOOD FAULT BY SM2 | MASK PGOOD FAULT BY SM3 | MASK PGOOD FAULT BY LDO1 | MASK PGOOD FAULT BY LDO2 | MASK PGOOD FAULT BY LDO3 | MASK PGOOD FAULT BY LDO4 | MASK PGOOD FAULT BY LDO5 |
| When 0 | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED |
| When 1 | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED |

8.6.2 System Status — I²C Registers

The I²C registers that have system status data are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Those registers are valid, after an initial power up, when the TPS65810 enters the normal operation mode.

Table 40. System Status Monitored By Interrupt Controller

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|-------------------|-------------------|----------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| PGOOD, Address = 02, All Bits Read Only - Power Up Defaults Show System Status When Exiting Power Down | | | | | | | | |
| Bit name | PGOOD SM1 | PGOOD SM2 | PGOOD SM3 | PGOOD LDO1 | PGOOD LDO2 | PGOOD LDO3 | PGOOD LDO4 | PGOOD LDO5 |
| Function | SM1 OUTPUT STATUS | SM2 OUTPUT STATUS | SM3 OVP STATUS | LDO1 OUTPUT STATUS | LDO2 OUTPUT STATUS | LDO3 OUTPUT STATUS | LDO4 OUTPUT STATUS | LDO5 OUTPUT STATUS |
| When 0 | OK | OK | OK | OK | OK | OK | OK | OK |
| When 1 | FAULT | FAULT | FAULT | FAULT | FAULT | FAULT | FAULT | FAULT |
| ADC STATUS | | | | | | | | |
| REGISTER ADC_READING_HI, B7: CONVERSION COMPLETE; INTERNAL STATUS BITS (NO I ² C REGISTER BIT AVAILABLE: INPUT OUT OF RANGE (HI OR LO), ANLG1 PIN IMPEDANCE TO AGND2 EXCEEDS 1 mΩ. See additional details in the Analog-to-Digital Converter section. | | | | | | | | |
| OTHER SYSTEM STATUS: THERMAL FAULT DETECTED | | | | | | | | |

8.6.3 Interrupt Controller – I²C Registers

The I²C registers that control an interrupt generation (INT: HI→LO) are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

Table 41. Interrupt and Power-Good Fault Management Register

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|------------------------------------|-----------------------------------|------------------------------------|------------------------------------|--------------------------------|------------------------------------|--------------------------------------|--------------------------------------|
| INTMASK1, Address = 03, All Bits R/W | | | | | | | | |
| Bit name | MASK_ISM1 | MASK_ISM2 | MASK_ISM3 | MASK_ILDO1 | MASK_ILDO2 | MASK_ILDO3 | MASK_ILDO4 | MASK_ILDO5 |
| Function | MASK INT by SM1 PGOOD FAULT | MASK INT by SM2 PGOOD FAULT | MASK INT by SM3 PGOOD FAULT | MASK INT by LDO1 PGOOD FAULT | MASK INT by LDO2 PGOOD FAULT | MASK INT by LDO3 PGOOD FAULT | MASK INT by LDO4 PGOOD FAULT | MASK INT by LDO5 PGOOD FAULT |
| When 0 | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED |
| When 1 | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED |
| INTMASK2, Address = 04, All Bits R/W | | | | | | | | |
| Bit name | MASK_IADC | MASK_IANLG1 | MASK_IGPIO2 | MASK_IGPIO1 | MASK_ITHSHUT | MASK_ICHGST | MASK_IADCH_I | MASK_IADCL_O |
| Function | MASKS INT BY ADC END OF CONVERSION | MASKS INT BY ANLG1 HIGH IMPEDANCE | MASKS INT BY GPIO2 EDGE TRANSITION | MASKS INT BY GPIO1 EDGE TRANSITION | MASKS INT BY THERMAL FAULT | MASK INT BY CHG_STAT REGISTER BITS | MASK INT BY ADC INPUT ABOVE HI LIMIT | MASK INT BY ADC INPUT BELOW LO LIMIT |
| When 0 | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED |
| When 1 | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED |
| INT_ACK1, Address = 05, All Bits R/W | | | | | | | | |
| Bit name | ACK_SM1 | ACK_SM2 | ACK_SM3 | ACK_LDO1 | ACK_LDO2 | ACK_LDO3 | ACK_LDO4 | ACK_LDO5 |
| Function | SM1 INT REQUEST | SM2 INT REQUEST | SM3 INT REQUEST | LDO1 INT REQUEST | LDO2 INT REQUEST | LDO3 INT REQUEST | LDO4 INT REQUEST | LDO5 INT REQUEST |
| When 0 | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG |
| When 1 | SM1 PGOOD FAULT GENERATED INT | SM2 PGOOD FAULT GENERATED INT | SM3 OVP FAULT GENERATED INT | LDO1 PGOOD FAULT GENERATED INT | LDO2 PGOOD FAULT GENERATED INT | LDO3 PGOOD FAULT GENERATED INT | LDO4 PGOOD FAULT GENERATED INT | LDO5 PGOOD FAULT GENERATED INT |

Table 41. Interrupt and Power-Good Fault Management Register (continued)

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|--------------------------------|--|----------------------------------|----------------------------------|-------------------------------------|---|--|--|
| INT_ACK2, Address = 06, All Bits Read Only | | | | | | | | |
| Bit name | ACK_ADC | ACK_ANLG1 | ACK_GPIO2 | ACK_GPIO1 | ACK_THSHUT | ACK_CHGSTAT | ACK_ADC_HI | ACK_ADC_LO |
| Function | ADC INT REQUEST 1 | ANLG1 COMPARATOR INT REQUEST | GPIO2 INT REQUEST | GPIO1 INT REQUEST | THERMAL FAULT INT REQUEST | CHARGER INT REQUEST | ADC INT REQUEST 2 | ADC INT REQUEST 3 |
| When 0 | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG | CLEAR FLAG |
| When 1 | ADC DONE GENERATED INT REQUEST | ANLG1 HIGH IMPEDANCE DETECTION GENERATED INT REQUEST | GPIO2 EDGE GENERATED INT REQUEST | GPIO1 EDGE GENERATED INT REQUEST | THERMAL FAULT GENERATED INT REQUEST | CHARGER STATUS CHANGE GENERATED INT REQUEST | ADC INPUT ABOVE HI LIMIT GENERATED INT REQUEST | ADC INPUT BELOW LO LIMIT GENERATED INT REQUEST |
| PGOODFAULT_MASK, Address = 07, All Bits R/W | | | | | | | | |
| Bit name | PGOOD SM1 | PGOOD SM2 | PGOOD SM3 | PGOOD LDO1 | PGOOD LDO2 | PGOOD LDO3 | PGOOD LDO4 | PGOOD LDO5 |
| Function | MASK PGOOD FAULT BY SM1 | MASK PGOOD FAULT BY SM2 | MASK PGOOD FAULT BY SM3 | MASK PGOOD FAULT BY LDO1 | MASK PGOOD FAULT BY LDO2 | MASK PGOOD FAULT BY LDO3 | MASK PGOOD FAULT BY LDO4 | MASK PGOOD FAULT BY LDO5 |
| When 0 | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED | UNMASKED |
| When 1 | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED | MASKED |

8.6.4 Charge and System Power Management — I²C Registers

The I²C registers that control charger and power path related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values. Note that the CHG_STAT register contents are valid only when either AC or USB power are applied to the TPS65810. The output of linear regulator LDO_PM can be used as an indicator of external input power detection; if LDO_PM is in regulation the CHG_STAT register contents are valid.

Table 42. CHG_CONFIG Address

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|--------------------------|------------------|----------|---|----------|-------------------|------------------------------------|--------------------------------------|
| CHG_CONFIG, Address = 9, All Bits R/W | | | | | | | | |
| Bit name | VCHG | CHGON | NOT USED | ISSET1_1 | ISSET1_0 | ISSET2 | PSEL | CE ⁽¹⁾ |
| Function | CHARGE VOLTAGE SELECTION | SUSPEND CHARGE | NOT USED | CHARGE CURRENT SCALING FACTOR | | USB CURRENT LIMIT | SELECTED INPUT CURRENT LIMIT | SYSTEM POWER SELECTION |
| When 0 | 4.36 V | CHARGE SUSPENDED | NOT USED | 00= 0.25 10=0.75 01= 0.5 11= 1 Note: Relative to charge current programmed by external ISET pin resistor. | | 100 mA | USE USB CURRENT LIMIT | BATTERY TO SYSTEM |
| When 1 | 4.20 V | CHARGE ON | NOT USED | | | 500 mA | INPUT CURRENT LIMIT SET TO MAXIMUM | INPUT POWER TO SYSTEM ⁽¹⁾ |

- (1) The CE bit state is latched inside the charger control logic (CE latch) during an OUT pin UVLO event, prior to resetting the charge control register bit CE to its power up default value. The charger CE latch controls the charger and power path state as long as the TPS65810 is in UVLO mode and an external supply is connected to the charger block. The CE latch is reset to its power-up value (CE = HI) only when the input power is removed from the charger block. The CE latch is disabled and the CE charge control register bit sets the charger and power path MOSFETs state when the TPS65810 exits the UVLO mode. This feature avoids a host software loop when the host algorithm requires a depleted (or absent) battery to be connected to the system bus while input power is present.

Table 43. GPIO3 Address

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|--------------|--------------|--------------|-------------------------------------|----------|--------------|--------------|--------------|
| GPIO3, Address = 1C, All Bits R/W⁽¹⁾ | | | | | | | | |
| Bit name | GPIO3i/O | GPIO3_LEVEL | LDO0_ENABLE | CHARGE_VLTG | NOT USED | GPIO2_INTSRC | GPIO1_INTSRC | GPIO2_SM2 |
| Function | See Table 23 | See Table 23 | See Table 23 | CHARGE VOLTAGE SELECTION SAFETY BIT | NOT USED | See Table 23 | Table 23 | See Table 23 |
| When 0 | | | | 4.2 V | | | | |
| When 1 | | | | 4.36 V | | | | |

(1) Only bit B4 controls charger-related functionality

Table 44. CHG_STAT Address

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|--------------------------------|-----------------------------|------------------------------|-----------------------|------------------------|---|-------|-------------------------------|
| CHG_STAT, Address = A, All Bits Read Only– Power Up Defaults Show System Status When Exiting Power Down | | | | | | | | |
| Bit name | BAT_STAT ^{(1) (2)} | INPUT_PWR | THDPPM_ON | ACPG ⁽³⁾ | USBPG ⁽³⁾ | STAT1 | STAT2 | INP_OV |
| Function | BATTERY SUPPLEMENT MODE STATUS | SELECTED INPUT POWER STATUS | THERMAL LOOP AND DPPM STATUS | AC INPUT POWER STATUS | USB INPUT POWER STATUS | CHARGE STATUS | | AC OR USB INPUT OVP DETECTION |
| When 0 | SUPPLEMENT MODE OFF | AC INPUT SELECTED | BOTH OFF | AC NOT DETECTED | USB NOT DETECTED | 00 = FAULT/SUSPEND/OFF 01 = CHARGE DONE 10 = FAST CHARGE ON 11 = PRECHARGE | | NO OVP |
| When 1 | SUPPLEMENT MODE ON | USB INPUT SELECTED | DPPM ON OR THERMAL ON | AC DETECTED | USB DETECTED | | | OVP DETECTED |

- (1) The battery supplement is entered when $V_{(BAT)} - V_{(OUT)} > 60$ mV (typical), and it ends when $V_{(BAT)} - V_{(OUT)} < 20$ mV. When the system power bus current exceeds the input current limit or the external supply current capability, the supplement mode is set. An oscillatory behavior for BAT_STAT bit can happen if the battery switch dropout voltage is less than 20 mV (typical) when in supplement mode.
- (2) The BAT_STAT is always masked internally, and does not generate interrupts.
- (3) The ACPG and USBPG bits have valid data only when $V_{(LDO_PM)} > 2$ V.

8.6.5 Linear Regulators — I²C Registers

The I²C registers that control LDO-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

Table 45. Linear Regulators Registers

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------------------------------|-------------------------------------|--|--|------------------|-------------------------------------|--|--|-----------------|
| EN_LDO: Address = B, All Bits R/W | | | | | | | | |
| Bit name | LDO1_EN | LDO2_EN | LDO3_EN | LDO4_EN | LDO5_EN | SIM_SET | SIM_EN1 | RTC_EN |
| Function | LDO1...5 ON/OFF CONTROL | | | | | SIM LDO output voltage | SIM/RTC ON/OFF CONTROL | |
| When 0 | OFF | OFF | OFF | OFF | OFF | 2.5 V, ON | OFF | OFF |
| When 1 | ON | ON | ON | ON | ON | 1.8 V | ON | ON |
| LDO12: Address = C, All Bits R/W | | | | | | | | |
| Bit name | LDO1_DISCH | LDO1_2 SET | LDO1_1 SET | LDO1_0 SET | LDO2_DISCH | LDO2_2 SET | LDO2_1 SET | LDO2_0 SET |
| Function | LDO1 output discharge switch enable | LDO1 OUTPUT VOLTAGE SETTING | | | LDO2 output discharge switch enable | LDO2 OUTPUT VOLTAGE SETTING | | |
| When 0 | OFF | 000 = 1.25 V 010 = 1.8 V 100 = 2.85 V 110 = 3.2 V | 001 = 1.5 V 011 = 2.5 V 110 = 3 V 111 = 3.3 V | Default = 1.25 V | OFF | 000 = 1.25 V 010 = 1.8 V 100 = 2.85 V 110 = 3.2 V | 001 = 1.5 V 011 = 2.5 V 110 = 3 V 111 = 3.3 V | Default = 3.3 V |
| When 1 | ON | | | | ON | | | |
| LDO3, Address = D, All Bits R/W | | | | | | | | |
| Bit name | LDO3_DISCH | LDO3_6 SET | LDO3_5 SET | LDO3_4 SET | LDO3_3 SET | LDO3_2 SET | LDO3_1 SET | LDO3_0 SET |
| Function | LDO3 output discharge switch enable | LDO3 OUTPUT VOLTAGE SETTING | | | | | | |
| When 0 | OFF | See Table 46 for LDO3-5 output voltage setting, Power-up default = 1.505 V | | | | | | |
| When 1 | ON | | | | | | | |

Table 45. Linear Regulators Registers (continued)

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|-------------------------------------|---|---------------------|------------------------------|------------|------------------------------|------------------------------|------------------------------|
| LDO4, Address = E, All Bits R/W | | | | | | | | |
| Bit name | LDO4_DISCH | LDO4_6 SET | LDO4_5 SET | LDO4_4 SET | LDO4_3 SET | LDO4_2 SET | LDO4_1 SET | LDO4_0 SET |
| Function | LDO4 output discharge switch enable | LDO4 OUTPUT VOLTAGE SETTING | | | | | | |
| When 0 | OFF | See Table 46 for LDO3-5 output voltage setting, Power-up default = 1.811 V | | | | | | |
| When 1 | ON | | | | | | | |
| LDO5, Address = F, All Bits R/W | | | | | | | | |
| Bit name | LDO5_DISCH | LDO5_6 SET | LDO5_5 SET | LDO5_4 SET | LDO5_3 SET | LDO5_2 SET | LDO5_1 SET | LDO5_0 SET |
| Function | LDO5 output discharge switch enable | LDO5 OUTPUT VOLTAGE SETTING | | | | | | |
| When 0 | OFF | See Table 46 for LDO3-5 output voltage setting, Power-up default = 3.111 V | | | | | | |
| When 1 | ON | | | | | | | |
| GPIO3, Address = 1C, All Bits R/W. NOTE: ONLY BIT B5 CONTROLS LDO-RELATED FUNCTIONALITY | | | | | | | | |
| Bit name | GPIO3i/O | GPIO3 LEVEL | LDO0 ENABLE | CHARGE_VLTG | NOT USED | GPIO2_INTSRC | GPIO1_INTSRC | GPIO2_SM2 |
| Function | See Table 23 | See Table 23 | LDO0 ON/OFF CONTROL | See Table 23 | NOT USED | See Table 23 | See Table 23 | See Table 23 |
| When 0 | | | LDO0 OFF | | | | | |
| When 1 | | | LDO0 ON | | | | | |

Table 46. LDO 3–5 Programming Step Values

| Step | B6–B0 | Vset | Step | B6–B0 | Vset | Step | B6–B0 | Vset | Step | B6–B0 | Vset |
|------|----------|-------|------|----------|-------|------|----------|-------|------|----------|-------|
| 0 | 000 0000 | 1.224 | 32 | 010 0000 | 2.040 | 64 | 100 0000 | 2.015 | 96 | 110 0000 | 2.856 |
| 1 | 000 0001 | 1.250 | 33 | 010 0001 | 2.066 | 65 | 100 0001 | 2.040 | 97 | 110 0001 | 2.882 |
| 2 | 000 0010 | 1.275 | 34 | 010 0010 | 2.091 | 66 | 100 0010 | 2.907 | 98 | 110 0010 | 3.723 |
| 3 | 000 0011 | 1.301 | 35 | 010 0011 | 2.117 | 67 | 100 0011 | 2.933 | 99 | 110 0011 | 3.749 |
| 4 | 000 0100 | 1.326 | 36 | 010 0100 | 2.142 | 68 | 100 0100 | 2.958 | 100 | 110 0100 | 3.774 |
| 5 | 000 0101 | 1.352 | 37 | 010 0101 | 2.168 | 69 | 100 0101 | 2.984 | 101 | 110 0101 | 3.800 |
| 6 | 000 0110 | 1.377 | 38 | 010 0110 | 2.193 | 70 | 100 0110 | 3.009 | 102 | 110 0110 | 3.825 |
| 7 | 000 0111 | 1.403 | 39 | 010 0111 | 2.219 | 71 | 100 0111 | 3.035 | 103 | 110 0111 | 3.851 |
| 8 | 000 1000 | 1.428 | 40 | 010 1000 | 2.244 | 72 | 100 1000 | 3.060 | 104 | 110 1000 | 3.876 |
| 9 | 000 1001 | 1.454 | 41 | 010 1001 | 2.270 | 73 | 100 1001 | 3.086 | 105 | 110 1001 | 3.902 |
| 10 | 000 1010 | 1.479 | 42 | 010 1010 | 2.295 | 74 | 100 1010 | 3.111 | 106 | 110 1010 | 3.927 |
| 11 | 000 1011 | 1.505 | 43 | 010 1011 | 2.321 | 75 | 100 1011 | 3.137 | 107 | 110 1011 | 3.953 |
| 12 | 000 1100 | 1.530 | 44 | 010 1100 | 2.346 | 76 | 100 1100 | 3.162 | 108 | 110 1100 | 3.978 |
| 13 | 000 1101 | 1.556 | 45 | 010 1101 | 2.372 | 77 | 100 1101 | 3.188 | 109 | 110 1101 | 4.004 |
| 14 | 000 1110 | 1.581 | 46 | 010 1110 | 2.397 | 78 | 100 1110 | 3.213 | 110 | 110 1110 | 4.029 |
| 15 | 000 1111 | 1.607 | 47 | 010 1111 | 2.423 | 79 | 100 1111 | 3.239 | 111 | 110 1111 | 4.055 |
| 16 | 001 0000 | 1.632 | 48 | 011 0000 | 2.448 | 80 | 101 0000 | 3.264 | 112 | 111 0000 | 4.080 |
| 17 | 001 0001 | 1.658 | 49 | 011 0001 | 2.474 | 81 | 101 0001 | 3.290 | 113 | 111 0001 | 4.106 |
| 18 | 001 0010 | 1.683 | 50 | 011 0010 | 2.499 | 82 | 101 0010 | 3.315 | 114 | 111 0010 | 4.131 |
| 19 | 001 0011 | 1.709 | 51 | 011 0011 | 2.525 | 83 | 101 0011 | 3.341 | 115 | 111 0011 | 4.157 |
| 20 | 001 0100 | 1.734 | 52 | 011 0100 | 2.550 | 84 | 101 0100 | 3.366 | 116 | 111 0100 | 4.182 |
| 21 | 001 0101 | 1.760 | 53 | 011 0101 | 2.576 | 85 | 101 0101 | 3.392 | 117 | 111 0101 | 4.208 |
| 22 | 001 0110 | 1.785 | 54 | 011 0110 | 2.601 | 86 | 101 0110 | 3.417 | 118 | 111 0110 | 4.233 |
| 23 | 001 0111 | 1.811 | 55 | 011 0111 | 2.627 | 87 | 101 0111 | 3.443 | 119 | 111 0111 | 4.259 |
| 24 | 001 1000 | 1.836 | 56 | 011 1000 | 2.652 | 88 | 101 1000 | 3.468 | 120 | 111 1000 | 4.284 |
| 25 | 001 1001 | 1.862 | 57 | 011 1001 | 2.678 | 89 | 101 1001 | 3.494 | 121 | 111 1001 | 4.310 |
| 26 | 001 1010 | 1.887 | 58 | 011 1010 | 2.703 | 90 | 101 1010 | 3.519 | 122 | 111 1010 | 4.335 |
| 27 | 001 1011 | 1.913 | 59 | 011 1011 | 2.729 | 91 | 101 1011 | 3.545 | 123 | 111 1011 | 4.361 |
| 28 | 001 1100 | 1.938 | 60 | 011 1100 | 2.754 | 92 | 101 1100 | 3.570 | 124 | 111 1100 | 4.386 |
| 29 | 001 1101 | 1.964 | 61 | 011 1101 | 2.780 | 93 | 101 1101 | 3.596 | 125 | 111 1101 | 4.412 |
| 30 | 001 1110 | 1.989 | 62 | 011 1110 | 2.805 | 94 | 101 1110 | 3.621 | 126 | 111 1110 | 4.437 |
| 31 | 001 1111 | 2.015 | 63 | 011 1111 | 2.831 | 95 | 101 1111 | 3.647 | 127 | 111 1111 | 4.463 |

8.6.6 Switched-Mode Step-Down Converters — I²C Registers

The I²C registers that control buck converter-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

Table 47. Switched-Mode Step-Down Converters Registers

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|-----------------------|----------------------------|------------------------------------|---|--|------------------------------|-------------|-------------|
| SM1_SET1, Address = 10, All Bits R/W | | | | | | | | |
| Bit name | SM1 EN | PFM_RPL1 | PFM_SM1 | SetV4_SM1 | SetV3_SM1 | SetV2_SM1 | SetV1_SM1 | SetV0_SM1 |
| Function | SM1 ON/OFF CONTROL | SM1 PFM FUNCTION OPERATION | SM1 PFM MODE ON/OFF CTRL | SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE NOT SET | | | | |
| When 0 | OFF | MAXIMIZE EFFICIENCY | PWM/PFM | See Table 48 for SM1, SM2 voltage setting, Power up default=1.24 V | | | | |
| When 1 | ON | MINIMIZE OUTPUT RIPPLE | Only PWM | | | | | |
| SM1_SET2, Address = 11, All Bits R/W | | | | | | | | |
| Bit name | NOT USED | STANDBY_SM1 | DISCHSM1 | S1S2PHASE_1 | S1S2PHASE_0 | SLEWSM1_2 | SLEWSM1_1 | SLEWSM1_0 |
| Function | NOT USED | SM1 STANDBY MODE ON | SM1 output discharge switch enable | SM2 PWM CLOCK DELAY, WITH RESPECT TO SM1 PWM CLOCK | | SM1 OUTPUT SLEW RATE SETTING | | |
| When 0 | NOT USED | OFF | OFF | 00 = 0° 01 = 90° | 10 = 180° 11 = 270° Default = 180° | 000 = 0.24 | 010 = 0.96 | 100 = 5.84 |
| When 1 | NOT USED | ON | ON | | | 001 = 0.48 | 011 = 1.92 | 101 = 7.68 |
| Unit: mV/μs Default= 15.36 | | | | | | | | |
| SM1_STANDBY, Address = 12, B4-B0 R/W, B7-B5 Read Only | | | | | | | | |
| Bit name | GPIO3LVL | GPIO2LVL | GPIO1LVL | SetV4_SM1SL | SetV3_SM1SL | SetV2_SM1SL | SetV1_SM1SL | SetV0_SM1SL |
| Function | GPIO3 pin logic level | GPIO2 pin logic level | GPIO1 pin logic level | SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE SET | | | | |
| When 0 | LO | LO | LO | See Table 48 for SM1, SM2 voltage setting, Power-up default = 1.24 V | | | | |
| When 1 | HI | HI | HI | | | | | |
| SM2_SET1, Address = 13, All Register Bits R/W | | | | | | | | |
| Bit name | SM2 EN | PFM_RPL2 | PFM_SM2 | SetV4_SM2 | SetV3_SM2 | SetV2_SM2 | SetV1_SM2 | SetV0_SM2 |
| Function | SM2 ON/OFF CONTROL | SM2 PFM FUNCTION OPERATION | SM2 PFM MODE ON/OFF CTRL | SM2 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE NOT SET | | | | |
| When 0 | OFF | MAXIMIZE EFFICIENCY | PWM/PFM | See Table 48 for SM1, SM2 voltage setting, Power-up default = 3.32 V | | | | |
| When 1 | ON | MINIMIZE OUTPUT RIPPLE | ONLY PWM | | | | | |
| SM2_SET2, Address = 14, All Register Bits R/W | | | | | | | | |
| Bit name | NOT USED | STANDBY_SM2 | DISCHSM2 | NOT USED | NOT USED | SLEWSM2_2 | SLEWSM2_1 | SLEWSM2_0 |
| Function | NOT USED | SM2 STANDBY MODE ON | SM2 output discharge switch enable | NOT USED | NOT USED | SM2 OUTPUT SLEW RATE SETTING | | |
| When 0 | NOT USED | OFF | OFF | NOT USED | NOT USED | 000 = 0.48 | 010 = 1.92 | 100 = 7.68 |
| When 1 | NOT USED | ON | ON | NOT USED | NOT USED | 110 = 30.72 | 001 = 0.096 | 011 = 3.84 |
| 101 = 15.36 111 = IMMEDIATE Unit: mV/μs Default = 30.72 | | | | | | | | |
| SM2_STANDBY, Address = 15, All Register Bits R/W | | | | | | | | |
| Bit name | NOT USED | NOT USED | NOT USED | SetV4_SM2SL | SetV3_SM2SL | SetV2_SM2SL | SetV1_SM2SL | SetV0_SM2SL |
| Function | NOT USED | NOT USED | NOT USED | SM1 OUTPUT VOLTAGE REGULATION VALUE, STANDBY MODE SET | | | | |
| When 0 | NOT USED | NOT USED | NOT USED | See Table 48 for SM1, SM2 voltage setting, Power up default=3.32 V | | | | |
| When 1 | NOT USED | NOT USED | NOT USED | | | | | |

Table 48. Programmable Settings for SM1 and SM2 (Including STANDBY)

| SetV4_ SM | SetV3_ SM | SetV2_ SM | SetV1_ SM | SetV0_ SM | Vset SM1 | Vset SM2 | SetV4_ SM | SetV3_ SM | SetV2_ SM | SetV1_ SM | SetV0_ SM | Vset SM1 | Vset SM2 |
|-----------|-----------|-----------|-----------|-----------|----------|----------|-----------|-----------|-----------|-----------|-----------|----------|----------|
| 0 | 0 | 0 | 0 | 0 | 0.6 | 1 | 1 | 0 | 0 | 0 | 0 | 1.24 | 2.28 |
| 0 | 0 | 0 | 0 | 1 | 0.64 | 1.08 | 1 | 0 | 0 | 0 | 1 | 1.28 | 2.36 |
| 0 | 0 | 0 | 1 | 0 | 0.68 | 1.16 | 1 | 0 | 0 | 1 | 0 | 1.32 | 2.44 |
| 0 | 0 | 0 | 1 | 1 | 0.72 | 1.24 | 1 | 0 | 0 | 1 | 1 | 1.36 | 2.52 |
| 0 | 0 | 1 | 0 | 0 | 0.76 | 1.32 | 1 | 0 | 1 | 0 | 0 | 1.4 | 2.6 |
| 0 | 0 | 1 | 0 | 1 | 0.8 | 1.4 | 1 | 0 | 1 | 0 | 1 | 1.44 | 2.68 |
| 0 | 0 | 1 | 1 | 0 | 0.84 | 1.48 | 1 | 0 | 1 | 1 | 0 | 1.48 | 2.76 |
| 0 | 0 | 1 | 1 | 1 | 0.88 | 1.56 | 1 | 0 | 1 | 1 | 1 | 1.52 | 2.84 |
| 0 | 1 | 0 | 0 | 0 | 0.92 | 1.64 | 1 | 1 | 0 | 0 | 0 | 1.56 | 2.92 |
| 0 | 1 | 0 | 0 | 1 | 0.96 | 1.72 | 1 | 1 | 0 | 0 | 1 | 1.6 | 3 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1.8 | 1 | 1 | 0 | 1 | 0 | 1.64 | 3.08 |
| 0 | 1 | 0 | 1 | 1 | 1.04 | 1.88 | 1 | 1 | 0 | 1 | 1 | 1.68 | 3.16 |
| 0 | 1 | 1 | 0 | 0 | 1.08 | 1.96 | 1 | 1 | 1 | 0 | 0 | 1.72 | 3.24 |
| 0 | 1 | 1 | 0 | 1 | 1.12 | 2.04 | 1 | 1 | 1 | 0 | 1 | 1.76 | 3.32 |
| 0 | 1 | 1 | 1 | 0 | 1.16 | 2.12 | 1 | 1 | 1 | 1 | 0 | 1.8 | 3.4 |
| 0 | 1 | 1 | 1 | 1 | 1.2 | 2.2 | 1 | 1 | 1 | 1 | 1 | 0.6 | 1 |

Table 49. Programmable Settings for SM1 and SM2 Phase and Slew Rate

| SM1, SM2 PHASE | | | SMX_SLEW RATE, SMX = SM1 OR SM2 | | | | |
|----------------|-------------|-------|---------------------------------|---------|---------|-----------|-----------|
| S1S2_PHASE1 | S1S2_PHASE0 | PHASE | SLEWX_2 | SLEWX_1 | SLEWX_0 | SM1 mV/μs | SM2 mV/μs |
| 0 | 0 | 0° | 0 | 0 | 0 | 0.24 | 0.48 |
| 0 | 1 | 90° | 0 | 0 | 1 | 0.48 | 0.96 |
| 1 | 0 | 180° | 0 | 1 | 0 | 0.96 | 1.92 |
| 1 | 1 | 270° | 0 | 1 | 1 | 1.92 | 3.84 |
| | | | 1 | 0 | 0 | 3.84 | 7.68 |
| | | | 1 | 0 | 1 | 7.68 | 15.36 |
| | | | 1 | 1 | 0 | 15.36 | 30.72 |
| | | | 1 | 1 | 1 | Immediate | |

8.6.7 ADC – I²C Registers

The I²C registers that control ADC-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Default, initial power-up values are shown in bold. In the timing equations, replace Bn with 1 for HI state, and 0 for LO state.

Table 50. ADC Registers

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--|---------------------------|-------------------------|--|---|---|-------------------------------|----------------------------------|---------------------------------------|
| ADC_SET, Address = 1E, All Bits R/W | | | | | | | | |
| Bit Name | ADC_ENABLE | ADC_REF_EN | CHSEL2_SET | CHSEL1_SET | CHSEL0_SET | READ_MODE2 | READ_MODE1 | READ_MODE0 |
| Function | ADC ON/OFF CONTROL | ADC REFERENCE SELECTION | ADC CHANNEL SELECTION | | | ADC SAMPLING SETTINGS | | |
| When 0 | OFF | Internal | 000 = ANLG1 001 = ANLG2 010 = V(ISET1) | 011 = V(TS) 100 = Tj 101 = V(RTC_OUT) | 110 = V(OUT) 111 = V(BAT) Default = ANLG1 | 000 = 1 001 = 4 010 = 8 | 011 = 16 100 = 32 101 = 64 | 110 = 128 111 = 256 Default = 1 |
| When 1 | ON | External | | | | | | |
| ADC_READING_HI, Address = 1F, Bits B3/B4 R/W, All Other Bits Read Only | | | | | | | | |
| Bit Name | ADC_STATUS | NOT USED | NOT USED | ADC_READ1 | ADC_READ0 | D10 | D9_MSB | D8 |
| Function | CURRENT CONVERSION STATUS | NOT USED | NOT USED | ALU OUTPUT DATA SELECTION | | ADC AVERAGE CARRYOVER BIT | ADC CONVERSION OUTPUT BITS | |

Table 50. ADC Registers (continued)

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|--------------------------|--|--|--|--|---|-------------|
| When 0 | DONE | NOT USED | NOT USED | 00=LAST 10 = MAXIMUM 01=AVERAGE 11 = MINIMUM Default= LAST | | | VALID ONLY AFTER ADC CONVERSION ENDS SEE ADC_READING_LO | |
| When 1 | BUSY | NOT USED | NOT USED | | | | | |
| ADC_READING_LO, Address = 20, Read Only | | | | | | | | |
| Bit Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0_LSB |
| Function | ADC CONVERSION OUTPUT BITS, VALID ONLY AFTER ADC CONVERSION ENDS | | | | | | | |
| Value | VALUE=[B10*512 + B9*256 + B8*128 + B7*64 + B6*32 + B5*16 + B4*8 + B3*4 + B2*2 + B1] * [VRNG(CHn) / 1023]; Unit=Volts, The LSB bit value is proportional to the ADC reference voltage - See V _{RNG(CHn)} in electrical parameters | | | | | | | |
| DHILIM1, Address = 21, All Bits R/W | | | | | | | | |
| Bit Name | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | DHILIM10 | DHILIM9 | DHILIM8 |
| Function | RESERVED | | | | | ADC MAX INPUT LIMIT RANGE SETTING (3 MSBs) | | |
| DHILIM2, Address = 22, All Bits R/W | | | | | | | | |
| Bit Name | DHILIM7 | DHILIM6 | DHILIM5 | DHILIM4 | DHILIM3 | DHILIM2 | DHILIM1 | DHILIM0_LSB |
| Function | ADC MAX INPUT LIMIT RANGE SETTING (8 LSBs) | | | | | | | |
| DLOLIM1, Address = 23, All Bits R/W | | | | | | | | |
| Bit Name | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | DLOLIM10 | DLOLIM9 | DLOLIM8 |
| Function | RESERVED | | | | | ADC MIN INPUT LIMIT RANGE SETTING (3 MSBs) | | |
| DLOLIM2, Address = 24, All Bits R/W | | | | | | | | |
| Bit Name | DLOLIM7 | DLOLIM6 | DLOLIM5 | DLOLIM4 | DLOLIM3 | DLOLIM2 | DLOLIM1 | DLOLIM0_LSB |
| Function | ADC MIN INPUT LIMIT RANGE SETTING (8 LSBs) | | | | | | | |
| ADC_DELAY, Address = 25, All Bits R/W | | | | | | | | |
| Bit Name | ADC_TRG_GPIO3 | EDGE_GPIO3 | HOLDOFF | REPEAT | Delay_3 | Delay_2 | Delay_1 | Delay_0 |
| Function | USE GPIO3 AS ADC TRIGGER | GPIO3 TRIGGER MODE | ADC HOLDOFF ON/OFF CONTROL | REPEAT MODE ON/OFF | ADC EXTERNAL TRIGGER DELAY SETTING | | | |
| When 0 | OFF | Falling Edge | OFF | OFF | t _{DLY(TRIG)} = B4*400 + B3 * 200 + B2*100 + B1* 50, Units = μs Default = 0 μs | | | |
| When 1 | ON | Rising Edge | ON | ON | | | | |
| ADC_WAIT, Address = 26, All Bits R/W | | | | | | | | |
| Bit Name | ADC_ch2I_D1 | ADC_ch2I_D0 | BATIDI_D1 | BATIDI_D0 | WAIT_D3 | WAIT_D2 | WAIT_D1 | WAIT_LSB |
| Function | ANLG2 PULL-UP CURRENT SOURCE VALUE | | ANLG1 PULL-UP CURRENT SOURCE VALUE | | ADC SAMPLE WAIT TIME, MULTIPLE SAMPLES MODE | | | |
| When 0 | 11:60 μA, 10:50 μA, 01:10 μA,00: 0 Default= 00 | | 11:60 μA, 10:50 μA, 01:10 μA, 00: WEAK PULL UP Default: 00 | | 0000 = 0 | 0100 = 0.08 | 1000 = 0.64 | 1100 = 5.12 |
| 0001 = 0.02 | | | | | 0101 = 0.16 | 1001 = 1.28 | 1101 = 10.24 | |
| 0010 = 0.04 | | | | | 0110 = 0.24 | 1010 = 1.92 | 1110 = 15.36 | |
| 0011 = 0.06 | | | | | 0111 = 0.32 | 1011 = 2.56 | 1111 = 20.48 | |
| When 1 | | | | | Units = ms | | | Default = 0 |

8.6.8 White LED, PWM Drivers — I²C Registers

The I²C registers that control LED AND PWM driver related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values. In the equations replace Bn with 1 for HI state, and 0 for LO state.

Table 51. White LED, PWM Drivers Registers

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------------------------------------|--|---|---|--|---|------------|------------|------------|
| SM3_SET, Address = 16, All Bits R/W | | | | | | | | |
| Bit Name | SM3_I7 set | SM3_I6 set | SM3_I5 set | SM3_I4 set | SM3_I3 set | SM3_I2 set | SM3_I1 set | SM3_I0 set |
| Function | SM3 DUTY CYCLE CONTROL | | | | | | | |
| Value | See Table 19 for SM3 duty cycle settings, default = 0 (OFF) | | | | | | | |
| RGB_FLASH, Address = 17, All Bits R/W | | | | | | | | |
| Bit Name | FLASH_EN | FLASH_ON2 | FLASH_ON1 | FLASH_ON0 | FLASH_PER3 | FLASH_PER2 | FLASH_PER1 | FLASH_PER0 |
| Function | FLASH MODE ON/OFF CTRL | FLASH MODE ON TIME | | | FLASH MODE PERIOD | | | |
| When 0 | OFF | See Table 20 for RGB ON TIME settings, default = 0.1 | | | See Table 20 for RGB FLASH settings, default = 1 | | | |
| When 1 | ON | | | | | | | |
| RGB_RED, Address = 18, All Bits R/W | | | | | | | | |
| Bit Name | RGB_ISET1 | RGB_ISET0 | PHASE | PWMR_D4 | PWMR_D3 | PWMR_D2 | PWMR_D1 | PWMR_D0 |
| Function | RGB LED CURRENT SETTINGS | | PHASE CONTROL | REG DRIVER DUTY CYCLE CONTROL | | | | |
| When 0 | 00= 0 10= 8 mA 01= 4 mA 11=12 mA | | GREEN out of Φ with RED & BLUE | See Table 20 for RGB_RED DUTY settings, default = 0 | | | | |
| When 1 | | | BLUE out of Φ with RED & GREEN | | | | | |
| RGB_GREEN, Address = 19, All Bits R/W | | | | | | | | |
| Bit Name | NOT USED | NOT USED | NOT USED | PWMG_D4 | PWMG_D3 | PWMG_D2 | PWMG_D1 | PWMG_D0 |
| Function | NOT USED | NOT USED | NOT USED | GREEN DRIVER DUTY CYCLE CONTROL | | | | |
| Value | NOT USED | NOT USED | NOT USED | See Table 20 for RGB_GREEN DUTY settings, default = 0 | | | | |
| RGB_BLUE, Address = 1A, All Bits R/W | | | | | | | | |
| Bit Name | NOT USED | NOT USED | NOT USED | PWMB_D4 | PWMB_D3 | PWMB_D2 | PWMB_D1 | PWMB_D0 |
| Function | NOT USED | NOT USED | NOT USED | BLUE DRIVER DUTY CYCLE CONTROL | | | | |
| Value | NOT USED | NOT USED | NOT USED | See Table 20 for RGB_BLUE DUTY settings, default = 0 | | | | |
| PWM, Address = 1D, All Bits R/W | | | | | | | | |
| Bit Name | PWM_EN | PWM1_F2 | PWM_F1 | PWM_F0 | PWM_D3 | PWM_D2 | PWM_D1 | PWM_D0 |
| Function | PWM ON/OFF CONTROL | PWM DRIVER FREQUENCY SETTINGS | | | PWM DRIVER DUTY CYCLE SETTINGS | | | |
| When 0 | Disabled | 000 = 15.6 kHz 001 = 7.8 kHz 010 = 4.5 kHz | 011 = 3 kHz 100 = 2 kHz 101 = 1.5 kHz | 110 = 1 kHz 111 = 500 Hz Default = 15.6 kHz | See Table 21 for PWM DUTY settings, default = 0.0625 | | | |
| When 1 | Enabled | | | | | | | |
| LED_PWM, Address = 27, All Bits R/W | | | | | | | | |
| Bit Name | LPWM_7 set | LPWM_6 set | LPWM_5 set | LPWM_4 set | LPWM_3 set | LPWM_2 set | LPWM_1 set | LPWM_0 set |
| Function | LED_PWM DRIVER DUTY CYCLE CONTROL | | | | | | | |
| Value | See Table 19 for LED_PWM DUTY settings, default = 0 (OFF) | | | | | | | |

8.6.9 GPIOs — I²C Registers

The I²C registers that control GPIO-related functions are shown below. The HEX address for each register is shown by the register name, together with the R or W functionality for the register bits. Shaded values indicate default initial power-up values.

Table 52. GPIOs Registers

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|------------|-------------------------------|-------------------------------|-------------------------------|--------------------------------|--------------------------------|--|---------------------------|
| GPIO12, Address = 1B, All Bits R/W | | | | | | | | |
| Bit Name | GPIO2I/O | GPIO1I/O | GPIO2OUT | GPIO1OUT | GPIO2LVL | GPIO1LVL | GPIO1SMSBY | GPIO1SM1 |
| Function | GPIO2 MODE | GPIO1 MODE | SET GPIO2 LEVEL (OUTPUT ONLY) | SET GPIO1 LEVEL (OUTPUT ONLY) | GPIO2 EDGE AND LEVEL DETECTION | GPIO1 EDGE AND LEVEL DETECTION | GPIO 1 CONTROLS SM1 AND SM2 STANDBY ON/OFF | GPIO1 CONTROLS SM1 ON/OFF |
| When 0 | INPUT | INPUT | LOW | LOW | RISING EDGE, LO LEVEL | RISING EDGE, LO LEVEL | DISABLED | DISABLED |
| When 1 | OUTPUT | OUTPUT | HIGH | HIGH | FALLING EDGE, HI LEVEL | FALLING EDGE, HI LEVEL | ENABLED | ENABLED |
| GPIO3, Address = 1C, All Bits R/W | | | | | | | | |
| Bit Name | GPIO3I/O | GPIO3OUT | LDO0_EN | CHG_VOLT | NOT USED | GPIO2 INT | GPIO1 INT | GPIO2SM2 |
| Function | GPIO3 MODE | SET GPIO3 LEVEL (OUTPUT ONLY) | LDO0 ON/OFF CONTROL | CHARGE VOLTAGE SAFETY BIT | NOT USED | GPIO2 TRIGGERS INT:HI→LO | GPIO1 TRIGGERS INT:HI→LO | SM2 ON/OFF CONTROL |
| When 0 | INPUT | LOW | OFF | 4.20 V | NOT USED | DISABLED | DISABLED | DISABLED |
| When 1 | OUTPUT | HIGH | ON | 4.36 V | NOT USED | ENABLED | ENABLED | ENABLED |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The target application for this device is a smart phone operated from a single Lithium Ion battery that can be recharged from either a USB port or an AC adaptor.

9.2 Typical Applications

9.2.1 SM1, SM2 Converter Design Example

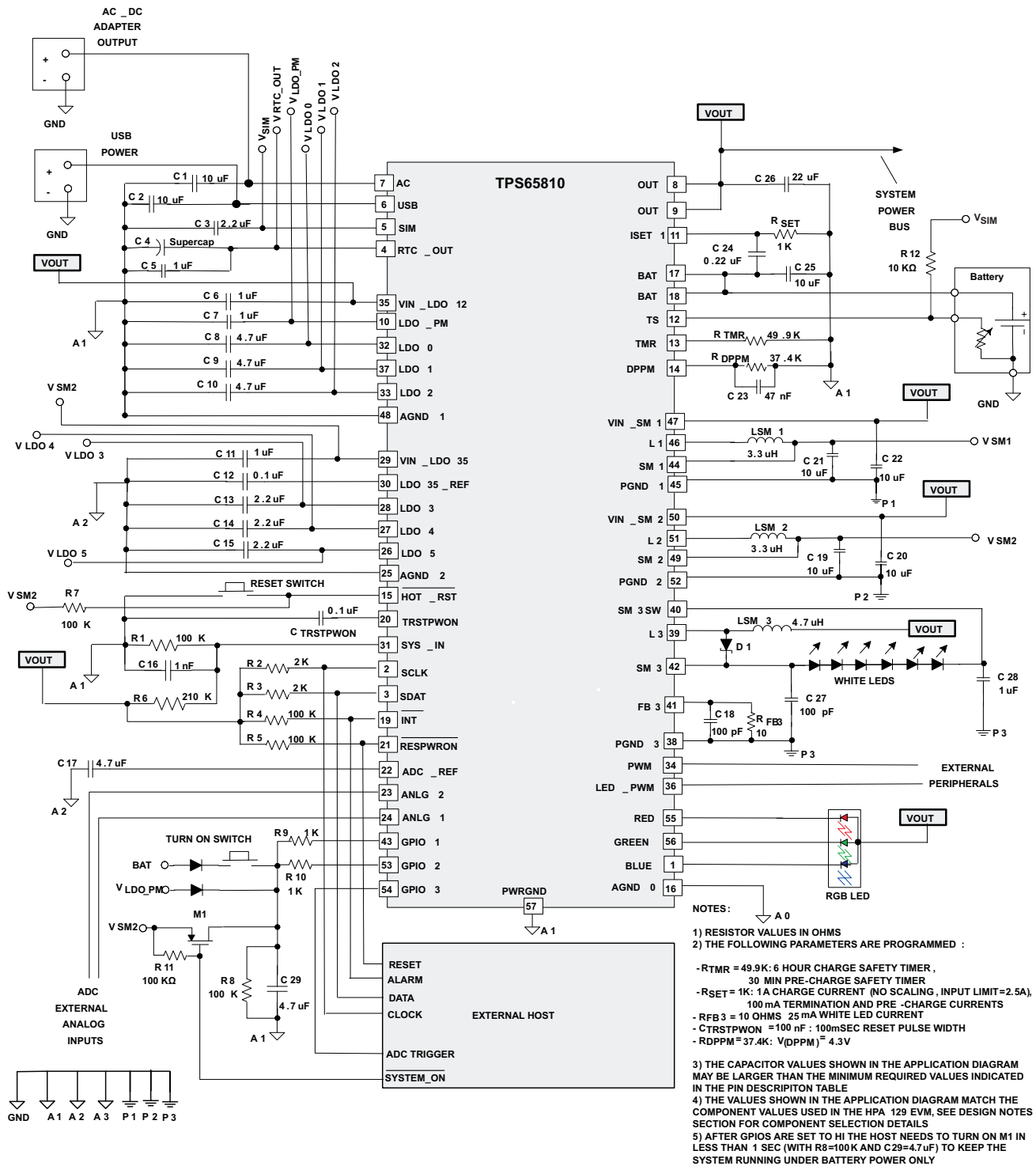


Figure 51. TPS65810 Application Diagram, Recommended External Components

Typical Applications (continued)

9.2.1.1 Design Requirements

Use values listed in [Table 53](#) as the design conditions and parameters for the SM1 or SM2 converter design example.

Table 53. Design Parameter

| DESIGN PARAMETER | EXAMPLE VALUE |
|------------------|--|
| VIN_SM1/2 | 4.6 V typical (may be less if input source is limited) |
| VOUT_SM1/2 | 1.24 V |
| IO(MAX) | 0.6 A |
| f _{SW} | 1500 kHz |
| f _C | 25 kHz |

Use [Equation 13](#) to calculate the target inductance for this design application.

$$L_{\text{target}} = \frac{V(\text{OUT})}{0.3 \times I_{O(\text{MAX})}} \times \frac{\left(1 - \frac{V(\text{OUT})}{V_{\text{IN_MAX}}}\right)}{f_{\text{SW}}} = 3.35 \mu\text{H}$$

where

- 3.3 μH is a good target value (13)

Use [Equation 14](#) to calculate the target capacitance for this design application.

$$C = \frac{1}{L(2 \times \pi \times f_C)^2} = 10.5 \mu\text{F}$$

where

- 10 μ is a good target value (14)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor and Capacitor Selection — Converters SM1 and SM2

SM1 and SM2 are designed with internal voltage mode compensation and the stabilization is based on the selection of an LC filter that has a corner frequency around 27 kHz. TI does not recommend using LC values that would be outside the range of 13 kHz to 40 kHz.

Use [Equation 15](#) to calculate the corner frequency of the output LC filter for $L = 3.3 \mu\text{H}$ and $C = 10 \mu\text{F}$ which are the standard recommended LC values.

$$F = \frac{1}{2\pi\sqrt{LC}} = 27.7 \text{ kHz} \quad (15)$$

The inductor value, along with the input voltage VIN, output voltage V_{OUT} and switching frequency f define the ripple current. Typically the ripple current target is 30% of the full load current. At light loads it is desirable for ripple current to be less than 150% of the light load current.

The inductor must be chosen with a rating to handle the peak ripple current, if a current of an inductor gets higher than its rated saturation level (DCR), the inductance starts to fall off, and the inductor's ripple current increases exponentially. The DCR of the inductor plays an important role in efficiency and size of the inductor. Larger diameter wire has less DCR but may increase the size of the inductor

Use [Equation 16](#) to calculate the target inductor value. If an inductor value was already selected, use [Equation 17](#) to calculate the ripple current of the inductor under static operating conditions. The ripple amplitude can be calculated during the ON-time (positive ramp) or during the OFF-time (negative ramp). Calculating the ripple using the off time is the easiest method because the voltage of the inductor is the output voltage.

$$I_{\text{target}} = \frac{V(\text{OUT})}{0.3 \times I_{\text{O(MAX)}}} \times \frac{\left(1 - \frac{V(\text{OUT})}{V_{\text{IN_MAX}}}\right)}{f} \quad (16)$$

$$\Delta I_L = \frac{V_L}{L} \times \Delta t = \frac{V(\text{OUT})}{L} \times \frac{\left(1 - \frac{V(\text{OUT})}{V_{\text{IN}}}\right)}{f} \quad (17)$$

Use Equation 18 to calculate the peak current because of the output load and ripple current.

$$I_{\text{Lmax}} = I_{\text{O(MAX)}} + \frac{\Delta I_L}{2} \quad (18)$$

For a faster transient response, a lower inductor and higher capacitance allows the output current to ramp faster, while the addition capacitance holds up the output longer (a 2.2-μH inductor in combination with a 22-μF output capacitor are recommended).

The highest inductor current occurs at the maximum input voltage. The peak inductor current during a transient may be higher than the steady state peak current and must be considered when selecting an inductor. Monitoring the inductor current for non-saturation operation during a transient of $1.2 \times I_{\text{Lmax}}$ at $V_{\text{IN_MAX}}$ ensures adequate saturation margin. Table 54 lists recommended inductors for typical operating conditions.

Table 54. Inductors for Typical Operation Conditions

| DEVICE | INDUCTOR VALUE | TYPE | COMPONENT SUPPLIER |
|-----------------|----------------|-------------------|--------------------|
| DCDC3 converter | 3.3 μH | CDRH2D14NP-3R3 | Sumida |
| | 3.3 μH | PDS3010-332 | Coilcraft |
| | 3.3 μH | VLF4012AT-3R3M1R3 | TDK |
| | 2.2 μH | VLF4012AT-2R2M1R5 | TDK |
| | 2.2 μH | NR3015T2R2 | Taoup-Uidem |
| DCDC2 converter | 3.3 μH | CDRH2D18/HPNP-3R3 | Sumida |
| | 3.3 μH | VLF4012AT-3R3M1R3 | TDK |
| | 2.2 μH | VLCF4020-2R2 | TDK |
| DCDC1 converter | 3.3 μH | CDRH3D14/HPNP-3R2 | Sumida |
| | 3.3 μH | CDRH4D28C-3R2 | Sumida |
| | 3.3 μH | MSS5131-332 | Coilcraft |
| | 2.2 μH | VLCF4020-2R2 | TDK |

9.2.1.2.2 Output Capacitor Selection, SM1, SM2 Converters

The advanced Fast Response voltage mode control scheme of the SM1, SM2 converters implemented in the TPS65020 allow the use of small ceramic capacitors with a typical value of 10 μF for a 3.3-μH inductor, without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors having low ESR values have low output voltage ripple, and recommended values and manufacturers are listed in Table 27. Often, because of the low ESR, the ripple current rating of the ceramic capacitor is adequate to meet the inductor's currents requirements.

Use Equation 19 to calculate the RMS ripple current.

$$V_{\text{RMSOut}} = \frac{1 - \frac{V(\text{OUT})}{V_{\text{IN}}}}{L \times f} \times \left(\frac{1}{8 \times C_{\text{OUT}} \times f} + \text{ESR} \right) \quad (19)$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor. The output voltage ripple is maximum at the highest input voltage V_{in} . Use Equation 20 to calculate the voltage spike caused by the output capacitor ESR (V_{RMSOut}).

$$V_{\text{RMS Cout}} = \frac{1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}}{L \times f} \times \left(\frac{1}{8 \times C_{\text{out}} \times f} + \text{ESR} \right) \quad (20)$$

At light load currents, the converters operate in PFM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal PFM output voltage comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage. [Table 55](#) lists recommend I/O capacitors for typical operating conditions.

Table 55. Input and Output Capacitors for Typical Operation Conditions

| CAPACITOR VALUE | CASE SIZE | COMPONENT SUPPLIER | COMMENTS |
|-----------------|-----------|---------------------------|----------|
| 22 µF | 1260 | TDK C3216X5R0J226M | Ceramic |
| 22 µF | 1260 | Taiyo Yuden JMK316BJ226ML | Ceramic |
| 10 µF | 0805 | Taiyo Yuden JMK212BJ106M | Ceramic |
| 10 µF | 0805 | TDK C2012X5R0J106M | Ceramic |
| 22 µF | 0805 | TDK C2012X5R0J226MT | Ceramic |
| 22 µF | 0805 | Taiyo Yuden JMK212BJ226MG | Ceramic |

9.2.1.2.3 Input Capacitor Selection, SM1, SM2 Converters

Buck converters have a pulsating input current that can generate high input voltage spikes at V_{IN} . A low ESR input capacitor is required to filter the input voltage, minimizing the interference with other circuits connected to the same power supply rail. Each DC–DC converter requires a 10-µF ceramic input capacitor on its input pin.

9.2.1.2.4 Output Voltage Selection, SM1, SM2 Converters

Typically the output voltage is programmed by the I²C. An external divider can be added to raise the output voltage, if the available I²C values do not meet the application requirements. Take care with this special option, because this external divider (gain factor) would apply to any selected I²C output voltage value for this converter.

Use [Table 54](#) to calculate the value of R1 with R2 = 20 kΩ.

$$R1 = \left(\frac{V_{\text{SMxOUT}}}{V_{\text{FB}}} - 1 \right) R2$$

where

- V_{SMxOUT} is the desired output voltage and R1/R2 is the feedback divider
- V_{FB} is the I²C selected voltage

(21)

9.2.1.3 Application Curves

The application curves were measured with the application circuit shown in Figure 51 (unless otherwise noted).

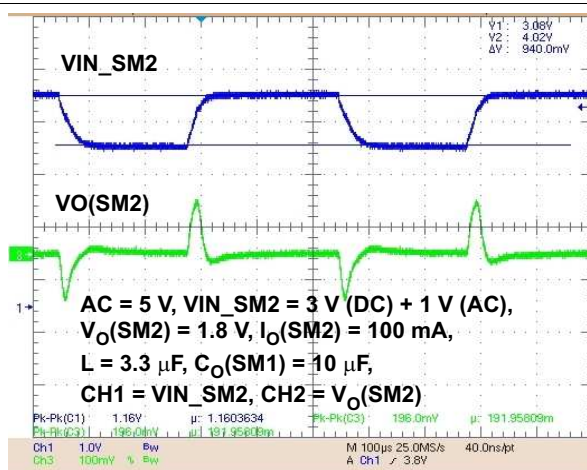


Figure 52. Line Transient

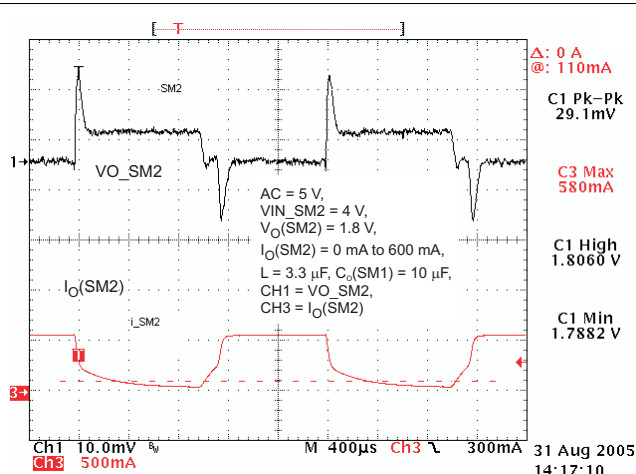


Figure 53. Load Transient

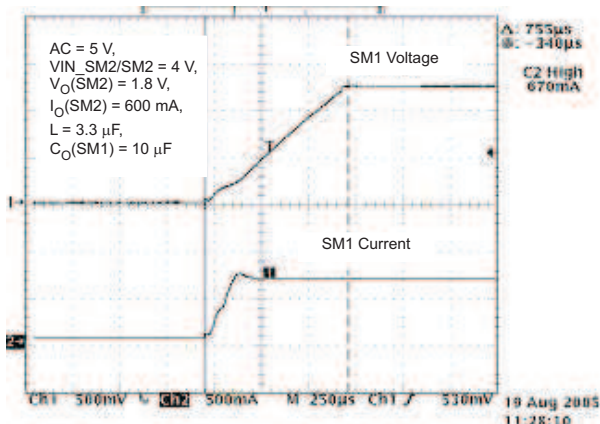


Figure 54. Transient - SM1 Start-Up

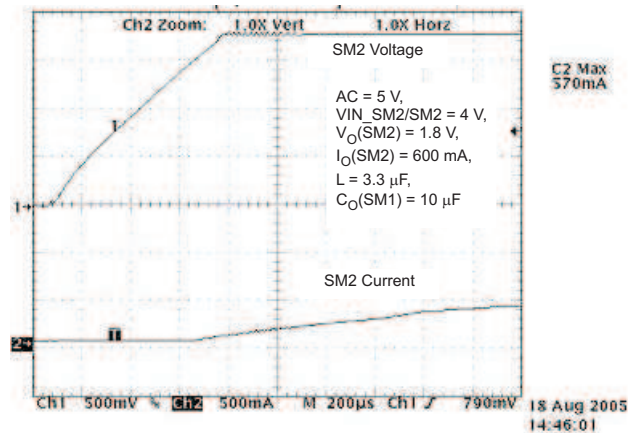


Figure 55. Transient - SM2 Start-Up

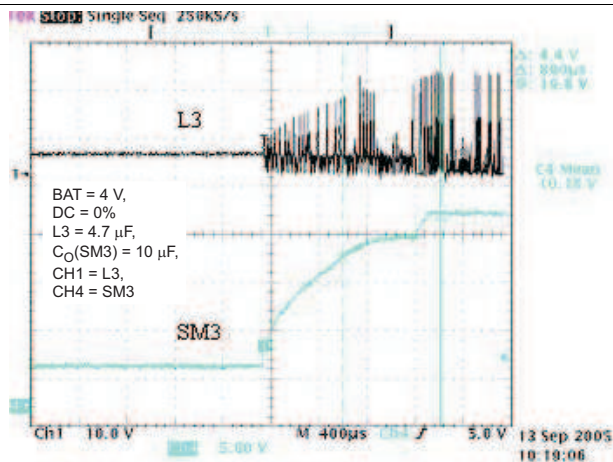


Figure 56. SM3 White LED Driver Soft-Start

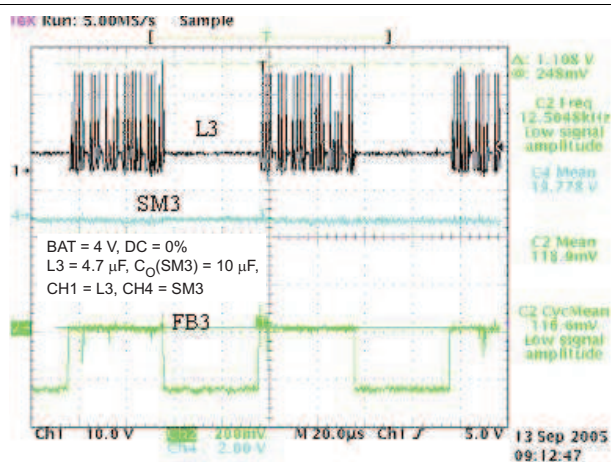


Figure 57. SM3 Led Current vs PWM Duty Cycle

9.2.2 Charger Design Example

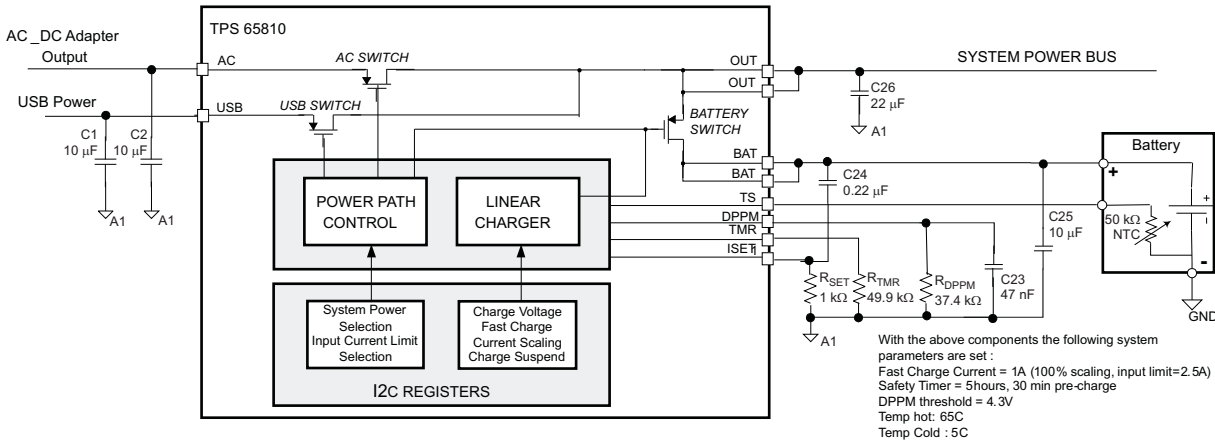


Figure 58. Required External Components, Recommended Values, External Connections

9.2.2.1 Design Requirements

Use values listed in [Table 56](#) as the design conditions and parameters for the charger design example.

Table 56. Design Parameter

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|--|
| V(OUT) | 4.6 V; (OUT pin is input to charger) |
| Fast-charge current, I _{PGM} | 1 A |
| DPPM-OUT threshold | 4.3 V; (charging current reduces when OUT falls to this level) |
| Safety timer | 5 h |
| Battery short-circuit delay, t _{DELAY} | 47 μs; (delays BAT short circuit during hot plug of battery) |
| TS temperature range | Disabled |
| K _(SET) | 400 |
| V _(SET) | 2.5 V |
| K _{DPPM} | 1.15 |
| I _{DPPM} | 100 μA |
| K _{TMR} | 0.36 s/Ω |

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Program the Fast Charge Current Level:

Use [Equation 22](#) to calculate the fast-charge current level.

$$R_{\text{ISET}} = \frac{K_{\text{(SET)}} \times V_{\text{(SET)}}}{I_{\text{PGM}}} = 1 \text{ k}\Omega \quad (22)$$

9.2.2.2.2 Program the DPPM_OUT Voltage Level

Use [Equation 23](#) to calculate the DPPM_OUT voltage level which is the level at which the charging current is reduced.

$$R_{\text{DPPM}} = \frac{V_{\text{DPPM_OUT}}}{K_{\text{DPPM}} \times I_{\text{DPPM}}} = 3.74 \text{ k}\Omega \quad (23)$$

9.2.2.2.3 Program the BAT Short Circuit Delay

Use [Equation 24](#) to calculate the BAT short-circuit delay which is used to insert the battery.

$$C_{DPPM} = t_{DELAY} \times I_{DPPM} = 4.7 \text{ Nf} \quad (24)$$

9.2.2.2.4 Program the 5-Hour Safety Timer

Use [Equation 25](#) to calculate the value of the safety timer.

$$R_{TMR} = \frac{t_{SAFETY-HR} \times 3600 \text{ s/hr}}{K_{TMR}} = 50 \text{ k}\Omega \quad (25)$$

10 Power Supply Recommendations

The power path control of this device allows it to be used with an input voltage from an AC adapter, a USB port, or a single-cell lithium ion (Li-Ion) battery. The AC and USB inputs must be well regulated and range from 4.35 to 5.5 V.

11 Layout

11.1 Layout Guidelines

The PCB layout for a switching power supply is an important step of the design, especially for high peak current and high switching frequency converters. To avoid stability and EMI problems, TI recommends that short and wide traces be used for the main current path and for the power ground tracks. The input capacitor, output capacitor and the inductor must be placed as close as possible to the IC. Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Both these ground nodes must be connected together at a point close to one of the IC ground pins.

The PGNDx pins are the ground connections for the power stage and therefore carry high DC and AC peak currents. A low impedance connection between the PGNDx pins and the power ground plane is recommended. No other pins must be connected to the PGNDx pins.

The AGNDx pins serve as the ground connections for the internal analog circuitry of the device. These pins must be connected directly to the PCB ground plane using vias.

11.2 Layout Example

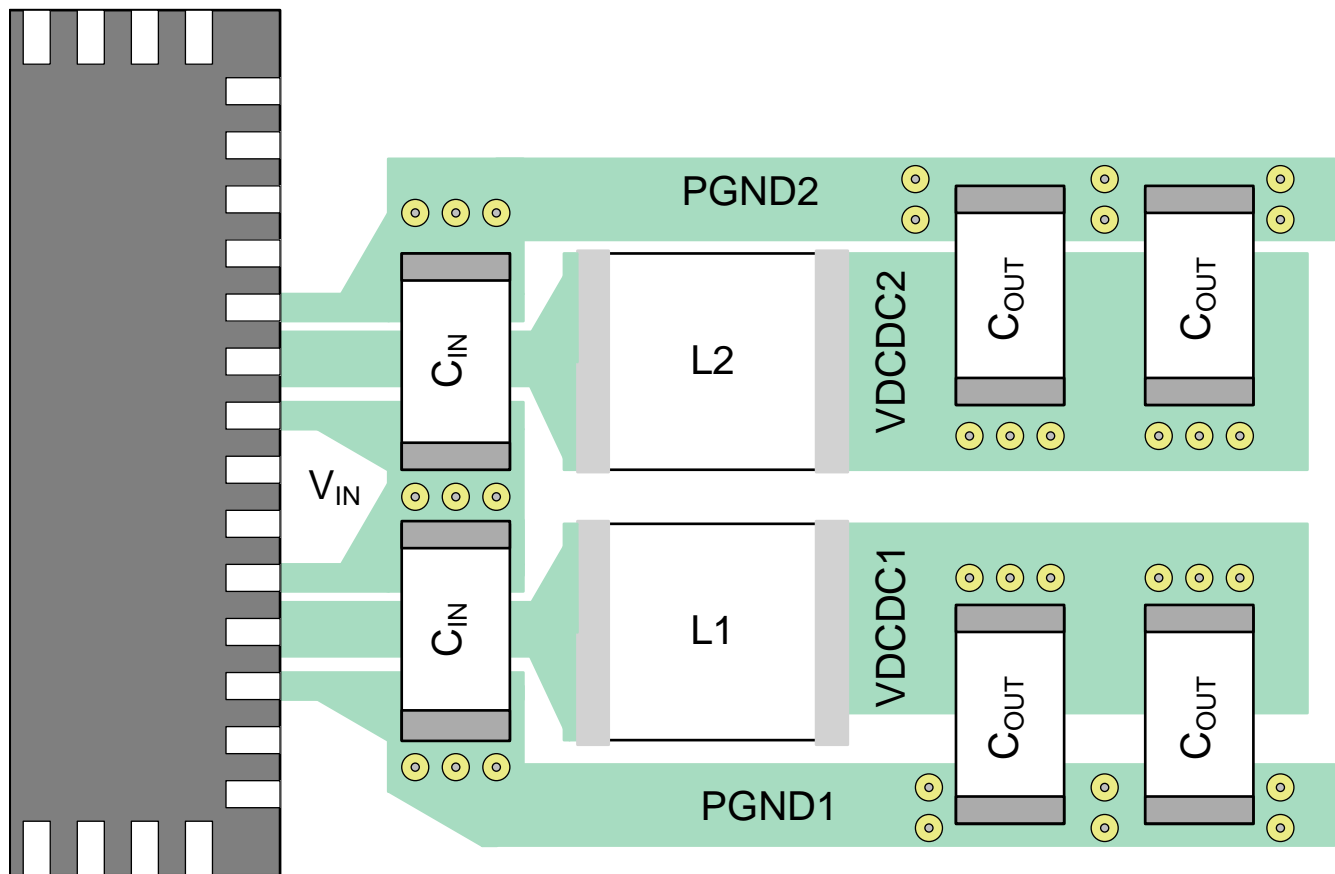


Figure 59. Converter Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Documentation

For related documentation see the following:

- *Differences Between the TPS65800/810/820 PMIC Devices*, [SLVA248](#)
- *Optimizing Resistor Dividers at a Comparator Input*, [SLVA450](#)
- *TPS658xxEVM Integrated Single-Cell, Lithium-Ion Battery- and Power-Management IC With I²C, LED Drives, Two Synchronous Buck, Boost, and Multiple LDOs*, [SLVU154](#)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 57. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS65810 | Click here | Click here | Click here | Click here | Click here |
| TPS65811 | Click here | Click here | Click here | Click here | Click here |

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS65810RTQT | ACTIVE | QFN | RTQ | 56 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | TPS 65810 | Samples |
| TPS65811RTQR | ACTIVE | QFN | RTQ | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | TPS 65811 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65810RTQT | QFN | RTQ | 56 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 2.25 | 12.0 | 16.0 | Q2 |
| TPS65811RTQR | QFN | RTQ | 56 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 2.25 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65810RTQT | QFN | RTQ | 56 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65811RTQR | QFN | RTQ | 56 | 2000 | 367.0 | 367.0 | 38.0 |

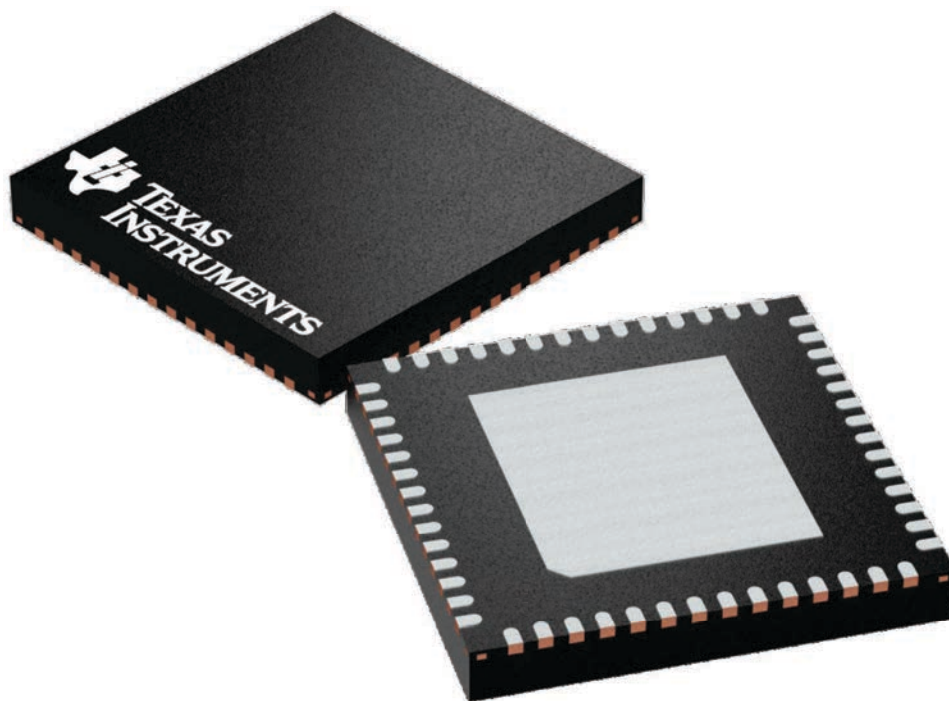
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A

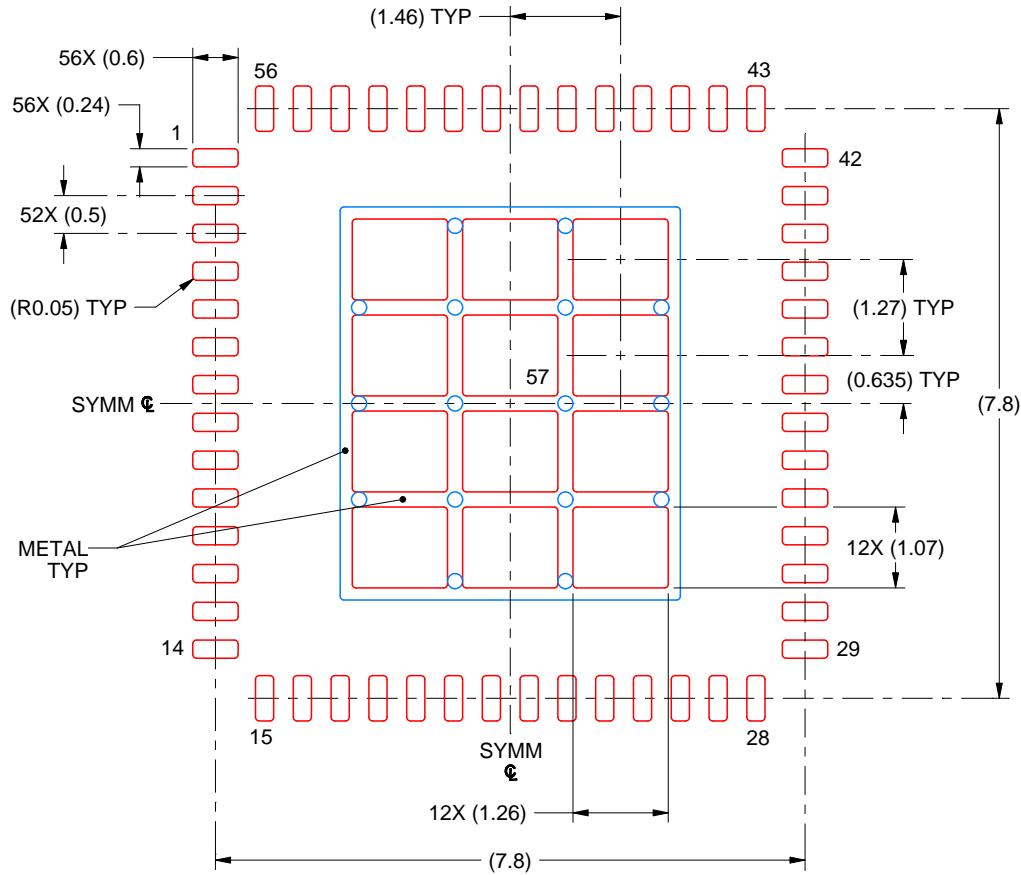
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RTQ0056B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219130/B 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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