TPS65100-Q1 Triple-Output LCD Supply With Linear Regulator and VCOM Buffer

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Input Voltage Range: 2.7-V to 5.8-V
- V_O1 Boost Converter
  - Up to 15 V Output Voltage
  - Virtual Synchronous Converter Topology
  - < 1% Output Voltage Accuracy
  - 1.6-MHz Fixed Switching Frequency
  - 2.3-A Switch Current Limit
- V_O2 Negative Regulated Charge Pump
  - Down to -12 V / 20 mA
- V_O3 Positive Regulated Charge Pump
  - Up to 30 V / 20 mA
- Three Independently Adjustable Outputs
- Integrated VCOM Buffer
- Auxiliary 3.3-V Linear Regulator Controller
- Internal Soft Start
- Internal Power-On Sequencing
- Protection Features
  - Short-Circuit Detection of all Outputs
  - Overvoltage Protection of all Outputs
  - Thermal Shutdown
- Available in TSSOP-24 PowerPAD™ Package

2 Applications

- Infotainment Systems
- Automotive Displays
- Instrument Clusters
- Center Consoles
- Rear Seat Entertainment

3 Description

The TPS65100-Q1 device offers a compact and small power supply solution that provides all three voltages required by thin-film transistor (TFT) LCD displays. The auxiliary linear regulator controller can be used to generate a 3.3-V logic power rail for systems powered by a 5-V supply rail only.

The main output, V_O1, is a 1.6-MHz fixed-frequency PWM boost converter that provides the source-drive voltage for the LCD display. The TPS65100-Q1 has a typical switch current limit of 2.3 A. A fully integrated adjustable charge pump doubler-tripler provides the positive LCD gate-drive voltage. An externally adjustable negative charge pump provides the negative gate-drive voltage.

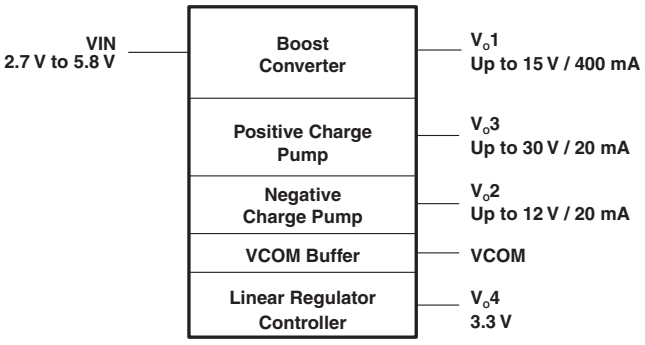
The TPS65100-Q1 has an integrated VCOM buffer to power the LCD backplane. For LCD panels powered by 5 V only, the TPS65100-Q1 device has a linear regulator controller using an external transistor to provide a regulated 3.3-V output for the digital circuits. For maximum safety, the TPS65100-Q1 device goes into shutdown as soon as one of the outputs is out of regulation. The device can be enabled again by toggling the input or the enable (EN) pin to GND.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65100-Q1	TSSOP (24) with PowerPAD	4.40 mm × 7.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TPS65100-Q1 Overview



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Changed Features List ... 1
- Changed from T_A to T_J in the Conditions statement of and changed temperature from 85°C to 125°C ... 6
- Changed the MAIN BOOST CONVERTER V_{REF} spec from 1.205 MIN to 1.198, and MAX from 1.203 to 1.230 ... 6
- Changed V_{FB} spec from 1.113 MIN to 1.126, and MAX from 1.154 to 1.161 ... 6
- Changed $r_{DS(ON)}$ for V_O1 = 10 V, Isw = 500 mA condition, from 290 to 325 MAX; and, for the V_O1 = 5 V, Isw = 500 mA condition, changed from 420 to 455 MAX ... 6
- Changed f_{SW} Condition from T_A to T_J and changed f_{SW} spec for 0°C ≤ T_J ≤ 125°C condition from 1.295 MIN to 1.195 MIN; and, changed the MIN from 1.191 to 1.091, for the –40°C ≤ T_J ≤ 125°C condition; ... 6
- Changed from T_A to T_J in the Conditions statement of and changed temperature from 85°C to 125°C ... 7
- Changed NEGATIVE CHARGE PUMP V_O2 V_{REF} spec from 1.205 MIN to 1.198, and MAX from 1.219 to 1.226 ... 7
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- Added *Device Information* table, *Pin Configuration and Functions* section, *Specifications* section, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table. See Mechanical, Packaging, and Orderable Information for more information. ... 4
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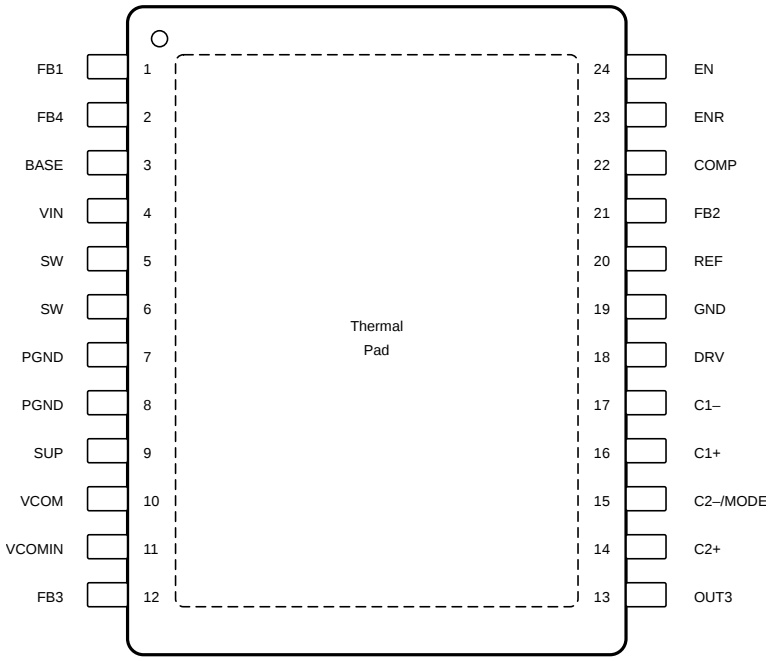
Changes from Original (July 2008) to Revision A **Page**

- Added thermal table for PWP Package 6

5 Pin Configuration and Functions

PWP Package
24-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BASE	3	O	Base drive output for the external transistor
C1+	16	—	Positive terminal of the charge pump flying capacitor
C1–	17	—	Negative terminal of the charge pump flying capacitor
C2+	14	—	Positive terminal for the charge pump flying capacitor. If the device runs in voltage doubler mode, this pin should be left open.
C2–/MODE	15	—	Negative terminal of the charge pump flying capacitor and charge pump MODE pin. If the flying capacitor is connected to this pin, the converter operates in a voltage tripler mode. If the charge pump needs to operate in a voltage doubler mode, the flying capacitor is removed and the C2–/MODE pin should be connected to GND.
COMP	22	—	Compensation pin for the main boost converter. A small capacitor is connected to this pin.
DRV	18	O	External charge pump driver
EN	24	I	Enable pin of the device. This pin should be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device.
ENR	23	I	Enable pin of the linear regulator controller. This pin should be terminated and not be left floating. Logic high enables the regulator and a logic low puts the regulator in shutdown.
FB1	1	I	Feedback pin of the boost converter
FB2	21	I	Feedback pin of negative charge pump
FB3	12	I	Feedback pin of positive charge pump
FB4	2	I	Feedback pin of the linear regulator controller. The linear regulator controller is set to a fixed output voltage of 3.3 V or 3 V depending on the version.
OUT3	13	PWR	Positive charge pump output
REF	20	O	Internal reference output typically 1.23 V
SUP	9	I	Supply of the positive and negative charge pump, boost converter gate-drive circuit, and VCOM buffer. Should be connected to the output of the main boost converter and cannot be connected to any other voltage source. For performance reasons, do not connect a bypass capacitor directly to this pin.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	5, 6	PWR	Switch pin of the boost converter
VCOM	10	PWR	VCOM buffer output
VCOMIN	11	I	Positive input terminal of the VCOM buffer. When the VCOM buffer is not used, this terminal can be connected to GND to reduce the overall quiescent current of the IC.
VIN	4	PWR	Input voltage pin of the device
GND	19	GND	Connect this pin to common ground plane under the thermal power pad.
PGND	7, 8	GND	Power ground
Thermal pad	—	GND	The exposed PowerPAD should be connected to the power ground (PGND).

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN	–0.3	6	V
	SUP	–0.3	15.5	
	EN, MODE, ENR	–0.3	V_I + 0.3	
Voltage	VCOMIN		14	V
Voltage(2)	SW		20	V
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature range		–40	150	°C
Lead temperature (soldering, 10 seconds)			260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM)	±100	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.7		5.8	V
L	Inductor(1)		4.7		µH
T_A	Operating free-air temperature	–40		125	°C

(1) See *Inductor Selection* for further information.

6.4 Thermal Information

THERMAL METRIC[1]		TPS65100-Q1 PWP (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_I = 3.3 V, EN = VIN, V_O1 = 10 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current into VIN	ENR = VCOMIN = GND, $V_O3 = 2 \times V_O1$, Boost converter not switching		0.7	0.9	mA
$I_{QCharge}$	Charge pump quiescent current into SUP	V_O1 = SUP = 10 V, $V_O3 = 2 \times V_O1$		1.7	2.7	mA
		V_O1 = SUP = 10 V, $V_O3 = 3 \times V_O1$		3.9	6	
I_{QVCOM}	VCOM quiescent current into SUP	ENR = GND, V_O1 = SUP = 10 V		750	1300	µA
I_{QEN}	LDO controller quiescent current into VIN	ENR = VIN, EN = GND		300	800	µA
I_{SD}	Shutdown current into VIN	EN = ENR = GND		1	10	µA
V_{UVLO}	Undervoltage lockout threshold	VIN falling		2.2	2.4	V
	Thermal shutdown	Temperature rising		160		°C
LOGIC SIGNALS EN, ENR						
V_{IH}	High-level input voltage		1.5			V
V_{IL}	Low-level input voltage				0.4	V
I_{Leak}	Input leakage current	EN = GND or VIN		0.01	0.1	µA
MAIN BOOST CONVERTER						
V_O1	Output voltage range		5		15	V
$V_O1 - V_I$	Minimum input to output voltage difference		1			V
V_{REF}	Reference voltage		1.198	1.213	1.230	V
V_{FB}	Feedback regulation voltage		1.126	1.146	1.161	V
I_{FB}	Feedback input bias current			10	100	nA
$r_{DS(ON)}$	N-MOSFET on-resistance (Q1)	V_O1 = 10 V, I_{sw} = 500 mA		195	325	mΩ
		V_O1 = 5 V, I_{sw} = 500 mA		285	455	
I_{LIM}	N-MOSFET switch current limit (Q1)		1.6	2.3	2.7	A
$r_{DS(ON)}$	P-MOSFET on-resistance (Q2)	V_O1 = 10 V, I_{sw} = 100 mA		9	15	Ω
		V_O1 = 5 V, I_{sw} = 100 mA		14	22	
I_{MAX}	Maximum P-MOSFET peak switch current				1	A
I_{Leak}	Switch leakage current	V_{sw} = 15 V		1	10	µA
f_{SW}	Oscillator frequency	0°C ≤ T_J ≤ 125°C	1.195	1.6	2.1	MHz
		–40°C ≤ T_J ≤ 125°C	1.091	1.6	2.1	

Electrical Characteristics (continued)

V_I = 3.3 V, EN = VIN, V_O1 = 10 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Line regulation	2.7 V ≤ V_I ≤ 5.7 V, I_{load} = 100 mA		0.012		%/V
	Load regulation	0 mA ≤ I_O ≤ 300 mA		0.2		%/A
NEGATIVE CHARGE PUMP V_O2						
V_O2	Output voltage range		–2			V
V_{REF}	Reference voltage		1.198	1.213	1.226	V
V_{FB}	Feedback regulation voltage		–36	0	36	mV
I_{FB}	Feedback input bias current			10	100	nA
$r_{DS(ON)}$	Q8 P-channel switch $r_{DS(ON)}$	I_O = 20 mA		4.3	8	Ω
	Q9 N-channel switch $r_{DS(ON)}$			2.9	4.4	
I_O	Maximum output current		20			mA
	Line regulation	7 V ≤ V_O1 ≤ 15 V, I_{load} = 10 mA, V_O2 = –5 V		0.09		%/V
	Load regulation	1 mA ≤ I_O ≤ 20 mA, V_O2 = –5 V		0.126		%/mA
POSITIVE CHARGE PUMP V_O3						
V_O3	Output voltage range				30	V
V_{REF}	Reference voltage		1.198	1.213	1.226	V
V_{FB}	Feedback regulation voltage		1.180	1.214	1.245	V
I_{FB}	Feedback input bias current			10	100	nA
$r_{DS(ON)}$	Q3 P-channel switch $r_{DS(ON)}$	I_O = 20 mA		9.9	15.5	Ω
	Q4 N-channel switch $r_{DS(ON)}$			1.1	1.8	
	Q5 P-channel switch $r_{DS(ON)}$			4.6	8.5	
	Q6 N-channel switch $r_{DS(ON)}$			1.2	2.2	
V_D	D1–D4 Shottky diode forward voltage	$I_{D1–D4}$ = 40 mA		610	800	mV
I_O	Maximum output current		20			mA
	Line regulation	10 V ≤ V_O1 ≤ 15 V, I_{load} = 10 mA, V_O3 = 27 V		0.56		%/V
	Load regulation	1 mA ≤ I_O ≤ 20 mA, V_O3 = 27 V		0.05		%/mA
LINEAR REGULATOR CONTROLLER V_O4						
V_O4	Output voltage	4.5 V ≤ V_I ≤ 5.5 V, 10 mA ≤ I_O ≤ 500 mA	3.2	3.3	3.4	V
I_{BASE}	Maximum base drive current	V_I - V_O4 - V_{BE} ≥ 0.5 V (1)	13.5	19		mA
		V_I - V_O4 - V_{BE} ≥ 0.75 V (1)	20	27		
	Line regulation	4.75 V ≤ V_I ≤ 5.5 V, I_{load} = 500 mA		0.186		%/V
	Load regulation	1 mA ≤ I_O ≤ 500 mA, V_I = 5 V		0.064		%/A
	Start up current	V_O4 ≤ 0.8 V	11	20	25	mA
VCOM BUFFER						
V_{CM}	Common mode input range		2.25		(V_O1) - 2	V
V_{OS}	Input offset voltage	I_O = 0 mA	–25		25	mV
	DC Load regulation	I_O = ±25 mA	–30		37	mV
		I_O = ±50 mA	–45		55	
		I_O = ±100 mA	–72		85	
		I_O = ±150 mA	–97		110	
I_B	VCOMIN Input bias current		–300	–30	300	nA
I_{Peak}	Peak output current	V_O1 = 15 V	1.2			A
		V_O1 = 10 V	0.65			A
		V_O1 = 5 V	0.15			A

(1) With V_I = supply voltage of the TPS65100-Q1, V_O4 = output voltage of the regulator, V_{BE} = basis emitter voltage of external transistor

Electrical Characteristics (continued)

V_I = 3.3 V, EN = VIN, V_O1 = 10 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT PROTECTION THRESHOLDS						
$V_{(th,\ Vo1)}$	Shutdown threshold	V_O1 Rising	–12	–8.75% V_O1	–6	V
$V_{(th,\ Vo2)}$		V_O2 Rising	–13	–9% V_O2	–5	V
$V_{(th,\ Vo3)}$		V_O3 Rising	–11	–8% V_O3	–5	V

6.6 Typical Characteristics

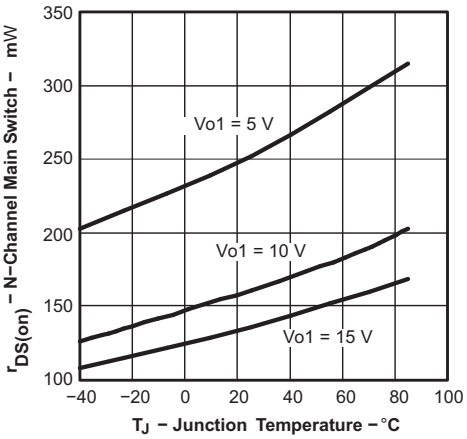


Figure 1. $r_{DS(ON)}$ N-Channel Main Switch vs Junction Temperature

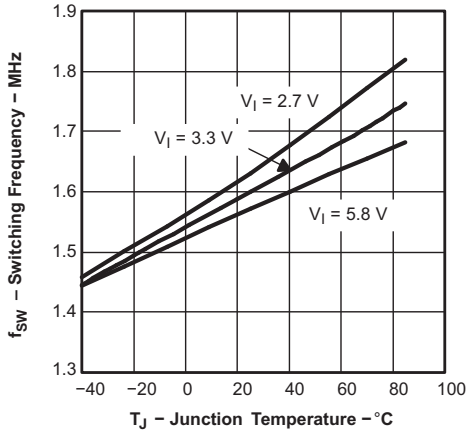


Figure 2. Switching Frequency vs Junction Temperature

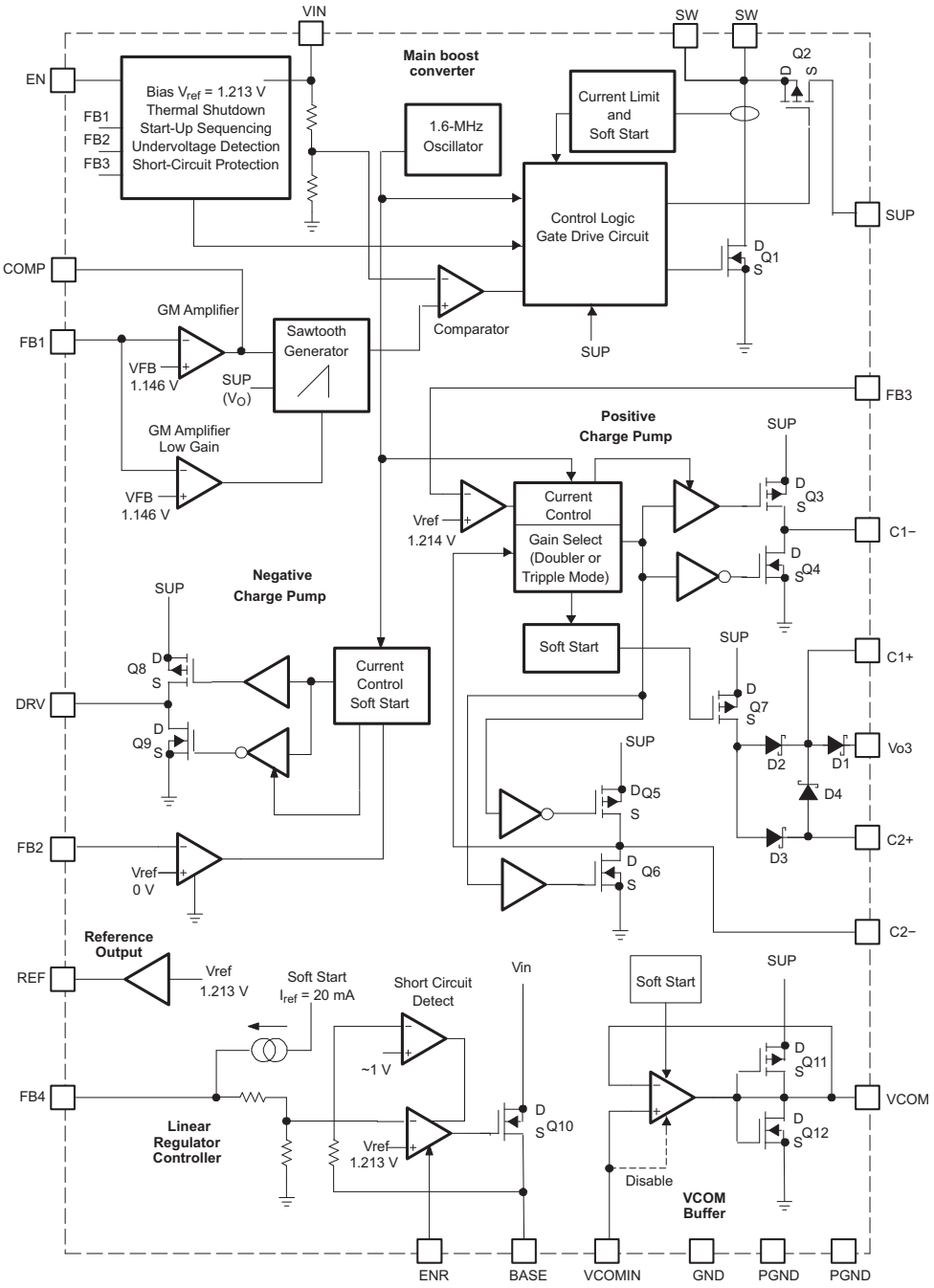
7 Detailed Description

7.1 Overview

The TPS65100-Q1 is a complete bias supply for LCD displays. It contains a main boost converter to supply the source driver. It operates with a fixed switching frequency of 1.6 MHz to allow for small external components. The boost converter output voltage V_O1 is also the input voltage, connected via the pin SUP, for the positive and negative charge pumps and the bias supply for the VCOM buffer.

The linear regulator controller is independent from this system with its own enable pin. This design allows the linear regulator controller to continue to operate while the other supply rails are disabled or in shutdown due to a fault condition on one of their outputs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Main Boost Converter

The main boost converter operates with PWM and a fixed switching frequency of 1.6 MHz. The converter uses a unique fast-response voltage-mode controller scheme with input voltage feedforward. This achieves excellent line and load regulation (0.2%/A load regulation typical) and allows the use of small external components. For higher flexibility to the selection of external component values the device uses external loop compensation. The TPS65100-Q1 device maintains continuous conduction even at light load currents because of an internal PMOS

Feature Description (continued)

in parallel connected between SW and SUP pin. When the inductor current is positive, the external schottky diode with the lower forward voltage conducts the current. This causes the converter to operate with a fixed frequency in continuous conduction mode over the entire load current range. This avoids the ringing on the switch pin as seen with a standard nonsynchronous boost converter and allows a simpler compensation for the boost converter.

7.3.2 VCOM Buffer

VCOMIN is the input of the VCOM buffer. If VCOM is not required connect VCOMIN pin to Ground and thereby reduce the overall quiescent current.

The VCOM buffer features soft start to avoid a large voltage drop at V_O1. During operation the VCOMIN pin cannot be pulled dynamically to ground.

7.3.3 Positive Charge Pump

The TPS65100-Q1 device has a fully regulated integrated positive charge pump generating V_O3. The input voltage for the charge pump is applied to the SUP pin that is equal to the output of the main boost converter V_O1. The charge pump is capable of supplying a minimum load current of 20 mA. Depending on the voltage difference between V_O1 and V_O3 higher load currents are possible (see Figure 17 and Figure 18).

7.3.4 Negative Charge Pump

The TPS65100-Q1 device has a regulated negative charge pump using two external Schottky diodes. The input voltage for the charge pump is applied to the SUP pin that is connected to the output of the main boost converter V_O1. The charge pump inverts the main boost converter output voltage and is capable of supplying a minimum load current of 20 mA. Depending on the voltage difference between V_O1 and V_O2, higher load currents are possible (see Figure 16).

7.3.5 Linear Regulator Controller

The TPS65100-Q1 device includes a linear regulator controller to generate a 3.3-V rail which is useful when the system is powered from a 5-V supply. The regulator is independent from the other voltage rails of the device and has its own enable (ENR). Since most of the systems require this voltage rail to come up first it is recommended to use a R-C delay on EN. This delays the start-up of the main boost converter which will reduce the inrush current as well.

7.4 Device Functional Modes

7.4.1 Enable and Power-ON Sequencing (EN, ENR)

The device has two enable pins. These pins should be terminated and should not be left floating to prevent unpredictable operation. Pulling the enable pin (EN) high enables the device and starts the power-on sequencing with the main boost converter V_O1 coming up first, then the negative and positive charge pump and the VCOM buffer. If the VCOMIN pin is held low, the VCOM buffer remains disabled. The linear regulator has an independent enable pin (ENR). Pulling this pin low disables the regulator, and pulling this pin high enables this regulator.

If the enable pin EN is pulled high, the device starts its power-ON sequencing. The main boost converter starts up first with its soft start. If the output voltage has reached 91.25% of its output voltage, the negative charge pump comes up next. The negative charge pump starts with a soft start and when the output voltage has reached 91% of the nominal value, the positive charge pump comes up with a soft start. The VCOM buffer is enabled as soon as the positive charge pump has reached its nominal value and VCOMIN is greater than typically 1 V. Pulling the enable pin low shuts down the device. Depended on load current and output capacitance, each of the outputs goes down.

7.4.2 Soft Start

The main boost converter as well as the charge pumps, linear regulator, and VCOM buffer have an internal soft start. This avoids heavy voltage drops at the input voltage rail or at the output of the main boost converter V_O1 during start-up caused by high inrush currents (see Figure 14 and Figure 15). During soft start of the main boost converter V_O1, the internal current limit threshold is increased in three steps. The device starts with the first step, where the current limit is set to 2/5 of the typical current limit (2/5 of 2.3 A) for 1024 clock cycles, then increased to 3/5 of the current limit for 1024 clock cycles, and finally raised to the full current limit.

7.4.3 Fault Protection

All the outputs of the TPS65100-Q1 device have short-circuit detection that can force the device into shutdown. The main boost converter has overvoltage and undervoltage protection. If the output voltage V_O1 rises above the overvoltage protection threshold of 105% of V_O1 (typical), the device stops switching but remains operational. When the output voltage falls below this threshold again, the converter continues operation. When the output voltage falls below power good threshold of 91.25% of V_O1 (typical), in case of a short-circuit condition, then the TPS65100-Q1 device goes into shutdown. Because there is a direct pass from the input to the output through the diode, the short-circuit condition remains. If this condition needs to be avoided, a fuse at the input or an output disconnect using a single transistor and resistor is required. The negative and positive charge pumps have an undervoltage lockout to protect the LCD panel from possible latchup conditions in the event of a short-circuit condition or faulty operation. When the negative output voltage is less than 90.5% (typical) of its output voltage (closer to ground), the device enters shutdown. When the positive charge pump output voltage V_O3 is below 92% (typical) of its output voltage, the device goes into shutdown as well. See the electrical characteristics table under fault protection thresholds. The device can be enabled again by toggling the enable pin (EN) below 0.4 V or by cycling the input voltage below the UVLO of 1.7 V. The linear regulator reduces the output current to typical 20 mA under a short-circuit condition when the output voltage is < 1 V (typical). See the functional block diagram. The linear regulator does not go into shutdown under a short-circuit condition.

7.4.4 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown threshold is 160°C. If this temperature is reached, the device goes into shutdown. The device can be enabled by toggling the enable pin to low and back to high or by cycling the input voltage to GND and back to V_I again.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 3 shows a general overview of the device and connections used in an application. Ranges are shown for several parameters to demonstrate the flexibility available to the application designer.

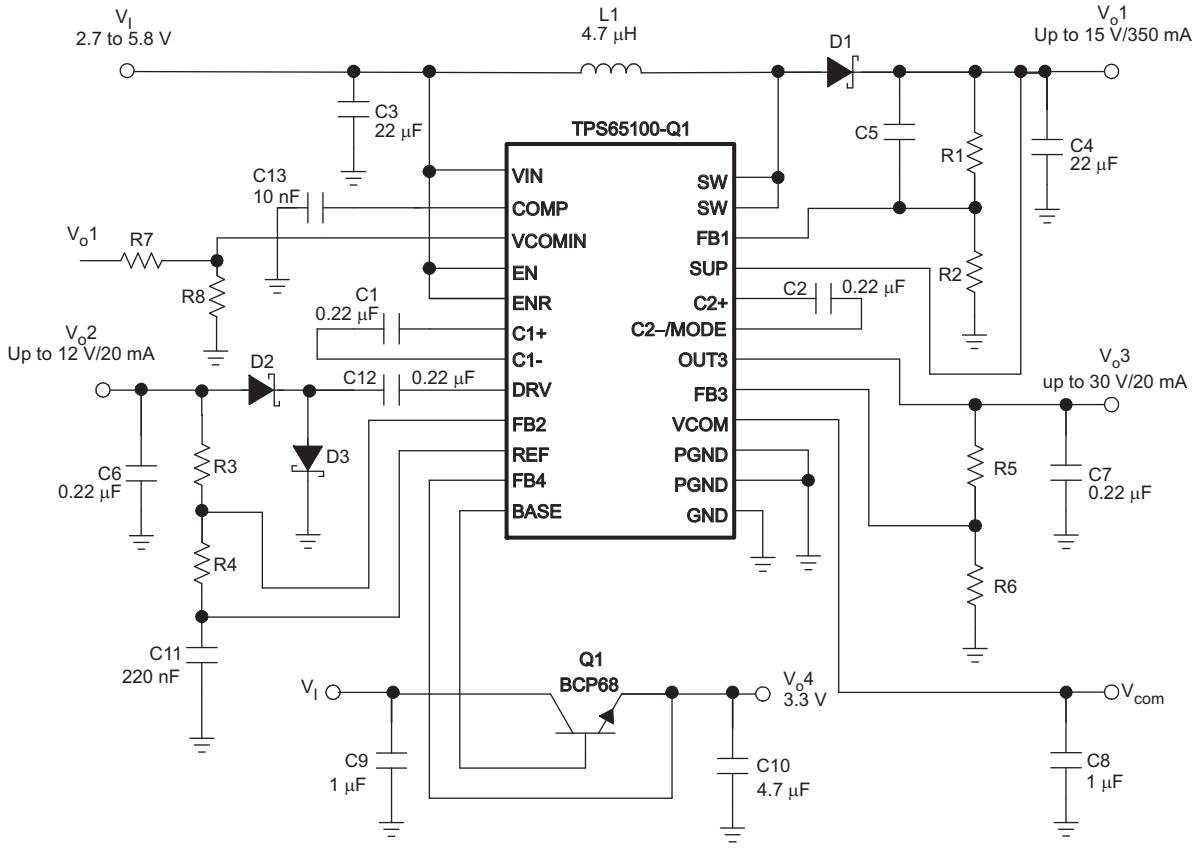


Figure 3. Simplified Schematic

8.2 Typical Applications

8.2.1 Supply for a Typical Approximately 7-inch Display

A typical application requirement is to boost a 3.3-V or 5-V input to a 10-V, 13.5-V, or 15-V output. The *Detailed Design Procedure* section explains the step-by-step development.

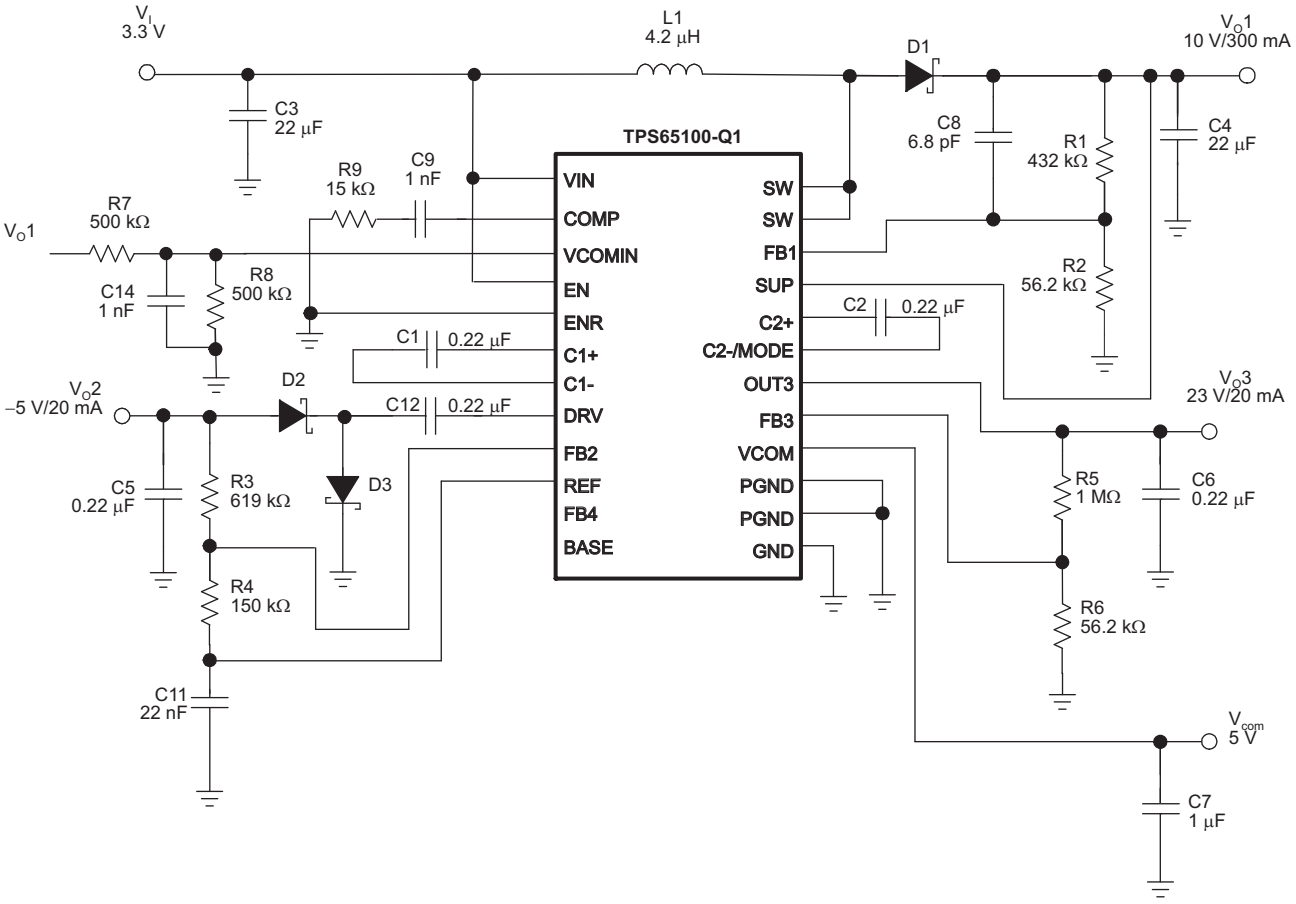


Figure 4. Supply for a 7-inch Display Diagram

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_I	3.3 V
V_O1	10 V
V_O2	–5 V
V_O3	23 V
Switch voltage drop, V_{SW}	0.5 V
Schottky diode forward voltage, V_D	0.8 V
V_{COM}	5 V

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Boost Converter Design Procedure

The first step in the design procedure is to calculate the maximum possible output current of the main boost converter under certain input and output voltage conditions. This example is for a 3.3-V to 10-V conversion:

1. Duty cycle

$$D = \frac{V_O + V_D - V_I}{V_O + V_D - V_{SW}} = \frac{10\ V + 0.8\ V - 3.3\ V}{10\ V + 0.8\ V - 0.5\ V} = 0.73 \quad (1)$$

2. Average inductor current

$$I_L = \frac{I_O}{1 - D} = \frac{300\ mA}{1 - 0.73} = 1.11\ A \quad (2)$$

3. Inductor peak-to-peak ripple current

$$\Delta I_L = \frac{(V_I - V_{SW}) \times D}{f_S \times L} = \frac{(3.3\ V - 0.5\ V) \times 0.73}{1.6\ MHz \times 4.2\ \mu H} = 304\ mA \quad (3)$$

4. Peak switch current

$$I_{swpeak} = I_L + \frac{\Delta I_L}{2} = 1.11\ A + \frac{304\ mA}{2} = 1.26\ A \quad (4)$$

The integrated switch, the inductor, and the external Schottky diode must be able to handle the peak switch current. The calculated peak switch current must be equal to or lower than the minimum N-MOSFET switch current limit specified in *Electrical Characteristics*. If the peak switch current is higher, the converter cannot support the required load current. This calculation must be done for the minimum input voltage, where the peak switch current is highest. The calculation includes conduction losses like switch $r_{DS(ON)}$ (0.5 V) and diode forward drop voltage losses (0.8 V). Additional switching losses and inductor core and winding losses require a slightly higher peak switch current in the actual application. This calculation still allows for good design and component selection.

8.2.1.2.1.1 Inductor Selection

Several inductors work with the TPS65100-Q1 device and, particularly with the external compensation, performance can be adjusted to application requirements. The main parameter for inductor selection is the saturation current of the inductor, which should be higher than the peak switch current as previously calculated, with additional margin to allow for heavy load transients and extreme start-up conditions. Another method is to choose an inductor with a saturation current at least as high as the minimum switch current limit of 1.6 A. The different switch-current limits allow selection of a physically smaller inductor when less output current is required. Another important parameter is inductor DC resistance. Usually, the lower the DC resistance, the higher the efficiency. However, inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and material of the inductor influences the efficiency as well. At the high switching frequency of 1.6 MHz, inductor core losses, proximity effects, and skin effects are more important. Usually, an inductor with a larger form factor yields higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. TI recommends inductor values between 3.3 μH and 6.8 μH.

8.2.1.2.1.2 Output Capacitor Selection

For the best output voltage filtering, TI recommends a low ESR output capacitor. Ceramic capacitors have a low ESR value, but depending on the application, tantalum capacitors can be used as well. A 22-µF ceramic output capacitor works for most of the applications. Higher capacitor values can be used to improve the load transient regulation. The output voltage ripple can be calculated as:

$$\Delta V_O = \frac{I_O}{C_O} \times \left(\frac{1}{f_S} - \frac{I_P \times L}{V_O + V_D - V_I} \right) + I_P \times ESR \quad (5)$$

where

- I_P = Peak switch current as calculated in the previous section with $I_{SW(peak)}$
- L = Selected inductor value
- I_O = Normal load current
- f_S = Switching frequency
- V_D = Rectifier diode forward voltage (typical 0.3 V)
- C_O = Selected output capacitor
- ESR = Output capacitor ESR value

8.2.1.2.1.3 Input Capacitor Selection

For good input voltage filtering, TI recommends low ESR ceramic capacitors. A 22-µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering, this value can be increased.

8.2.1.2.1.4 Rectifier Diode Selection

To achieve high efficiency, a Schottky diode should be used. The voltage rating must be higher than the maximum output voltage of the converter. The average forward current must be equal to the average inductor current of the converter. The main parameter influencing the efficiency of the converter is the forward voltage and the reverse leakage current of the diode; both must be as low as possible.

8.2.1.2.1.5 Converter Loop Design and Stability

The TPS65100-Q1 device converter loop can be externally compensated and allows access to the internal transconductance error amplifier output at the COMP pin. A small feedforward capacitor across the upper feedback resistor divider speeds up the circuit as well. To test the converter stability and load transient performance of the converter, a load step from 50 mA to 250 mA is applied, and the output voltage of the converter is monitored. Applying load steps to the converter output is a good tool to judge the stability of such a boost converter.

8.2.1.2.1.6 Design Procedure Quick Steps

1. Select the feedback resistor divider to set the output voltage.
2. Select the feedforward capacitor to place a zero at 50 kHz.
3. Select the compensation capacitor on pin COMP. The smaller the value, the higher the low frequency gain.
4. Use a 50-kΩ potentiometer in series to C_C and monitor V_O1 during load transients. Fine tune the load transient by adjusting the potentiometer. Select a resistor value that comes closest to the potentiometer resistor value. This needs to be done at the highest V_I and highest load current since the stability is most critical at these conditions.

8.2.1.2.1.7 Setting the Output Voltage and Selecting the Feedforward Capacitor

The output voltage is set by the external resistor divider and is calculated as:

$$V_O = 1.146\ V \times \left(1 + \frac{R1}{R2}\right) \quad (6)$$

Across the upper resistor a bypass capacitor is required to speed up the circuit during load transients as shown in Figure 5.

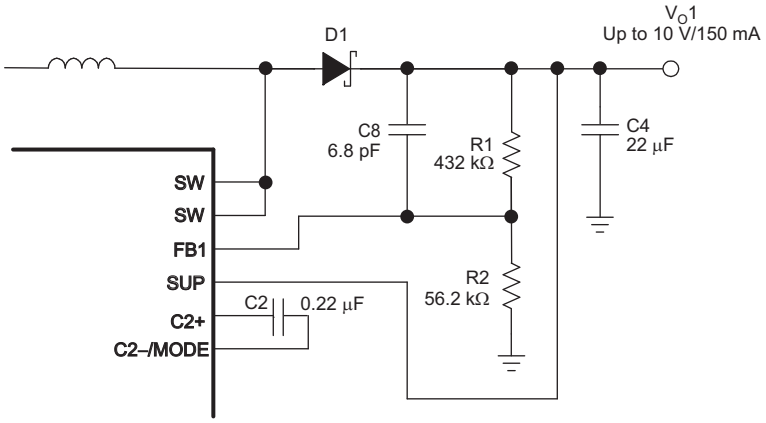


Figure 5. Feed-forward Capacitor

Together with R1 the bypass capacitor C8 sets a zero in the control loop at approximately 50 kHz:

$$f_Z = \frac{1}{2 \times \pi \times C8 \times R1} \quad (7)$$

A value closest to the calculated value should be used. Larger feedforward capacitor values reduce the load regulation of the converter and cause load steps as shown in Figure 6.

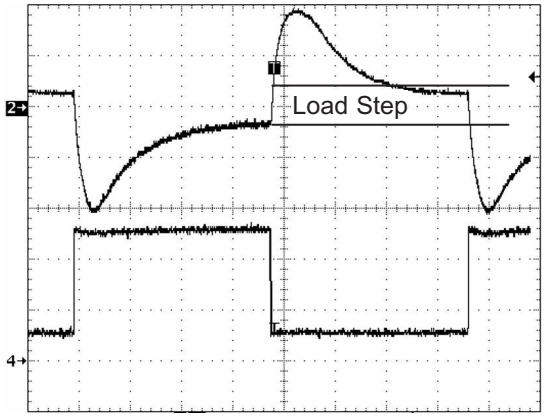


Figure 6. Load Step Caused By A Too Large Feed-forward Capacitor Value

For more information on how to calculate a Boost Converter's Output Stage refer to *Basic Calculation of a Boost Converter's Power Stage*.

8.2.1.2.2 Negative Charge Pump

The negative charge pump provides a regulated output voltage by inverting the main output voltage V_O1. The negative charge pump output voltage within its output voltage range is set with external feedback resistors.

The maximum load current of the negative charge pump depends on the voltage drop across the external Schottky diodes and the internal on resistance of the charge pump MOSFETS. When the voltage drop across these components is larger than the voltage difference from V_O1 to V_O2, the charge pump is in dropout, providing the maximum possible output current. Therefore, the higher the voltage difference between V_O1 and V_O2, the higher the possible load current. See Figure 16 for the possible output current versus boost converter voltage V_O1.

Estimating the maximum output voltage range of a single negative charge-pump stage:

$$V_{O(min)} = -(V_O1 - 2 \times V_D - I_O \times (2 \times r_{DS(ON)Q8} + 2 \times r_{DS(ON)Q9})) \quad (8)$$

Setting the output voltage:

$$V_O = -V_{REF} \times \frac{R3}{R4} = -1.213\ V \times \frac{R3}{R4} \quad (9)$$

$$R3 = R4 \times \frac{|V_O|}{V_{REF}} = R4 \times \frac{|V_O|}{1.213\ V} \quad (10)$$

The lower feedback resistor value R4 should be in a range between 40 kΩ to 120 kΩ or the overall feedback resistance should be within 500 kΩ to 1 MΩ. Smaller values load the reference too heavily and larger values may cause stability problems. For this design, 619 kΩ and 150 kΩ were chosen, delivering –5 V. The negative charge pump requires two external-Schottky diodes. The peak current rating of the Schottky diode has to be twice the load current of the output. For a 20-mA output current, the dual Schottky diode BAT54 or similar is a good choice.

8.2.1.2.3 Positive Charge Pump

The positive charge pump can be operated in a voltage doubler mode or a voltage tripler mode.

The output voltage needs to be within the voltage ranges of the configuration, see *Voltage Doubler Mode* and *Voltage Tripler Mode*. The output voltage within its limitation is set by the external resistor divider and is calculated as:

$$V_{OUT} = 1.214 \times \left(1 + \frac{R5}{R6}\right) \quad (11)$$

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R6 \times \left(\frac{V_{OUT}}{1.214} - 1\right) \quad (12)$$

The maximum load current of the positive charge pump depends on the voltage drop across the internal Schottky diodes, the internal ON-resistance of the charge pump MOSFETS, and the impedance of the flying capacitor. When the voltage drop across these components is larger than the voltage difference $V_{O1} \times 2$ to V_{O3} (doubler mode) or $V_{O1} \times 3$ to V_{O3} (tripler mode), then the charge pump is in dropout, providing the maximum possible output current. Therefore, the higher the voltage difference between V_{O1} x 2 (doubler) or $V_{O1} \times 3$ (tripler) to V_{O3}, the higher the possible load current. See Figure 17 and Figure 18 for output current versus boost converter voltage, V_{O1}, and the following calculations.

8.2.1.2.3.1 Voltage Doubler Mode

- Leave C2+ pin open
- Connect C2–/Mode to GND

The following shows first order formulas to calculate the minimum and maximum output voltages of the positive charge pump in doubler mode

- Minimum: $V_{O3min} = V_O1$
- Maximum: $V_{O3max} = 2 \times V_O1 – (2\ V_F + 2 \times I_O \times (2 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$

For detailed information how to estimate the output voltage ranges refer to *How to Estimate the Output Voltage Range of the Charge Pumps in the TPS6510x and TPS6514x*. SLVA918

8.2.1.2.3.2 Voltage Tripler Mode

- Connect flying capacitor to C2+ and C2–/MODE

The following shows first order formulas to calculate the minimum and maximum output voltages of the positive charge pump in doubler mode

- Minimum: $V_{O3min} = 2 \times V_O1 – (2 V_F + 2 \times I_O \times (2 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$
- Maximum: $V_{O3max} = 3 \times V_O1 – (4 \times V_F + 2 \times I_O \times (3 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$

For detailed information how to estimate the output voltage ranges refer to *How to Estimate the Output Voltage Range of the Charge Pumps in the TPS6510x and TPS6514x* SLVA918.

8.2.1.2.4 VCOM Buffer

The VCOM buffer is typically used to drive the backplane of a TFT panel. The VCOM output voltage is typically set to half of the main output voltage V_O1 plus a small shift to implement the specific compensation voltage. The TFT video signal gets coupled through the TFT storage capacitor plus the LCD cell capacitance to the output of the VCOM buffer. Because of these, short current pulses in the positive and negative direction appear at the output of the VCOM buffer. To minimize the output voltage ripple caused by the current pulses, a transconductance amplifier having a current source output and an output capacitor is used. The output capacitor supports the high frequency part of the current pulses drawn from the LCD panel. The VCOM buffer only needs to handle the low frequency portion of the current pulses. A 1-µF ceramic output capacitor is sufficient for most of the applications. When using other output capacitor values it is important to keep in mind that the output capacitor is part of the VCOM buffer loop stabilization.

The VCOM buffer has an integrated soft start to avoid voltage drops on V_O1 during start-up. The soft start is implemented as such that the VCOMIN is held low until the VCOM buffer is fully biased and the common mode range is reached. Then the positive input is released and the VCOM buffer output slowly comes up. Usually a 1-nF capacitor on VCOMIN to GND is used to filter high frequency noise coupled in from V_O1. The size of this capacitor together with the upper feedback resistor value determines the start-up time. The larger the capacitor from VCOMIN to GND, the slower the soft start.

8.2.1.2.5 Linear Regulator Controller

The TPS65100-Q1 device includes a linear regulator controller to generate a 3.3-V rail when the system is powered from a 5-V supply. Because an external NPN transistor is required, the input voltage of the TPS65100-Q1 device applied to VIN needs to be higher than the output voltage of the regulator. To provide a minimum base drive current of 13.5 mA, a minimum internal voltage drop of 500 mV from V_I to V_{base} is required. This can be translated into a minimum input voltage on V_I for a certain output voltage as Equation 13 shows:

$$V_{I(min)} = V_O4 + V_{BE} + 0.5\ V \quad (13)$$

The current design operating from V_I = 3.3 V cannot support this and the linear regulator is not used. The second example operating from V_I = 5 V has the 3.3-V regulator implemented.

The base drive current together with the h_{FE} of the external transistor determines the possible output current. External transistors are selected depending on the output current, power dissipation, and PCB space requirements of the application. The device is stable with a 4.7-µF ceramic output capacitor. Larger output capacitor values can be used to improve the load transient response when higher load currents are required.

8.2.1.3 Application Curves

Table 2. Table Of Graphs

		FIGURE
Main Boost Converter		
Efficiency V_O1	vs Load current	Figure 7
Efficiency V_O1	vs Load current	Figure 8
Efficiency V_O1	vs Input voltage	Figure 9
PWM operation, continuous mode		Figure 10
PWM operation at light load		Figure 11
Load transient response, C_O = 22 µF		Figure 12
Load transient response, C_O = 2 × 22 µF		Figure 13
Power-up sequencing		Figure 14
Soft start V_O1		Figure 15

Table 2. Table Of Graphs (continued)

		FIGURE
Negative Charge Pump		
V_O2 Maximum load current	vs Output voltage V_O1	Figure 16
Positive Charge Pump		
V_O3 Maximum load current	vs Output voltage V_O1 (doubler mode)	Figure 17
V_O3 Maximum load current	vs Output voltage V_O1 (tripler mode)	Figure 18

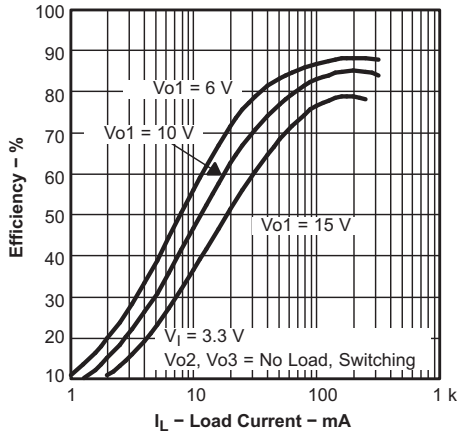


Figure 7. Efficiency V_O1 vs Load Current

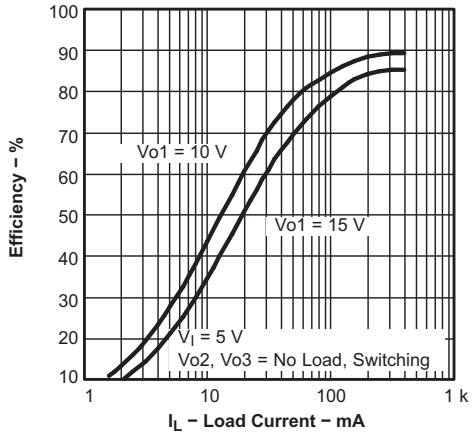


Figure 8. Efficiency V_O1 vs Load Current

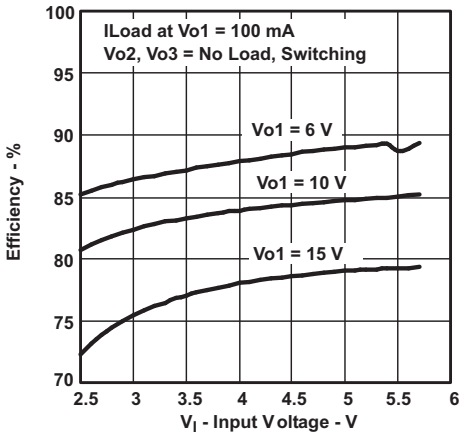


Figure 9. Efficiency V_O1 vs Input Voltage

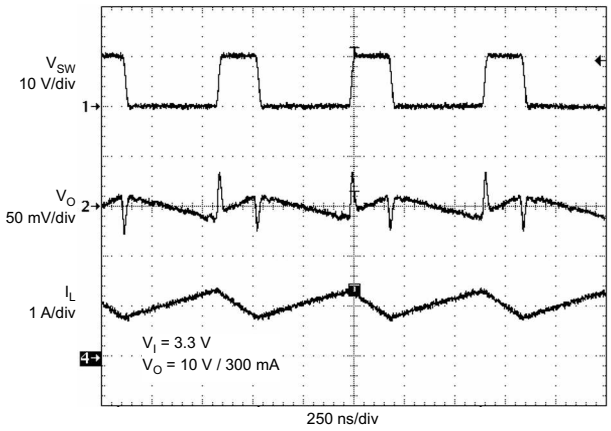


Figure 10. PWM Operation Continuous Mode

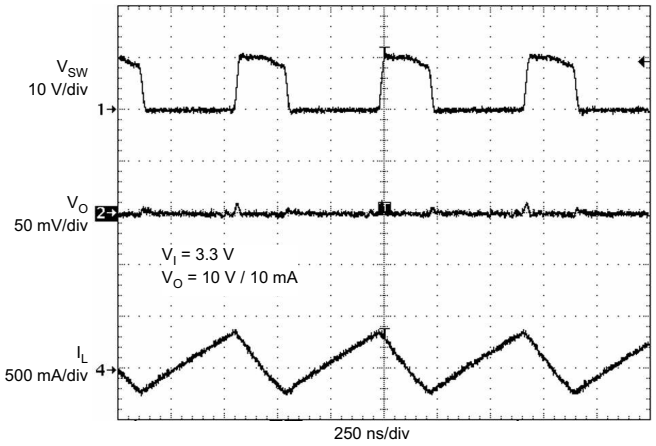


Figure 11. PWM Operation At Light Load

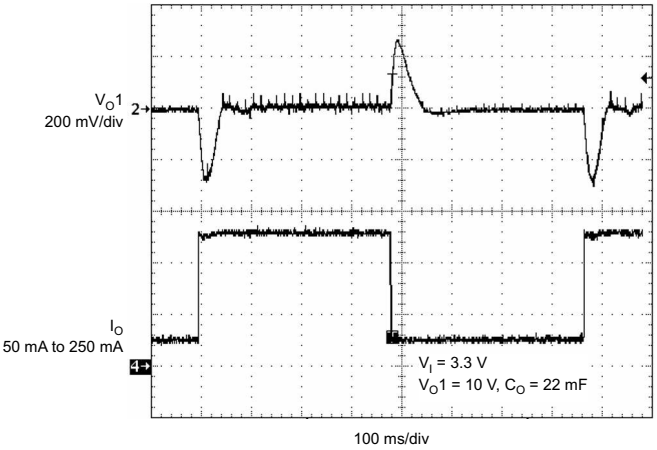


Figure 12. Load Transient Response 1 x C_O

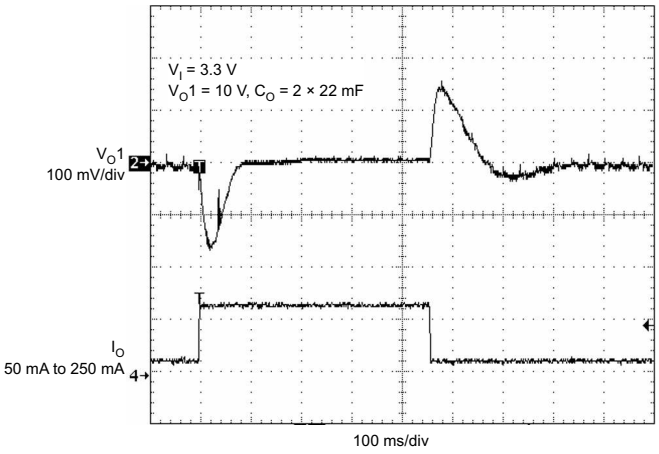


Figure 13. Load Transient Response 2 x C_O

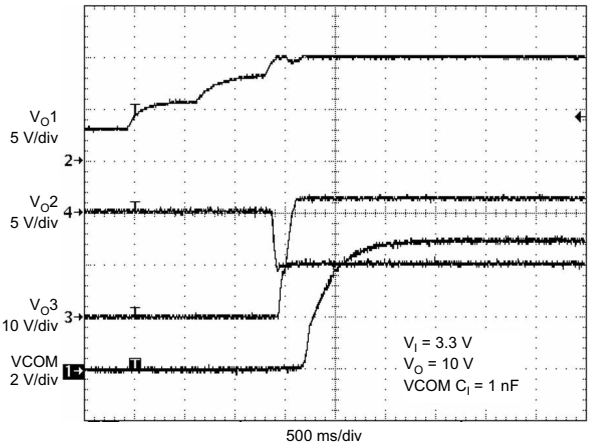


Figure 14. Power-Up Sequencing

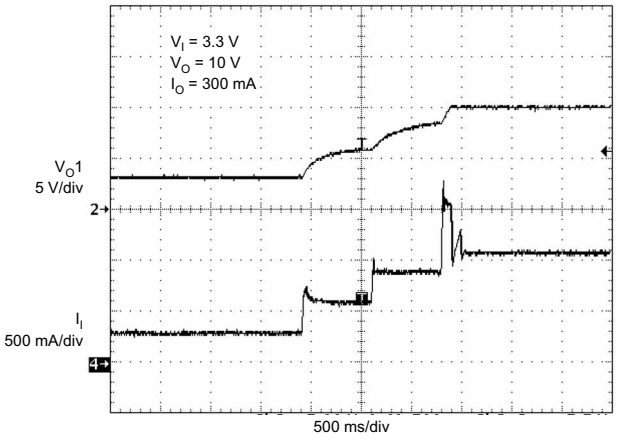


Figure 15. Soft Start V_O1

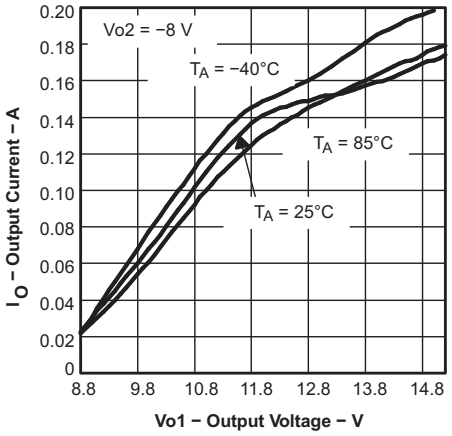


Figure 16. V_O2 Maximum Load Current

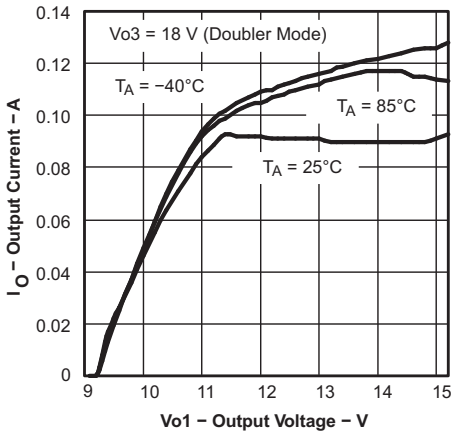


Figure 17. V_O3 Maximum Load Current (Doubler Mode)

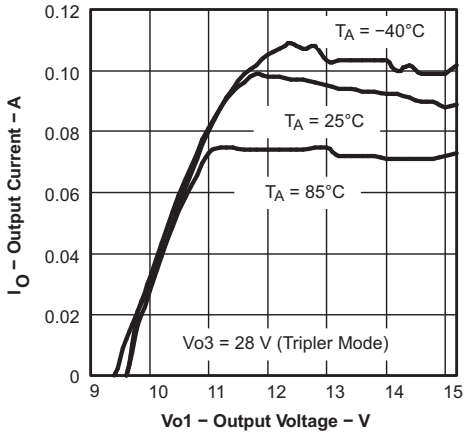


Figure 18. V_O3 Maximum Load Current (Tripler Mode)

8.2.2 Supply for a Typical Approximately 8-inch Display

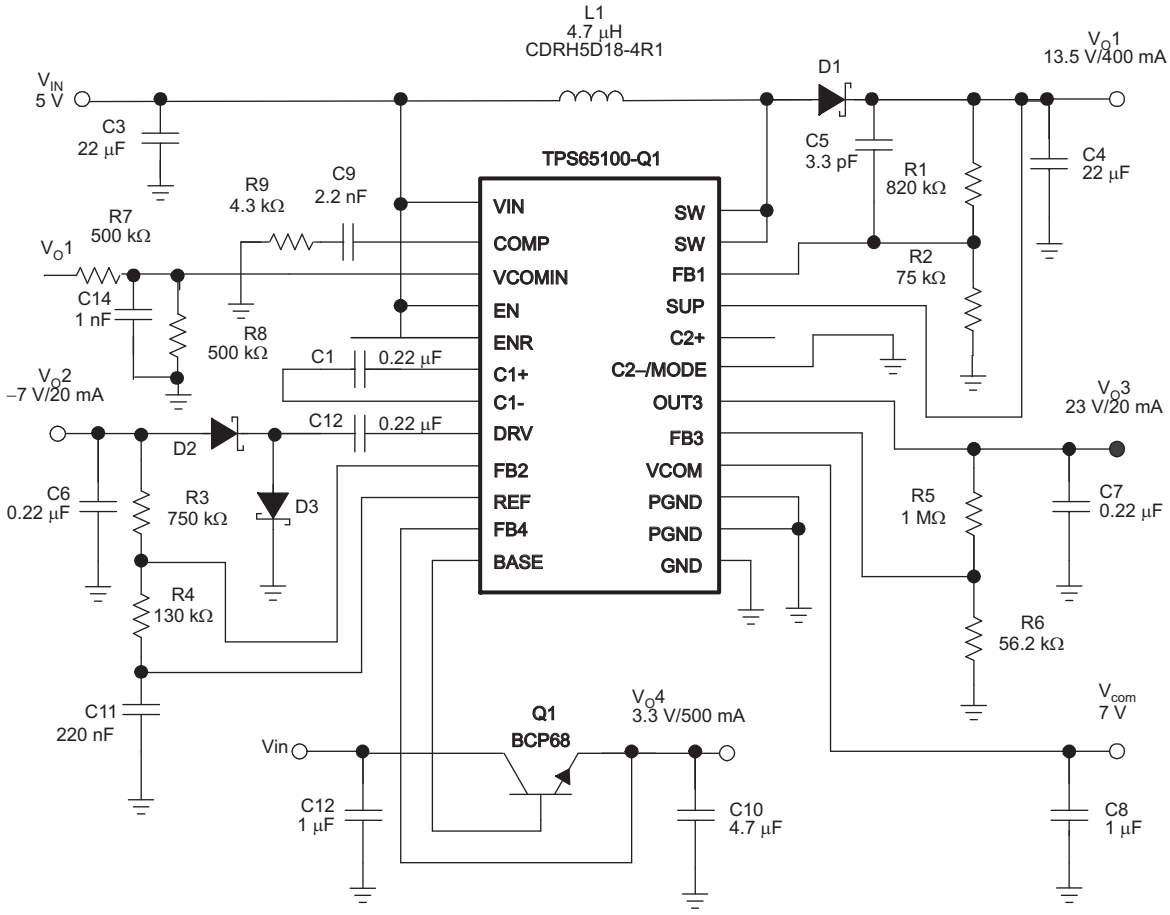


Figure 19. Simplified Schematic for a Typical Approximately 8-inch Display

9 Power Supply Recommendations

Apply a supply voltage of 2.7 V to 5.8 V to the VIN pin. In case the 3.3-V linear regulator is supposed to be used, a higher minimum voltage needs to be applied, allowing for some drop-out. As in most cases, the 3.3-V rail needs to come up before the main boost-converter does, an RC-element on the EN pin can delay the ramp of the boost converter.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high-peak currents and switching frequencies. If the layout is not carefully designed, the regulator might show stability and EMI problems. TI recommends the following PCB layout guidelines for the TPS65100-Q1 device:

- Connect PGND and AGND together on the same ground plane.
- Connect all capacitor grounds and PGND together on a common ground plane.
- Place the input filter capacitor as close as possible to the input pin of the IC.
- Route first the traces carrying high-switching currents with wide and short traces.
- Isolate analog signal paths from power paths.
- If vias are necessary, try to use more than one in parallel to decrease parasitics, especially for power traces.
- Solder the thermal pad to the PCB for good thermal performance

10.2 Layout Example

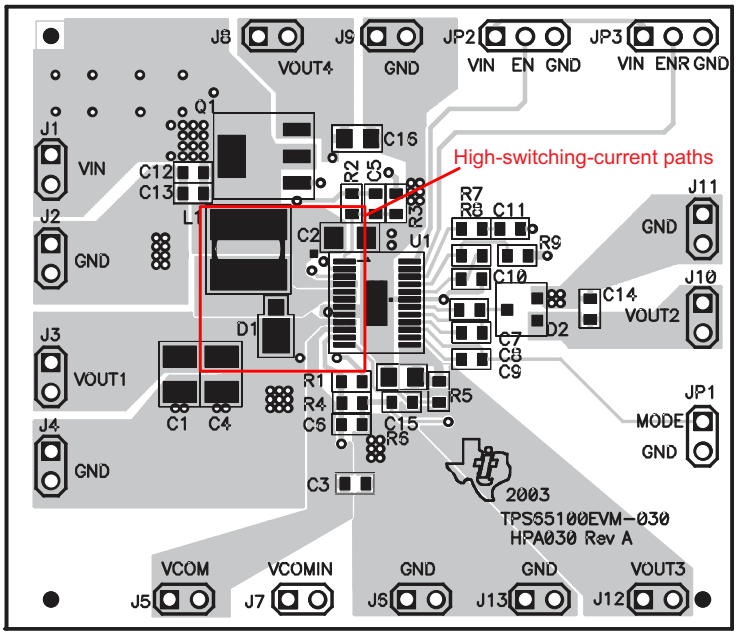


Figure 20. Layout Example

10.3 Thermal Considerations

An influential component of thermal performance of a package is board design. To take full advantage of the heat dissipation abilities of the PowerPAD package with exposed thermal die, a board that acts similar to a heat sink and allows the use of an exposed (and solderable) deep downset pad should be used. For further information, see *PowerPAD Thermally Enhanced Package*, SLMA002, and *PowerPAD Made Easy*, SLMA004.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *PowerPAD Thermally Enhanced Package*, SLMA002
- *PowerPAD Made Easy*, SLMA004
- *How to Compensate with the TPS6510x and TPS6514x*, SLVA813.
- *Basic Calculation of a Boost Converter's Power Stage*, SLVA372
- *Customizing Your TPS6510x/TPS6514x*, SLVA192
- *Power Management Guide 2016* at www.ti.com

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65100QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	65100Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS65100-Q1 :

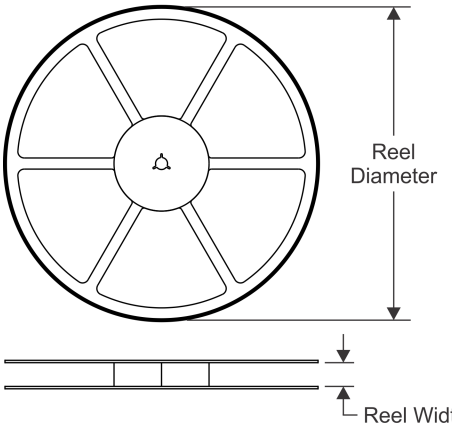
- Catalog: TPS65100

NOTE: Qualified Version Definitions:

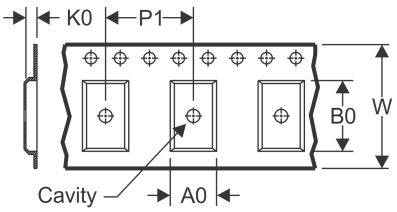
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

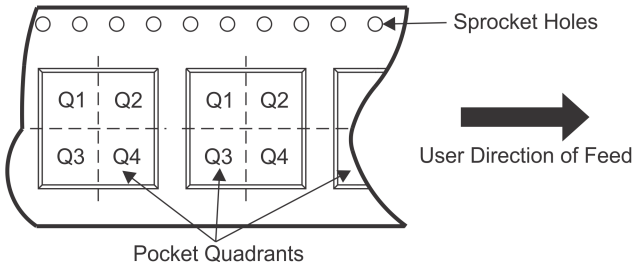


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

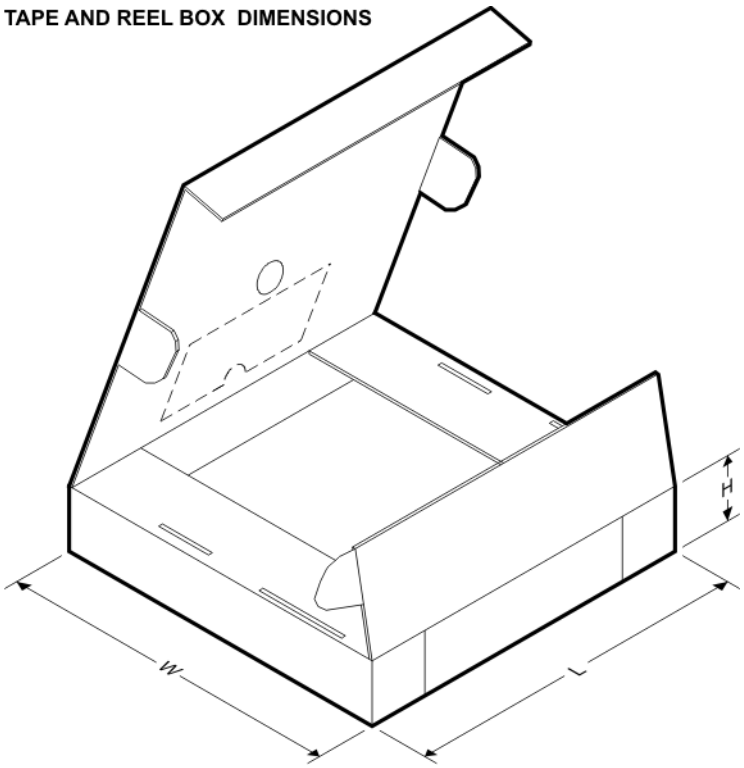
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65100QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65100QPWPRQ1	HTSSOP	PWP	24	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

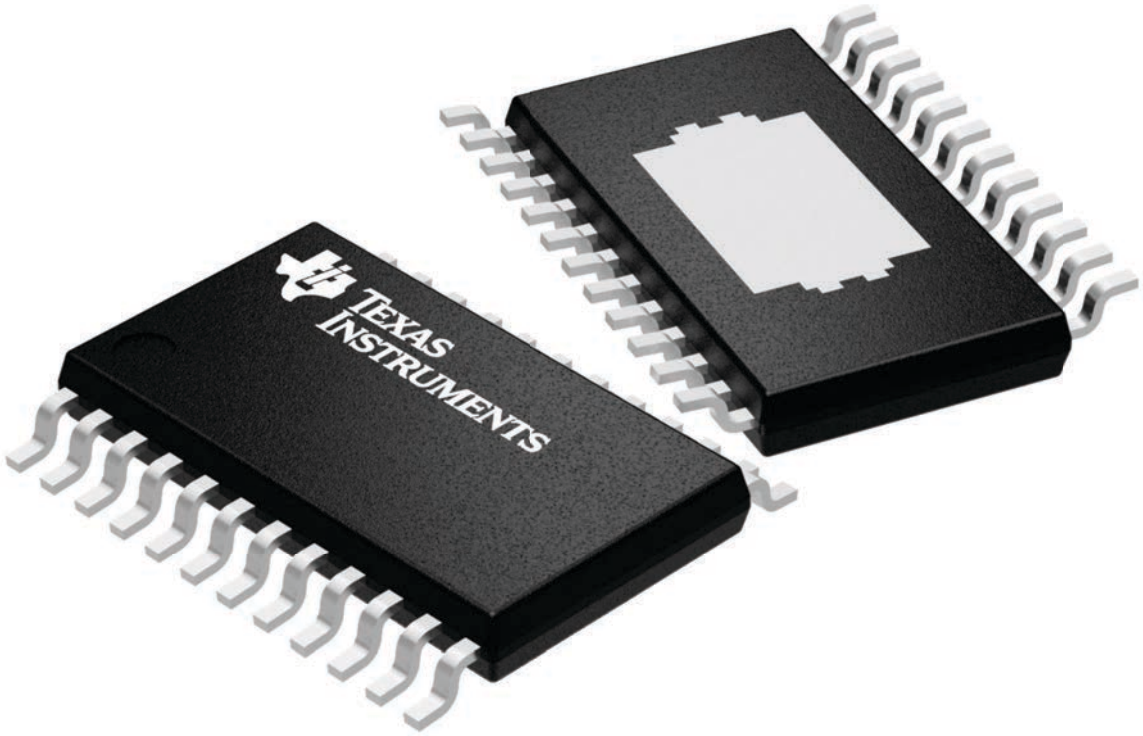
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



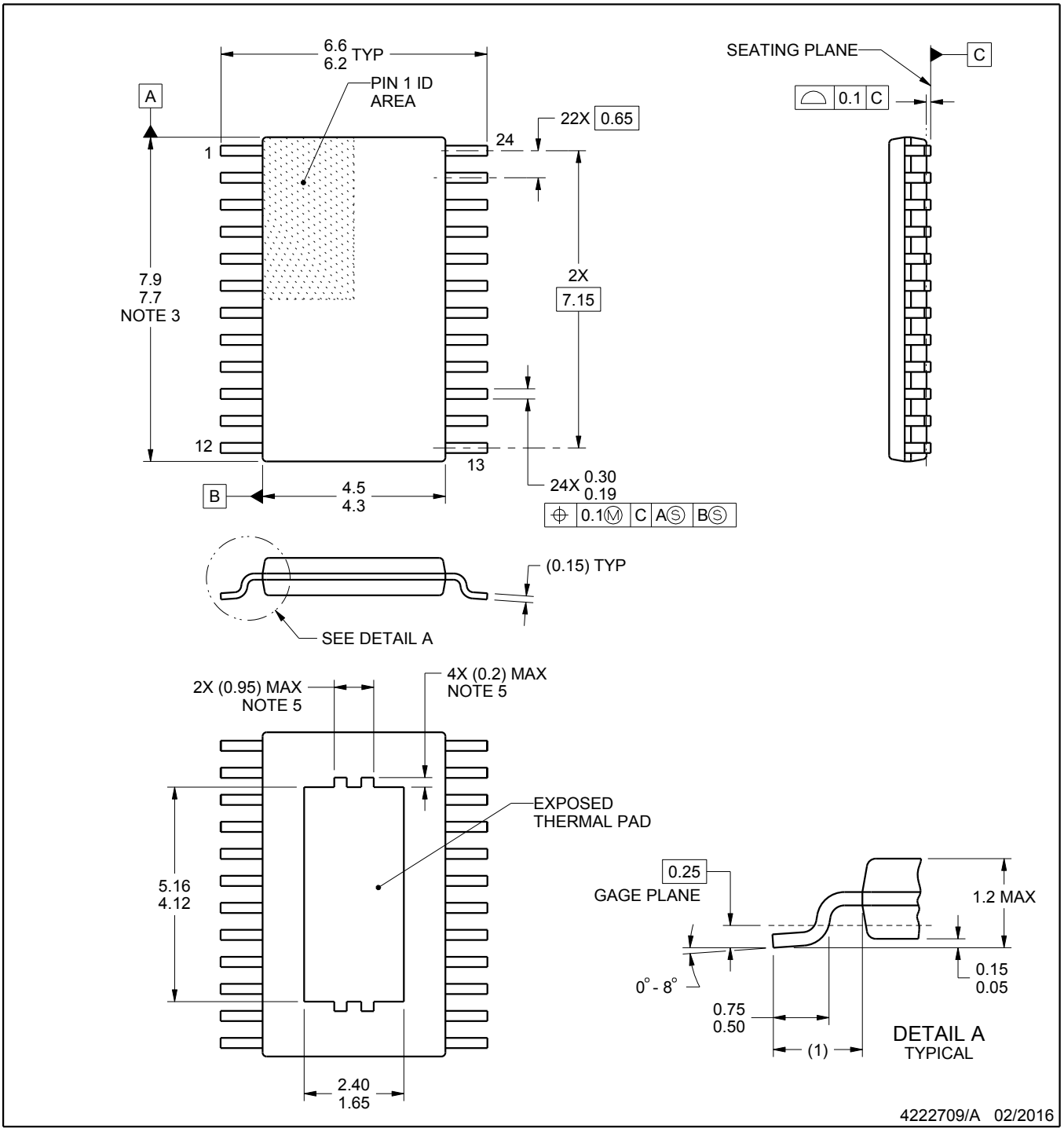
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

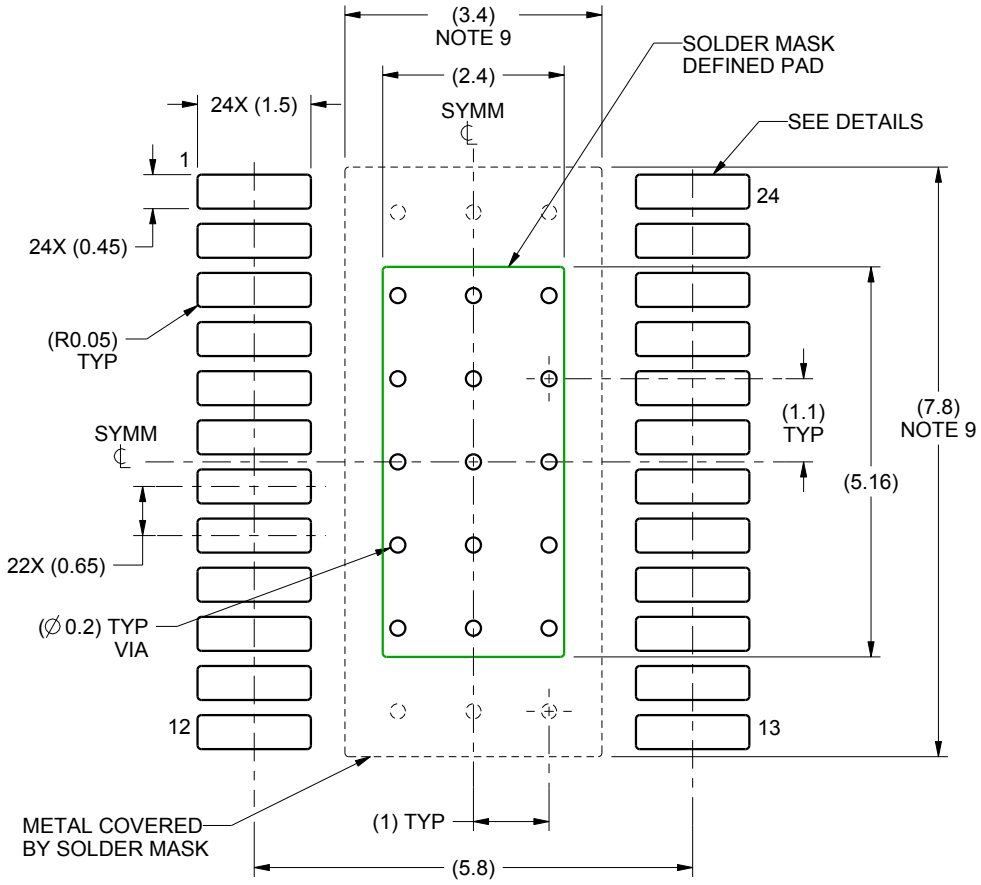
PLASTIC SMALL OUTLINE



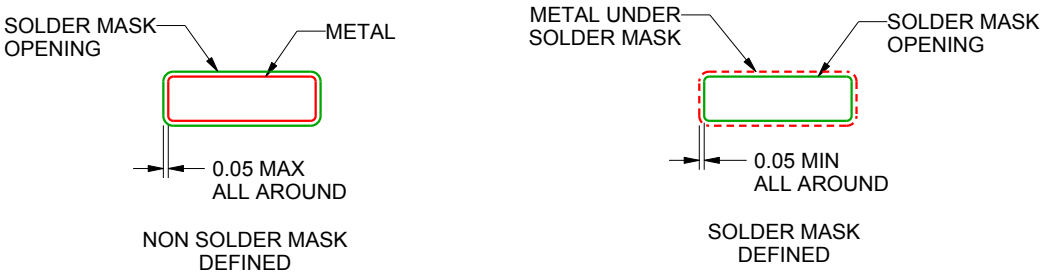
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

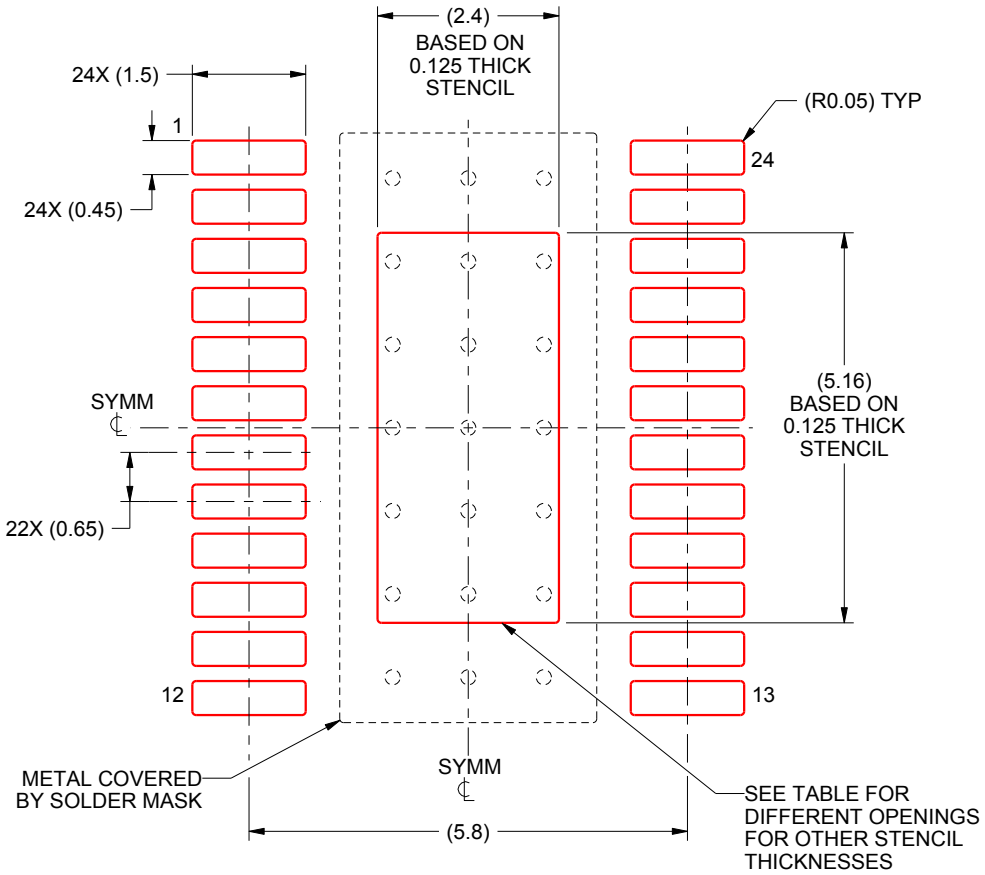


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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