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TPS65090

SLVSBO6B - JANUARY 2013 - REVISED JULY 2015

TPS65090 Front-End PMU With Switched-Mode Charger for 2 to 3 Cells In Series

Technical

Documents

1 Features

- Wide Input Voltage Charger and Power Path Management:
 - V_{IN} Range From 6 V to 17 V
 - Up to 4-A Output Current on the Power Path
 - Switched-Mode Charger; up to 4-A Maximum Charge Current
 - JEITA Compliant Charging Control
 - Thermal Regulation, Safety Timers
 - 2 Temperature Sense Inputs
- 3 Step-Down Converters:
 - High Efficiency Over a Wide Output Current Range
 - V_{IN} Range From 6 V to 17 V
 - 2 Fixed Output Voltages (5 V and 3.3 V)
 - Up to 5 A of Continuous Output Current
 - 1 Adjustable Output Voltage (From 1 V to 5 V)
 - Up to 4 A of Continuous Output Current
 - Output Voltage Accuracy ±1%
 - Typical 30-µA Quiescent Current Per Converter
- 2 Always-On LDOs:
 - 2 Fixed Output Voltages (5 V and 3.3 V)
 - Output Voltage Accuracy ±1%
 - Typical 10-µA Quiescent Current per LDO _
- 7 Current-Limited Load Switches:
 - One System Voltage Switch With 1-A Current Limit
 - One 5-V Switch With 200-mA Current Limit, **Reverse-Voltage Protected**
 - One 3.3-V Switch With 3-A Current Limit
 - Four 3.3-V Switches With 1-A Current Limit
 - All Switches Controlled by I²C Interface
- I²C Interface
 - _ Standard-Mode (100 kHz) Supported
 - Fast-Mode (400 kHz) Supported
 - Fast-Mode Plus (1000 kHz) Supported
 - High-Speed (3.4 MHz) Supported
- 16-Channel, 10-Bit Analog-to-Digital Converter (ADC)
- Available in a 9-mm × 9-mm, VQFN-100 Package

2 Applications

Battery-Powered Products Using 2 to 3 Li-Cells in Series

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Notebook Computers

Tools &

Software

- Mobile PCs and Mobile Internet Devices .
- Industrial Metering Equipment
- Personal Medical Products

3 Description

The TPS65090A device is a single-chip power management IC for portable applications consisting of a battery charger with power path management for a dual or triple Li-Ion or Li-Polymer cell battery pack. The charger can be directly connected to an external wall adapter. Three highly efficient step-down converters are targeted for providing a fixed 5-V system voltage, a fixed 3.3-V system voltage, and an adjustable voltage rail. The step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents. The step-down converters allow the use of small inductors and capacitors to achieve a small solution size. The TPS65090A also integrates two general-purpose always-on LDOs for powering circuit blocks which control the system while shut down. Each LDO operates with an input voltage range from 6 V to 17 V, allowing the LDOs to be supplied from the wall adapter or directly from the main battery pack.

Seven load switches are built into the device. These load switches can be used to control the power supply individually for certain circuit blocks in the application circuit. The current flowing through the load switches, as well as the output current of the step-down converters, the input current from the AC adapter and the charge current is monitored and can be read out using the digital interface.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)	
TPS65090A	VQFN-MR (100)	9.00 mm × 9.00 mm	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DC-DC Block Diagram





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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2013) to Revision B

Page

CI	Changes from Original (January 2013) to Revision A	
•	Added Differential Voltage spec condition "between CBC and LC", -0.3 MIN and 7 MAX	6
•	Changed text in ALWAYS ON LDOs and POWER PATH CONTROL sections for clarification	27
•	Changed text in CHARGER section for clarification	29
•	Added INTERRUPTS section for clarification	33
•	Added text to REVERSE VOLTAGE PROTECTION section for clarification	53
•	Changed graph title from "ADAPTER INPUT POWER UP AND POWER DOWN" to "SUPPLEMENT MODE OPERATION"	56
•	Added text to THERMAL INFORMATION section for clarification.	61



5 Pin Configuration and Functions



Pin Functions

PIN		1/0	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
POWER PATH	I CONTROL			
ACG	A51	0	Gate connection for AC adapter input switches	
ACN	A50	Ι	Shunt resistor sense connection for input current sensing	
ACP	B47	Ι	Shunt resistor sense connection for input current sensing	
ACS	B48	Ι	Source connection for AC adapter input switches	
BATG	A2	0	Gate connection for the battery switch	
VAC	A13	Ι	AC adapter supply input for charger control	
VACS	A14	I	AC adapter sense input for the charger	
CHARGER	•		•	
CBC	B2	Ι	Bootstrap capacitor connection for charger step-down converter	
ENC	A41	Ι	Enable input for charger (1: enabled, 0: disabled), must be connected to a valid logic signal	
FBC	A52	I	Voltage feedback input for charger step-down converter. Must be connected to an external feedback divider to program charge voltage.	
LC	A5, B4, B5	0	Inductor connection for switched-mode battery charger step-down converter	
PGNDC	A6, B6	_	Power Ground	
SRN	B1	Ι	Shunt resistor connection for battery charge current sensing	
SRP	A1	I	Shunt resistor connection for battery charge current sensing	
STAT	B13	0	Charge status pin, open-drain (charge in progress, charge complete, sleep mode, fault)	
TS1	A24	I	Temperature sensor input for temperature sensor 1	
TS2	B23	Ι	Temperature sensor input for temperature sensor 2	
VACG	A39	0	VAC good pin, open drain (1, high impedance : voltage good; 0 : voltage not available)	
VBAT	A15	Ι	Battery sense connection	

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FEXAS

Pin Functions (continued)

PIN			DECODIDETION	
NAME	NO.	1/0	DESCRIPTION	
VBATG	A38	0	VBAT good pin, open drain (1, high impedance : voltage good; 0 : voltage not available), pullup voltage should not be higher than voltage connected to	
VREFT	A25	I	Reference voltage output for temperature measurements	
VSYSC	A3, A4, B3	I	Switched-mode battery charger step-down converter supply voltage	
VSYSG	B36	0	VSYS good pin, open drain (1, high impedance : voltage good; 0 : voltage not available)	
DCDC1	I			
CB1	B44	I	Bootstrap capacitor connection for DCDC1	
EN1	B38	I	Enable input for DCDC1 (1: enabled, 0: disabled), must be connected to a valid logic signal	
FB1	B37	I	Output voltage sense input for DCDC1	
L1	A45, B41, B42	0	Inductor connection for DCDC1 step-down converter	
PGND1	A43, A44, B40	_	Power Ground	
VDCDC1	A48	I	Output voltage connection of DCDC1	
VSYS1	A46, A47, B43	I	Supply voltage input for DCDC1 step-down converter	
DCDC2				
CB2	B17	I	Bootstrap capacitor connection for DCDC2	
EN2	A42	I	Enable input for DCDC2 (1: enabled, 0: disabled), must be connected to a valid logic signal	
FB2	B24	I	Output voltage sense input for DCDC2	
L2	A21, B19, B20	0	Inductor connection for DCDC2 step-down converter	
PGND2	A22, A23, B21, B22	_	Power Ground	
VDCDC2	A18	I	Output voltage connection of DCDC2	
VSYS2	A19, A20, B18	I	Supply voltage input for DCDC2 step-down converter	
DCDC3				
CB3	A12	I	Bootstrap capacitor connection for DCDC3	
EN3	A26	I	Enable input for DCDC3 (1: enabled, 0: disabled), must be connected to a valid logic signal	
FB3	B14	I	Output voltage feedback input for DCDC3, a resistive feedback divider must be connected	
L3	A9, B8, B9	0	Inductor connection for DCDC3 step-down converter	
PGND3	A7, A8, B7	—	Power Ground	
VDCDC3	A16	I	Output voltage sense input for DCDC3	
VSYS3	A10, A11, B10, B11	I	Supply voltage input for DCDC3 step-down converter	
LDO1				
FB_L1	B46	I	Output voltage sense input for LDO1	
VLDO1	B45	0	Output of the LDO1 linear regulator	
VSYS_L1	A49	I	Supply voltage input for LDO1 linear regulator	
LDO2				
FB_L2	B15	I	Output voltage sense input for LDO2	
VLDO2	B16	0	Output of the LDO2 linear regulator	
VSYS_L2	A17	I	Supply voltage input for LDO2 linear regulator	
FET1				
INFET1	B28	I	Supply voltage input for load switch FET1, connect to GND, if not used	
VFET1	A30	0	Output of load switch FET1, leave unconnected if not used	
FET2		1		
INFET2	B29	I	Supply voltage input for load switch FET2, connect to GND, if not used	

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Pin Functions (continued)

PIN			DECODIDEION	
NAME	NO.	1/0	DESCRIPTION	
VFET2	A31	0	Output of load switch FET2, leave unconnected if not used	
FET3				
INFET3	A34, B31	I	Supply voltage input for load switch FET3, connect to GND, if not used	
VFET3	A32, B30	0	Output of load switch FET3, leave unconnected if not used	
FET4				
INFET4	B34	I	Supply voltage input for load switch FET4, connect to GND, if not used	
VFET4	A37	0	Output of load switch FET4, leave unconnected if not used	
FET5	-		•	
INFET5	B33	I	Supply voltage input for load switch FET5, connect to GND, if not used	
VFET5	A36	0	Output of load switch FET5, leave unconnected if not used	
FET6				
INFET6	B32	I	Supply voltage input for load switch FET6, connect to GND, if not used	
VFET6	A35	0	Output of load switch FET6, leave unconnected if not used	
FET7				
INFET7	B27	I	Supply voltage input for load switch FET7, connect to GND, if not used	
VFET7	A29	0	Output of load switch FET7, leave unconnected if not used	
DIGITAL INTE	ERFACE/CONT	ROL		
AGND	A33	—	Analog ground	
GND	A40	—	Logic ground	
IRQ	B12	0	Interrupt output, open drain, (1, high impedance : no interrupt; 0 : interrupt) details on events available through I ² C	
PGND	C1, C2, C3, C4	_	Internally connected to PowerPAD [™]	
PowerPAD		_	Must be soldered to achieve appropriate power dissipation. Must be connected to PGND.	
SCL	B25	I/O	Clock input for the I ² C interface	
SDA	A27	I/O	Data line for the I ² C interface	
VCTRL	B39	0	Internal control supply decoupling capacitor connection	
VREF	B35	0	Reference voltage decoupling capacitor connection	
VREFADC	B26	0	ADC reference voltage decoupling capacitor connection	



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
POWER PATH CONT	ROL			I
(2)	VAC, VACS	-0.3	30	
Voltage	ACP, ACN, ACS, BATG	-0.3	20	- V
	between ACP and ACN	-0.5	0.5	
Differential Voltage	between ACG and ACS	-0.3	7	V
CHARGER				
	VSYSC, VBAT, LC, SRP, SRN, STAT	-0.3	20	
Voltage ⁽²⁾	FBC, TS1, TS2, VREFT	-0.3	7	V
-	ENC	-0.3	3.6	
	between SRP and SRN	-0.5	0.5	
Differential Voltage	between CBC and LC	-0.3	7	V
DCDC1				1
	VSYS1, L1	-0.3	20	
Voltage ⁽²⁾	FB1, VDCDC1	-0.3	7	V
	EN1	-0.3	3.6	_
Differential Voltage	between CB1 and L1	-0.3	7	V
DCDC2				1L
	VSYS2, L2	-0.3	20	
Voltage ⁽²⁾	FB2, VDCDC2	-0.3	3.6	V
	EN2	-0.3	3.6	
Differential Voltage	between CB2 and L2	-0.3	7	V
DCDC3				
	VSYS3, L3	-0.3	20	
Voltage ⁽²⁾	FB3, VDCDC3	-0.3	7	V
	EN3	-0.3	3.6	
Differential Voltage	between CB3 and L3	-0.3	7	V
LDO1				
Valtage ⁽²⁾	VSYS_L1	-0.3	20	V
vollage	VLDO1, FB_L1	-0.3	7	V
LDO2				
Valtage ⁽²⁾	VSYS_L2	-0.3	20	N/
Vollage	VLDO2, FB_L2	-0.3	3.6	v
FET1				
Voltage ⁽²⁾	INFET1, VFET1	-0.3	20	V
FET2				
Voltage ⁽²⁾	INFET2, VFET2	-0.3	6	V
FET3				
Voltage ⁽²⁾	INFET3, VFET3	-0.3	6	V
FET4				
Voltage ⁽²⁾	INFET4, VFET4	-0.3	6	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.



Absolute Maximum Ratings (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
FET5				
Voltage ⁽²⁾	INFET5, VFET5	-0.3	6	V
FET6				
Voltage ⁽²⁾	INFET6, VFET6	-0.3	6	V
FET7				
Voltage ⁽²⁾	INFET7, VFET7	-0.3	6	V
DIGITAL INTERFA	CE/CONTROL			
Voltage ⁽²⁾	SDAT, SCLK, IRQ, VCTRL, VCTRL2, VACG, VSYSG, VBATG	-0.3	7	N
	VREFADC, VREF	-0.3	3.6	V
GENERAL				
Temperature	Operating junction, T _J	-40	150	*0
	Storage temperature, T _{stg}	-65	150	C

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101 $^{\left(2\right) }$	±500	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM MAX	UNIT
POWER PATH CONTROL			
Supply voltage at VAC	6	17	V
Differential voltage between ACP and ACN	-0.2	0.2	V
CHARGER			
Supply voltage at VSYSC, VBAT	6	17	V
Differential voltage between SRP and SRN	-0.2	0.2	V
DCDC1			
Supply voltage at VSYS1	6	17	V
DCDC2			
Supply voltage at VSYS2	6	17	V
DCDC3			
Supply voltage at VSYS3	6	17	V
LD01			
Supply voltage at VSYS_L1	6	17	V
LDO2			
Supply voltage at VSYS_L2	6	17	V
FET1			
Supply voltage at INFET1	5	17	V
FET2			
Supply voltage at INFET2	4.5	5.5	V
FET3			
Supply voltage at INFET3	3	5.5	V
FET4			
Supply voltage at INFET4	3	5.5	V

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Recommended Operating Conditions (continued)

	MIN	NOM MAX	UNIT
FET5			
Supply voltage at INFET5	3	5.5	V
FET6			
Supply voltage at INFET6	3	5.5	V
FET7			
Supply voltage at INFET7	3	5.5	V
CONTROL			
Supply voltage at VCTRL2	3	5.5	V
GENERAL			
Operating free-air temperature, T _A	-40	85	°C
Operating junction temperature, T _J	-40	125	°C

6.4 Thermal Information

		TPS65090A	
	THERMAL METRIC ⁽¹⁾	RVN [VQFN-MR]	UNIT
		100 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	24.8	°C/W
R _{0JC(top)}	Junction-to-case(top) thermal resistance	5.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.9	°C/W
TLΨ	Junction-to-top characterization parameter	0.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	3.9	°C/W
R _{0JC(bot)}	Junction-to-case(bottom) thermal resistance	0.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics - Power Path Control

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VAC overvoltage disconnect		17	17.6	18.2	V
VAC overvoltage hysteresis			550		mV
VAC undervoltage lockout	V _{AC} voltage decreasing	5	5.5	6	V
VAC undervoltage lockout hysteresis			550		mV
Maximum input DPM current programming range		1000		4000	mA
(V _{ACP} - V _{ACN}) voltage to maximum input DPM current gain			100		A / V
	$V_{ACP} - V_{ACN}$, IACSET = 0	40	44	48	mV
Input DPM current regulation	$V_{ACP} - V_{ACN}$, IACSET = 1	36	40	44	mV
Maximum battery discharge current	V_{BAT} - V_{SRN} , IBATSET = 0, $T_A = 25^{\circ}C$	17.5	20	21	mV
comparator threshold	V_{BAT} - V_{SRN} , IBATSET = 1, $T_A = 25^{\circ}C$	15	17.5	18.5	mV
VACS input impedance			1000		kΩ
VAC input impedance			25		kΩ
Gate drive current on ACG		12			μA
Gate drive current on BATG	Turnon	500			μA
Gate drive current on BATG	Turnoff	25			mA
BATG turnoff delay time after adapter is detected			30		ms



Electrical Characteristics - Power Path Control (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Quiescent current into VAC	Charging enabled, V _{AC} = 11.5 V		2.5	5	mA
		Charging disabled, V_{AC} = 11.5 V		1	1.5	mA
	Leakage current into ACP and ACN	Charging disabled			80	μA
V _{SUPPL}	Supplement threshold to turn on battery switch	V _{SRN} - V _{ACN} rising	13	45	84	mV
V _{SUPPL_} hys	Supplement mode hysteresis to turn off battery switch	V _{SRN} - V _{ACN} falling		20		mV
I _{ACRC}	Reverse adapter current threshold	V _{ACN} - V _{ACP} rising		45		mV
V _{SLEEP}	SLEEP mode threshold	V _{AC} – V _{SRN} falling	20	90	150	mV
V _{SLEEP_} HYS	SLEEP mode hysteresis	V _{AC} – V _{SRN} rising		200		mV

6.6 Electrical Characteristics - Charger

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARG	ER - POWER					
		VSET = 00, default for T_{01} and T_{40}	1.98	2	2.02	
V	Charger feedback valters	VSET = 01, default for T_{12}	2.03	2.05	2.07	N/
VFBC	Charger feedback voltage	VSET = 10, default for T_{34}	2.055	2.075	2.095	V
		VSET = 11, default for T ₂₃	2.08	2.1	2.12	-
	Leakage current into FBC				0.1	μA
		VSET = 00, ENRECG = 1	1.925	1.950	1.975	
V	Charger feedback voltage for automatic	VSET = 01, ENRECG = 1	1.975	2	2.025	
V _{FBCR}	charge restart	VSET = 10, ENRECG = 1	2	2.025	2.05	V
		VSET = 11, ENRECG = 1	2.025	2.05	2.075	
I _{CHARGE}	Maximum charge current programming		1000		4000	mA
	(V _{SRP} - V _{SRN}) voltage to maximum charge current gain			100		A / V
		ISET = 000		0%		
		ISET = 001		25%		
	20	ISET = 010		37.5%		
		ISET = 011, default for T_{12} and T_{34} battery temperature range		50%		
	I-C programmable charge current	ISET = 100		62.5%		
		ISET = 101		75%		
		ISET = 110		87.5%		
		ISET = 111, default for T ₂₃ battery temperature range		100%		
		V_{SRP} - V_{SRN} = 40 mV typical, T_J < 100 °C	38.5	40	42.5	
	Charge current sense regulation voltage	V_{SRP} - V_{SRN} = 20 mV typical, T _J < 100 °C	18.5	20	22	mV
		V_{SRP} - V_{SRN} = 4 mV typical, T_J < 100 °C	2.3	4	5.9	
	Minimum programmable charge current			100		mA
	Precharge current			0.1 *		
				I _{CHARGE}		
	Termination current			0.1 *		
	Lookage aurrent into SBN and SBD	V ~ 12 V		CHARGE	AE	
	Leakage current into SKN and SKP	VBAT < IZ V			40	μΑ

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Electrical Characteristics - Charger (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Switching frequency		1360	1600	1840	kHz
R _{DSON}	High-side switch ON-resistance			25		mΩ
R _{DSON}	Low-side switch ON-resistance			60		mΩ
CHARG	ER - CONTROL					
	Precharge timer		1600	1800	2000	S
	Fast-charge safety timer programming		2		10	h
	Fast-charge safety timer accuracy				10%	
		FASTTIME = 000, default setting		2		
		FASTTIME = 001		3		
		FASTTIME = 010		4		
	I ² C programmable values for fast-charge	FASTTIME = 011		5		h
	safety timer	FASTTIME = 100		6		
		FASTTIME = 101		7		
		FASTTIME = 110		8		
		FASTTIME = 111		10		
	Battery detection discharge timer			1		S
	Battery detection discharge current		5		20	mA
	Battery detection discharge current after timer fault			2		mA
V _{FBCL}	Battery detection discharge feedback voltage threshold for battery OK		1.43	1.45	1.47	V
	Battery feedback voltage threshold for precharge to fast-charge transition		1.43	1.45	1.47	V
	Battery detection charge timer			0.5		S
	Battery detection charge current sense regulation voltage	V_{SRP} - V_{SRN} = 2 mV typical, T _J < 100 °C	0.5	2	3.8	mV
		VSET = 00	1.925	1.95	1.975	
	Battery detection charge feedback voltage	VSET = 01	1.975	2	2.025	N/
	threshold for battery OK	VSET = 10	2	2.025	2.05	V
		VSET = 11	2.025	2.05	2.075	
	Minimum battery feedback voltage for battery good detection	Voltage at FBC increasing	1.44	1.5	1.54	V
	Maximum battery feedback voltage for battery good detection	Voltage at FBC increasing	2.18	2.25	2.28	V
	Battery cell temperature measurement, ratio of V _{TS1,2} compared to V _{REFTS} , l^2C programming option for T ₁	Sensor temperature is -10°C, T_SET = 000	71.9%	72.4%	72.9%	
	Voltage ratio threshold hysteresis	Sensor temperature is -10°C, voltage decreasing		0.2%		
T ₁	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	Default value, Sensor temperature is 0°C, T_SET = 001	70.4%	71%	71.5%	
	Voltage ratio threshold hysteresis	Sensor temperature is 0°C, voltage decreasing		0.2%		
T ₂	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	Default value, Sensor temperature is 10°C, T_SET = 010	68.1%	68.7%	69.2%	
	Voltage ratio threshold hysteresis	Sensor temperature is 10°C, voltage decreasing		0.4%		
	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS} , I^2C programming option for T_2	Sensor temperature is 15°C, T_SET = 011	67%	67.4%	67.9%	



Electrical Characteristics - Charger (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
	Voltage ratio threshold hysteresis	Sensor temperature is 15°C, voltage decreasing		0.4%		
	Battery cell temperature measurement, ratio of V _{TS1,2} compared to V _{REFTS} , I^2C programming option for T ₃	Sensor temperature is 40°C, T_SET = 100	59.3%	59.7%	60.1%	
	Voltage ratio threshold hysteresis	Sensor temperature is 40°C, voltage increasing		0.9%		
T ₃	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	Default value, Sensor temperature is 45°C, T_SET = 101	57.1%	57.6%	57.9%	
	Voltage ratio threshold hysteresis	Sensor temperature is 45°C, voltage increasing		0.9%		
	Battery cell temperature measurement, ratio of V _{TS1,2} compared to V _{REFTS} , I^2C programming option for T ₃ or T ₄	Sensor temperature is 50°C, T_SET = 110	54.7%	55.2%	55.8%	
	Voltage ratio threshold hysteresis	Sensor temperature is 50°C, voltage increasing		1.1%		
T ₄	Battery cell temperature measurement, ratio of $V_{TS1,2}$ compared to V_{REFTS}	Default value, Sensor temperature is 60°C, T_SET = 111	49.6%	50.1%	50.5%	
	Voltage ratio threshold hysteresis	Sensor temperature is 60°C, voltage increasing		1.1%		
	Output voltage at VREFT	Internally connected to VLDO2		3.3		V
	Output impedance of VREFT			4		kΩ
	Quiescent current into VBAT	Charging active			25	μA
	Quiescent current into VBAT	Charging suspended			150	μA
V _{IL}	ENC input low voltage				0.4	V
VIH	ENC input high voltage		1.2			V
	ENC input current	Clamped on GND or 3.3V		0.01	0.1	μA
	Charge current derating starting temperature	Junction temperature increasing		100		°C
	Charge current derating starting voltage	V _{SYSC} decreasing	6.7	7.3	7.6	V
	Overtemperature protection		125	140	150	°C
	Overtemperature hysteresis			20		°C

6.7 Electrical Characteristics - DC-DC Converters

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCDC1	- POWER					
	Output voltage	Power save mode disabled	5	5.05	5.125	V
	Switch valley current limit	$T_A = 25^{\circ}C$	5500			mA
	High-side switch ON-resistance			20		mΩ
	Low-side switch ON-resistance			20		mΩ
	Maximum line regulation			0.5%		
	Maximum load regulation			0.5%		
	Output auto-discharge resistance			300	400	Ω
	FB1 input impedance	V _{EN1} = 1		1		MΩ
	Shutdown current into VSYS1	V _{SYS1} = 7.2 V, EN1 = 0			1	μA
DCDC1	- CONTROL					
VIL	EN1 input low voltage				0.4	V
V_{IH}	EN1 input high voltage		1.2			V

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Electrical Characteristics - DC-DC Converters (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	EN1 input current	Clamped on GND or 3.3 V		0.01	0.1	μA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
DCDC	2 - POWER					
	Output voltage	Power save mode disabled	3.3	3.333	3.383	V
	Switch valley current limit	$T_A = 25^{\circ}C$	5500			mA
	High-side switch ON-resistance			20		mΩ
	Low-side switch ON-resistance			20		mΩ
	Maximum line regulation			0.5%		
	Maximum load regulation			0.5%		
	Output auto-discharge resistance			300	400	Ω
	FB2 input impedance	V _{EN2} = 1		1		MΩ
	Shutdown current into VSYS2	V _{SYS2} = 7.2 V, EN2 = 0			1	μA
DCDC	2 - CONTROL					
V _{IL}	EN2 input low voltage				0.4	V
V _{IH}	EN2 input high voltage		1.2			V
	EN2 input current	Clamped on GND or 3.3 V		0.01	0.1	μA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
DCDC	3 - POWER					
	Feedback voltage		792	800	808	mV
	Switch valley current limit	$T_A = 25^{\circ}C$	4200			mA
	High-side switch ON-resistance			20		mΩ
	Low-side switch ON-resistance			20		mΩ
	Maximum line regulation			0.5%		
	Maximum load regulation			0.5%		
	Output auto-discharge resistance			300	400	Ω
	Leakage current into FB3				0.1	μA
	Shutdown current into VSYS3	V _{SYS3} = 7.2 V, EN3 = 0			1	μA
DCDC	3 - CONTROL					
V _{IL}	EN3 input low voltage				0.4	V
V _{IH}	EN3 input high voltage		1.2			V
	EN3 input current	Clamped on GND or 3.3 V		0.01	0.1	μA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C



6.8 Electrical Characteristics - Linear Regulators

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO1					
Output voltage	I _{OUTLDO1} = 1 mA	4.90	4.95	5	V
LDO1 current limit	$T_A = 25^{\circ}C$	30	50	120	mA
LDO1 maximum output current	DCDC1 active (bypass switch turned on), V_{SYS} = 7.5 V		120		mA
Maximum line regulation			0.5%		
Maximum load regulation			0.5%		
FB_L1 input impedance			1		MΩ
Quiescent current into VSYS_L1 and VSYS_L2	DCDC1 and DCDC2 are enabled			35	μA
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C
LDO2					
Output voltage	I _{OUTLDO2} = 1 mA	3.233	3.267	3.3	V
LDO2 current limit	$T_A = 25^{\circ}C$	30	50	120	mA
LDO2 maximum output current	DCDC2 active (bypass switch turned on), V_{SYS} = 7.5 V		120		mA
Maximum line regulation			0.5%		
Maximum load regulation			0.5%		
FB_L2 input impedance			1		MΩ
Quiescent current into VSYS_L2 and VSYS_L1	DCDC1 and DCDC2 are enabled			35	μA
Overtemperature protection			140		°C
Overtemperature hysteresis			20		°C

6.9 Electrical Characteristics - Load Switches

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FET1				·	
Overcurrent detect threshold	$T_A = 25^{\circ}C$	1000		1200	mA
Switch ON-resistance				120	mΩ
Output auto-discharge resistance			800		Ω
Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
Switch current limit - time-out	Multiplier set to 1, WTFET1 = 00	200		250	μs
Switch current limit - time-out	Multiplier set to 4, WTFET1 = 01	800		1000	μs
Switch current limit - time-out	Multiplier set to 8, WTFET1 = 10	1600		2000	μs
Switch current limit - time-out	Multiplier set to 16, WTFET1 = 11	3200		4000	μs
Leakage current into INFET1	FET1 disabled, V _{FET1} = 0 V		1		μA
FET2					
Overcurrent detect threshold	$T_A = 25^{\circ}C$	200		240	mA
Switch ON-resistance				500	mΩ
Output auto-discharge resistance			300		Ω
Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
Switch current limit - time-out	Multiplier set to 1, WTFET2 = 00	200		250	μs
Switch current limit - time-out	Multiplier set to 4, WTFET2 = 01	800		1000	μs
Switch current limit - time-out	Multiplier set to 8, WTFET2 = 10	1600		2000	μs
Switch current limit - time-out	Multiplier set to 16, WTFET2 = 11	3200		4000	μs

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Electrical Characteristics - Load Switches (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Shutdown current into INFET2	FET2 disabled, V _{FET2} = 0 V		5		μA
	Reverse leakage current	FET disabled, VFET2 > INFET2		10		μA
FET3					ļ	
	Overcurrent detect threshold	$T_A = 25^{\circ}C$	3000		3600	mA
	Switch ON-resistance				45	mΩ
	Output auto-discharge resistance			300		Ω
	Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
	Switch current limit - time-out	Multiplier set to 1, WTFET3 = 00	200		250	μs
	Switch current limit - time-out	Multiplier set to 4, WTFET3 = 01	800		1000	μs
	Switch current limit - time-out	Multiplier set to 8, WTFET3 = 10	1600		2000	μs
	Switch current limit - time-out	Multiplier set to 16, WTFET3 = 11	3200		4000	μs
	Leakage current into INFET3	FET3 disabled, $V_{FET3} = 0 V$		3		μA
FET4						
	Overcurrent detect threshold	$T_A = 25^{\circ}C$	1000		1200	mA
	Switch ON-resistance				80	mΩ
	Output auto-discharge resistance			300		Ω
	Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
	Switch current limit - time-out	Multiplier set to 1, WTFET4 = 00	200		250	μs
	Switch current limit - time-out	Multiplier set to 4, WTFET4 = 01	800		1000	μs
	Switch current limit - time-out	Multiplier set to 8, WTFET4 = 10	1600		2000	μs
	Switch current limit - time-out	Multiplier set to 16, WTFET4 = 11	3200		4000	μs
	Leakage current into INFET4	FET4 disabled, $V_{FET4} = 0 V$		1		μΑ
FET5		1				
	Overcurrent detect threshold	$T_A = 25^{\circ}C$	1000		1200	mA
	Switch ON-resistance				80	mΩ
	Output auto-discharge resistance			300		Ω
	Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
	Switch current limit - time-out	Multiplier set to 1, WTFET5 = 00	200		250	μs
	Switch current limit - time-out	Multiplier set to 4, WTFET5 = 01	800		1000	μs
	Switch current limit - time-out	Multiplier set to 8, WTFET5 = 10	1600		2000	μs
	Switch current limit - time-out	Multiplier set to 16, WTFET5 = 11	3200		4000	μs
	Leakage current into INFET5	FET5 disabled, $V_{FET5} = 0 V$		1		μA
FET6		1	1			
	Overcurrent detect threshold	$T_A = 25^{\circ}C$	1000		1200	mA
	Switch ON-resistance				80	mΩ
	Output auto-discharge resistance			300		Ω
	Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
	Switch current limit - time-out	Multiplier set to 1, WTFET6 = 00	200		250	μs
	Switch current limit - time-out	Multiplier set to 4, WTFET6 = 01	800		1000	μs
	Switch current limit - time-out	Multiplier set to 8, WTFET6 = 10	1600		2000	μs
	Switch current limit - time-out	Multiplier set to 16, WTFET6 = 11	3200		4000	μs
	Leakage current into INFET6	FET6 disabled, V _{FET6} = 0 V		1		μA
FET7			1			
	Overcurrent detect threshold	$T_A = 25^{\circ}C$	1000		1200	mA
	Switch ON-resistance				80	mΩ

Electrical Characteristics - Load Switches (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output auto-discharge resistance			300		Ω
Maximum output voltage slew rate after turnon		0.1	0.5	1	V / µs
Switch current limit - time-out	Multiplier set to 1, WTFET7 = 00	200		250	μs
Switch current limit - time-out	Multiplier set to 4, WTFET7 = 01	800		1000	μs
Switch current limit - time-out	Multiplier set to 8, WTFET7 = 10	1600		2000	μs
Switch current limit - time-out	Multiplier set to 16, WTFET7 = 11	3200		4000	μs
Leakage current into INFET7	FET7 disabled, V _{FET7} = 0 V		1		μA

6.10 Electrical Characteristics - Control

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM - CONTROL					
VBATG, VACG, VSYSG, IRQ output low voltage	I _{VxxxGL} = 1 mA		0.04	0.4	V
VBATG, VACG, VSYSG, IRQ output leakage current			0.01	0.4	μA
STAT output low voltage	I _{STAT} = 1 mA		0.04	0.4	V
STAT output low voltage	I _{STAT} = 5 mA			0.6	V
STAT output leakage current			0.01	0.1	μA
System undervoltage lockout threshold	V _{SYS} voltage decreasing	5.5	5.6	5.7	V
System undervoltage lockout threshold hysteresis			300		mV
LDO undervoltage lockout threshold	V _{SYS} voltage decreasing	4.4	4.6	4.7	V
LDO undervoltage lockout threshold hysteresis			300		mV
V _{IL} SDA, SCL input low voltage				0.4	V
V _{IH} SDA, SCL input high voltage		1.2			V
SDA, SCL input current	Clamped on GND or 3.3 V		0.01	0.3	μA
SDA output low voltage	I _{SDA} = 5 mA		0.04	0.4	V
AD - CONVERTER					
ADC resolution			10		Bits
Differential linearity error			±1		LSB
Offset error			1	5	LSB
Offset error, voltage				12.7	mV
Gain error			±8		LSB
Sampling time			150		μs
Conversion time			20		μs
Wait time after enable	Time needed to stabilize the internal voltages			10	ms
Quiescent current, ADC enabled by I ² C	includes current needed for I ² C block		500		μA
AD - CONVERTER - MEASUREMENT RANGES	·			·	
Voltage on VAC		0		17	V
Battery voltage VBAT		0		17	V
Input current IAC	V _{ACP} - V _{ACN} is measured	0		33	mV
Battery charge current IBAT	V _{SRP} - V _{SRN} is measured	0		40	mV
DCDC1 output current IDCDC1		0		4	А
DCDC2 output current IDCDC2		0		4	А

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Electrical Characteristics - Control (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	ΤΥΡ ΜΑ	
DCDC3 output current IDCDC3		0		4 A
FET1 output current IFET1		0	1.	1 A
FET2 output current IFET2		0	22) mA
FET3 output current IFET3		0	3.	3 A
FET4 output current IFET4		0	1.	1 A
FET5 output current IFET5		0	1.	1 A
FET6 output current IFET6		0	1.	1 A
FET7 output current IFET7		0	1.	1 A
AD - CONVERTER - SIGNAL CONDITIONING				
Voltage sense error referenced to maximum value			29	, D
Current sense error referenced to maximum value for IAC and IBAT			209	0
Current sense error referenced to maximum value for DC-DC converter currents	Measurements at VSYS > 7.2 V, low side switch duty cycle at DCDC1-3 > 30%		159	0
Current sense error referenced to maximum value for load switch currents			109	0

6.11 Timing Requirements - I²C Interface

over recommended free-air temperature range and over recommended input voltage range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
		Standard-mode		100	kHz
		Fast-mode		400	kHz
f _(SCL) SCL clock frequency	SCL clock frequency	Fast-mode Plus		1000	kHz
		High-speed mode, C _b - 100 pF maximum		3.4	MHz
	High-speed mode, $C_b - 400 \text{ pF} \text{ maximum}^{(2)}$		1.7	MHz	
		Standard-mode	4.7		μs
t _{BUF}	Bus free time between a STOP and START condition	Fast-mode	1.3		μs
and		Fast-mode Plus	0.5		μs
, Hold time (repeated) START		Standard-mode	4		μs
	Hold time (repeated) START condition	Fast-mode	600		ns
^I HD; STA		Fast-mode Plus	260		ns
		High-speed mode	160		ns
		Standard-mode	4.7		μs
		Fast-mode	1.3		μs
t _{LOW}	LOW period of the SCL clock	Fast-mode Plus	0.5		μs
		High-speed mode, C _b - 100 pF maximum	160		ns
		High-speed mode, C _b - 400 pF maximum ⁽²⁾	320		ns
		Standard-mode	4		μs
		Fast-mode	600		ns
t _{HIGH}	HIGH period of the SCL clock	Fast-mode Plus	260		ns
		High-speed mode, C _b - 100 pF maximum	60		ns
		High-speed mode, $C_b - 400 \text{ pF} \text{ maximum}^{(2)}$	120		ns

(1) All values referred to $V_{IH}\xspace$ min and $V_{IH}\xspace$ max levels.

(2) For bus line loads C_b from 100 pF to 400 pF, the timing parameters must be linearly interpolated.



Timing Requirements - I²C Interface (continued)

over recommended free-air temperature range and over recommended input voltage range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
		Standard-mode	4.7		μs
	Setup time for a repeated	Fast-mode	600		ns
^I SU; STA	START condition	Fast-mode Plus	260		ns
		High-speed mode	160		ns
		Standard-mode	250		ns
		Fast-mode	100		ns
t _{SU;} DAT	Data setup time	Fast-mode Plus	50		ns
		High-speed mode	MIN MIN 4.7 600 260 160 250 100 50 100 50 100 11 250 100 50 110 11 24 11 250 100 11 26 11 27 100 pF maximum ⁽²⁾ 100 pF maximum ⁽²⁾ 20 100 pF maximum ⁽²⁾ 20 x (V _{DD} / 5.5 V) 10 400 pF maximum ⁽²⁾ 20 100 400 pF maximum ⁽²⁾ 20 x (V _{DD} / 5.5 V) 20 x (ns
		Standard-mode	1	3450	ns
		Fast-mode	1	900	ns
t _{HD; DAT}	Data hold time	Fast-mode Plus	1		ns
		High-speed mode, C _b – 100 pF maximum	1 ⁽³⁾	70	ns
	STA Setup time for a repeated START condition DAT Data setup time DAT Data setup time : DAT Data hold time : DAT Data hold time : DAT Rise time of SCL signal after a repeated START condition and after an acknowledge bit : Fall time of SCL signal Fall time of SCL signal : Fall time of SDA signal Fall time of SDA signal : STO Setup time for STOP condition	High-speed mode, C _b – 400 pF maximum ⁽²⁾	1 ⁽³⁾	150	ns
		Standard-mode		1000	ns
		Fast-mode	20	300	ns
t _{rCL}	Rise time of SCL signal	Fast-mode Plus		120	ns
		High-speed mode, C _b – 100 pF maximum	10	40	ns
		High-speed mode, C _b – 400 pF maximum ⁽²⁾	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	80	ns
		Standard-mode		1000	ns
	Rise time of SCL signal after a repeated START condition and	Fast-mode	20	300	ns
Ri: t _{rCL1} rej aft	repeated START condition and	Fast-mode Plus		120	ns
	after an acknowledge bit	High-speed mode, C _B – 100 pF maximum	10	80	ns
		High-speed mode, C _B – 400 pF maximum ⁽²⁾	20	160	ns
		Standard-mode		300	ns
		Fast-mode	20 × (V _{DD} / 5.5 V)	300	ns
t _{fCL}	Fall time of SCL signal	Fast-mode Plus	20 × (V _{DD} / 5.5 V)	120	ns
		High-speed mode, C _b – 100 pF maximum	10	40	ns
	STA START condition DAT Data setup time DAT Data hold time DAT Data hold time Rise time of SCL signal Rise time of SCL signal after a repeated START condition and after an acknowledge bit Fall time of SCL signal Fall time of SCL signal Fall time of SDA signal Fall time of SDA signal STO Setup time for STOP condition Capacitive load for SDA and SCL SDA and SCL	High-speed mode, C _b – 400 pF maximum ⁽²⁾	20	80	ns
		Standard-mode		1000	ns
		Fast-mode	20	300	ns
t _{rDA}	Rise time of SDA signal	Fast-mode Plus		120	ns
		High-speed mode, C _b – 100 pF maximum	10	80	ns
		High-speed mode, C _b – 400 pF maximum ⁽²⁾	20	160	ns
		Standard-mode		300	ns
	Rise time of SDA signal	Fast-mode	20 × (V _{DD} / 5.5 V)	300	ns
t _{fDA}	Fall time of SDA signal	Fast-mode Plus	20 × (V _{DD} / 5.5 V)	120	ns
		High-speed mode, C _b – 100 pF maximum	10	80	ns
		High-speed mode, $C_b - 400 \text{ pF} \text{ maximum}^{(2)}$	20	160	ns
		Standard-mode	4		μs
+	Satur time for STOD condition	Fast-mode	600		ns
⁽ SU; STO	Setup time for STOP condition	Fast-mode Plus	260		ns
		High-speed mode	160		ns
C _b	Capacitive load for SDA and SCL			400	pF

(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.



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Figure 1. Serial Interface Timing Diagram

6.12 Typical Characteristics

Table of Graphs

		FIGURE
	vs Output Current, DCDC1, V _{OUT} = 5 V	Figure 2
	vs Output Current, DCDC2, V _{OUT} = 3.3 V	Figure 3
	vs Output Current, DCDC3, V _{OUT} = 1 V	Figure 4
Efficiency	vs Output Current, DCDC3, V _{OUT} = 1.35 V	Figure 5
Efficiency	vs Output Current, DCDC3, V _{OUT} = 1.8 V	Figure 6
	vs Output Current, DCDC3, V _{OUT} = 3.3 V	Figure 7
	vs Output Current, DCDC3, V _{OUT} = 4 V	Figure 8
	vs Output Current, DCDC3, V _{OUT} = 5 V	Figure 9
Efficiency	vs Output Current, Charger, V_{OUT} = 8.4 V	Figure 10
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	vs Input Voltage, DCDC1, V _{OUT} = 5 V	Figure 12
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	vs Input Voltage, DCDC3, V _{OUT} = 1 V	Figure 14
Efficiency	vs Input Voltage, DCDC3, V _{OUT} = 1.35 V	Figure 15
Enciency	vs Input Voltage, DCDC3, V _{OUT} = 1.8 V	Figure 16
	vs Input Voltage, DCDC3, V _{OUT} = 3.3 V	Figure 17
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Switching froguones:	vs Output Current, DCDC3, V _{OUT} = 1.35 V	Figure 26
Switching requency	vs Input Voltage, DCDC1, V _{OUT} = 5 V	Figure 27
	vs Input Voltage, DCDC2, V _{OUT} = 3.3 V	Figure 28
	vs Input Voltage, DCDC3, V _{OUT} = 1.35 V	Figure 29



Typical Characteristics (continued)

Table of Graphs (continued)

		FIGURE
	vs Output Current, DCDC1, V _{OUT} = 5 V	Figure 30
	vs Output Current, DCDC2, V _{OUT} = 3.3 V	Figure 31
	vs Output Current, DCDC3, V _{OUT} = 1.35 V	Figure 32
	vs Input Voltage, DCDC1, V _{OUT} = 5 V	Figure 33
	vs Input Voltage, DCDC2, V_{OUT} = 3.3 V	Figure 34
	vs Input Voltage, DCDC3, V _{OUT} = 1.35 V	Figure 35



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7 Detailed Description

7.1 Overview

The TPS65090A is a single-chip power management IC for portable applications consisting of a battery charger with power path management for a dual or triple Li-Ion or Li-Polymer cell battery pack, three step-down converters, two always-on LDOs, and seven load switches with independent inputs.



7.2 Functional Block Diagram





7.3 Feature Description

As soon as a valid voltage at VSYS is applied, the LDOs start operating and providing a regulated output voltage at each of them. If DCDC1 is started, the output of the DCDC1 converter will be connected to the output of LDO1 with an internal bypass switch to ensure seamless transition. Finally, LDO1 will stop operating. LDO1 will restart when the voltage at its output drops below its regulation voltage. In this case, both outputs will be disconnected from each other. There will be no current flowing backward from the LDO1 output to the DCDC1 output. The same function is implemented for DCDC2 and LDO2.

7.3.2 Power Path Control

The device automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or if the adapter power is not available. As soon as a valid voltage is detected on VACS and the voltage at VAC is higher than the battery voltage, the battery is disconnected and the AC power path switches controlled through the pins ACG and ACS are turned on. The system is powered through the adapter input. If the voltage on VACS is higher than the overvoltage protection threshold the AC power path switches are turned off or not turned on to protect the system from damage. Any voltage on VACS lower than the input undervoltage lockout (UVLO) threshold voltage will cause the AC power path switches to be off.

To protect the device and the system against reverse voltage additional external components are required to protect the pins VAC, VACS ACG and ACS which would be exposed to the reverse voltage. See the EVM documentation SLVU778 for more details.

In case the maximum adapter output current is not high enough to supply the complete system, the system can be powered through the adapter and the battery at the same time. If the adapter current is limited, the adapter voltage will drop to the battery voltage level and the backgate diode of the battery switch will conduct current.

To minimize the losses in this mode of operation, the battery switch is turned on. To detect whether there is still a power source connected at the AC input, the AC power path switches are turned off every 0.5 s for a few milliseconds. While the AC power path switches are off, VAC is discharged through a 1-k Ω resistor to GND. If the voltage at VACS did not drop below the input UVLO threshold voltage, the AC power path switches are turned on again to allow the power source connected to the AC input to supply the system again.

7.3.3 Supply Status Outputs

The status of the power supply is indicated through the status pins VACG, VBATG and VSYSG. All pins are open-drain outputs and need a pullup resistor to the respective logic supply voltage they are connected to.

VACG will be high if a voltage is detected at VAC and VACS which is in a useable window. This means the voltage detected at VACS must be lower than the overvoltage threshold and it must be higher than the input UVLO threshold voltage. Also, the voltage at VAC must be higher than battery voltage. If no battery is connected, the minimum voltage is above the UVLO threshold.

VSYSG will be high as soon as the system voltage, detected at VSYS_L1 and VSYS_L2, is above its undervoltage thresholds.

VBATG will be high if the voltage detected at FBC is between the minimum and the maximum voltage for battery good detection and the differential voltage V_{SRN} - V_{VBAT} is lower than 20 mV. This indicates that the battery discharge current is not exceeding the programmed maximum level.

7.3.4 Charger

Charging can be enabled by using the ENC pin or by programming the respective register through I²C. The charger will then start working when VACG is detected. If the battery is completely charged or charging has been terminated for any other reason, the charger will stay idle. Charging can be restarted by disabling the charger and enabling it again.

As soon as the charger is enabled it starts with battery detection as shown in Figure 36. If no battery or a battery short is detected the charger will continue with battery detection. If the battery is detected it will start charging.



Feature Description (continued)





The charger controls a low constant-charge current during a precharge phase when the battery is at a very low voltage and must be recovered. The charger controls a high fast-charge current if the battery voltage is greater than the low voltage threshold and less than the charge termination voltage. If the battery voltage has reached the charge termination voltage, the charger controls this voltage until the charge current has decayed below the charge termination threshold or the fast-charge safety timer has timed out. Precharge current and charge termination current are either 10% of the programmed fast-charge current if the fast-charge current is set to 1 A or higher. Otherwise they will be controlled to 100 mA. A complete charging cycle is shown in Figure 37.



Feature Description (continued)



Figure 37. Charging Cycle

To support charging with weak power sources, the charger stays in operation even if it cannot control the charge current at the programmed level. For this operating condition, the charge termination based on low charge current can be turned off by programming the respective register.

The fast-charge safety timer is programmed to its lowest value by default. The time-out time can be increased by programming higher values in the respective registers. It cannot be turned off.

All charge currents are defined depending on the current sense resistor connected between the pins SRN and SRP. The maximum fast-charge current generates a 40 mV voltage drop across this resistor. All other currents are lower.

The charge termination voltage is defined by a resistive voltage divider connected between battery, feedback input of the charger (FBC), and GND. The maximum voltage at FBC which is controlled is typically 2.1 V.

The charger has also inputs to measure the battery cell temperature. It supports using two different temperature sensors which can be placed at different locations in the battery pack. For more details on the temperature sensing circuit, refer to *Application and Implementation*. For biasing the temperature sense resistor networks and the internal comparator reference the voltage at the VREFT pin is used. It is turned off if the charger is disabled.

Charge current and charge termination voltage can be programmed to lower than the maximum values using the digital interface. They are also controlled and forced to lower values depending on the measured battery cell temperature. The respective values for the five different temperature regions can be programmed in the charge control registers (CG_CTRLx) using the digital interface. Default settings for temperature thresholds and the respective fast-charge current and charge termination voltages are defined according to JEITA recommendations



Feature Description (continued)

for multicell battery packs. The definitions for the thresholds and temperature zones are shown in Figure 38. Figure 38 also shows the default values for temperature thresholds, charge current and charge termination voltage, which are programmed in TPS65090A. The optional values which can be programmed through the digital interface, can be found in *Electrical Characteristics*. The actual temperature zones the charger operates in, can be read out from the charge status register CG_STATUS1.



Figure 38. JEITA Charging Profile

If the adapter current measured with a sense resistor between the pins ACN and ACP exceeds its programmed value or the adapter voltage measured at VACS drops below a certain level (typically 7 V, see *Electrical Characteristics*) the charge current is reduced automatically to avoid an overload condition of the AC adapter and an undervoltage condition for the system. The charge current is also reduced if the charger temperature measured in the IC is exceeding 100°C.

The charger indicates its current status of operation in two ways. One is the STAT output pin which can be used to drive an LED. The STAT pin can have three different states as described in Table 1. To get details about the current state of charging the charging status register CG_STATUS1 can be read.

CHARGING STATE	STAT PIN STATE
Charging complete Sleep mode Charging disabled	HIGH
Charging in progress (including recharging)	LOW
Charging suspended No battery detected Safety timer fault (precharge, fast-charge)	Blinking with 0.5 Hz

Table 1. Charger Status Pin STAT



A status change from charging suspended to charging active and back sets the interrupt CGACT and charging completed sets the interrupt CGCPL. Both interrupts can be masked. If not masked, they will trigger IRQ pin to go low when they are set.

7.3.5 DC-DC Converters

The built in DC-DC converters are completely integrated except the required passive components. To maintain high efficiency, they are implemented as synchronous step-down converters. At medium and heavy loads they are operating in a PWM mode. As soon as the inductor current gets discontinuous, which means that the output current gets lower than half of the inductor ripple current the converters enter Power Save Mode. In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

All DC-DC converters can be enabled using their ENx pins. If they should be enabled using the digital interface the enable pin function can be masked in the DCDCx_CTRL register. If masked enable only works by writing a 1 to the EN bit in the DCDCx_CTRL register.

As soon as the output voltage reaches 80% of the input voltage, the power good register bit for this converter is set to 1. If the output voltage drops below this threshold the power good bit is set back to 0.

The start-up of the converter is controlled by an internal soft-start to make sure the output voltage is built up smoothly and the inrush current during start-up is kept at minimum.

All converters are current limited. The current limit is controlling the maximum output current. If the current limit is controlling the converter its respective OLDCDCx interrupt bits are set to 1. The OLDCDCx interrupt bits can be masked. If not masked, they will trigger IRQ pin to go low when they are set.

To make sure that the output voltage of the DC-DC converters is decreasing fast to a safe low value a built in output auto-discharge function can be enabled using the ADENDCDC bit in the respective DCDCx_CTRL register. If enabled, the output capacitors are actively discharged as soon as the converter is disabled. While the converter is enabled, its output discharge circuit is off to save power.

7.3.6 Load Switches

Load switches are turned on using the digital control interface by writing 1 in the ENFETx bit of their load switch control register FETx_CTRL. They cannot be enabled before DCDC1 and DCDC2 have been started and their output voltage is above their power good level. If DCDC1 or DCDC2 will be disabled, load switches will be immediately disabled as well and enabled if both DC-DC converters are enabled again.

After being turned on, the output voltage of the load switch is ramped up with a controlled slope (<1 V / μ s). The current limit is active during that time and does not allow the current to overshoot. This means the slope can be slower if controlled by the current limit.

After being turned on, a timer is started. If the timer terminates, the output voltage must have reached the input voltage. Otherwise, the load switch is turned off again expecting an overload condition. The minimum value of the timer is 200 μ s. This timer is used as well if the load switch control limits the current. The timer can be extended through the digital control interface using 4 steps (max factor 16 up to 3 ms). If the load switch has been turned off by this safety timer, the load switch can only been turned on again by reprogramming its ENFETx bit to 1 again.

As soon as the output voltage reaches 80% of the input voltage, the power good register bit for this load switch is set to 1. If the output voltage drops below this threshold, the power good bit is set back to 0.

All load switches are current limited. The current limit is regulating the maximum output current. A temperature sensor can trigger the turnoff of the load switch as well. If the current limit is controlling the switch, their respective OLFETx interrupt bits are set to 1. The OLFETx interrupt bits can be masked. If not masked, they will trigger IRQ pin to go low when they are set.

To make sure that a voltage on the output of FET2 is not supplying its input while turned off, it is reverse-current protected. This feature is only available at FET2 to support controlling circuit blocks which can get power from an external source while the system is turned off, like HDMI.

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To make sure that the output voltage of the load switches is decreasing fast to a safe low value, a built-in output auto-discharge function can be enabled using the ADENFETx bit in the respective FETx_CTRL register. If enabled, the output capacitors are actively discharged as soon as the load switch is disabled. While the load switch is enabled, its output discharge circuit is off to save power.

7.3.7 ADC

Analog-to-digital conversion is controlled according to the flow chart shown in Figure 39. After enabling the ADC, the channel which should be measured must be defined in the ADC control register. Analog-to-digital conversion is started by writing the start command in the ADC register. As soon as conversion is finished, ADEOC is set to 1 and the data is available in the ADOUT registers.



Figure 39. Analog-to-Digital Conversion

7.3.8 Protection

The device has 2 built-in undervoltage detectors. If the system voltage is not high enough to safely operate the DC-DC converters, they are shut down with the higher undervoltage threshold which also sets VSYSG high as soon as the system voltage has increased above this threshold. In this condition, the LDOs are still on to supply the internal control circuitry. If the system voltage further decreases and hits the second lower undervoltage threshold, the LDOs are turned off as well and the internal control circuit is disabled. The control circuit is reset and restarted if the supply voltage increases above the lower undervoltage threshold.



The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see *Electrical Characteristics*), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

7.3.9 Interrupts

The device monitors several internal states of power path, charger, DC-DC converters, and load switches. If any of those states changes, an interrupt can be asserted. By default, all states are masked, so any state which should generate an interrupt must be unmasked. If an unmasked state changes, it will generate an interrupt, which means the output impedance of the IRQ pin will go low, and if properly connected, the voltage will go low. What has caused the interrupt can be read out from the interrupt status registers IRQ1 and IRQ2. The interrupt will be cleared by writing a zero to the IRQ bit in the interrupt status register IRQ1. The content of the status registers are refreshed only after an interrupt has occurred.

7.4 Device Functional Modes

The TPS65090A is designed with two LDOs that have a fixed voltage and are 'always on'. It is also designed with two fixed-voltage converters. Using external feedback resistors, a third DC-DC converter can be programmed to any voltage within the range of 1 V to 5 V. The devices also has seven load switches (one system voltage switch, one 5-V switch, and five 3.3-V switches) that can be connected as needed by the end application.

7.5 Programming

7.5.1 I²C Interface

I²C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see I²C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

TPS6509x works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast-mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to TPS6509x higher than the UVLO threshold. The I²C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode.

The TPS6509x supports 7-bit addressing; 10-bit addressing and general call address are not supported. The default device address is set to *1001000*. The 2 LSB bits of the address are factory programmable. Contact TI about availability of different default device addresses.

All registers are set to their default value when the supply voltage is below the UVLO threshold.

7.5.1.1 F/S-Mode Protocol

The master initiates data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 40. All I²C-compatible devices should recognize a START condition.

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Programming (continued)

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 41. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 42, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high, see Figure 40. This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, all devices know that the bus is released, and they wait for a START condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in FFh being read out.

7.5.1.2 H/S-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pullup devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated START condition (a repeated START condition has the same timing as the START condition). After this repeated START condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A STOP condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a STOP condition, repeated START conditions are used to secure the bus in HS-mode.

Trying to read data from register addresses not listed in this section results in FFh being read out.





Figure 41. Bit Transfer on the I²C-Bus



Programming (continued)









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Programming (continued)



Figure 45. I²C Interface READ from in F/S Mode



7.6 Register Maps

Table 2. IRQ1 Register Address: 0x00

B7	B6	B5	B4	B3	B2	B1	B0		
OLDCDC2	OLDCDC1	CGCPL	CGACT	VBATG	VSYSG	VACG	IRQ		
0	0	0	0	0	0	0	0		
r	r	r	r	r	r	r	r/w		
OLDCDC2	Overload on DCDC2, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload								
OLDCDC1	Overload on DCDC1, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload								
CGCPL	Charging completed, IRQ on change to 1, cleared on interrupt clear 0: charging not completed 1: charging completed								
CGACT	Charging status, in 0: charging suspen 1: charging active	terrupt on change ded							
VBATG	VBAT status, interr 0: VBAT not availal 1: VBAT available a	upt on change ble and useable							
VSYSG	VSYS status, interr 0: VSYS not availa 1: VSYS available a	upt on change ble and useable							
VACG	VAC status, interrupt on change 0: VAC not available 1: VAC available and useable								
IRQ	Interrupt 0: interrupt cleared 1: interrupt asserte	d							

Table 3. IRQ2 Register Address: 0x01

B7	B6	B5	B4	B3	B2	B1	B0		
OLFET7	OLFET6	OLFET5	OLFET4	OLFET3	OLFET2	OLFET1	OLDCDC3		
0	0	0	0	0	0	0	0		
r	r	r	r	r	r	r	r		
OLFET7	Overload on FET7, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload								
OLFET6	Overload on FET6, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload								
OLFET5	Overload on FET5, IRQ on change to 1, cleared on interrupt clear 0: normal operation 1: overload								
OLFET4	Overload on FET4, 0: normal operation 1: overload	IRQ on change to 1	, cleared on interrup	t clear					
OLFET3	Overload on FET3, 0: normal operation 1: overload	IRQ on change to 1	, cleared on interrup	t clear					
OLFET2	Overload on FET2, 0: normal operation 1: overload	IRQ on change to 1	, cleared on interrup	t clear					
OLFET1	Overload on FET1, 0: normal operation 1: overload	IRQ on change to 1	, cleared on interrup	t clear					
OLDCDC3	Overload on DCDC 0: normal operation 1: overload	3, IRQ on change to	o 1, cleared on interr	upt clear					

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Table 4. IRQ1MASK Register Address: 0x02

B7	B6	B5	B4	B3	B2	B1	B0
OLDCDC2MASK	OLDCDC1MASK	CGCPLMASK	CGACTMASK	VBATGMASK	VSYSGMASK	VACGMASK	reserved
0	0	0	0	0	0	0	0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r
OLDCDC2MASK	Enable overload on 0: disabled 1: enabled	n DCDC2 interrupt					
OLDCDC1MASK	Enable overload on 0: disabled 1: enabled	DCDC1 interrupt					
CGCPLMASK	Enable charging co 0: disabled 1: enabled	mpleted status inter	rupt				
CGACTMASK	Enable charging sta 0: disabled 1: enabled	atus interrupt					
VBATGMASK	Enable VBAT statu 0: disabled 1: enabled	s interrupt					
VSYSGMASK	Enable VSYS statu 0: disabled 1: enabled	is interrupt					
VACGMASK	Enable VAC status 0: disabled 1: enabled	interrupt					
reserved							

Table 5. IRQ2MASK Register Address: 0x03

B7	B6	B5	B4	B3	B2	B1	B0		
OLFET7MASK	OLFET6MASK	OLFET5MASK	OLFET4MASK	OLFET3MASK	OLFET2MASK	OLFET1MASK	OLDCDC3MASK		
0	0	0	0	0	0	0	0		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
OLFET7MASK	Enable overload or 0: disabled 1: enabled	FET7 interrupt							
OLFET6MASK	Enable overload on FET6 interrupt 0: disabled 1: enabled								
OLFET5MASK	Enable overload or 0: disabled 1: enabled	Enable overload on FET5 interrupt 0: disabled 1: enabled							
OLFET4MASK	Enable overload or 0: disabled 1: enabled	FET4 interrupt							
OLFET3MASK	Enable overload or 0: disabled 1: enabled	FET3 interrupt							
OLFET2MASK	Enable overload or 0: disabled 1: enabled	FET2 interrupt							
OLFET1MASK	Enable overload or 0: disabled 1: enabled	FET1 interrupt							
OLDCDC3MASK	Enable overload or 0: disabled 1: enabled	DCDC3 interrupt							



Table 6. CG_CTRL0 Register Address: 0x04

B7	B6	B5	B4	B3	B2	B1	B0		
reserved	IBATSET	IACSET	FASTTIME[2]	FASTTIME[1]	FASTTIME[0]	ENCMASK	ENC		
0	0	0	0	0	0	1	0		
r	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
reserved		•		·		•	•		
IBATSET	Maximum battery discharge current 0: 100% of programmed current 1: 90% of programmed current								
IACSET	Maximum adapter current 0: 100% of programmed current 1: 90% of programmed current								
FASTTIME[2:0]	Fast-charge safety 000: 2 hrs 001: 3 hrs 010: 4 hrs 010: 6 hrs 100: 6 hrs 101: 7 hrs 110: 8 hrs 111: 10 hrs	timer							
ENCMASK	Enable external characteristics 0: external control 1: external control	arge enable pin off on							
ENC	Enable charger 0: disabled 1: enabled								

Table 7. CG_CTRL1 Register Address: 0x05

B7	B6	B5	B4	B3	B2	B1	В0		
T1_SET[2]	T1_SET[1]	T1_SET[0]	T01_VSET[1]	T01_VSET[0]	T01_ISET[2]	T01_ISET[1]	T01_ISET[0]		
0	0	1	0	0	0	0	0		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
T1_SET[2:0]	Temperature threshold for T1 000: -10°C (for a default NTC resistor network) 001: 0°C (for a default NTC resistor network) 010: 10°C (for a default NTC resistor network) 011: 15°C (for a default NTC resistor network) 100: 40°C (for a default NTC resistor network) 101: 45°C (for a default NTC resistor network) 110: 50°C (for a default NTC resistor network) 111: 60°C (for a default NTC resistor network)								
T01_VSET[1:0]	Charge termination 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V	i feedback voltage fo	r T01 temperature ra	ange					
T01_ISET[2:0]	Maximum fast char 000: 0% of resistor 001: 25% of resisto 010: 37.5% of resist 011: 50% of resist 100: 62.5% of resist 101: 75% of resist 110: 87.5% of resist 111: 100% of resist	ge current for T01 te programmed curren or programmed curren stor programmed curre or programmed curre stor programmed curre stor programmed curre tor programmed curre tor programmed curre	emperature range t nt rent nt rent nt rent ent						

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Table 8. CG_CTRL2 Register Address: 0x06

B7	B6	B5	B4	B3	B2	B1	В0		
T2_SET[2]	T2_SET[1]	T2_SET[0]	T12_VSET[1]	T12_VSET[0]	T12_ISET[2]	T12_ISET[1]	T12_ISET[0]		
0	1	0	0	1	0	1	1		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
T2_SET[2:0]	Temperature threshold for T2 000: -10°C (for a default NTC resistor network) 001: 0°C (for a default NTC resistor network) 010: 10°C (for a default NTC resistor network) 101: 15°C (for a default NTC resistor network) 100: 40°C (for a default NTC resistor network) 101: 45°C (for a default NTC resistor network) 110: 50°C (for a default NTC resistor network) 111: 60°C (for a default NTC resistor network)								
112_VSE1[1:0]	Charge termination 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V	feedback voltage fo	r 112 temperature ra	ange					
T12_ISET[2:0]	Maximum fast char, 000: 0% of resistor 001: 25% of resisto 010: 37.5% of resisto 010: 62.5% of resisto 100: 62.5% of resisto 101: 75% of resisto 110: 87.5% of resisto 111: 100% of resisto	ge current for T12 te programmed curren r programmed curren tor programmed current tor programmed current tor programmed current tor programmed current tor programmed current tor programmed current	emperature range t nt rent nt rent nt rent rent rent						

Table 9. CG_CTRL3 Register Address: 0x07

B7	B6	B5	B4	B3	B2	B1	B0		
T3_SET[2]	T3_SET[1]	T3_SET[0]	T23_VSET[1]	T23_VSET[0]	T23_ISET[2]	T23_ISET[1]	T23_ISET[0]		
1	0	1	1	1	1	1	1		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
T3_SET[2:0]	Temperature threshold for T3 000: -10°C (for a default NTC resistor network) 001: 0°C (for a default NTC resistor network) 010: 10°C (for a default NTC resistor network) 011: 15°C (for a default NTC resistor network) 100: 40°C (for a default NTC resistor network) 101: 45°C (for a default NTC resistor network) 110: 50°C (for a default NTC resistor network) 110: 50°C (for a default NTC resistor network) 111: 60°C (for a default NTC resistor network)								
T23_VSET[1:0]	Charge termination 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V	n feedback voltage fo	or T23 temperature ra	ange					
T23_ISET[2:0]	Maximum fast char 000: 0% of resistor 001: 25% of resisto 010: 37.5% of resist 011: 50% of resist 100: 62.5% of resist 101: 75% of resist 111: 100% of resist	rge current for T23 te programmed curren or programmed curren stor programmed curren or programmed curren stor programmed curren stor programmed curren stor programmed current tor programmed current tor programmed current	emperature range it int int int int int rent rent rent						



Table 10. CG_CTRL4 Register Address: 0x08

B7	B6	B5	B4	B3	B2	B1	В0		
T4_SET[2]	T4_SET[1]	T4_SET[0]	T34_VSET[1]	T34_VSET[0]	T34_ISET[2]	T34_ISET[1]	T34_ISET[0]		
1	1	1	1	0	0	1	1		
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w		
T4_SET[2:0]	Temperature threshold for T4 000: -10°C (for a default NTC resistor network) 001: 0°C (for a default NTC resistor network) 010: 10°C (for a default NTC resistor network) 011: 15°C (for a default NTC resistor network) 100: 40°C (for a default NTC resistor network) 101: 45°C (for a default NTC resistor network) 110: 50°C (for a default NTC resistor network) 110: 60°C (for a default NTC resistor network)								
T34_VSET[1:0]	Charge termination 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V	feedback voltage fo	r T34 temperature ra	ange					
T34_ISET[2:0]	11. 2.1 v OI Maximum fast charge current for T34 temperature range 000: 0% of resistor programmed current 001: 25% of resistor programmed current 010: 37.5% of resistor programmed current 100: 62.5% of resistor programmed current 100: 62.5% of resistor programmed current 101: 75% of resistor programmed current 110: 87.5% of resistor programmed current 110: 87.5% of resistor programmed current 111: 100% of resistor programmed current								

Table 11. CG_CTRL5 Register Address: 0x09

B7	B6	B5	B4	B3	B2	B1	В0			
reserved	ENRECG	NOITERM	T40_VSET[1]	T40_VSET[0]	T40_ISET[2]	T40_ISET[1]	T40_ISET[0]			
1	1	0	0	0	0	0	0			
r	r/w	r/w	r/w	r/w	r/w	r/w	r/w			
reserved						·				
ENRECG	Enable of automatic recharge based on battery voltage detected 0: disabled 1: enabled									
NOITERM	Disable charging termination based on low charge current detected 0: charging stops when low charge current is detected 1: charging continues when low charge current is detected									
T40_VSET[1:0]	Charge termination feedback voltage for T40 temperature range 00: 2.0 V 01: 2.05 V 10: 2.075 V 11: 2.1 V									
T40_ISET[2:0]	Maximum fast char 000: 0% of resistor 001: 25% of resisto 010: 37.5% of resisto 101: 50% of resisto 100: 62.5% of resisto 101: 75% of resisto 111: 87.5% of resisto 111: 100% of resisto	ge current for T40 te programmed currer or programmed curre stor programmed curre stor programmed curre stor programmed curre stor programmed curre stor programmed curre	emperature range t nt rent nt rent nt rent rent ent							

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57		55	54	50	50	54	50		
B/	Bo	BO	В4	ВЗ	BZ	BI	BU		
STATECG[3]	STATECG[2]	STATECG[1]	STATECG[0]	TOC[1]	TOC[0]	000	OTC		
0	0	0	0	0	0	0	0		
r	r	r	r	r	r	r	r		
STATECG[3:0]	Charger status indication: 0000: not used 0011: not used 0010: charger idle 0011: battery detection 0100: battery detection 0101: charging in precharge 0110: charging in fast-charge 0111: not used 1000: not used 1001: not used 1010: charging completed 1011: not used 1010: not used 1100: not used 1100: not used 1101: battery detection, wait for start charging 1110: not used 1111: not used 1111: not used								
TOC[1:0]	Charger time-out indication 00: no time-out 01: precharge time-out 10: fast-charge time-out 11: no time-out								
OCC	Overcurrent charge 0: no overcurrent d 1: overcurrent dete	er etected cted							
отс	Overtemperature cl 0: no overtermpera 1: overtemperature	harger ture detected detected							

Table 13. CG_STATUS2 Register Address: 0x0B

B7	B6	B5	B4	B3	B2	B1	B0			
reserved	reserved	TS2_ZONE[2]	TS2_ZONE[1]	TS2_ZONE[0]	TS1_ZONE[2]	TS1_ZONE[1]	TS1_ZONE[0]			
0	0	0	0	0	0	0	0			
r	r	r	r	r	r	r	r			
reserved[1:0]										
TS2_ZONE[2:0]	Temperature zone reading for TS2 000: temperature zone 01 001: temperature zone 12 010: temperature zone 23 011: temperature zone 34 100: temperature zone 40 101: not used 110: not used 111: not used									
TS1_ZONE[2:0]	Temperature zone 000: temperature z 001: temperature z 010: temperature z 011: temperature z 100: temperature z 101: not used 110: not used 111: not used	reading for TS1 one 01 one 12 one 23 one 34 one 40								



Table 14. DCDC1_CTRL Register Address: 0x0C

B7	B6	B5	B4	B3	B2	B1	B0		
reserved	OC	ОТ	PG	ADENDCDC	reserved	ENMASK	EN		
1	0	0	0	1	1	1	0		
r	r	r	r	r/w	r	r/w	r/w		
reserved									
oc	Overcurrent DCDC1 0: no overcurrent detected 1: overcurrent detected								
OT	Overtemperature DCDC1 0: no overtermperature detected 1: overtemperature detected								
PG	Power good of DCI 0: no output voltage 1: output voltage po	DC1 status e power good ower good							
ADENDCDC	Enable output auto 0: disabled 1: enabled	-discharge of DCDC	1						
reserved									
ENMASK	Enable external DC 0: external control o 1: external control o	CDC1 enable pin off on							
EN	Enable DCDC1 0: disabled 1: enabled								

Table 15. DCDC2_CTRL Register Address: 0x0D

B7	B6	B5	B4	B3	B2	B1	B0			
reserved	OC	ОТ	PG	ADENDCDC	reserved	ENMASK	EN			
1	0	0	0	1	1	1	0			
r	r	r	r	r/w	r	r/w	r/w			
reserved										
oc	Overcurrent DCDC2 0: no overcurrent detected 1: overcurrent detected									
OT	Overtemperature DCDC2 0: no overtemperature detected 1: overtemperature detected									
PG	Power good of DCI 0: no output voltage 1: output voltage po	DC2 status e power good ower good								
ADENDCDC	Enable output auto 0: disabled 1: enabled	-discharge of DCDC	2							
reserved										
ENMASK	Enable external DCDC2 enable pin 0: external control off 1: external control on									
EN	Enable DCDC2 0: disabled 1: enabled									

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Table 16. DCDC3_CTRL Register Address: 0x0E

B7	B6	B 5	B/	B3	B2	B1	BO				
reserved	OC	OT	PG	ADENDCDC	reserved	ENMASK	EN				
1	0	0	0	1	1	1	0				
r	r	r	r	r/w	r	r/w	r/w				
reserved	reserved										
OC	Overcurrent DCDC3 0: no overcurrent detected 1: overcurrent detected										
OT	Overtemperature DCDC3 0: no overtemperature detected 1: overtemperature detected										
PG	Power good of DCDC3 status 0: no output voltage power good 1: output voltage power good										
ADENDCDC	Enable output auto 0: disabled 1: enabled	-discharge of DCDC	3								
reserved											
ENMASK	Enable external DC 0: external control o 1: external control o	DC3 enable pin off on									
EN	Enable DCDC3 0: disabled 1: enabled										

Table 17. FET1_CTRL Register Address: 0x0F

B7	B6	B5	B4	B3	B2	B1	B0				
TOFET1	OCFET1	OTFET1	PGFET1	WTFET1[1]	WTFET1[0]	ADENFET1	ENFET1				
0	0	0	0	0	0	1	0				
r	r	r	r	r/w	r/w	r/w	r/w				
TOFET1	Time-out FET1, start-up, overload 0: no time-out detected 1: time-out detected										
OCFET1	Overcurrent FET1 0: no overcurrent detected 1: overcurrent detected										
OTFET1	Overtemperature FET1 0: no overtermperature detected 1: overtemperature detected										
PGFET1	Power good of FET 0: no output voltage 1: output voltage po	⁻ 1 status e power good ower good									
WTFET1[1:0]	Wait time for current limited time-out of FET1 00: 200-µs minimum wait time 01: 800-µs minimum wait time 10: 1600-µs minimum wait time										
ADENFET1	Enable output auto-discharge of FET1 0: disabled 1: enabled										
ENFET1	Enable FET1 0: disabled 1: enabled										



Table 18. FET2_CTRL Register Address: 0x10

B7	B6	B5	B4	B3	B2	B1	B0			
TOFET2	OCFET2	OTFET2	PGFET2	WTFET2[1]	WTFET2[0]	ADENFET2	ENFET2			
0	0	0	0	0	0	1	0			
r	r	r	r	r/w	r/w	r/w	r/w			
TOFET2	Time-out FET2, start-up, overload 0: no time-out detected 1: time-out detected 0: converse EET2									
OCFET2	Overcurrent FET2 0: no overcurrent detected 1: overcurrent detected									
OTFET2	Overtemperature FET2 0: no overtermperature detected 1: overtemperature detected									
PGFET2	Power good of FET 0: no output voltage 1: output voltage po	2 status e power good ower good								
WTFET2[1:0]	Wait time for current limited time-out of FET2 00: 200-µs minimum wait time 01: 800-µs minimum wait time 10: 1600-µs minimum wait time 11: 3200-µs minimum wait time									
ADENFET2	Enable output auto-discharge of FET2 0: disabled 1: enabled									
ENFET2	Enable FET2 0: disabled 1: enabled									

Table 19	FET3		Register	Address:	0x11
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B7	B6	B5	B4	B3	B2	B1	B0		
TOFET3	OCFET3	OTFET3	PGFET3	WTFET3[1]	WTFET3[0]	ADENFET3	ENFET3		
0	0	0	0	0	0	1	0		
r	r	r	r	r/w	r/w	r/w	r/w		
TOFET3	Time-out FET3, sta 0: no time-out dete 1: time-out detected	art-up, overload cted d							
OCFET3	Overcurrent FET3 0: no overcurrent detected 1: overcurrent detected								
OTFET3	Overtemperature FET3 0: no overtermperature detected 1: overtemperature detected								
PGFET3	Power good of FET 0: no output voltage 1: output voltage po	Γ3 status e power good ower good							
WTFET3[1:0]	Wait time for current limited time-out of FET3 00: 200-us minimum wait time 01: 800-us minimum wait time 10: 1600-us minimum wait time 11: 3200-us minimum wait time								
ADENFET3	Enable output auto 0: disabled 1: enabled	-discharge of FET3							
ENFET3	Enable FET3 0: disabled 1: enabled								

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Table 20. FET4_CTRL Register Address: 0x12

B7	B6	B5	B4	B3	B2	B1	B0		
TOFET4	OCFET4	OTFET4	PGFET4	WTFET4[1]	WTFET4[0]	ADENFET4	ENFET4		
0	0	0	0	0	0	1	0		
r	r	r	r	r/w	r/w	r/w	r/w		
TOFET4	Time-out FET4, sta 0: no time-out detected 1: time-out detected	rrt-up, overload cted d							
OCFET4	Overcurrent FET4 0: no overcurrent detected 1: overcurrent detected								
OTFET4	Overtemperature FET4 0: no overtermperature detected 1: overtemperature detected								
PGFET4	Power good of FET 0: no output voltage 1: output voltage po	4 status e power good ower good							
WTFET4[1:0]	1: output voitage power good Wait time for current limited time-out of FET4 00: 200-µs minimum wait time 01: 800-µs minimum wait time 10: 1600-µs minimum wait time 11: 3200-µs minimum wait time								
ADENFET4	Enable output auto 0: disabled 1: enabled	-discharge of FET4							
ENFET4	Enable FET4 0: disabled 1: enabled								

Table 21.	FET5_	CTRL	Register	Address:	0x13
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B7	B6	B5	B4	B3	B2	B1	B0		
TOFET5	OCFET5	OTFET5	PGFET5	WTFET5[1]	WTFET5[0]	ADENFET5	ENFET5		
0	0	0	0	0	0	1	0		
r	r	r	r	r/w	r/w	r/w	r/w		
TOFET5	Time-out FET5, sta 0: no time-out dete 1: time-out detected	art-up, overload cted d							
OCFET5	Overcurrent FET5 0: no overcurrent detected 1: overcurrent detected								
OTFET5	Overtemperature FET5 0: no overtermperature detected 1: overtemperature detected								
PGFET5	Power good of FET 0: no output voltage 1: output voltage po	۲5 status e power good ower good							
WTFET5[1:0]	Wait time for current limited time-out of FET5 00: 200-µs minimum wait time 01: 800-µs minimum wait time 10: 1600-µs minimum wait time 11: 3200-µs minimum wait time								
ADENFET5	Enable output auto-discharge of FET5 0: disabled 1: enabled								
ENFET5	Enable FET5 0: disabled 1: enabled								



Table 22. FET6_CTRL Register Address: 0x14

B7	B6	B5	B4	B3	B2	B1	B0	
TOFET6	OCFET6	OTFET6	PGFET6	WTFET6[1]	WTFET6[0]	ADENFET6	ENFET6	
0	0	0	0	0	0	1	0	
r	r	r	r	r/w	r/w	r/w	r/w	
TOFET6	Time-out FET6, sta 0: no time-out detected 1: time-out detected	rt-up, overload cted d						
OCFET6	Overcurrent FET6 0: no overcurrent detected 1: overcurrent detected							
OTFET6	Overtemperature FET6 0: no overtermperature detected 1: overtemperature detected							
PGFET6	Power good of FET 0: no output voltage 1: output voltage po	6 status e power good ower good						
WTFET6[1:0]	Wait time for current limited time-out of FET6 00: 200-µs minimum wait time 01: 800-µs minimum wait time 10: 1600-µs minimum wait time 11: 3200-µs minimum wait time							
ADENFET6	Enable output auto-discharge of FET6 0: disabled 1: enabled							
ENFET6	Enable FET6 0: disabled 1: enabled							

Table 23. FET7	_CTRL Register	Address: 0x15
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B7	B6	B5	B4	B3	B2	B1	B0		
TOFET7	OCFET7	OTFET7	PGFET7	WTFET7[1]	WTFET7[0]	ADENFET7	ENFET7		
0	0	0	0	0	0	1	0		
r	r	r	r	r/w	r/w	r/w	r/w		
TOFET7	Time-out FET7, sta 0: no time-out dete 1: time-out detected	art-up, overload cted d							
OCFET7	Overcurrent FET7 0: no overcurrent detected 1: overcurrent detected								
OTFET7	Overtemperature FET7 0: no overtermperature detected 1: overtemperature detected								
PGFET7	Power good of FET 0: no output voltage 1: output voltage po	F7 status e power good ower good							
WTFET7[1:0]	Wait time for current limited time-out of FET7 00: 200 us minimum wait time 01: 800 us minimum wait time 10: 1600 us minimum wait time 11: 3200 us minimum wait time								
ADENFET7	Enable output auto 0: disabled 1: enabled	-discharge of FET7							
ENFET7	Enable FET7 0: disabled 1: enabled								

Table 24. AD_CTRL Register Address: 0x16

B7	B6	B5	B4	B3	B2	B1	B0			
reserved	ADSTART	ADEOC	ENADREF	ADC[3]	ADC[2]	ADC[1]	ADC[0]			
0	0	1	0	0	0	0	0			
r	r/w	r	r/w	r/w	r/w	r/w	r/w			
reserved							1			
ADSTART	ADC conversion start, bit is set to 0 if conversion is completed 0: no conversion in progress, conversion completed 1: start conversion									
ADEOC	ADC end of conversion 0: conversion not finished 1: conversion finished									
ENADREF	Enable ADC reference voltage 0: disabled 1: enabled									
ADC[3:0]	ADC input channel 0000: VAC 0001: VBAT 0010: IAC 0011: IBAT 0100: IDCDC1 0101: IDCDC2 0110: IDCDC3 0111: IFET1 1000: IFET2 1001: IFET3 1010: IFET4 1011: IFET5 1100: IFET6 1101: IFET7 1110: not used 1111: not used	select								

Table 25. AD_OUT1 Register Address: 0x17

B7	B6	B5	B4	B3	B2	B1	В0
AD0	AD0	AD0	AD0	AD0	AD0	AD0	AD0
0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r
AD0[7:0]	ADC result data [7:	0]	•	•			•

Table 26. AD_OUT2 Register Address: 0x18

B7	B6	B5	B4	B3	B2	B1	B0
reserved	reserved	reserved	reserved	reserved	reserved	AD0	AD0
0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r
reserved[5:0]				•			
AD0[9:8]	ADC result data [9:	8]					

Table 27. SPARE2 Register Address: 0x1B

B7	B6	B5	B4	B3	B2	B1	B0
OTP_RELOAD	SPARE2[6]	SPARE2[5]	SPARE2[4]	SPARE2[3]	SPARE2[2]	SPARE2[1]	SPARE2[0]
0	0	0	0	0	0	0	0
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
OTP_RELOAD	Register reset, bit is set to 0 after reset 0: no reset 1: reset register content						
SPARE2[6:0]	Spare user register	cells					



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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65090A front-end PMU integrated circuit is intended for systems powered by a 2- or 3-cell Li-lon or Li-Polymer battery with a typical voltage from 6 V to 17 V. Additionally, any other voltage source with a typical output voltage from 6 V to 7 V can power systems where the TPS65090A is used.

8.2 Typical Applications

8.2.1 Front-End PMU Application



Figure 46. Front-End PMU Application Diagram

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 28 as the input parameters.

PARAMETER	EXAMPLE VALUE
Input voltage range (VAC)	6 V to 17 V
VLDO1	5 V (on by default)
VLDO2	3.3 V (on by default)
DCDC1	5 V (off by default)
DCDC2	3.3 V (off by default)
DCDC3	3.3 V (off by default)

Table 28. Design Parameters

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Programming the Converter or Charger Output Voltage

Within the TPS65090A device, there are fixed and adjustable outputs. In the case where the voltage is adjustable, an external resistor divider is used to set the output voltage. The resistor divider must be connected between the output, the feedback pin and GND. When the output voltage is regulated properly, the voltage at the feedback pin will be in the range as defined in *Electrical Characteristics*, that is, 800 mV for DCDC3 and 2.1 V for the charger. The feedback pin typically has 0.1 μ A of leakage; to meet this current requirement and maintain the feedback voltage, TI recommends setting the feedback divider current by at least a factor of ten to one-hundred times that of the pin leakage. Using the feedback voltage of 2.1 V and 10 μ A (100 × 0.1 μ A), the resistor between the feedback pin and GND can be calculated to be less than 210 k Ω . This value for the resistor will provide sufficient current through the resistor divider at the typical feedback voltage. Selecting resistor values is a trade off between noise immunity and light load efficiency. The lower the resistor value, the higher the noise immunity; however, the more current through the resistor, the less efficient the converter is at light loads. Consider R1 is connected from the output of the inductor to the feedback pin and R2 from the feedback pin to ground. From the recommendations for R2, less than 210 k Ω , the value of the resistor connected between the output and feedback, R1, depending on the desired output voltage V_{OUT}, can be calculated using Equation 1.

$$R1 = R2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

Table 29 contains recommended values for the feedback divider for the most common output voltages.

Table 29. Feedback Resistor Values for Common Converter Output Voltages

OUTPUT VOLTAGE	1.2 V	1.35 V	1.8 V	3.3 V
R1 [kΩ]	260	330	510	750
R2 [kΩ]	510	470	400	240

Table 30. Feedback Resistor values for Common Charger Output voltages	Table 30.	Feedback	Resistor	Values	for	Common	Charger	Output	Voltages
-----------------------------------------------------------------------	-----------	----------	----------	--------	-----	--------	---------	--------	----------

OUTPUT VOLTAGE	8.4 V	12.6 V
R1 [kΩ]	330	1100
R2 [kΩ]	110	220

8.2.1.2.2 Programming Input DPM Current and Charge Current

Maximum input DPM current and charge current are defined by the values of the sense resistors used. The sense resistor value RS can be calculated using Equation 2.

$$RS = \frac{v_s}{l_s}$$
is the differential voltage at the sense input pins. For input current DPM, it is the differential voltage at the sense input pins.

V_S is the differential voltage at the sense input pins. For input current DPM, it is the differential voltage between ACP and ACN, and for charge current regulation, between SRP and SRN. For the differential voltage, TI recommends a maximum value of 40 mV here. More details can be found in *Electrical Characteristics - Power Path Control*.

I_S is the maximum current which must be controlled. For input current DPM, it is the maximum input current where charging is still allowed, and for charge current regulation, it is the maximum charge current.

8.2.1.2.3 Output Filter Design (Inductor and Output Capacitor)

The external components must fulfill the needs of the application, but also the stability criteria of the devices control loop. The is optimized to work within a range of L and C combinations. The LC output filter inductance and capacitance must be considered together, creating a double pole, responsible for the corner frequency of the converter.

8.2.1.2.4 Inductor Selection

At the L pins of the DC-DC converters and the charger, connecting an inductor is required.



(1)

(2)



(3)

At the DC-DC converters, TI recommends using a $2.2-\mu$ H inductor with an appropriate current rating for the application. The derated inductance at high currents should not drop lower than 1 μ H.

At the charger, TI recommends using a 2.2- μ H inductor for fast-charge currents of 3 A and above. For lower fast charge currents, 3.3 μ H can be used. The current rating of the inductor must be suitable for the maximum fast-charge current required in the application.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PSM transition point, the output voltage ripple, and the efficiency. The selected inductor must be rated for its DC resistance and saturation current. The inductor ripple current decreases with higher inductance and increases with higher V_{IN} or V_{OUT} .

To properly configure the converter, an inductor must be connected between pin L the output capacitors. To estimate the inductance value, Equation 3 can be used.

$$L = (V_{IN} - V_{OUT}) \times 0.5 \times \frac{\mu s}{A}$$

In Equation 3, the minimum inductance value, *L*, is calculated. V_{IN} is the minimum input voltage. As an example, a suitable inductor for generating 1.35 V from a two-cell Li-Ion battery is 2.2 μ H.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 4 shows how to calculate the peak current I_{MAX} in step-down mode operation.

$$I_{MAX} = \frac{I_{OUT}}{0.8} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times V_{IN} \times f \times L}$$
(4)

In the equation, *f* is the minimum switching frequency, which typically is in the range of 1 MHz. V_{IN} is the minimum input voltage. The critical current value for selecting the right inductor is the value of I_{MAX} . Consideration must be given to the load transients and error conditions that can cause higher inductor currents. This must be taken into consideration when selecting an appropriate inductor.

In DC-DC converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and by the inductor DCR value. To achieve high-efficiency operation, care must be taken in selecting inductors featuring a quality factor greater than 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The following inductor types from different suppliers have been used with TPS65090 converters:

VENDOR	INDUCTOR SERIES
Coilcraft	XAL4020-222, XAL5030-222
Cyntec	PILE061E-2R2MS-11
Toko	FDV0530-2R2M
Wurth Elektronik	WE 74437324022

Table 31. List of Inductors

8.2.1.2.5 Capacitor Selection

8.2.1.2.5.1 Input Capacitor

Because of the nature of the switching converter and charger with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, TI recommends a ceramic capacitor of at least $10-\mu$ F. The voltage rating and DC bias characteristic of ceramic capacitors must be considered. The input capacitor can be increased without any limit for better input voltage filtering. TI recommends a ceramic capacitor placed as close as possible to the respective VSYS and PGND pins of the IC.

8.2.1.2.5.2 DC-DC Converter and Charger Bootstrap Capacitors

To make sure that the internal high side gate drivers are supplied with a stable low noise supply voltage, a capacitor must be connected between the CBx pins and the respective Lx pins.

TI recommends using a ceramic capacitor with a value of 4700 pF. The value of this capacitor should not be lower than 2200 pF or higher than 0.01 μ F. For testing, a 4700-pF, size 0402, 6.3-V capacitor was used.

8.2.1.2.5.3 DC-DC Converter and Charger Output Capacitors

TI recommends ceramic capacitors with low ESR values that provide the lowest output voltage ripple. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance overtemperature, become resistive at high frequencies.

At light load currents, the converter operates in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC - bias voltage.

For the output capacitors of the DC-DC converters and the charger, TI recommends the use of small ceramic capacitors placed as close as possible to the output pins and the respective PGND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the output pins of the IC.

At the DC-DC converters, TI recommends the capacitance close to the IC to be close to 22 μ F. It should not be lower than 10 μ F or higher than 47 μ F.

At the charger, TI recommends a 22-µF capacitance.

To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

$$C_{OUT} \ge \frac{22 \cdot \mu F \cdot \mu H}{L}$$
(5)

A capacitor with a value in the range of or higher than the calculated minimum should be used. This is required to maintain control loop stability.

8.2.1.2.5.4 LDO Output Capacitors

To achieve stable and accurate output voltage regulation of the LDO's, a small ceramic capacitor is required at their outputs. TI recommends using at least 2.2 μ F.

8.2.1.2.5.5 Load Switches Output Capacitors

The maximum expected output capacitance at the load switches is 47 µF. Any lower value can be used.

8.2.1.2.6 Charger Battery Temperature Sensing

To measure the battery cell temperature, resistors with temperature dependent resistance (NTC) must be placed close to the cells which must be measured. The device supports using two independent measuring points with its TS1 and TS2 input pins. The temperature sense resistor and the linearizing resistor network must be the same. If only one temperature sense resistor is used, the sense resistor network must be connected to TS1 and TS2.

As a default, the internal circuit is optimized to work with a 10-k Ω NTC resistor with a temperature characteristic described with a B value in the range of 3450 with one resistor in parallel and one resistor in series for linearization and to define the resistor-divider connected to VREFT, TSx and AGND. A possible default example would be NTCS0805E3103FLT from Vishay in parallel with a 6.8-k Ω resistor and a 2.2-k Ω resistor in series.

8.2.1.2.7 Reverse Voltage Protection

To protect the design against reverse voltage at the AC adapter input, additional external components are required. The pins VAC, VACS and the input path switches are exposed to the negative voltage and need some protection.

To protect the VAC pin, TI recommends using a small signal diode between the adapter input and the VAC pin.

Protecting VACS can be done either by connecting this pin to the protected VAC with the tradeoff of losing accuracy or connecting VACS to the adapter input with a $10-k\Omega$ resistor.



To make sure that the AC switches are not turned on with the reverse voltage at the AC adapter input, a small signal N-channel FET can be used to short the voltage at ACG to ACS. The source of this FET must be connected to ACS, the drain to ACG. The gate must be connected to the AC adapter input GND either direct, or if the maximum gate voltage rating does not match the maximum input voltage, with a resistor-divider between AC adapter input GND and ACS. An example for the small signal FET would be BSS138W-7-F. To protect the ACS and the ACG pin resistors with values in the range of 4.7 k Ω or higher between the pins and the gate and source pins of the AC FET's must be used.

An example for this additional reverse protection circuit can be found in the *TPS65090EVM User's Guide*, SLVU778.

8.2.1.2.8 AC Switches

The AC adapter protection switches are recommended as CSD17304Q3: MOSFET, NChan, 30 V, 56 A, 9.8 mΩ.

8.2.1.2.9 Battery Switches

The battery switches are recommended as CSD25401Q3: MOSFET, PChan, -20 V, 60 A, 8.7 mΩ.



8.2.1.3 Application Curves



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8.2.2 DC-DC Converters



Figure 69.	DC-DC	Converters	Circuit	Drawing
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Table 32.	List of	Components	- DCDC1
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REFERENCE	DESCRIPTION	MANUFACTURER
L	2.2 μH, 5 mm × 5 mm × 3 mm	XAL5030-222, Coilcraft
C _{IN}	10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata
C _{OUT}	4 × 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	2.2 µF 10 V, 0603, X7R ceramic	GRM155R61A225KE95, Murata
C _{B1}	4700 pF, X7R ceramic	
R _{FB1}	Not used, FB1 is directly connected to VDCDC1	
R _{FB2}	Not used	

Table 33. List of Components - DCDC2

REFERENCE	DESCRIPTION	MANUFACTURER
L	2.2 μH, 5 mm × 5 mm × 3 mm	XAL5030-222, Coilcraft
C _{IN}	10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata
C _{OUT}	4 x 10 µF, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata
	2.2 µF 10 V, 0603, X7R ceramic	GRM155R61A225KE95, Murata
C _{B2}	4700 pF, X7R ceramic	
R _{FB1}	Not used, FB2 is directly connected to VDCDC2	
R _{FB2}	Not used	

Table 34. List of Components - DCDC3

REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS
L	2.2 μH, 5 mm × 5 mm × 3 mm	XAL5030-222, Coilcraft	
C _{IN}	10 $\mu F,25$ V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata	
C _{OUT}	4 \times 10 $\mu F,$ 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	2.2 µF 10 V, 0603, X7R ceramic	GRM155R61A225KE95, Murata	
C _{B1}	4700 pF, X7R ceramic	Any	

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Table 34. List of Com	ponents - DCDC3	(continued)
		· /

REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS		
R _{FB1}	162 kΩ, 1%, 0402	Any	$V_{DCDC3} = 1 V$		
	330 kΩ, 1%, 0402	Any	V _{DCDC3} = 1.35 V		
	453 kΩ, 1%, 0402	Any	$V_{DCDC3} = 1.8 V$		
	590 kΩ, 1%, 0402	Any	$V_{DCDC3} = 3.3 V$		
	649 kΩ, 1%, 0402	Any	$V_{DCDC3} = 4 V$		
	787 kΩ, 1%, 0402	Any	V _{DCDC3} = 5 V		
R _{FB2}	649 kΩ, 1%, 0402	Any	V _{DCDC3} = 1 V		
	470 kΩ, 1%, 0402	Any	V _{DCDC3} = 1.35 V		
	365 kΩ, 1%, 0402	Any	V _{DCDC3} = 1.8 V		
	187 kΩ, 1%, 0402	Any	V _{DCDC3} = 3.3 V		
	162 kΩ, 1%, 0402	Any	V _{DCDC3} = 4 V		
	150 kΩ, 1%, 0402	Any	$V_{DCDC3} = 5 V$		

8.2.3 Charger



Figure 70. Charger Circuit Drawing

Table 35. List of Components - Charger

REFERENCE	DESCRIPTION	MANUFACTURER	COMMENTS
L	2.2 μH, 5 mm × 5 mm × 3 mm	XAL5030-222, Coilcraft	
C _{IN}	$2 \times 10 \ \mu$ F, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata	
C _{OUT}	$2 \times 10 \ \mu$ F, 25 V, 0603, X7R ceramic in parallel to	GRM188R61E106ME73, Murata	
	1 µF, 25 V, 0402, X7R ceramic	GRM155R61E105MA12, Murata	
C _{BC}	4700 pF, X7R ceramic	Any	
R _S	10 mΩ, 0.1%, 1206	Any	Maximum charge current 4 A
R _{FB1}	330 kΩ, 1%, 0402	Any	Charge termination voltage $V_{BAT} = 8.4$ V
	1100 kΩ, 1%, 0402	Any	Charge termination voltage $V_{BAT} = 12.6$ V
R _{FB2}	110 kΩ, 1%, 0402	Any	Charge termination voltage $V_{BAT} = 8.4$ V
	220 kΩ, 1%, 0402	Any	Charge termination voltage $V_{BAT} = 12.6$ V



9 Power Supply Recommendations

The TPS65090A device integrates a power path management system that automatically switches power to the load from either an AC adapter or from battery power. The voltage range for the AC adapter should fall within the 6 V to 17 V range. Battery power can be provided by either a dual or triple Li-Ion or Li-Polymer cell battery pack. On power up, the battery pack is connected to the load by default. However, if a valid voltage is detected on the VACS pin and the voltage on the VAC pin is higher than the battery voltage, the battery is disconnected and the AC adapter is connected to the load through the external power path switches.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, TI recommends short traces, as well as separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

A complete layout example can be found in the TPS65090EVM User's Guide (SLVU778).

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10.2 Layout Example



Figure 71. DCDC1 Layout Example



10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB by soldering the PowerPAD.
- Introducing airflow in the system.

For more details on how to use the thermal parameters in the dissipation ratings table, see the *Thermal Characteristics Application Note* (SZZA017) and the *IC Package Thermal Metrics Application Note* (SPRA953).

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Thermal Characteristics Application Note, SZZA017
- IC Package Thermal Metrics Application Note, SPRA953
- TPS65090EVM User's Guide, SLVU778

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TPS65090ARVNR	ACTIVE	VQFN-MR	RVN	100	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65090A	Samples
TPS65090ARVNT	ACTIVE	VQFN-MR	RVN	100	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65090A	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



*All dimensions are nominal



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65090ARVNR	VQFN- MR	RVN	100	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TPS65090ARVNT	VQFN- MR	RVN	100	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

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PACKAGE MATERIALS INFORMATION

16-Jun-2015



*All dimensions are nominal

Device Package Type		Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65090ARVNR	VQFN-MR	RVN	100	2500	367.0	367.0	38.0
TPS65090ARVNT	VQFN-MR	RVN	100	250	210.0	185.0	35.0

MECHANICAL DATA



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
 Quad Flatpack, No-leads (QFN) staggered multi-row pack
- C. Quad Flatpack, No-leads (QFN) staggered multi-row package configuration.
- A Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated.
 - The Pin A1 identifiers are either a molded, marked, or metal feature.
- E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- F. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



RVN (S-PVQFN-N100)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.





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