TPS6216x-Q1 3-V to 17-V 1-A Step-Down Converter with DCS-Control™

1 Features

- DCS-Control™ Topology
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade: –40°C to 125°C Operating Junction Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range: 3 V to 17 V
- Up to 1-A Output Current
- Adjustable Output Voltage from 0.9 V to 6 V
- Fixed Output Voltage Versions
- Seamless Power Save Mode Transition
- Typically 17-µA Quiescent Current
- Power Good Output
- 100% Duty Cycle Mode
- Short Circuit Protection
- Over Temperature Protection
- Pin to Pin Compatible With TPS62170-Q1
- Available in a 2 × 2 mm WSON-8 Package

2 Applications

- Automotive 12-V Rail Supplies
- Power Over Coax POL Supply
- Camera, Video Modules
- LDO Alternative

3 Description

The TPS6216x-Q1 are easy to use synchronous step down DC-DC converters optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology.

With their wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. It supports up to 1-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

Power sequencing is also possible by configuring the Enable and open-drain Power Good pins.

In Power Save Mode, the devices draw quiescent current of about 17 µA from VIN. Power Save Mode, entered automatically and seamlessly if load is small, maintains high efficiency over the entire load range. In Shutdown Mode, the device is turned off and shutdown current consumption is less than 2 µA.

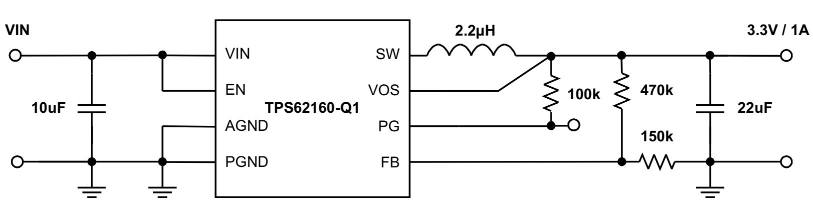
The devices are available in adjustable and fixed output voltage versions and are packaged in an 8-pin WSON package measuring 2 × 2 mm (DSG).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62160-Q1	WSON (8)	2.00 mm × 2.00 mm
TPS62162-Q1	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



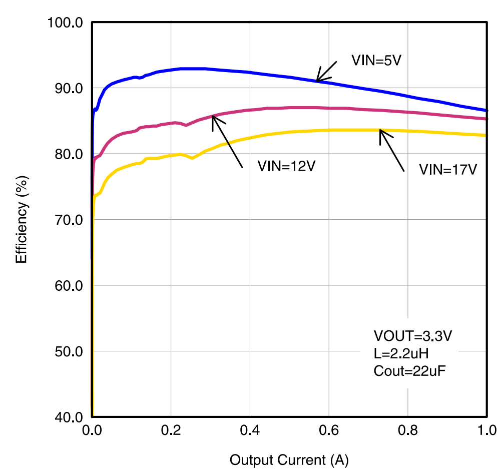


Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2014) to Revision A	Page
• Added device TPS62162-Q1	1
• Added the *Device Comparison Table*	3
• Changed the *Thermal Information* table	4
• Added Warranty disclaimer NOTE: at *Application and Implementation* section.	12
• Added *Related Links* section	25
• Added *Receiving Notification of Documentation Updates* and *Community Resources* sections	25

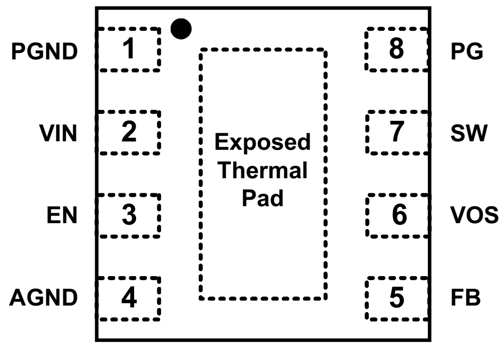
6 Device Comparison Table

PART NUMBER(1)	OUTPUT VOLTAGE
TPS62160-Q1	adjustable
TPS62162-Q1	3.3 V

(1) For detailed ordering information please check the Mechanical, Packaging, and Orderable Information section at the end of this datasheet.

7 Pin Configuration and Functions

8-Pin WSON
DSG Package
(Top View)



Pin Functions

PIN(1)		I/O	DESCRIPTION
NAME	NUMBER		
PGND	1		Power ground
VIN	2	I	Supply voltage
EN	3	I	Enable input (High = enabled, Low = disabled)
AGND	4		Analog Ground
FB	5	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
VOS	6	I	Output voltage sense pin and connection for the control loop circuitry.
SW	7	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	8	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pull-up resistor; goes high impedance, when device is switched off)
Exposed Thermal Pad			Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application Information* sections.

8 Specifications

8.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range(2)	VIN	–0.3	20	V
	EN, SW	–0.3	V_{IN}+0.3	V
	FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Operating junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	3		17	V
V_{OUT}	Output voltage range	0.9		6	V
T_J	Operating junction temperature	–40		125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS6216x-Q1	UNIT
		DSG (8 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Over junction temperature range (T_J = –40°C to +125°C), typical values at V_{IN} = 12 V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range(1)		3		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, Device not switching		17	30	µA
I_{SD}	Shutdown current(2)	EN = Low		1.8	25	µA
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage	2.6	2.7	2.82	V
		Hysteresis		180		mV
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
CONTROL (EN, PG)						
V_{EN_H}	High level input threshold voltage (EN)		0.9			V
V_{EN_L}	Low level input threshold voltage (EN)				0.3	V
I_{LKG_EN}	Input leakage current (EN)	EN = V_{IN} or GND		0.01	1	µA
V_{TH_PG}	Power Good threshold voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	93%	
V_{OL_PG}	Power Good output low	I_{PG} = –2 mA		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V		1	400	nA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V		300	600	mΩ
		V_{IN} = 3 V		430		
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V		120	200	mΩ
		V_{IN} = 3 V		165		
I_{LIMF}	High-side MOSFET forward current limit(3)	V_{IN} = 12 V, T_A = 25°C	1.45	1.95	2.45	A
OUTPUT						
VREF	Internal reference voltage			0.8		V
I_{LKG_FB}	Pin leakage current (FB)	V_{FB} = 1.2 V		5	400	nA
V_{OUT}	Output voltage range (TPS62160-Q1)	V_{IN} ≥ V_{OUT}	0.9		6.0	V
	Feedback voltage accuracy(4)	PWM Mode operation, V_{IN} ≥ V_{OUT} + 1 V	–3%		3%	
		Power Save Mode operation, C_{OUT} = 2x22 µF(5)	–3%		4%	
	DC output voltage load regulation(6)	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM Mode operation		0.05		% / A
	DC output voltage line regulation (6)	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A, PWM Mode operation		0.02		% / V

(1) The device is still functional down to Under Voltage Lockout (see parameter V_{UVLO}).
(2) Current into VIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see *Current Limit and Short Circuit Protection*).
(4) For fixed voltage versions, the (internal) resistive feedback divider is included.
(5) The output voltage accuracy in Power Save Mode can be improved by increasing the C_{OUT} value, reducing the output voltage ripple.
(6) Line and load regulation are depending on external component selection and layout (see Figure 16 and Figure 17).

8.6 Typical Characteristics

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

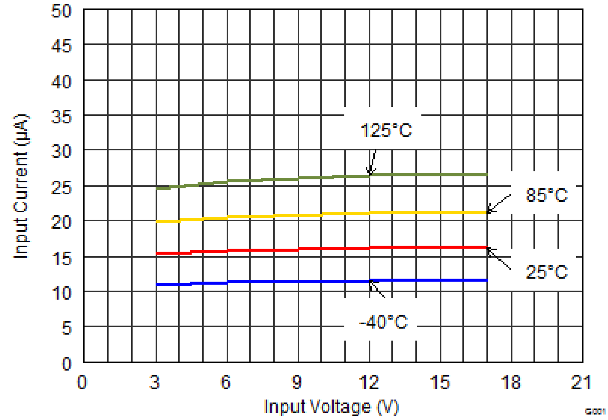


Figure 1. Quiescent Current

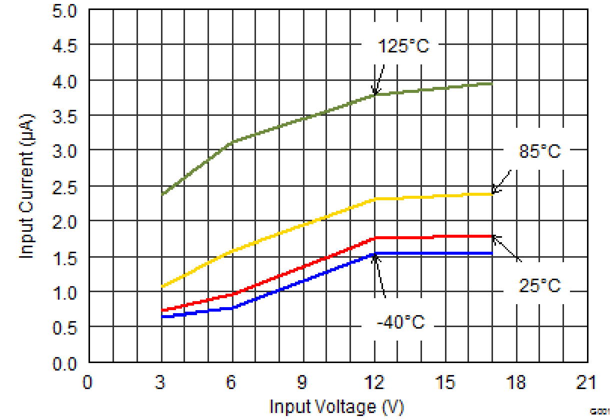


Figure 2. Shutdown Current

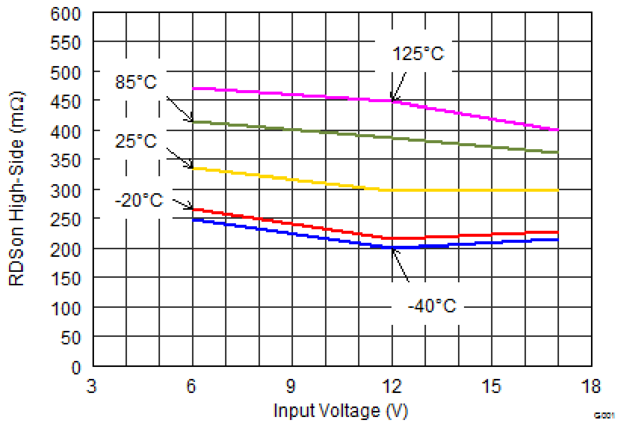


Figure 3. High-Side Static Drain-Source-Resistance (R_{DSon})

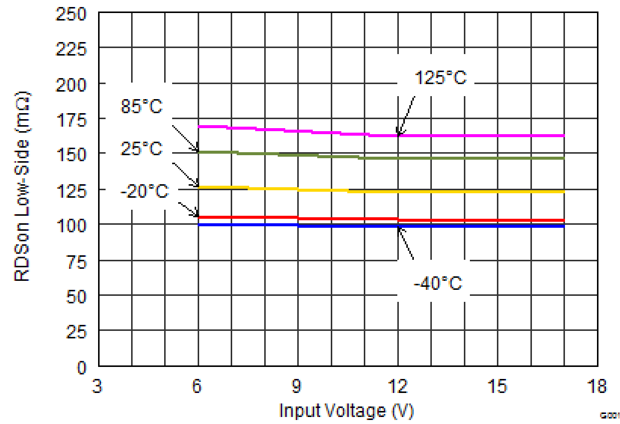


Figure 4. Low-Side Static Drain-Source-Resistance (R_{DSon})

9 Detailed Description

9.1 Overview

The TPS6216x-Q1 synchronous switched mode power converter is based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless transition into power save mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

9.2 Functional Block Diagram

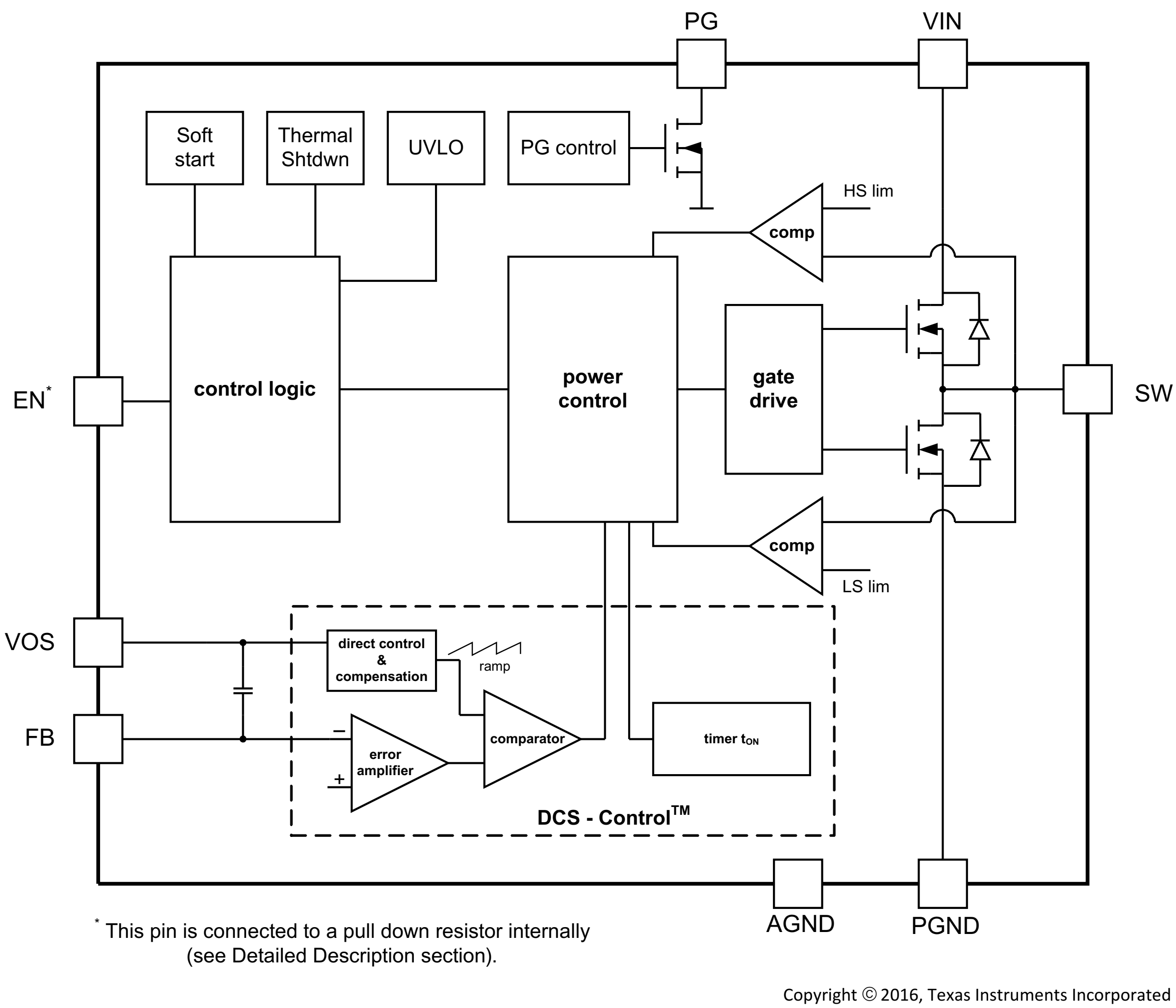


Figure 5. TPS62160-Q1 (Adjustable Output Voltage)

Functional Block Diagram (continued)

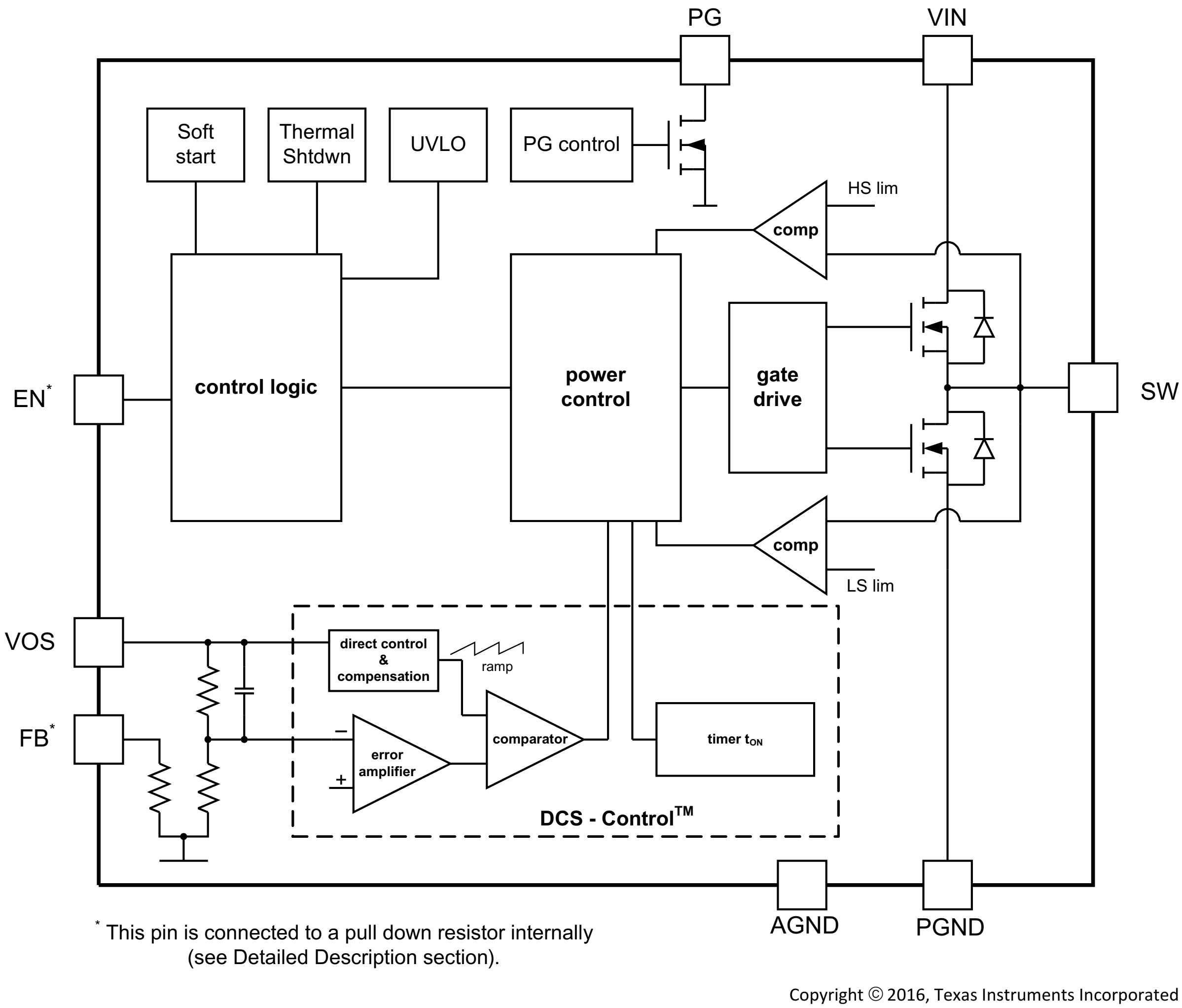


Figure 6. TPS62162-Q1 (Fixed Output Voltage)

9.3 Feature Description

9.3.1 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation.

Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.8 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin is Low, an internal pull-down resistor of about 400 kΩ is connected and keeps it Low in case of floating pin.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

9.3.2 Softstart

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and V_{OUT} rises with a slope of about 25 mV/µs. See Figure 28 and Figure 29 for typical startup operation.

Feature Description (continued)

The TPS6216x-Q1 can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

9.3.3 Power Good (PG)

The TPS6216x-Q1 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown.

9.3.4 Under Voltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180 mV.

9.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

The TPS6216x-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25 MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

9.4.2 Power Save Operation

The TPS6216x-Q1's built in Power Save Mode will be entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

The TPS6216x-Q1 includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 420ns \quad (1)$$

For very small output voltages, the on-time increases beyond the result of Equation 1, to stay above an absolute minimum on-time, $t_{ON(min)}$, which is around 80 ns to limit switching losses.

Device Functional Modes (continued)

The peak inductor current in PSM can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ON} \quad (2)$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS6216x-Q1 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

9.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences, e.g. for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (3)$$

where

I_{OUT} is the output current,
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET and
R_L is the DC resistance of the inductor used.

9.4.4 Current Limit and Short Circuit Protection

The TPS6216x-Q1 is protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET will be turned off. Avoiding shoot through current, the low-side FET is then switched on to allow the inductor current to decrease. The high-side FET will turn on again, only if the current in the low-side FET has decreased below the low side current limit threshold.

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time.

The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \times t_{PD} \quad (4)$$

where

I_{LIMF} is the static current limit, specified in the electrical characteristic table,
L is the inductor value,
V_L is the voltage across the inductor and
t_{PD} is the internal propagation delay.

Device Functional Modes (continued)

The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF\_HS} + \frac{(V_{IN} - V_{OUT})}{L} \times 30ns \quad (5)$$

Care on the current limit has to be taken if the input voltage is high and very small inductances are used.

9.4.5 Operation Above T_J = 125°C

The operating junction temperature of the device is specified up to 125°C. In power supply circuits, the self heating effect causes, that the junction temperature, T_J, is even higher than the ambient temperature T_A. Depending on T_A and the load current, the maximum operating temperature T_J can be exceeded. However, the electrical characteristics are specified up to a T_J of 125°C only. The device operates as long as thermal shutdown threshold is not triggered.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6216x-Q1 is a synchronous switched mode step-down converter, able to convert a 3 V to 17 V input voltage into a lower, 0.9 V to 6 V, output voltage, providing up to 1-A load current. The following section gives guidance on the external component selection to operate the device within the recommended operating conditions.

10.2 Typical TPS62160-Q1 Application

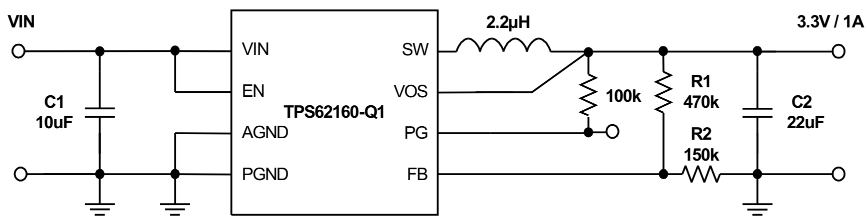


Figure 7. 3.3-V / 1-A Power Supply

10.2.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole VIN, VOUT, and load current range of TPS6216x-Q1. Using Table 2, the design procedure needs minimum effort.

Table 1. Components Used for Application Characteristics

REFERENCE	DESCRIPTION	MANUFACTURER(1)
IC	17-V, 1-A step-down converter, WSON	TPS62160QDSG, Texas Instruments
L1	2.2-µH, 1.4-A, 3 x 2.8 x 1.2 mm	VLF3012ST-2R2M1R4, TDK
C1	10-µF, 25-V, ceramic, 0805	Standard
C2	22-µF, 6.3-V, ceramic, 0805	Standard
R1	Depending on Vout	
R2	Depending on Vout	
R3	100-kΩ, chip, 0603, 1/16-W, 1%	Standard

(1) See *Third-Party Products Disclaimer*

10.2.2 Detailed Design Procedure

10.2.2.1 Programming the Output Voltage

While the output voltage of the TPS62160-Q1 is adjustable, the TPS62162-Q1 is programmed to a fixed output voltage of 3.3V. For the fixed output voltage version, the FB pin is pulled down internally and may be left floating. It is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2 uA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{6}$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin to about 7.4 V.

10.2.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6216x-Q1 is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter And Loop Stability* section). Table 2 can be used to simplify the output filter component selection.

Table 2. Recommended LC Output Filter Combinations(1)

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
1µH							
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.
(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in SLVA463.

10.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \tag{7}$$

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L(min) \times f_{SW}} \right) \quad (8)$$

where

- I_L(max) is the maximum inductor current,
- ΔI_L is the Peak-to-Peak Inductor Ripple Current,
- L(min) is the minimum effective inductor value and
- f_{SW} is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6216x-Q1 and are recommended for use:

Table 3. List of Inductors

TYPE	INDUCTANCE [µH]	CURRENT [A][1]	DIMENSIONS [L x B x H] mm	MANUFACTURER[2]
VLF3012ST-2R2M1R4	2.2 µH, ±20%	1.9 A	3.0 x 2.8 x 1.2	TDK
VLF302512MT-2R2M	2.2 µH, ±20%	1.9 A	3.0 x 2.5 x 1.2	TDK
VLS252012T-2R2M1R3	2.2 µH, ±20%	1.3 A	2.5 x 2.0 x 1.2	TDK
XFL3012-222MEC	2.2 µH, ±20%	1.9 A	3.0 x 3.0 x 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.6 A	3.0 x 3.0 x 1.2	Coilcraft
LPS3015-332ML_	3.3 µH, ±20%	1.4 A	3.0 x 3.0 x 1.4	Coilcraft
NR3015T-2R2M	2.2 µH, ±20%	1.5 A	3.0 x 3.0 x 1.5	Taiyo Yuden
744025003	3.3 µH, ±20%	1.5 A	2.8 x 2.8 x 2.8	Wuerth
PSI25201B-2R2MS	2.2 µH, ±20%	1.3 A	2.0 x 2.5 x 1.2	Cyntec

(1) I_{RMS} at 40°C rise or I_{SAT} at 30% drop.
(2) See *Third-Party Products Disclaimer*

The TPS6216x-Q1 can be run with an inductor as low as 2.2 µH. However, for applications with low input voltages, 3.3 µH is recommended, to allow the full output current. The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (9)$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

10.2.2.2.2 Capacitor Selection

10.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22 uF. The architecture of the TPS6216x-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

NOTE

In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

10.2.2.2.2.2 Input Capacitor

For most applications, 10 µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

10.2.2.3 Output Filter And Loop Stability

The TPS6216x-Q1 is internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 10:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \quad (10)$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which might be affected. More information including a detailed L-C stability matrix can be found in SLVA463.

The TPS6216x-Q1 includes an internal 25-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 11 and Equation 12:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 25\ \text{pF}} \quad (11)$$

$$f_{pole} = \frac{1}{2\pi \times 25\ \text{pF}} \times \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \quad (12)$$

Though the TPS6216x-Q1 is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability vs transient response can be found in SLVA289 and SLVA466.

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see **NOTE** in DC Bias effect section).

10.2.3 Application Performance Plots

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

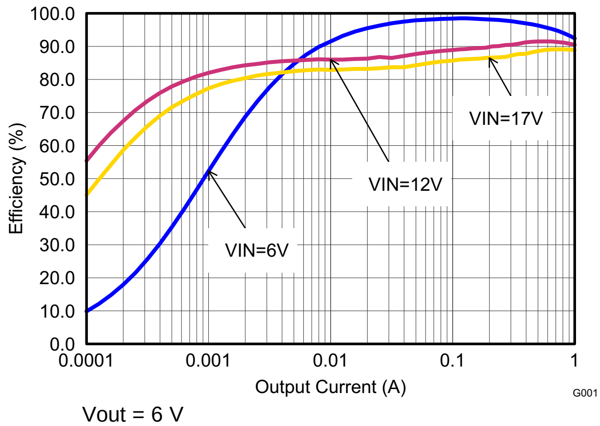


Figure 8. Efficiency vs Output Current

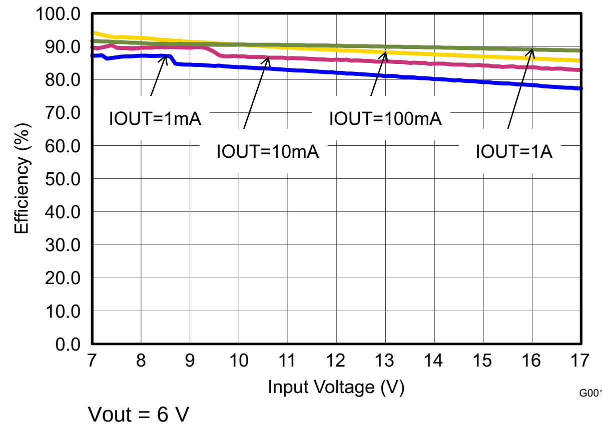


Figure 9. Efficiency vs Input Voltage

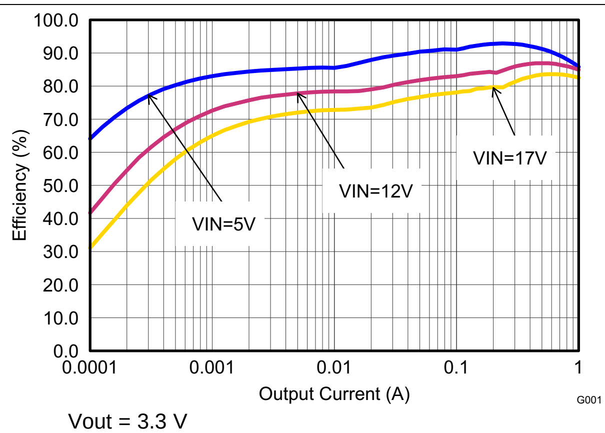


Figure 10. Efficiency vs Output Current

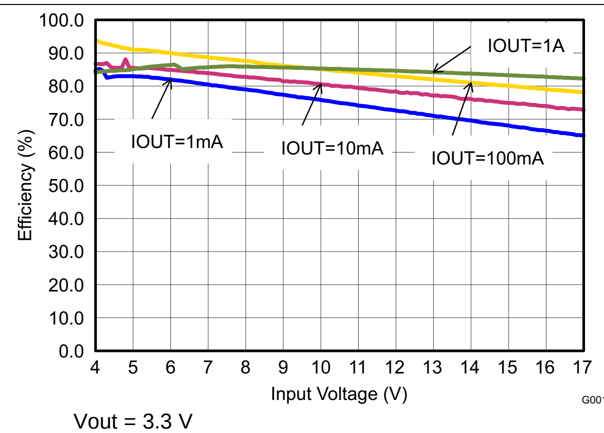


Figure 11. Efficiency vs Input Voltage

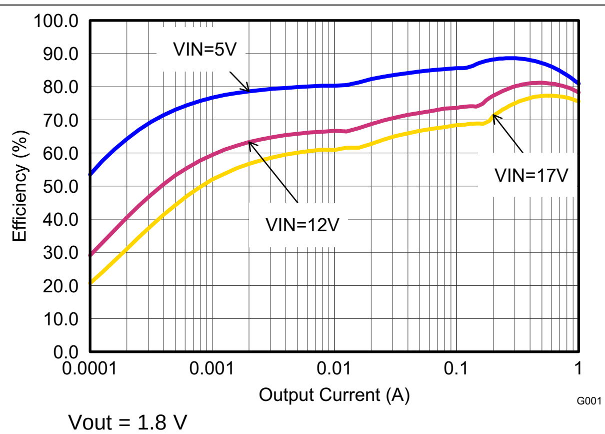


Figure 12. Efficiency vs Output Current

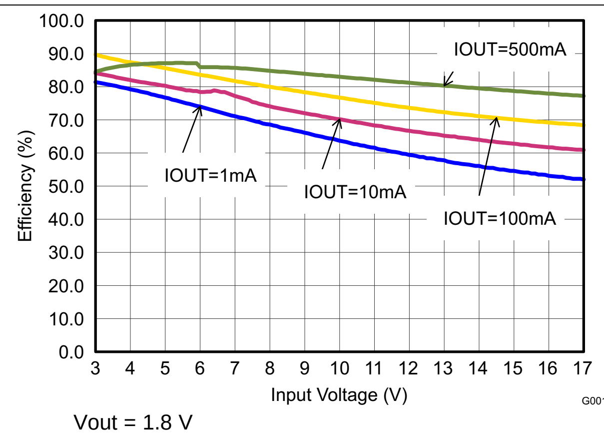
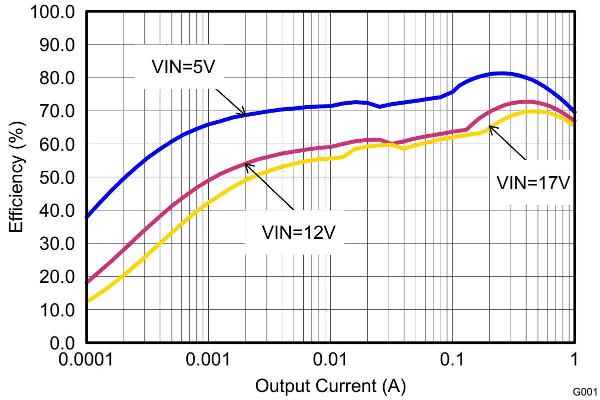


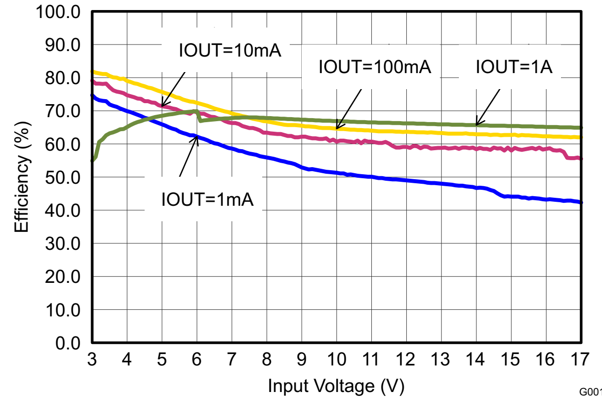
Figure 13. Efficiency vs Input Voltage

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)



Vout = 0.9 V

Figure 14. Efficiency vs Output Current



Vout = 0.9 V

Figure 15. Efficiency vs Input Voltage

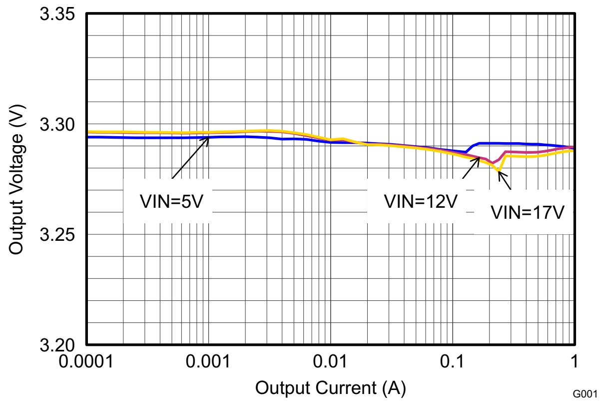


Figure 16. Output Voltage Accuracy (Load Regulation)

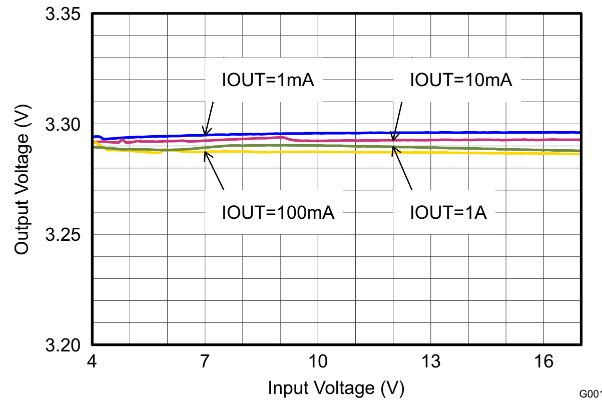


Figure 17. Output Voltage Accuracy (Line Regulation)

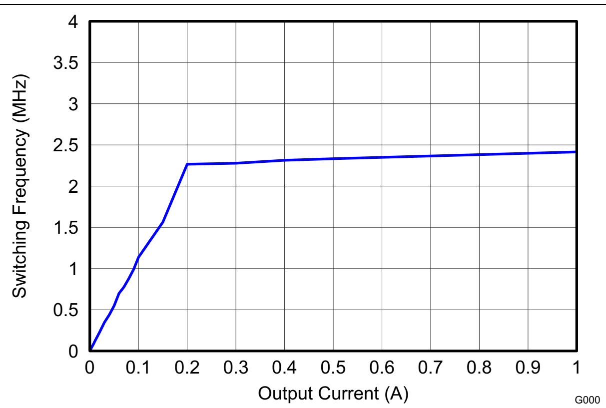


Figure 18. Switching Frequency vs Output Current

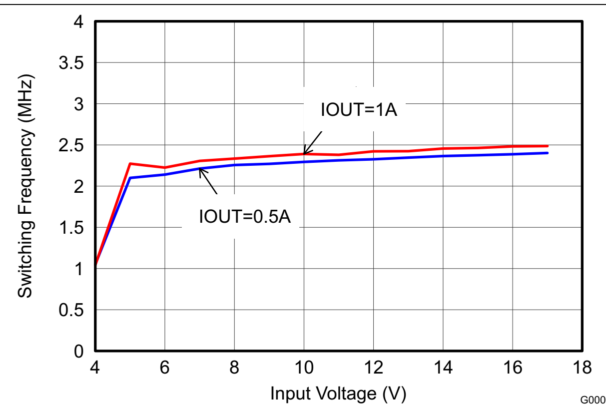


Figure 19. Switching Frequency vs Input Voltage

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)

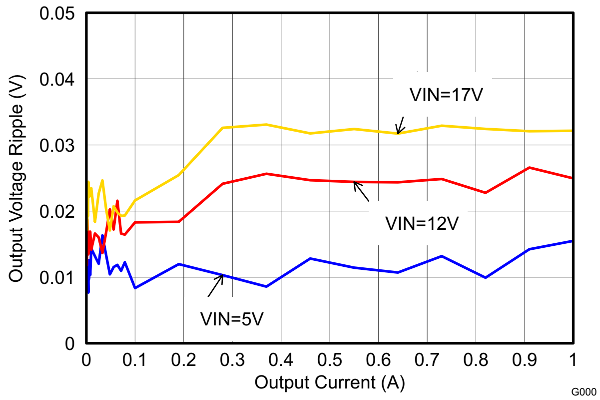


Figure 20. Output Voltage Ripple

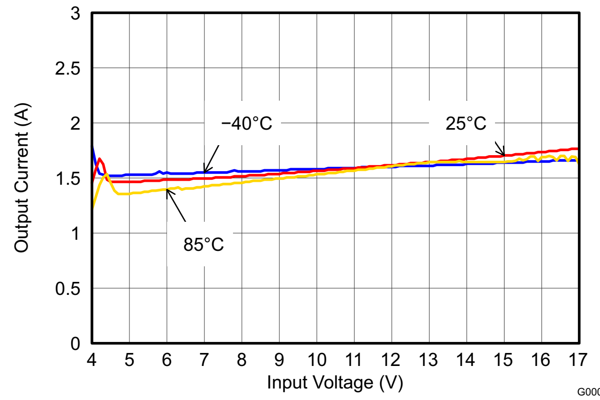


Figure 21. Maximum Output Current

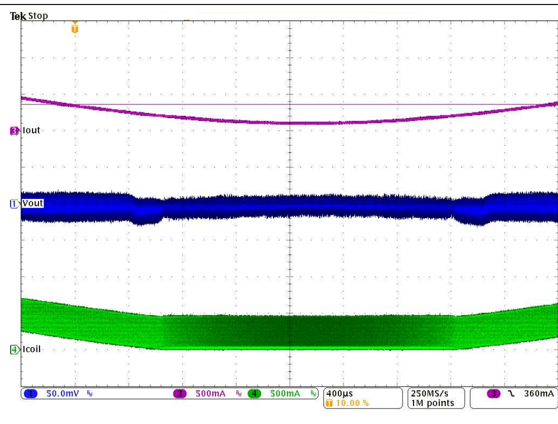


Figure 22. PWM / PSM Mode Transitions

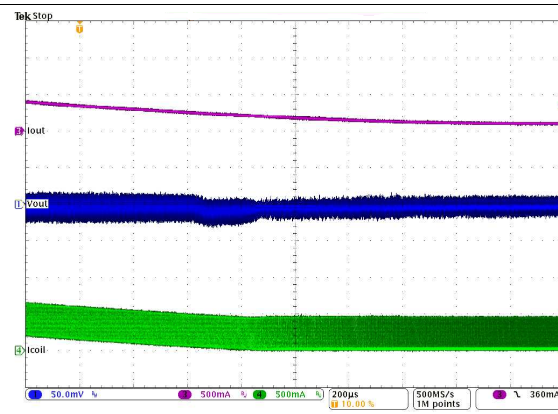
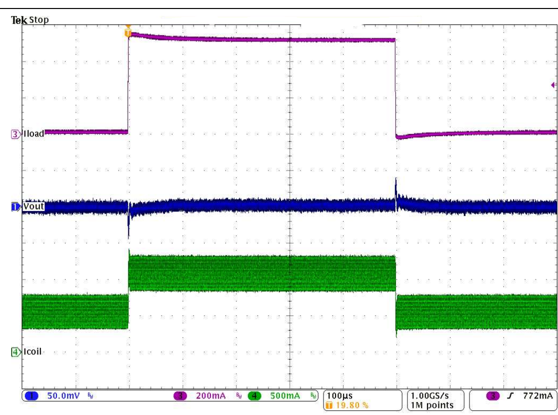
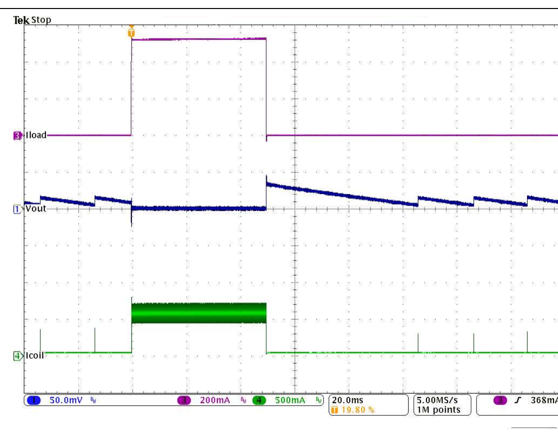


Figure 23. PWM to PSM Mode Transition



500 mA to 1 A

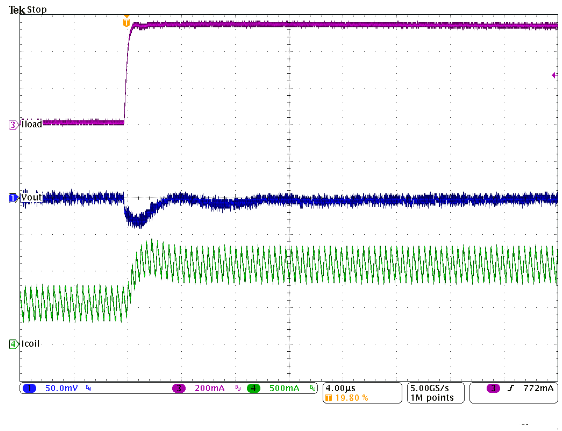
Figure 24. Load Transient Response in PWM Mode



100 mA to 500 mA

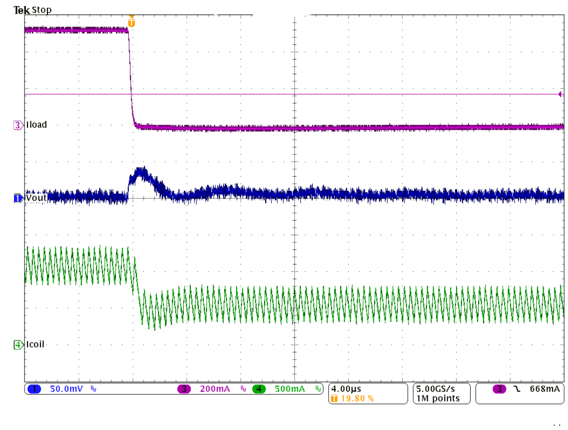
Figure 25. Load Transient Response from Power Save Mode

At V_{IN} = 12 V, V_{OUT} = 3.3 V and T_J = 25°C (unless otherwise noted)



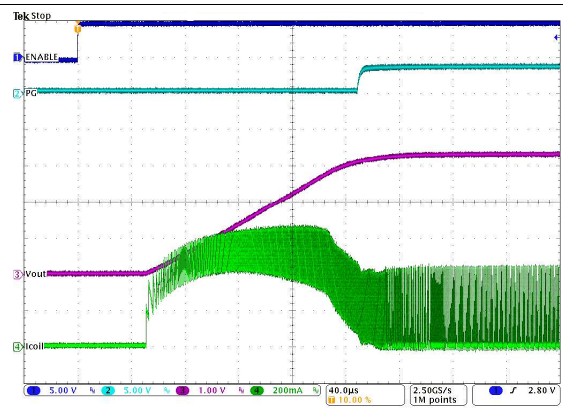
500 mA to 1 A, Rising edge

Figure 26. Load Transient Response in PWM Mode



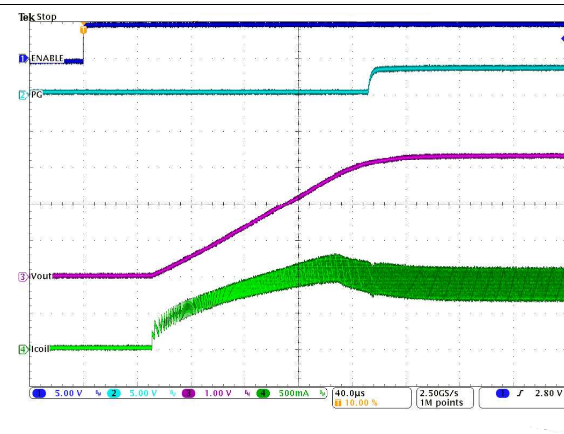
500 mA to 1 A, Falling edge

Figure 27. Load Transient Response in PWM Mode



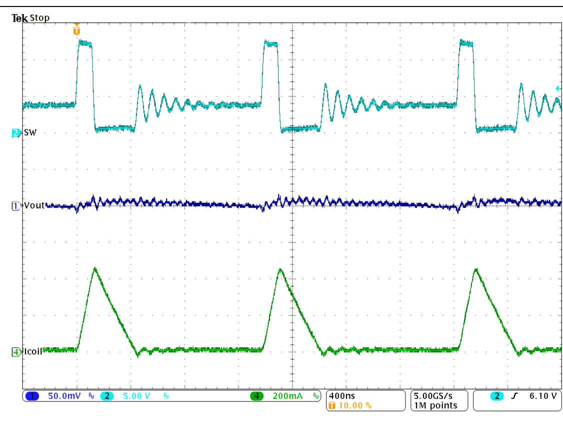
Iout = 100 mA

Figure 28. Startup



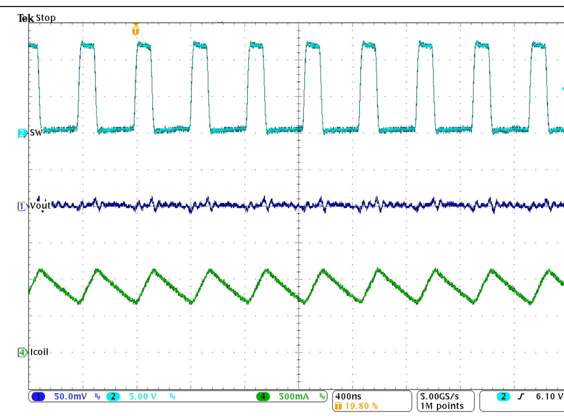
Iout = 1 A

Figure 29. Startup



Iout = 66 mA

Figure 30. Typical Operation in Power Save Mode



Iout = 1 A

Figure 31. Typical Operation in PWM Mode

10.3 System Examples

10.3.1 Inverting Power Supply

The TPS6216x-Q1 can be used as inverting power supply by rearranging external circuitry as shown in Figure 32. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17 V (see Equation 13).

$$V_{IN} + |V_{OUT}| \leq V_{IN\,max} \tag{13}$$

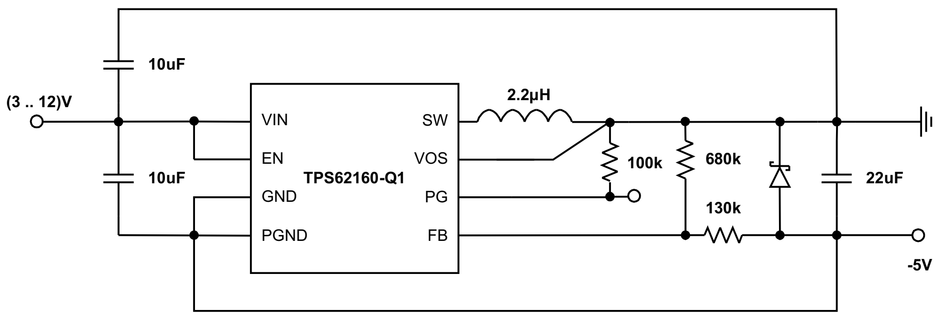


Figure 32. –5-V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in SLVA469.

10.3.2 Various Output Voltages

The TPS62160-Q1 can be set for different output voltages between 0.9 V and 6 V. Some examples are shown below.

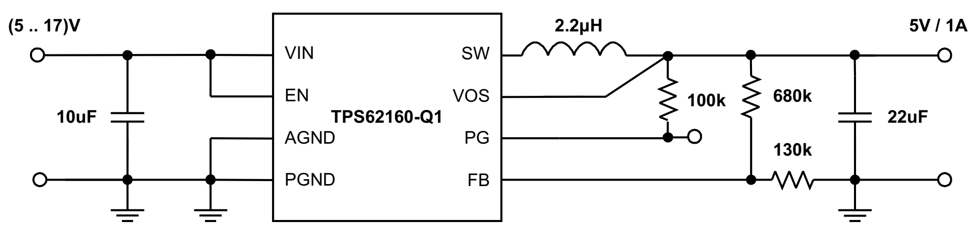


Figure 33. 5-V/1-A Power Supply

System Examples (continued)

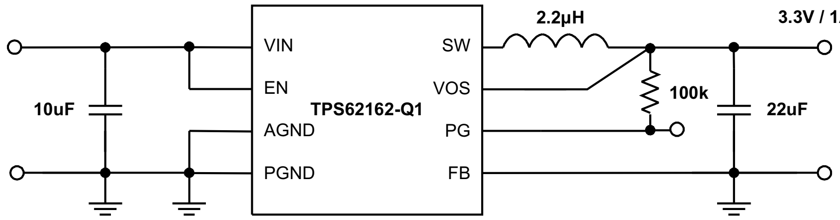


Figure 34. 3.3-V/1-A Power Supply

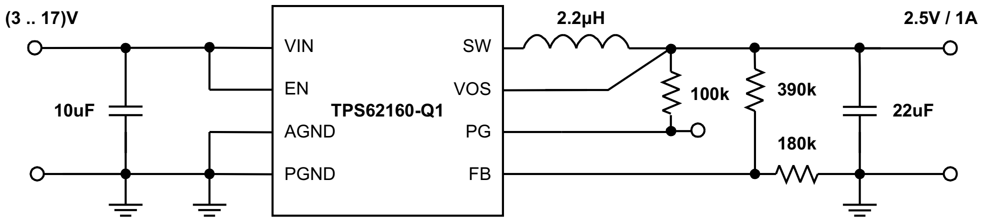


Figure 35. 2.5-V/1-A Power Supply

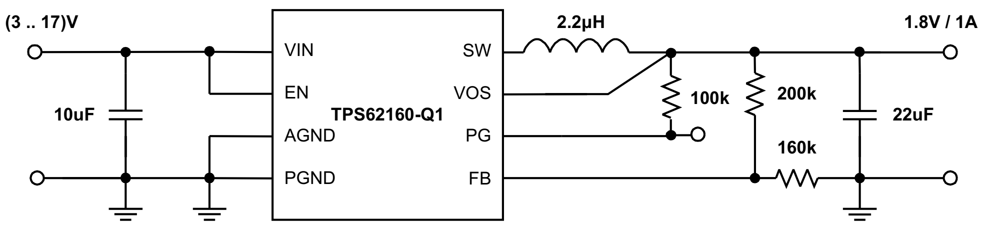


Figure 36. 1.8-V/1-A Power Supply

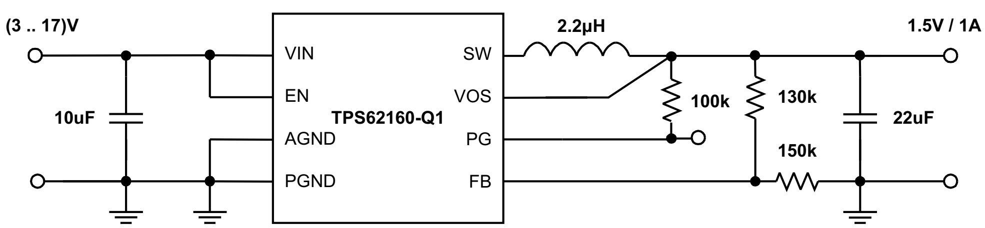


Figure 37. 1.5-V/1-A Power Supply

System Examples (continued)

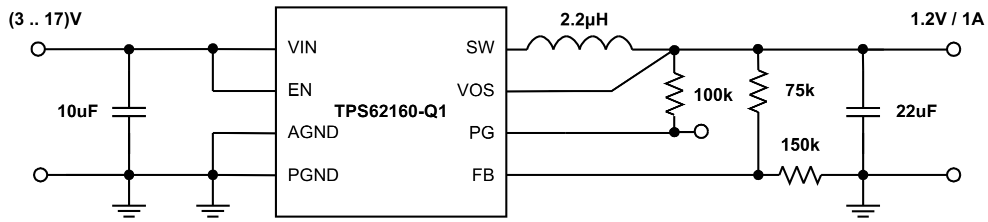


Figure 38. 1.2-V/1-A Power Supply

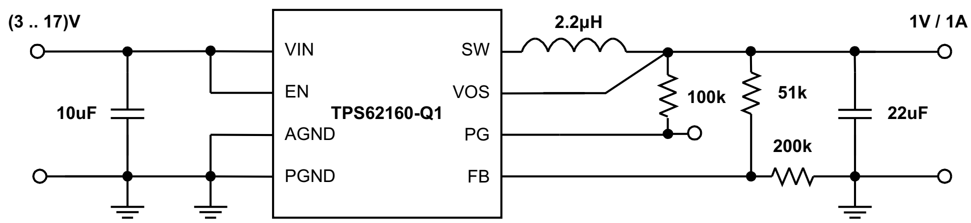


Figure 39. 1-V/1-A Power Supply

11 Power Supply Recommendations

The TPS6216x-Q1 are designed to operate from a 3-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6216x-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity. Considering the following topics ensures best electrical and optimized thermal performance:

1) The input capacitor must be placed as close as possible to the VIN and PGND pin of the IC. This provides low resistive and inductive path for the high di/dt input current.

2) The VOS pin must be connect in the shortest way to VOUT at the output capacitor - avoiding noise coupling.

3) The feedback resistors, R1 and R2 must be connected close to the FB and AGND pins - avoiding noise coupling.

4) The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces.

5) The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin.

More detailed information can be found in the *EVM Users Guide*, SLVU483.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the Exposed Thermal Pad can be connected to a floating circuit board trace, the device will have better thermal performance if it is connected to a larger ground plane. The Exposed Thermal Pad is electrically connected to AGND.

12.2 Layout Example

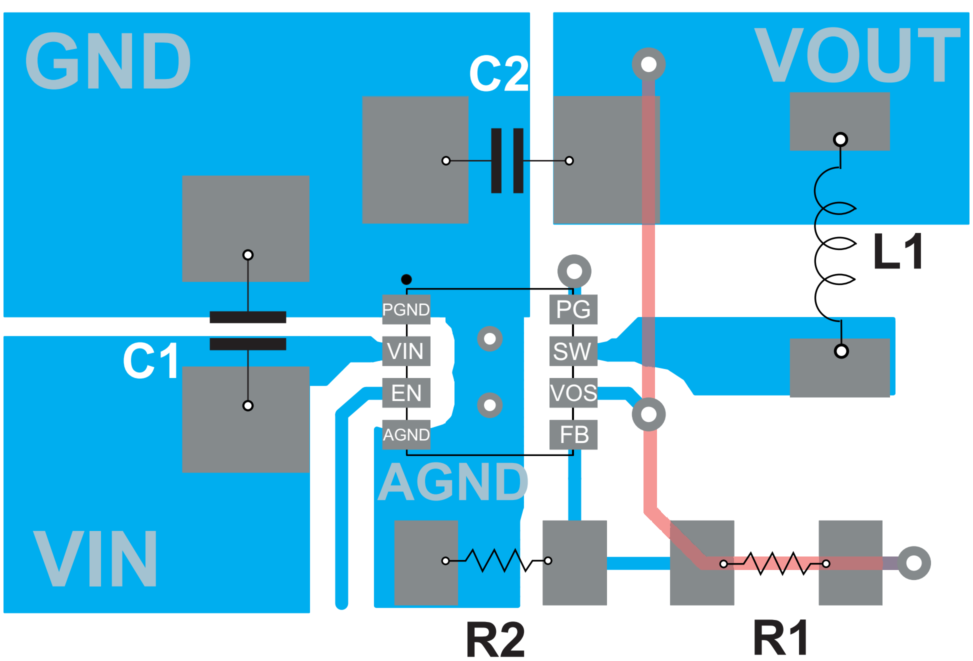


Figure 40. Layout Example

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics Application Note* (SZZA017), and (SPRA953).

The TPS6216x-Q1 are designed for a maximum operating junction temperature (T_J) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Since the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

Optimizing the TPS62130/40/50/60/70 Output Filter Application Report (SLVA463)

Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor Application Report (SLVA289)

Using a Feedforward Capacitor to Improve Stability and Bandwidth of TPS62130/40/50/60/70 Application Report (SLVA466)

TPS62160EVM-627 and TPS62170EVM-627 Evaluation Modules User's Guide (SLVU483)

Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report (SZZA017)

Semiconductor and IC Package Thermal Metrics Application Report (SPRA953)

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62160-Q1	Click here	Click here	Click here	Click here	Click here
TPS62162-Q1	Click here	Click here	Click here	Click here	Click here

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.6 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62160QDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTVQ	Samples
TPS62160QDSGTQ1	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTVQ	Samples
TPS62162QDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUCQ	Samples
TPS62162QDSGTQ1	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUCQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62160-Q1, TPS62162-Q1 :

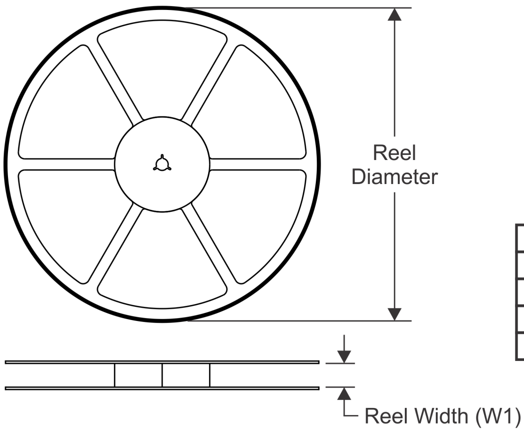
- Catalog: TPS62160, TPS62162

NOTE: Qualified Version Definitions:

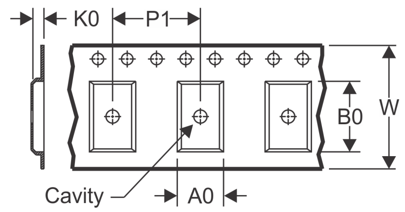
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

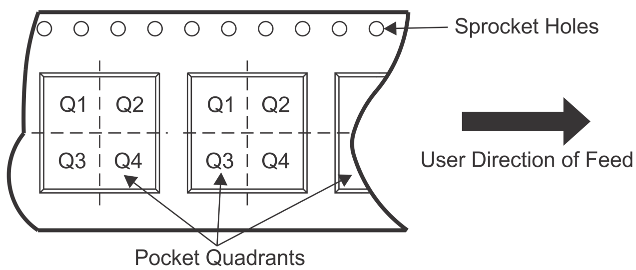


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

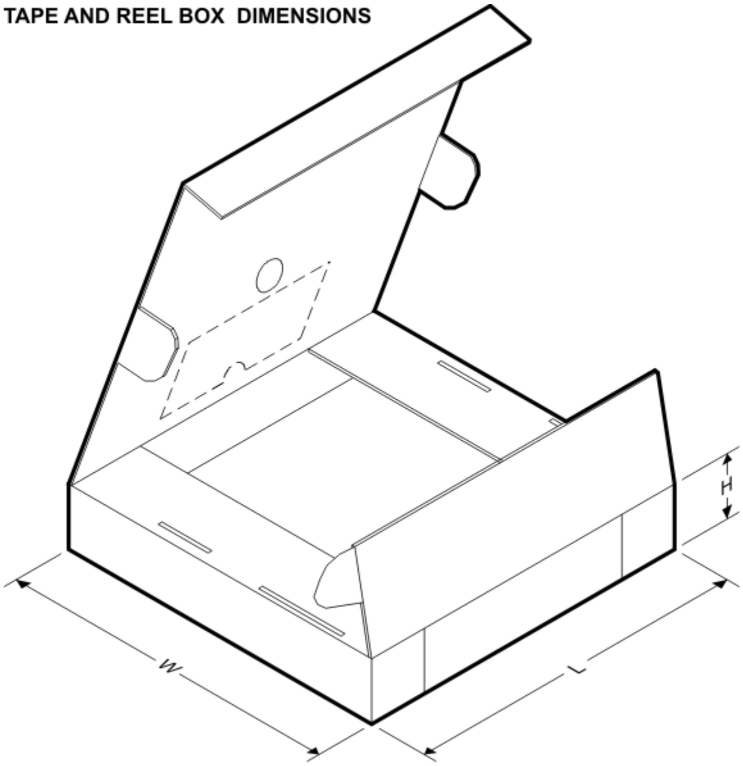
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62160QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62160QDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162QDSGTQ1	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62160QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62160QDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0
TPS62162QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62162QDSGTQ1	WSON	DSG	8	250	210.0	185.0	35.0

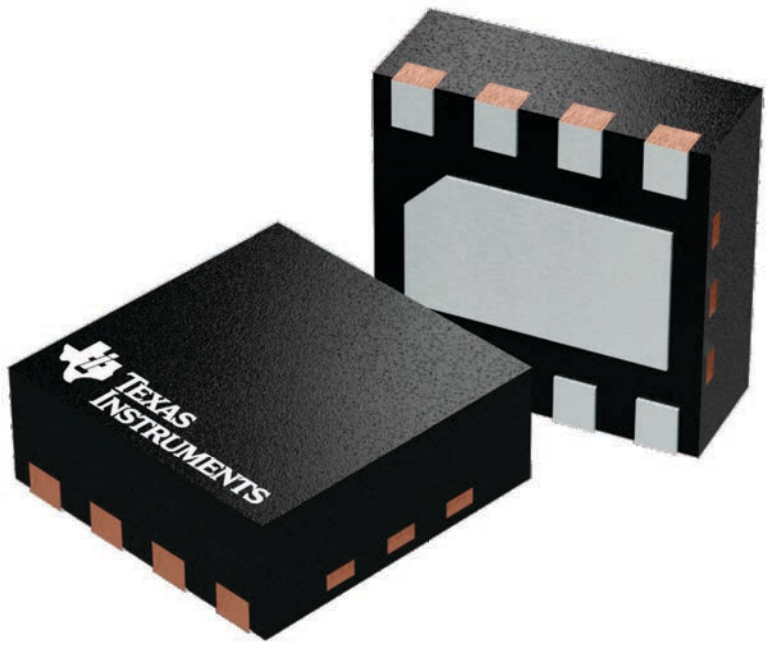
DSG 8

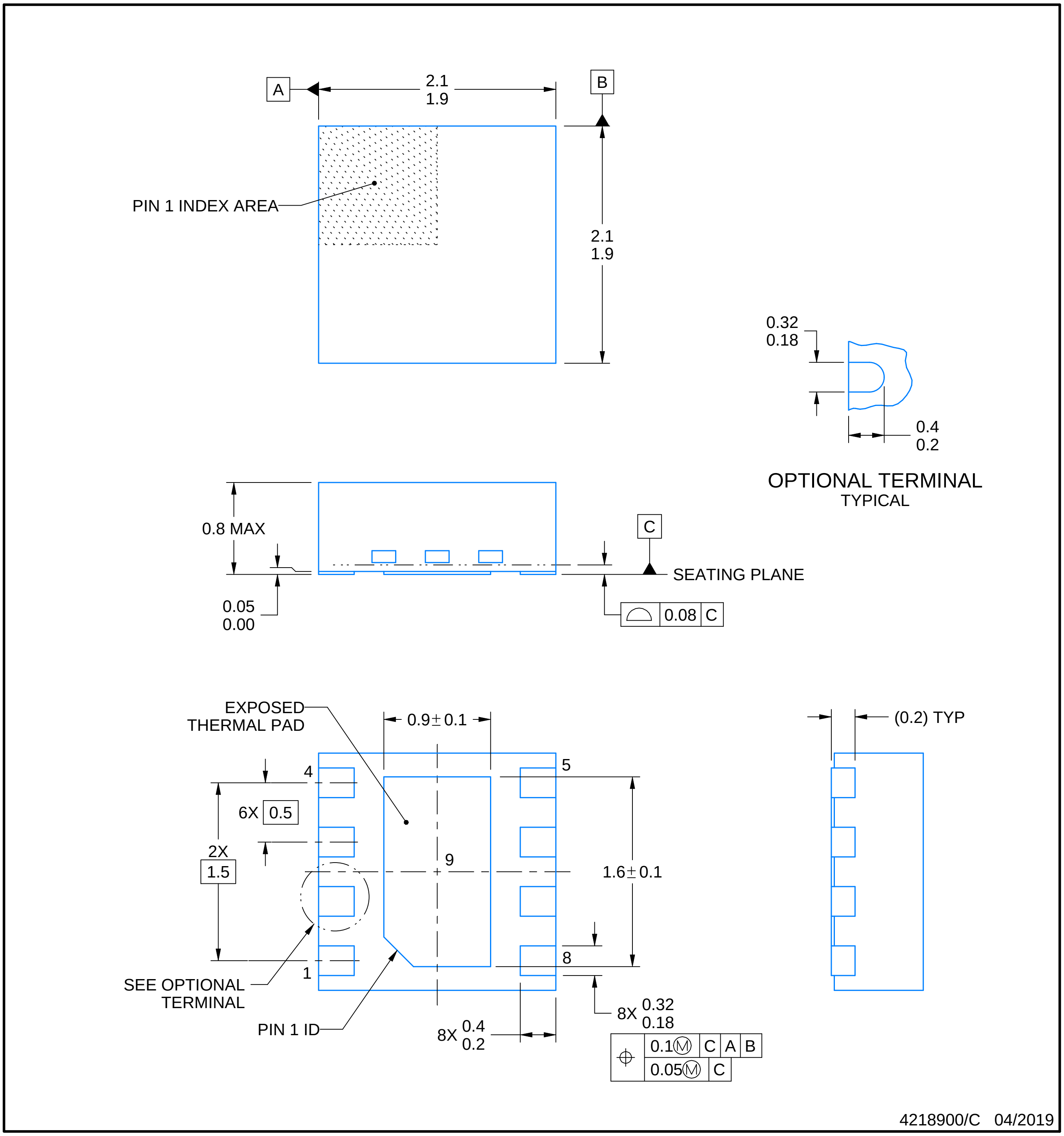
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

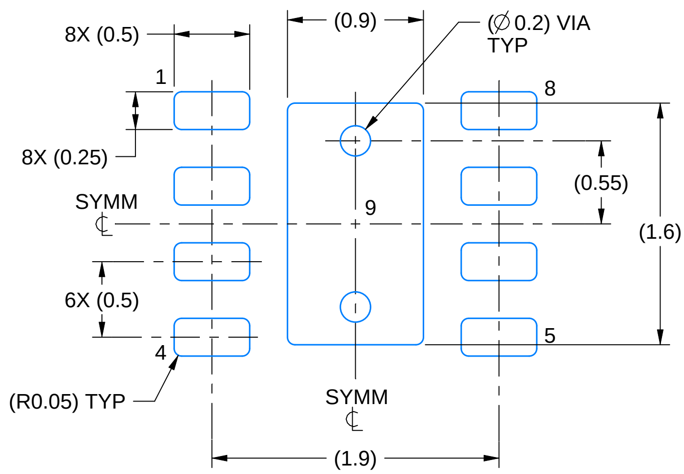
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



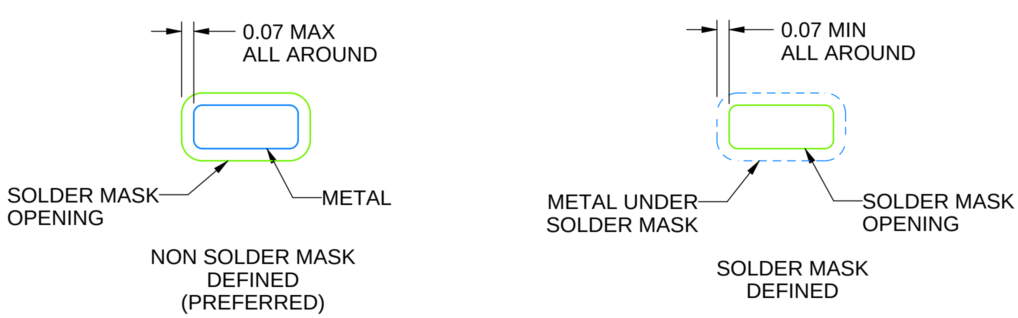


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

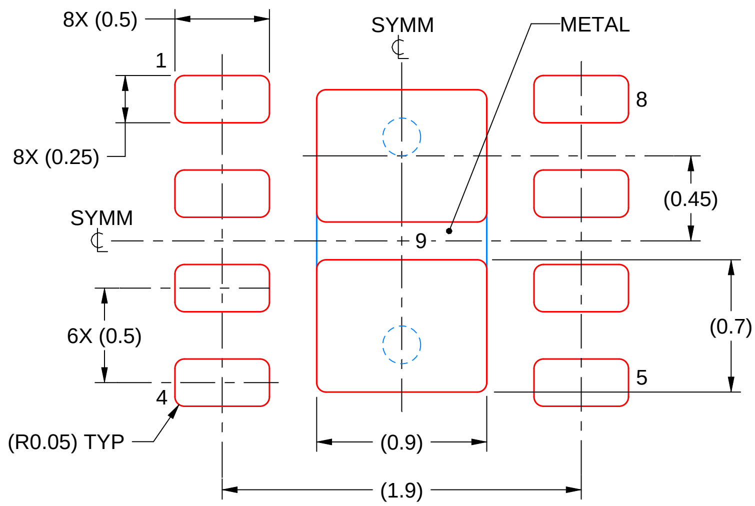


SOLDER MASK DETAILS

4218900/C 04/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/C 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.