TPS566250 4.5-V to 17-V Input, 6-A Synchronous Step-Down Converter With V_{ID} Control

1 Features

- Integrated FETs Optimized for Lower Duty Cycle Applications
  - 44 mΩ (High Side) and 23 mΩ (Low Side)
- Output Voltage Range: 0.6 V to 1.87 V with 5.5-mV Feedback Voltage Step
- V_{ID} Control with Multibyte Interface with Read-Back
- ±1% Output Voltage at 25°C for V_{ID} Control at 12 V V_{IN} / 1.1 V V_{OUT}
- D-CAP2™ Control Mode
- Advanced Eco-mode™ for High Efficiency at Light Load and Low Output Voltage Ripple
- 650-kHz Switching Frequency
- Fixed Soft Start: 1 ms
- Monotonic Pre-Biased Soft Start
- Hiccup Timer for Overload Protection

2 Applications

- Media Processors for Consumer Applications: Digital TVs, Set Top Boxes
- System On-Chip Power
- High Density Power Distribution Systems

3 Description

The TPS566250 is a synchronous buck converter that enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count and low standby current solution.

After the initial power-up, the output voltage can be changed by codes sent to the IC via an I^2C compatible V_{ID} Control bus.

The main control loops of the TPS566250 use the D-CAP2™ mode control which provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Advanced Eco-mode™ operation at light loads. Advanced Eco-mode™ allows the TPS566250 to maintain high efficiency during lighter load conditions. The TPS566250 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR, ceramic capacitors.

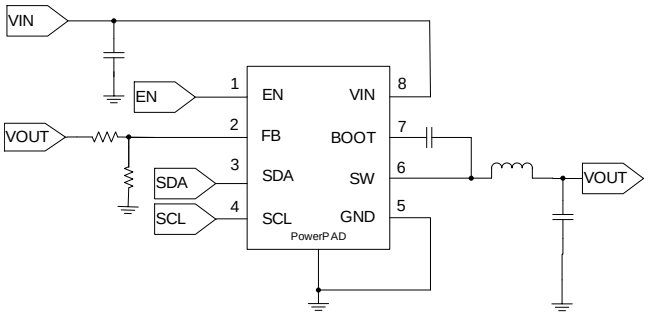
The device offers on chip overcurrent, undervoltage lockout and thermal shutdown protection.

Device Information(1)

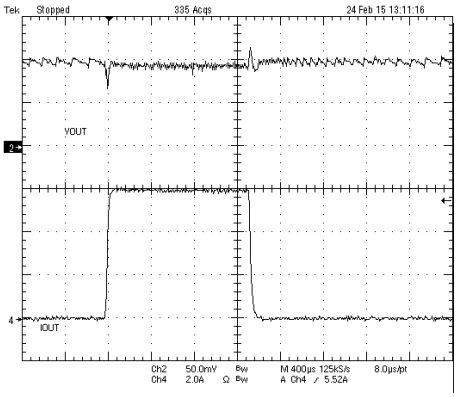
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS566250	HSOP (8)	4.90 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



Load Transient Response



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5 Revision History

Changes from Revision A (March 2015) to Revision B — **Page**

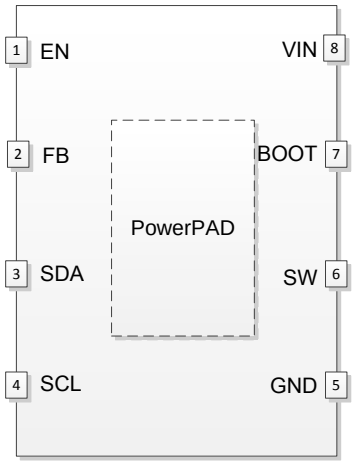
- Added Table 4 ... 16

Changes from Original (March 2015) to Revision A — **Page**

- Changed the $V_{(FB)}$ MIN value From: –2% to –1.6% in the *Electrical Characteristics* ... 5
- Added Test Condition: "T_A = 0°C to 85°C" to $V_{(FB)}$ in the *Electrical Characteristics* ... 5

6 Pin Configuration and Functions

TPS566250
8-Pin DDA
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	7	I/O	Supply input for high-side NFET gate drive circuit. Connect 0.1-µF ceramic capacitor between VBST and SW pins.
EN	1	I	Enable input control. Pull High to enable converter.
FB	2	I	Converter feedback input. Connect to output voltage with resistor divider.
GND	5	–	Power ground
SCL	4	I/O	Clock I/O terminal.
SDA	3	I/O	Data I/O terminal.
SW	6	I/O	Switch node connections for both the high-side NFET and low–side NFET.
VIN	8	I	Input voltage supply pin.
PowerPAD™	–	–	Thermal pad of the package. Must be soldered down to operate normally and achieve appropriate power dissipation. Connect sensitive FB returns to GND at a single point.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage range	VIN, EN	–0.3	19	V
	BOOT	–0.3	25	
	BOOT (10ns transient)	–0.3	27	
	BOOT (vs SW)	–0.3	6.5	
	FB, SDA, SCL	–0.3	3.6	
	SW	–2	19	
	SW (10ns transient)	–3.5	21	
Operating Junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.
(2) All voltages are with respect to IC GND terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
	Input voltage range	BOOT	–0.1	23	
		BOOT (10 ns transient)	–0.1	26	
		BOOT (vs SW)	–0.1	6	
		EN	–0.1	17	
		FB, SDA, SCL	–0.1	3.3	
		SW	–1.8	17	
		SW (10 ns transient)	–3.5	20	
T_J	Operating junction temperature range		–40	150	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS566250 DDA (8)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	55.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.9	
ψ_{JT}	Junction-to-top characterization parameter	9.5	
ψ_{JB}	Junction-to-board characterization parameter	24.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over operating junction temperature range, V_{IN} = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
I_{IN}	VIN supply current	T_A = 25°C, EN = 5 V, FB = 0.7 V (non switching)		450	525	µA
$I_{(VINSDN)}$	VIN shutdown current	T_A = 25°C, EN = 0 V		6.5	10	µA
LOGIC THRESHOLD						
$V_{(ENH)}$	EN H-level threshold voltage			1.1	1.6	V
$V_{(ENL)}$	EN L-level threshold voltage		0.6	0.94		V
	Hystersis			160		mV
$R_{(EN)}$	EN pin resistance to GND	$V_{(EN)}$ = 12 V	225	350	800	kΩ
FEEDBACK VOLTAGE						
$V_{(FB)}$	FB voltage	T_A = 0°C to 85°C V_{OUT} = 1.1 V, Upper/lower feedback resistors: 1.37 kΩ / 1.65 kΩ	–1.6%	0	1.6%	
		T_A = 25°C, V_{OUT} = 1.1 V, I_{OUT} = 10 mA, pulse skipping		0.606		V
		T_A = 25°C, V_{OUT} = 1.1 V, continuous current mode	0.594	0.6	0.606	V
MOSFET						
$r_{DS(on)H}$	High side switch resistance	BOOT - SW = 5.5 V		44	74	mΩ
$r_{DS(on)L}$	Low side switch resistance	V_{IN} = 12 V		23	35	mΩ
	Discharge FET			200		Ω
ON-TIME TIMER CONTROL						
f_{sw}	Switching frequency	L_{OUT} = 1.5 µH, C_{OUT} = 22 µF x 2, V_{OUT} = 1.1 V		650		kHz
CURRENT LIMIT						
I_{OCL}	Valley current limit	L_{OUT} = 1.5 µH, V_{OUT} = 1.1 V, V_{IN} = 12 V	7.6	9.5	11.4	A
	Reverse valley current limit	L_{OUT} = 1.5 µH, V_{OUT} = 1.1 V	1.5	4.5	7	A
OUTPUT UNDERVOLTAGE PROTECTION						
$V_{(UVP)}$	Output UVP trip threshold	UVP detect (H > L)		65%		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown Threshold	Shutdown temperature(1)		165		°C
		Hysteresis(1)		15		°C
UVLO						
UVLO	UVLO Threshold	V_{IN} rising voltage	3.26	3.75	4.05	V
		Hysteresis V_{IN} voltage	0.13	0.33	0.48	V
PGOOD VIA I^2C						
$V_{(PGOODTH)}$	PGOOD threshold	FB falling (fault) V_O = 1.1 V		80%		
		FB rising (good) V_O = 1.1 V		85%		
		FB rising (fault) V_O = 1.1 V		125%		
		FB falling (good) V_O = 1.1 V		120%		
SERIAL INTERFACE(1) (2) (3)						
V_{IL}	LOW level input voltage				0.6	V
V_{IH}	HIGH level input voltage		1.85			V
V_{hys}	Hysteresis of schmitt trigger inputs		0.11			V
V_{OL}	LOW level output voltage (Open drain, 3 mA sink current)				0.4	V
f_{SCL}	SCL clock frequency				400	kHz
Cb	Capacitive load for each bus line				400	pF

(1) Specified by design. Not production tested.
(2) Refer to Figure 1 for I^2C Timing Definitions
(3) Cb = capacitance of bus line in pF

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{on}	SW On time	V_{IN} = 12 V, V_{OUT} = 1.1 V		165		ns
t_{off}	SW Minimum off time	T_A = 25 °C, FB = 0.5 V		275	325	ns
SOFT START						
t_{SS}	Soft start time	Internal soft start time	0.7	1	1.3	ms
OUTPUT UNDERVOLTAGE PROTECTION						
$t_{(UVPDEL)}$	Hiccup delay time (power into short)			1.3		ms
$t_{(UVPEN)}$	Hiccup off time before restart			10		ms
SERIAL INTERFACE(1) (2) (3)						
$t_{(SP)}$	Pulse width of spikes suppressed by input filter		32			ns
$t_{(HD;STA)}$	Hold time (repeated) START condition.		0.6			µs
t_{LOW}	LOW period of SCL clock		1.3			µs
t_{HIGH}	HIGH period of SCL clock		0.6			µs
$t_{(SU;STA)}$	Set-up time for a repeated START condition		0.6			µs
$t_{(HD;DAT)}$	Data Hold time		50		900	ns
$t_{(SU;DAT)}$	Data set-up time		100			ns
t_r	Rise time (SDA or SCL)		20+0.1Cb(3)		300	ns
t_f	Fall time (SDA or SCL)		20+0.1Cb(3)		300	ns
$t_{(SU;STO)}$	Set-up time for STOP condition		0.6			µs
$t_{(BUF)}$	Bus free time between STOP and START condition		1.3			µs

(1) Specified by design. Not production tested.
(2) Refer to Figure 1 below for I²C Timing Definitions
(3) Cb = capacitance of bus line in pF

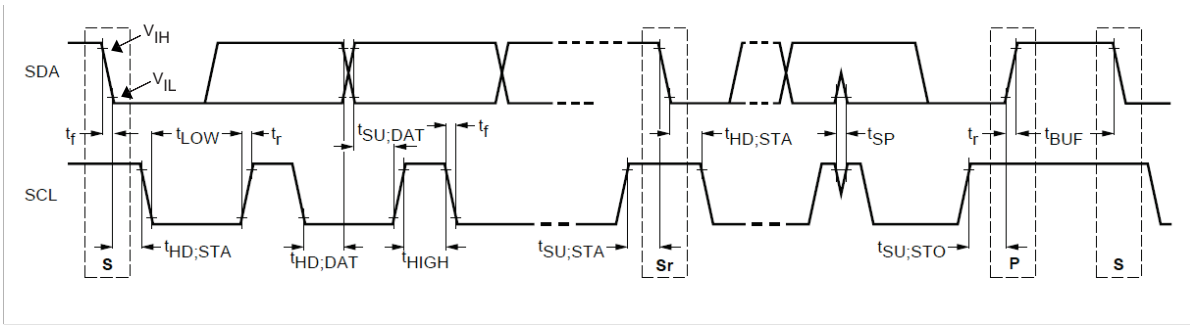


Figure 1. I²C Timing Definitions (reproduced from Phillips I²C spec Version 1.1)

7.7 Typical Characteristics

V_{IN} = 12 V, T_A = 25 °C, unless otherwise specified.

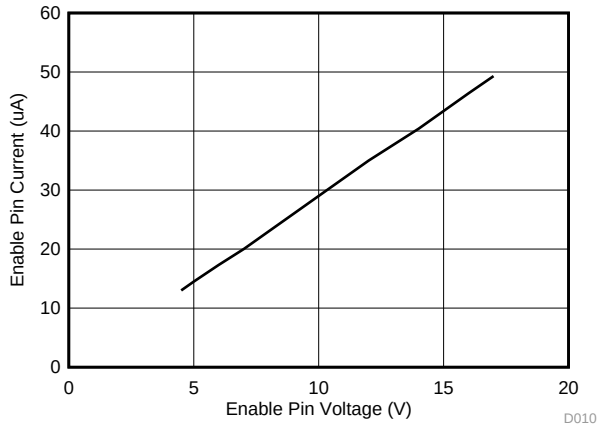


Figure 2. Enable Current vs Enable Voltage

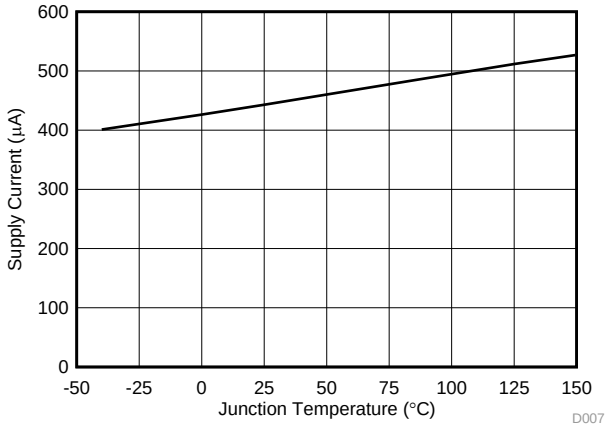


Figure 3. Supply Current vs Junction Temperature

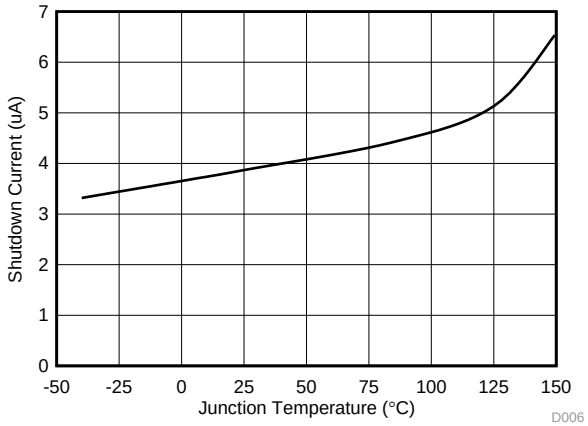


Figure 4. Shutdown Current vs Junction Temperature

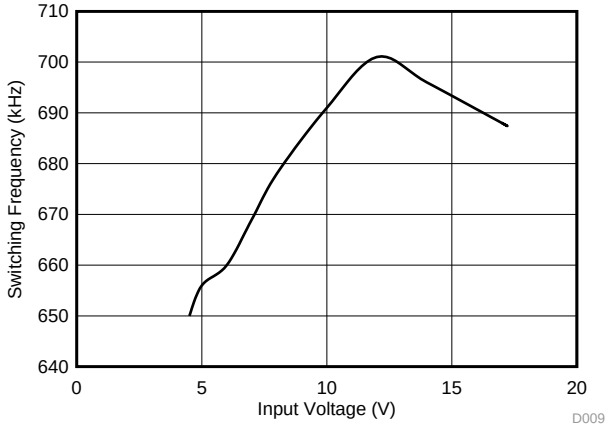


Figure 5. Switching Frequency vs Input Voltage

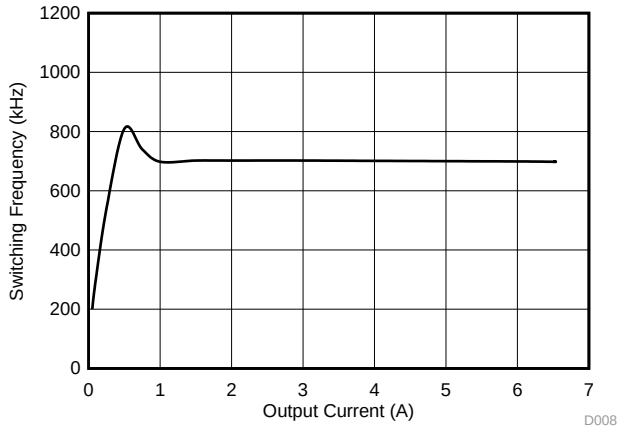


Figure 6. Switching Frequency vs Output Current

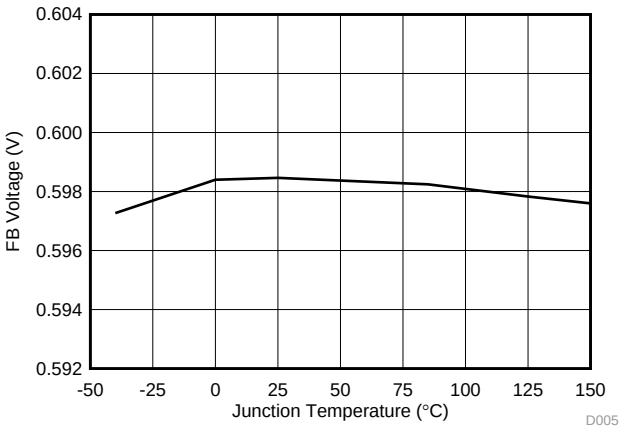


Figure 7. Feedback Voltage vs Junction Temperature

Typical Characteristics (continued)

V_{IN} = 12 V, T_A = 25 °C, unless otherwise specified.

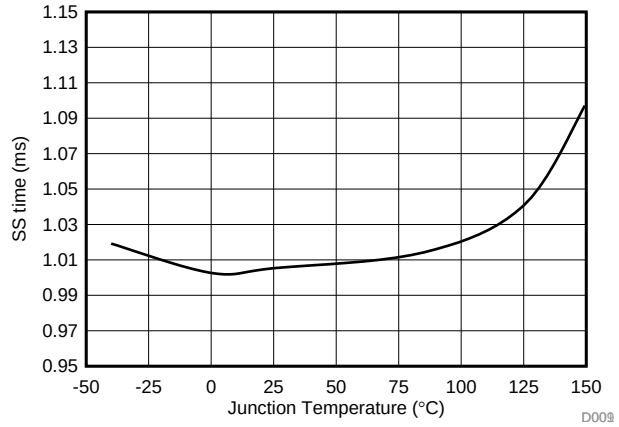


Figure 8. Soft Start Time vs Junction Temperature

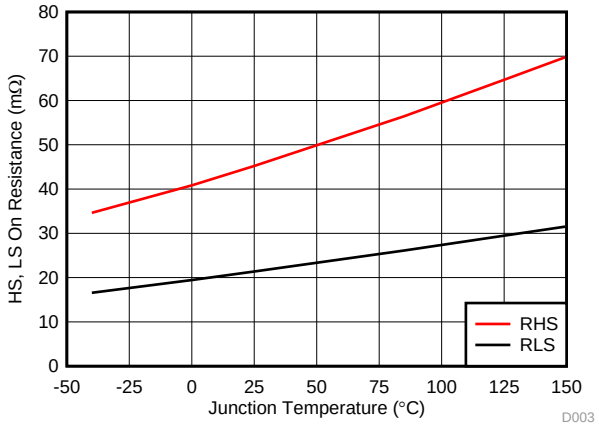


Figure 9. HS and LS $r_{DS(on)}$ vs Junction Temperature

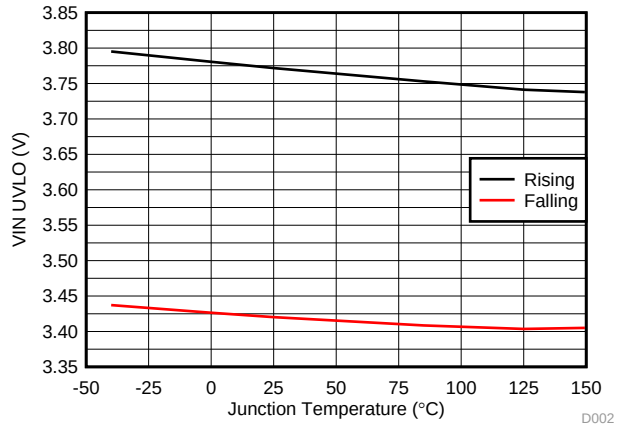


Figure 10. Input Voltage UVLO vs Junction Temperature

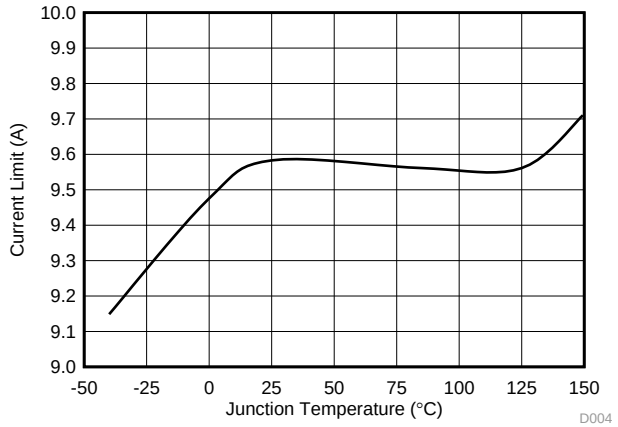


Figure 11. Current Limit vs Junction Temperature

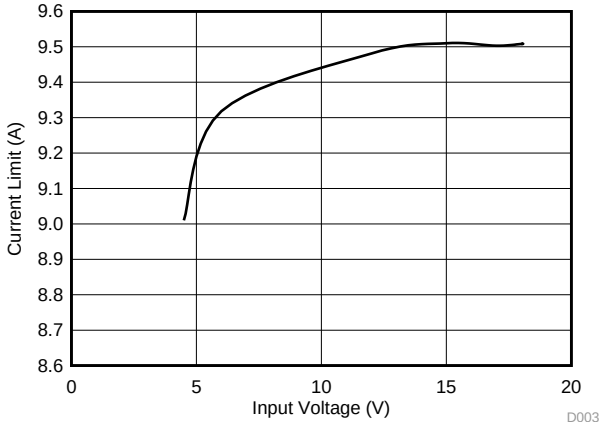


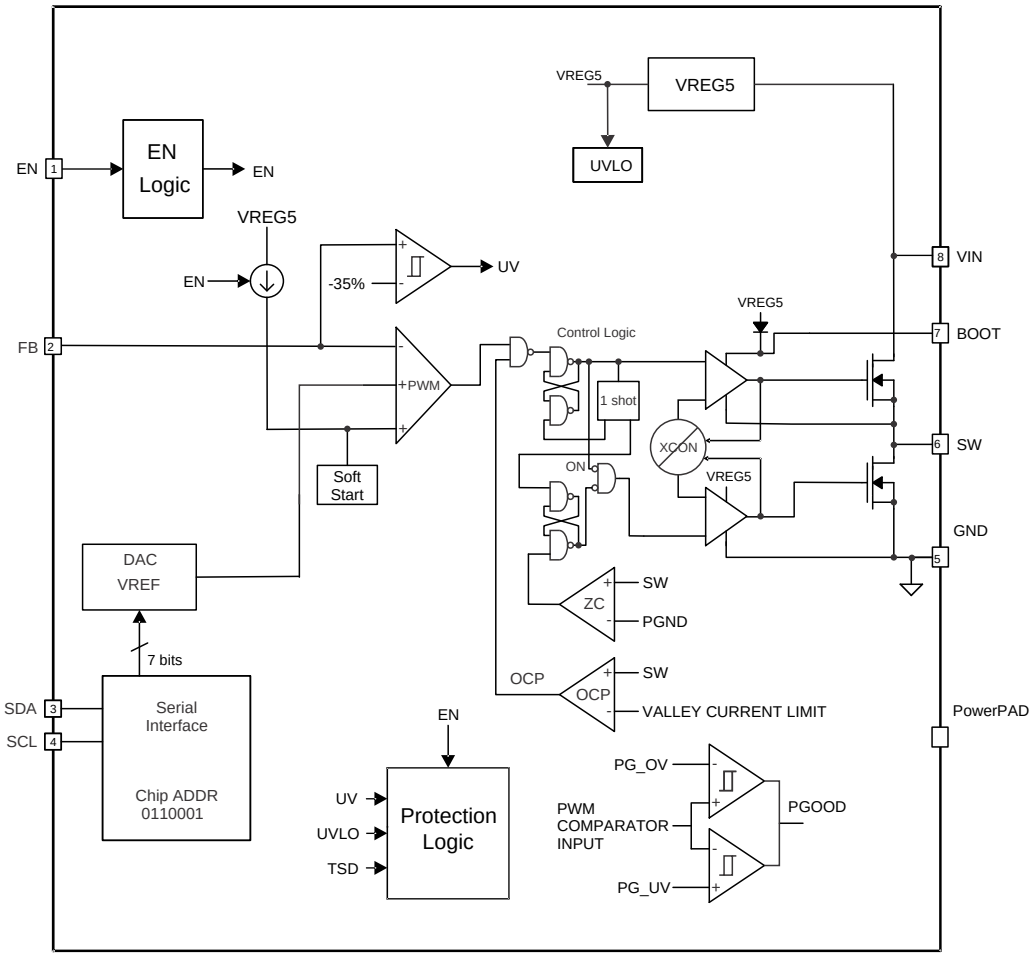
Figure 12. Current Limit vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS566250 is a synchronous step-down (buck) converter with two integrated N-channel MOSFETs for each channel. It operates using D-CAP2™ control mode. The fast transient response of D-CAP2™ control reduces the required output capacitance required to meet a specific level of performance. The output voltage of the device can be set by either FB with divider resistors and I^2C compatible interface.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Operation

The main control loop of the TPS566250 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off when the internal timer expires. This timer is set by the converter's input voltage, V_{IN}, and the output voltage, V_{OUT}, to maintain a pseudo-fixed frequency over the input voltage range hence it is called adaptive on-time control. The timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the nominal output voltage. An internal ramp is added to the reference voltage to simulate output voltage ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

Feature Description (continued)

8.3.2 PWM Frequency and Adaptive On-Time Control

TPS566250 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The device runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is V_{OUT}/V_{IN}, the switching frequency is constant.

8.3.3 Soft Start and Pre-Biased Soft Start

The TPS566250 has an internal 1 ms soft-start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator. The device contains a unique circuit to prevent sinking current from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage FB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from output pre-biased startup to normal mode operation.

8.3.4 Overcurrent Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. The device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the overcurrent condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for valley overcurrent protection. The average load current is half the peak-to-peak inductor current plus the valley overcurrent threshold during current limit. The output voltage falls as the demanded load current exceeds the current limit. When the FB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it and the Hiccup sequence is initiated. After 10 µs detecting the UVP voltage, device shuts down and re-starts after the hiccup time.

When the over current condition is removed, the output voltage returns to the regulated value.

8.3.5 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the VIN terminal. When the VIN voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

8.3.6 Thermal Shutdown

TPS566250 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

8.4 Device Functional Modes

8.4.1 Auto-Skip Eco-mode™ Control

The TPS566250 is designed with Advanced Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the where its ripple valley touches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is lowered to reduce the output voltage ripple. The transition point to the light load operation $I_{O(LL)}$ current can be estimated with Equation 1 with 650 kHz used as f_{SW}.

$$I_{O(LL)} = \frac{1}{2 \times L_O \times f_{SW}} \times \frac{(VIN - V_O) \times V_O}{VIN} + 0.5\ A \quad (1)$$

8.5 Programming

8.5.1 I²C Interface

The TPS566250 implements a subset of the Phillips I²C specification Ver. 1.1. The TPS566250 is a Slave-Only (it never becomes a Master, and so never pulls down the **SCL** pin on the I²C bus). An I²C transaction consists of either writing a data byte to one of the device internal registers which requires a 3-byte transaction or reading back one byte from a register which requires a 4-byte transaction. The protocols follow the System Management Bus (SMBUS) Specification Ver. 2.0 *Write Byte and Read Byte* protocols. This spec is available on the Internet for further reading, but the subset implemented in TPS566250 is described as:

- Long-form address modes, multi-byte data transfers and Packet Error Code (PEC) protocols are not supported in this implementation, though a unique to the TPS566250.
- The I²C interface pins are composed of the **SDA** (Data) and **SCL** (Clock) pins. **SDA** and **SCL** are designed to be used with pullup resistors to 3.3 V.

8.5.2 I²C Protocol

8.5.2.1 Input Voltage

Logic levels for I²C **SDA** and **SCL** pins are not fixed. For the TPS566250, a logic “0” (LOW) should be 0 V and a logic “1” (HIGH) can be any voltage between 2.5 V and 3.3 V. Logic HIGH is generated by external pullup resistors (see Output Voltage).

8.5.2.2 Output Voltage

the I²C bus has external pullup resistors, one for SCL and one for SDA. These pull up to a voltage called V_{DD} which must lie between 2.5 V and 3.3 V. The outputs are pulled down to their logic LOW levels by open-drain outputs and pulled up to their logic HIGH levels by these external pullups. The pullups must be selected so that the current into any chip when pulled LOW by that chip’s open drain output (=VDD/RPULLUP) is less than 3 mA.

8.5.2.3 Data Format

One clock pulse on the **SCL** clock line is generated for each bit of data to be transferred. The data on the **SDA** line must be stable during the HIGH period of the **SCL** clock line. The HIGH or LOW state of the data line can only change when the clock signal on the **SCL** line is LOW.

8.5.2.4 START and STOP Conditions

A HIGH to LOW transition on the **SDA** line while the **SCL** line is HIGH defines a START condition. A LOW to HIGH transition on the **SDA** line while the **SCL** line is HIGH defines a STOP condition. START and STOP conditions are always generated by the Master. The bus is considered to be BUSY after the condition. It is considered to be free again after a minimum of 4.7 µS after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. START and repeated START are functionally identical.

Programming (continued)

Every byte of data out on the **SDA** line is 8 bits long. 9 clocks occur for each byte (the additional clock being for an ACK signal put onto the bus by the device pulling down on the bus to acknowledge receipt of the data). In the Figure 13 and Figure 14, shaded blocks indicate **SDA** data generated by the device being sent to the Master I^2C controller, while white blocks indicate **SDA** data generated by the Master being received by the device. The Master always generates the **SCL** signal.

Sending data to the TPS566250 is accomplished using the following 3-byte sequence, referred to as a *Write Byte* transaction:

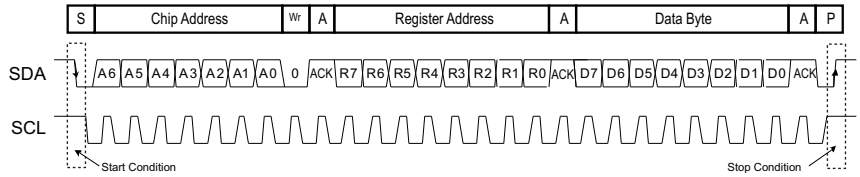


Figure 13. A Complete Write Byte Transfer, Adapted From SMBUS Spec

Reading back data from the TPS566250 is accomplished using the following 4-byte sequence, referred to as a *Read Byte* transaction:

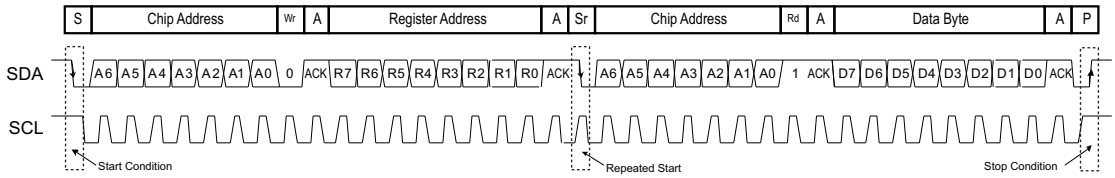


Figure 14. A Complete Read Byte Transfer, Adapted From SMBUS Spec

On the TPS566250, the I^2C bus is inactive until:

1. Both SDA and SCL have been at a logic high simultaneously to prevent power sequencing issues.
2. VOUT is in regulation.

Control registers can be written after soft start is complete (1.7 times soft start time).

Until a VOUT command has been accepted, the device output voltage is determined by the external resistor divider feedback to the **FB** pin, the initial FB voltage (typically 0.6 V), and the condition of the **EN** pin.

When the device receives a Chip Address code it recognizes to be its own, it responds by sending an ACK (pulling down on the **SDA** bus during the next clock on the **SCL** bus). If the address is not recognized, the device assumes that the I^2C message is intended for another chip on the bus, and it takes no action. It disregards data sent thereafter until the next START is begun.

If, after recognizing its Chip Address, the TPS566250 receives a valid Register Address, it sends an ACK and prepare to receive a Data Byte to be sent to that Register.

If a valid Data Byte is then received, it sends an ACK and sets the output voltage to the desired value. It is recommended to readback to verify the output voltage code. When sending data to the Output Voltage register, the output voltage only changes upon receipt of a valid data byte.

8.5.3 I^2C Chip Address Byte

The 7-bit address of the TPS566250 is set at **31h** in hex notation (**0110001** in binary notation) internally. When the Master is sending the address as an 8-bit value, the 7-bit address should be sent followed by a trailing 0 to indicate this is a WRITE operation.

8.6 Register Maps

8.6.1 I²C Register Address Byte

The TPS566250 contains 2 customer-accessible registers. Register 0d (0h) is the output voltage register. Register 24d (18h) is the power good register

8.6.1.1 Output Voltage Register (offset = 00000000) [reset = 0h]

Register 0d (0h) is the Output Voltage resister.

Figure 15. Output Voltage Register

7	6	5	4	3	2	1	0
Odd Parity	VOUT						
R/W	R/W						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 1. Output Voltage Register

Bit	Field	Type	Reset	Description
7	Odd Parity	R/W	0h	See *CheckSum Bit*
6:0	VOUT	R/W	0h	See Table 3

8.6.1.2 Power Good State Register (offset = 00011000) [reset = 18h]

Register 24d (18h) provides the power good state

Figure 16. Power Good State Register

7	6	5	4	3	2	1	0
TI only							PGOOD
R							R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 2. Power Good Register

Bit	Field	Type	Reset	Description
7:1	TI only	R	0h	TI only
0	PGOOD	R	18h	1 = FB voltage within PGOOD threshold limits 0 = FB Voltage outside PGOOD threshold limits

8.6.2 CheckSum Bit

The CheckSum bit should be set by the Master controller to be the exclusive-OR of the D[6:0] bits (odd parity). This is used by the TPS566250 to check that a valid data byte was received. If CheckSum is not equal to the exclusive-OR of these bits, the TPS566250 assumes that an error occurred during the data transmission, nor does not reset the V_{OUT} to the received code (or, if the Control register does not reset the register contents as requested). The Master should try again to send the data.

8.6.3 Output Voltage Registers

The lower 7 bits of the Output Voltage Register controls the V_{OUT} of the device. These bits are the 7-bit selector for one of the output voltages. The default output voltage is 1.1 V, that is 50d (32h)

When the IC powers up, the startup and output voltage regulation conditions are set by the external resistor divider feedback to the **FB** pin, the initial FB voltage and the condition of the **EN** pin. Bringing the **EN** pin high begins a soft-start ramp on the regulator.

After applying V_{IN}, V_{OUT} comes into regulation and the I^2C interface actives.

By default, the device regulates V_{OUT} using the external feedback resistors connected to the **FB** pin and the initial FB voltage. The user can then program V_{OUT} by writing any V_{OUT} code.

Table 3. Ideal V_{OUT} vs VOUT [6:0] Code (Upper/lower Feedback Resistors: 1.37 kΩ / 1.65 kΩ (1) (2)

Code	Binary	V_{OUT}	Code	Binary	VOUT	Code	Binary	VOUT	Code	Binary	VOUT
0	0000000	0.60	32	0100000	0.92	64	1000000	1.24	96	1100000	1.56
1	0000001	0.61	33	0100001	0.93	65	1000001	1.25	97	1100001	1.57
2	0000010	0.62	34	0100010	0.94	66	1000010	1.26	98	1100010	1.58
3	0000011	0.63	35	0100011	0.95	67	1000011	1.27	99	1100011	1.59
4	0000100	0.64	36	0100100	0.96	68	1000100	1.28	100	1100100	1.60
5	0000101	0.65	37	0100101	0.97	69	1000101	1.29	101	1100101	1.61
6	0000110	0.66	38	0100110	0.98	70	1000110	1.30	102	1100110	1.62
7	0000111	0.67	39	0100111	0.99	71	1000111	1.31	103	1100111	1.63
8	0001000	0.68	40	0101000	1.00	72	1001000	1.32	104	1101000	1.64
9	0001001	0.69	41	0101001	1.01	73	1001001	1.33	105	1101001	1.65
10	0001010	0.70	42	0101010	1.02	74	1001010	1.34	106	1101010	1.66
11	0001011	0.71	43	0101011	1.03	75	1001011	1.35	107	1101011	1.67
12	0001100	0.72	44	0101100	1.04	76	1001100	1.36	108	1101100	1.68
13	0001101	0.73	45	0101101	1.05	77	1001101	1.37	109	1101101	1.69
14	0001110	0.74	46	0101110	1.06	78	1001110	1.38	110	1101110	1.70
15	0001111	0.75	47	0101111	1.07	79	1001111	1.39	111	1101111	1.71
16	0010000	0.76	48	0110000	1.08	80	1010000	1.40	112	1110000	1.72
17	0010001	0.77	49	0110001	1.09	81	1010001	1.41	113	1110001	1.73
18	0010010	0.78	50	0110010	1.10	82	1010010	1.42	114	1110010	1.74
19	0010011	0.79	51	0110011	1.11	83	1010011	1.43	115	1110011	1.75
20	0010100	0.80	52	0110100	1.12	84	1010100	1.44	116	1110100	1.76
21	0010101	0.81	53	0110101	1.13	85	1010101	1.45	117	1110101	1.77
22	0010110	0.82	54	0110110	1.14	86	1010110	1.46	118	1110110	1.78
23	0010111	0.83	55	0110111	1.15	87	1010111	1.47	119	1110111	1.79
24	0011000	0.84	56	0111000	1.16	88	1011000	1.48	120	1111000	1.80
25	0011001	0.85	57	0111001	1.17	89	1011001	1.49	121	1111001	1.81
26	0011010	0.86	58	0111010	1.18	90	1011010	1.50	122	1111010	1.82
27	0011011	0.87	59	0111011	1.19	91	1011011	1.51	123	1111011	1.83
28	0011100	0.88	60	0111100	1.20	92	1011100	1.52	124	1111100	1.84
29	0011101	0.89	61	0111101	1.21	93	1011101	1.53	125	1111101	1.85
30	0011110	0.90	62	0111110	1.22	94	1011110	1.54	126	1111110	1.86
31	0011111	0.91	63	0111111	1.23	95	1011111	1.55	127	1111111	1.87

(1) 10-mV output voltage steps can be applied to 1.1-V output voltage setting only.
(2) For other default voltage setting, the output voltage step are shown in Equation 2.

$$\text{Output Voltage Step} = 10 \times \text{Target Output Voltage}/1.1\ \text{mV} \quad (2)$$

8.6.4 Summary of Default Control Bits

8.6.4.1 DAC Settle

When a new V_{OUT} voltage is selected, this happens by setting an internal DAC to a new internal V_{REF} voltage. If this happens instantly, the regulator loop is thrown out of regulation and the DCAP2 loop must respond to bring the V_{OUT} back into regulation at its new chosen value. To reduce V_{OUT} overshoots (or undershoots) or high transient input currents due to the internal V_{REF} change, There is an analog filter on the DAC output. The filter is set at 20 µs constant.

8.6.4.2 Operation During V_{ID} Transition

The device temporarily goes into forced CCM mode during V_{ID} transitions for approximately 100 µs. This helps discharge V_{OUT} during a step down when there is a light load present. The Power Good is masked for approximately 100 µs to prevent a power good flag during the transition.

CONTROL BIT(S)	DEFAULT	FUNCTION
VOUT[7:0]	0110010 (32h)	V_{OUT} code, 7 bits VOUT[6:0] + odd parity checksum bit at VOUT[7]. Writing a valid code to this register also sets VID Mode. Sending an invalid code (checksum incorrect) to this register does not change register contents or set Internal/Enable bits.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are synchronous step down DC-DC converters rated at different output currents whose output voltage can be dynamically scaled by sending commands over an I^2C interface. This section discusses the design of the external components to complete the power supply design by using a typical application as a reference.

9.2 Typical Application

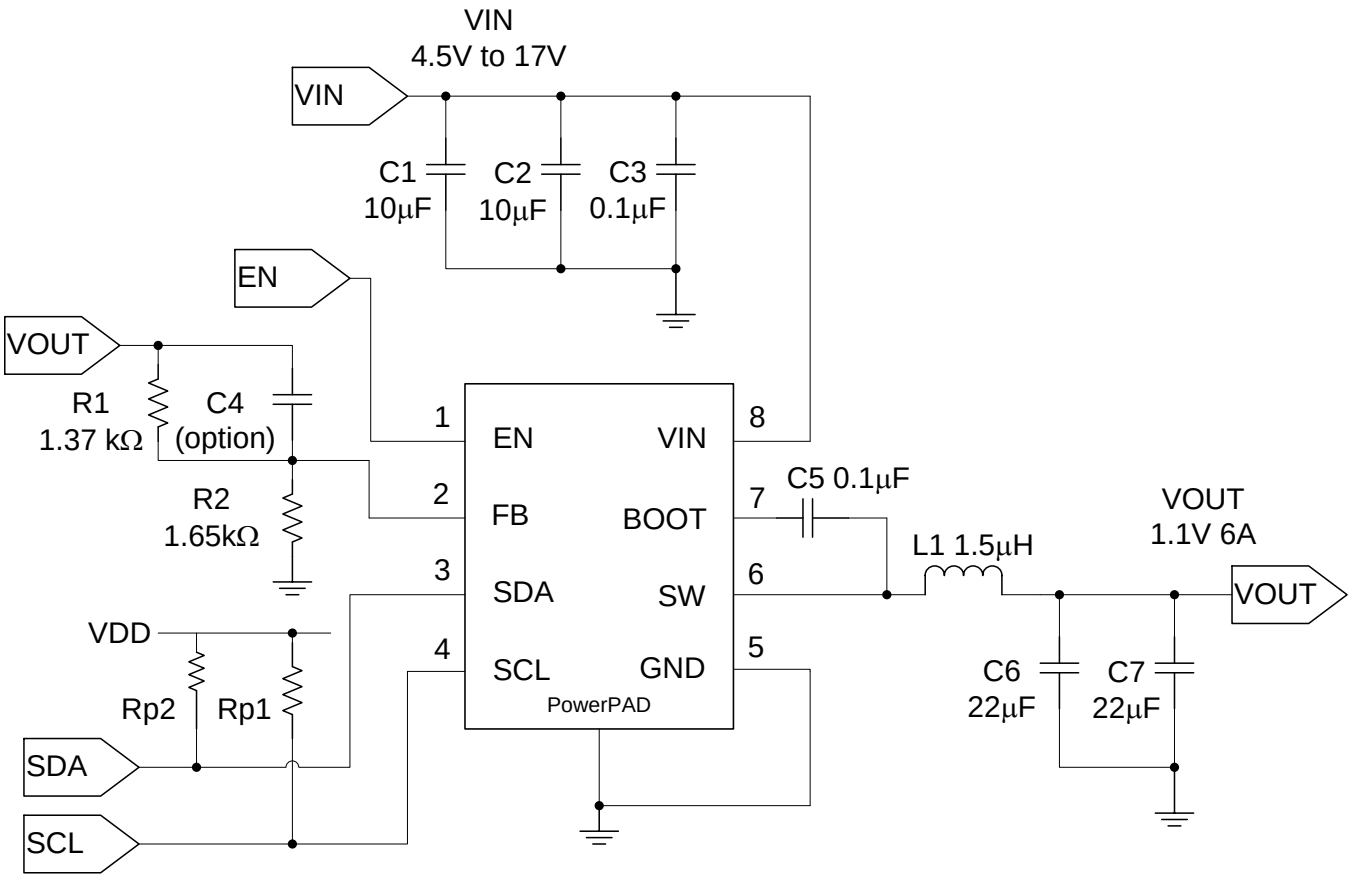


Figure 17. Typical Application Schematic

Table 4. Components

REFERENCE DESIGNATOR	PART NUMBER	MANUFACTURER
L1	744 314 150	Wurth Electronics
C6 , C7	C1210C226K9RACTU	Kemet

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 5.

Table 5. Design Example

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V
Output voltage	1.1 V
Transient response, 0 A – 6 A load step	ΔV_{OUT} = ±5%
Output voltage ripple	25 mV
Input ripple voltage	400 mV
Output current rating	6 A
Operating Frequency	650 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. Use 1.37 kΩ for R1 and 1.65 kΩ for R2.

$$V_{(FB)} = V_O \times \frac{R2}{R1 + R2} \quad (3)$$

9.2.2.2 Output Filter Selection

The output filter used with the TPS566250 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi \sqrt{L_O \times C_O}} \quad (4)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 6.

Table 6. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)			L1 (µH)			C67 (µF)
			MIN	TYP	MAX	MIN	TYP	MAX	
1	1.37	1.65					1.5		22 - 68
1.1 (Default)	1.37	1.65					1.5		22 - 68
1.2	1.37	1.65					1.5		22 - 68
1.5	1.37	1.65					1.5		22 - 68
1.8	1.37	1.65					1.5		22 - 68

(1) Optional

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6 and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. For the calculations, use 500 kHz as the switching frequency, f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$\Delta I_{LO} = \frac{V_O}{VIN_{(MAX)}} \times \frac{VIN_{(MAX)} - V_O}{L_O \times f_{SW}} \quad (5)$$

$$I_{LPEAK} = I_O + \frac{\Delta I_L}{2} \quad (6)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12}\Delta I_L^2} \quad (7)$$

The capacitor value and ESR determines the amount of output voltage ripple. The TPS566250 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 µF to 68 µF.

9.2.2.3 Input Capacitor Selection

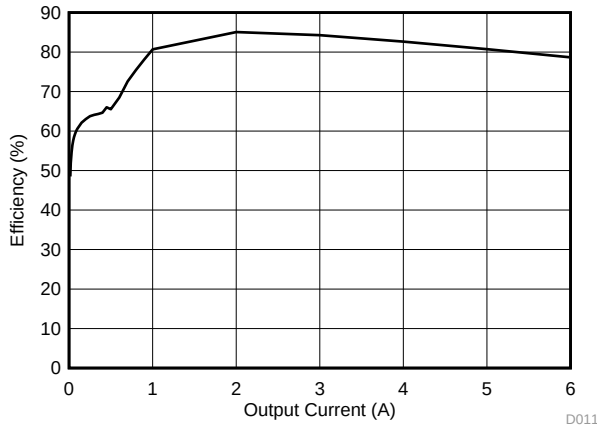
The TPS566250 requires an input decoupling capacitor and a bulk capacitor depending on the application. A ceramic capacitor of 10 µF or above is recommended for the decoupling capacitor. Additionally, a 0.1-µF ceramic capacitor from V_{IN} to GND is also recommended to improve the stability and reduce the SW node overshoots. The capacitors voltage rating needs to be greater than the maximum input voltage.

9.2.2.4 Bootstrap Capacitor Selection

The 0.1-µF ceramic capacitors must be connected between the BOOT to SW pins for proper operation. It is recommended to use ceramic capacitors with a dielectric of X5R or better.

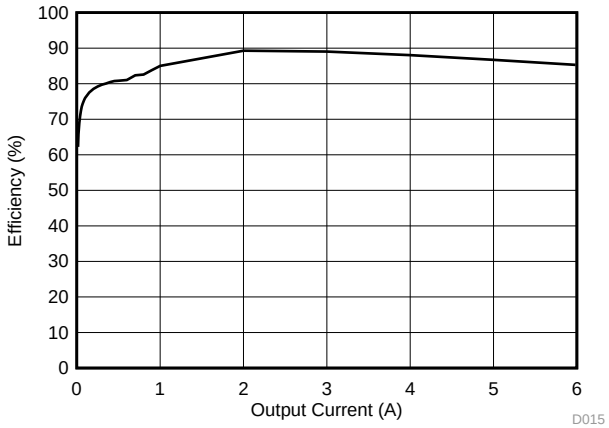
9.2.3 Application Performance Curves

V_{IN} = 12 V, V_{OUT} = 1.1 V, T_A = 25°C, unless otherwise specified.



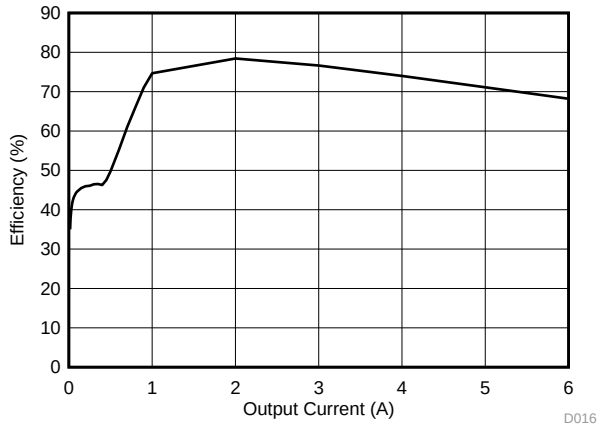
V_{IN} = 12 V

Figure 18. Efficiency vs Output Current



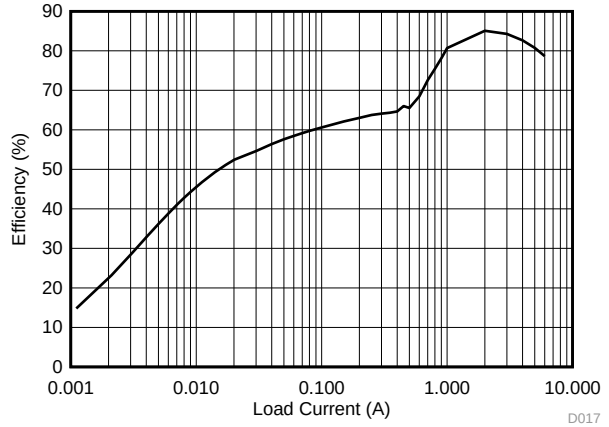
V_{OUT} = 1.87 V

Figure 19. Efficiency vs Output Current



V_{OUT} = 0.6 V

Figure 20. Efficiency vs Output Current



V_{OUT} = 1.1 V

Figure 21. Efficiency vs Load Current

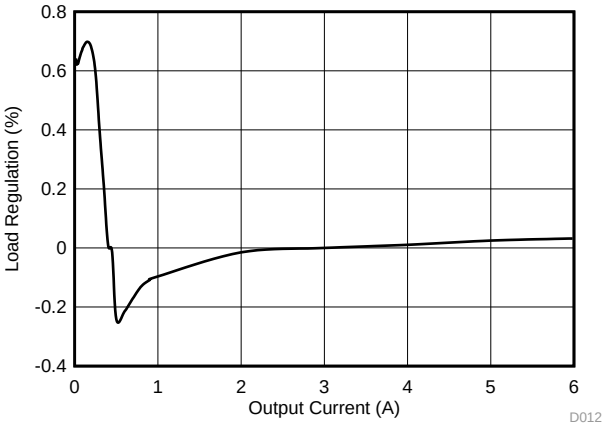


Figure 22. Load Regulation

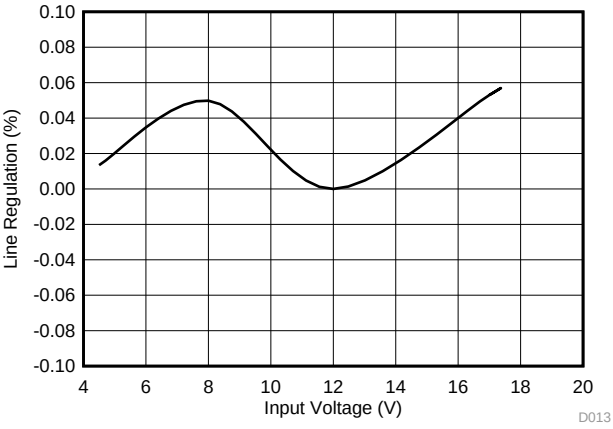


Figure 23. Line Regulation

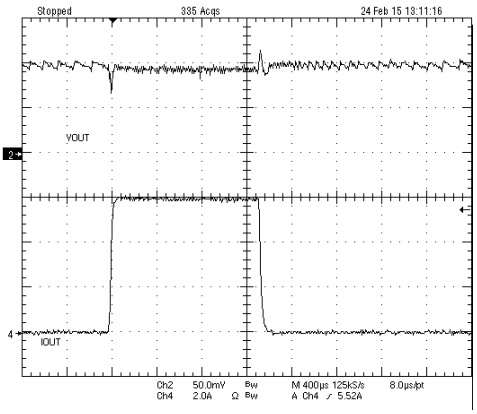


Figure 24. Load Transient

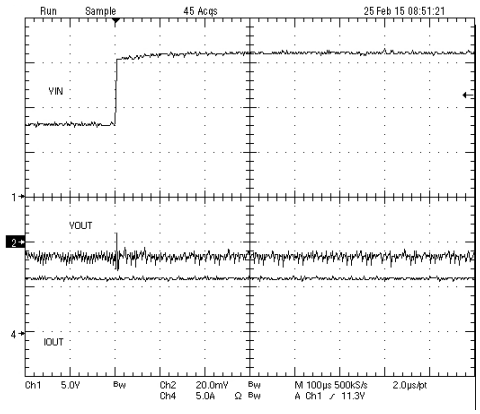


Figure 25. Line Transient

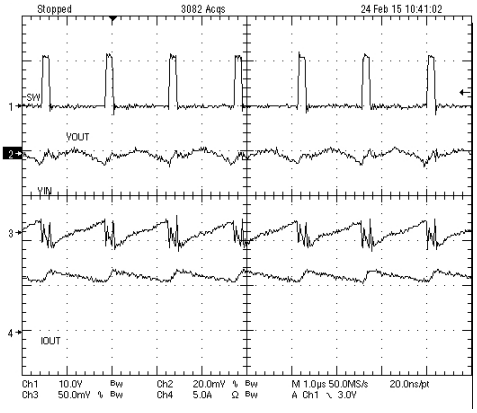


Figure 26. Continuous Conduction Mode (Inductor Current)

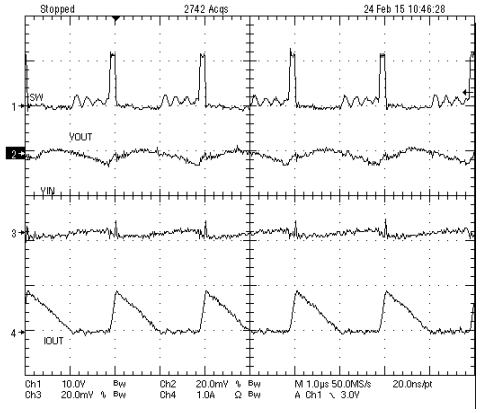


Figure 27. Discontinuous Conduction Mode (Inductor Current)

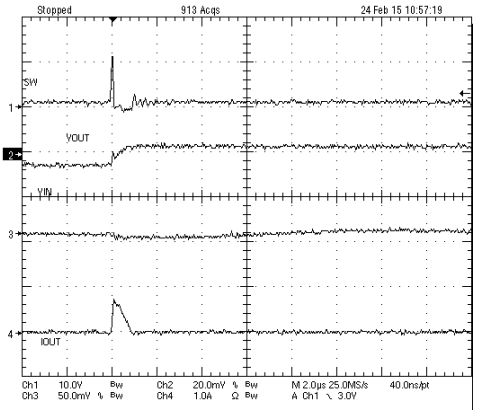


Figure 28. Skip Mode (Inductor Current)

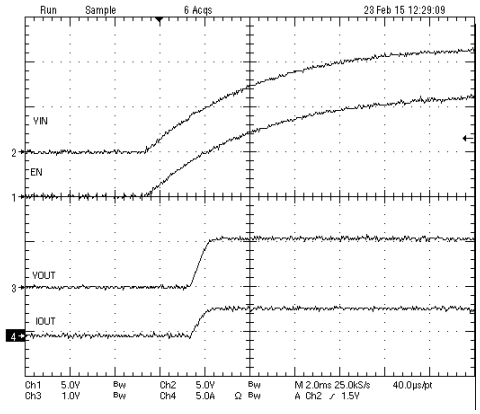


Figure 29. Start Up With VIN

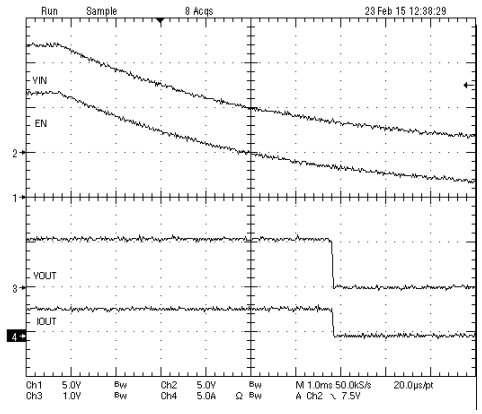


Figure 30. Power Down VIN

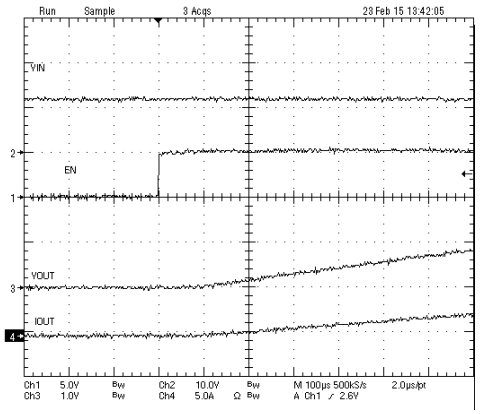


Figure 31. Start Up With EN

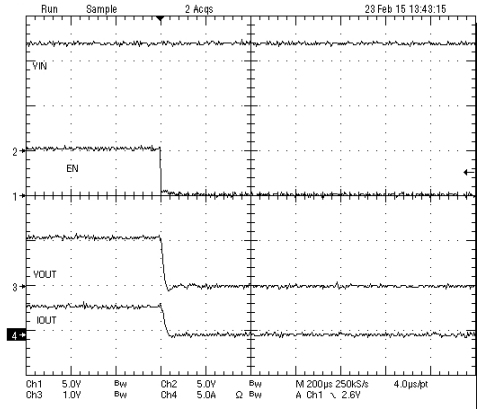


Figure 32. Power Down with EN

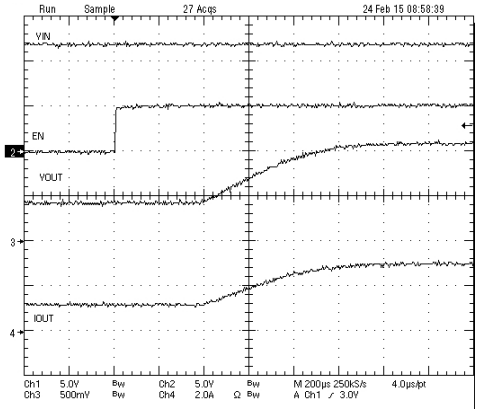


Figure 33. Start Up With EN and Prebias

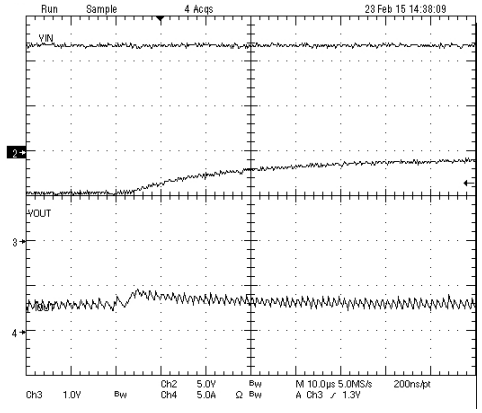


Figure 34. V_{OUT} Step Up With V_{ID}

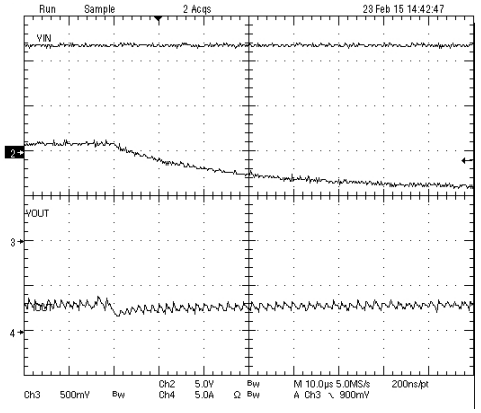


Figure 35. V_{OUT} Step Down With V_{ID}

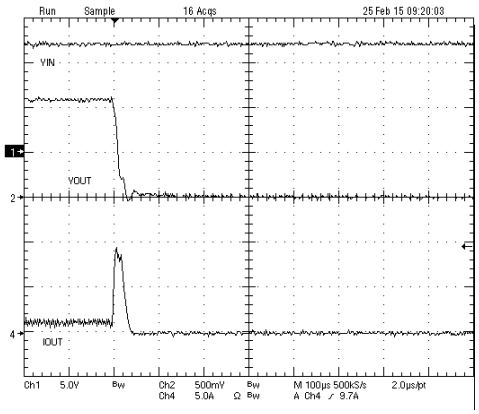


Figure 36. Hiccup Current Limit

10 Power Supply Recommendations

The devices are designed to operate from an input supply range between 4.5 V and 17 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS566250 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback terminal of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground
- Keep the pattern lines for VIN and GND broad.
- Exposed pad of device must be connected to GND with solder.
- Output capacitor should be connected to a broad pattern of the GND.
- Voltage feedback loop should be as short as possible, and preferably with ground shield.
- Kelvin connections should be brought from the output to the feedback terminal of the device.
- Providing sufficient via is preferable for VIN, SW and GND connection.
- PCB pattern for VIN, SW, and GND should be as broad as possible.
- Input capacitors should be placed as near as possible to the device.
- If possible, it is preferred not to allow switching current to flow under the device

11.2 Layout Example

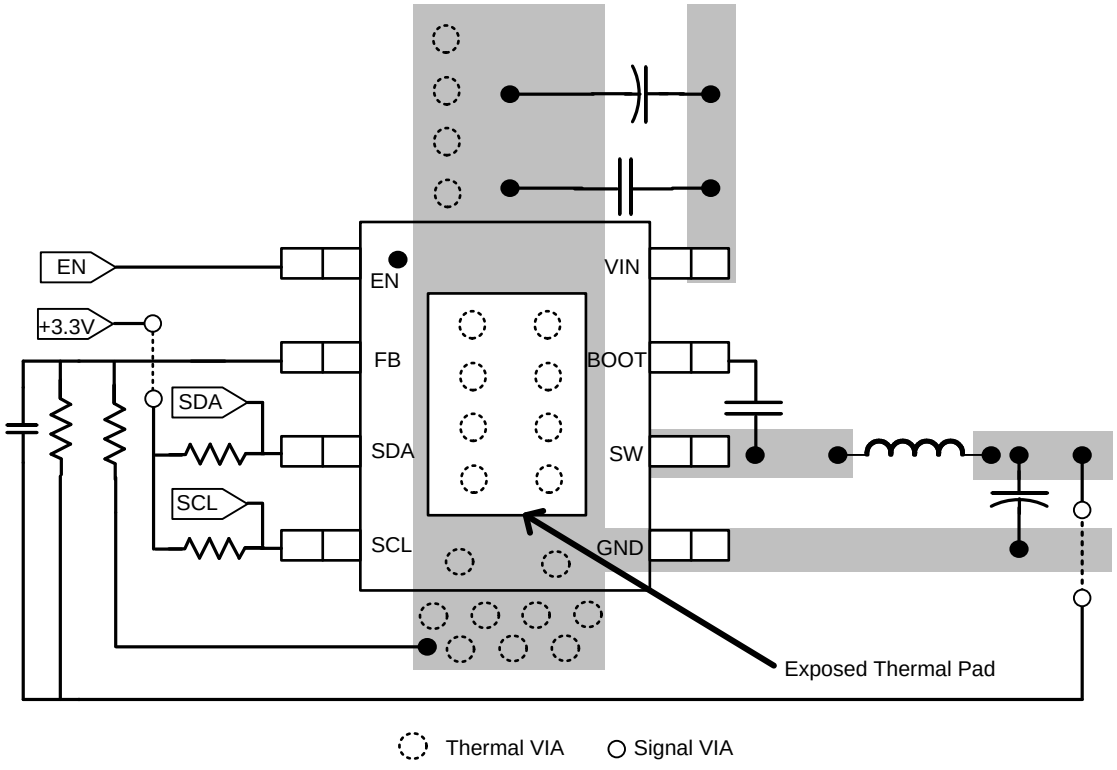


Figure 37. Layout

12 Device and Documentation Support

12.1 Documentation Support

12.2 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

D-CAP2, Eco-mode, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Thermal Information

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see the Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004. The exposed thermal pad dimensions for this package are shown in the following illustration.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS566250DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	566250	Samples
TPS566250DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	566250	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

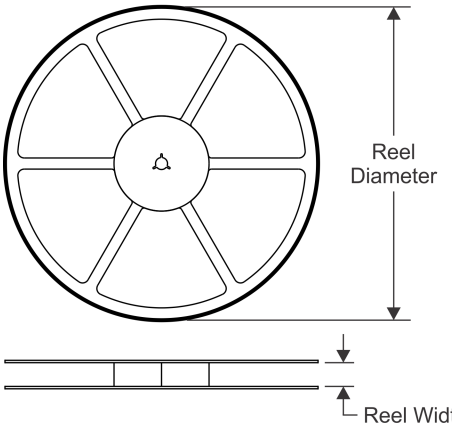
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

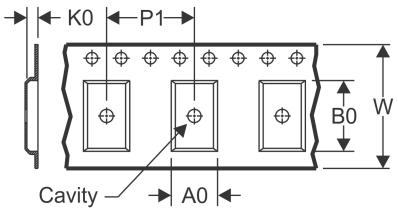
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

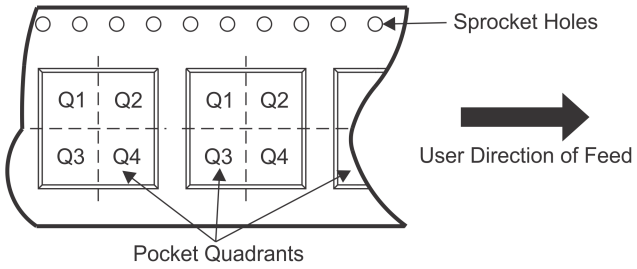


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

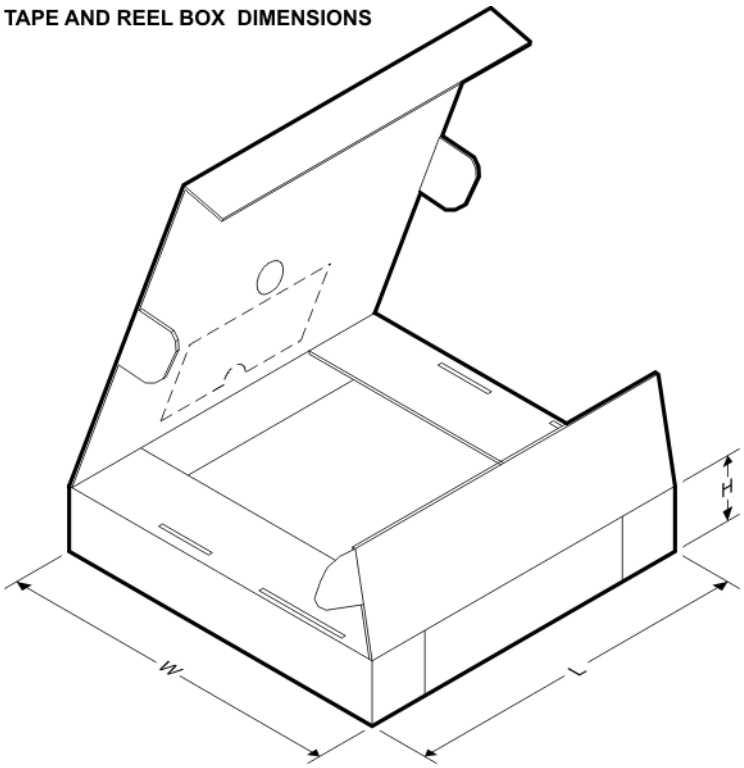
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS566250DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

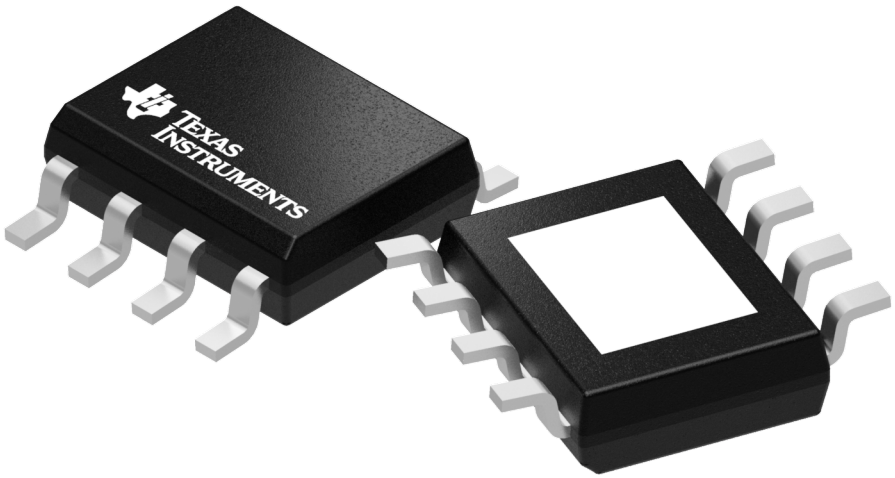


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS566250DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

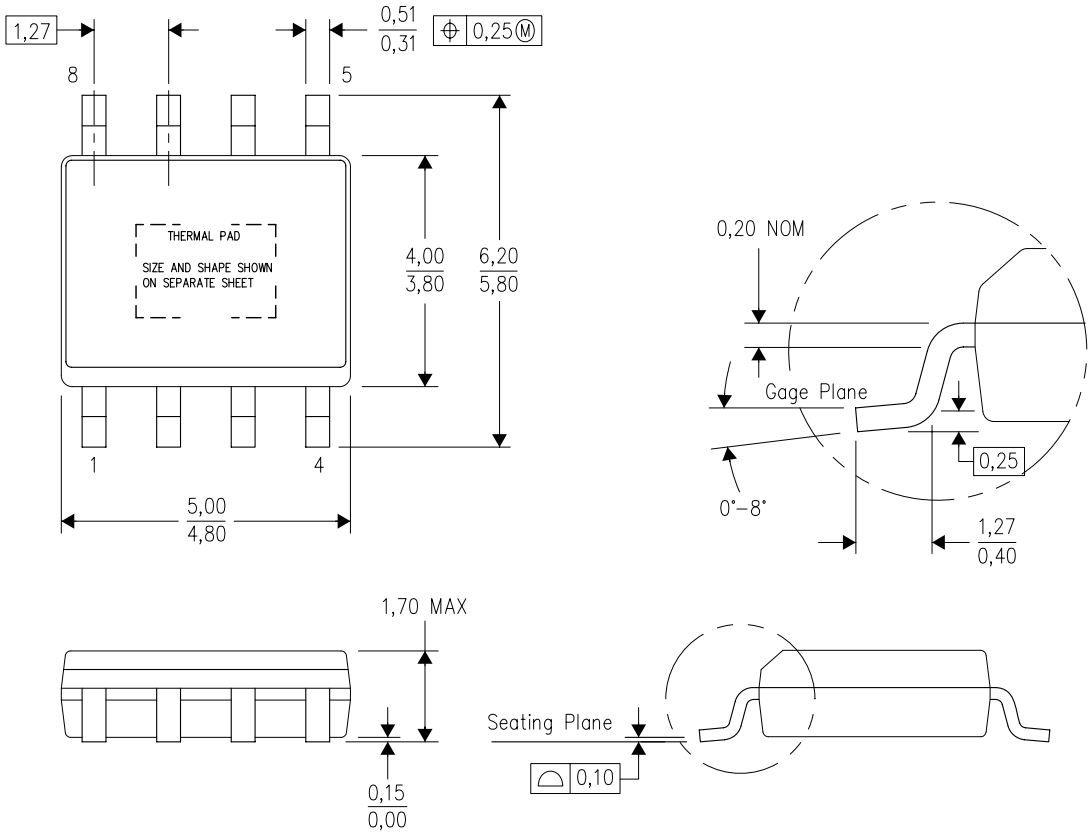
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

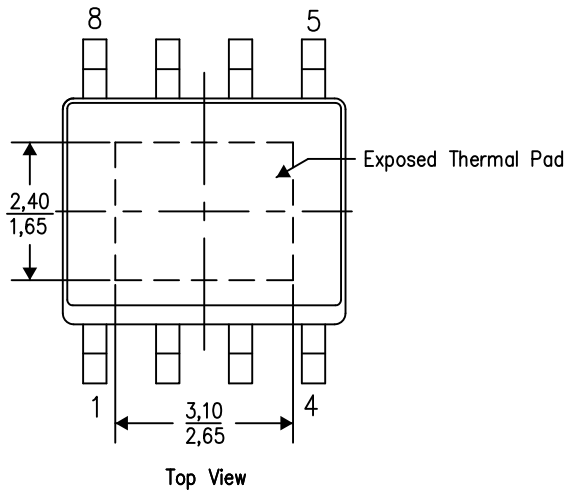
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



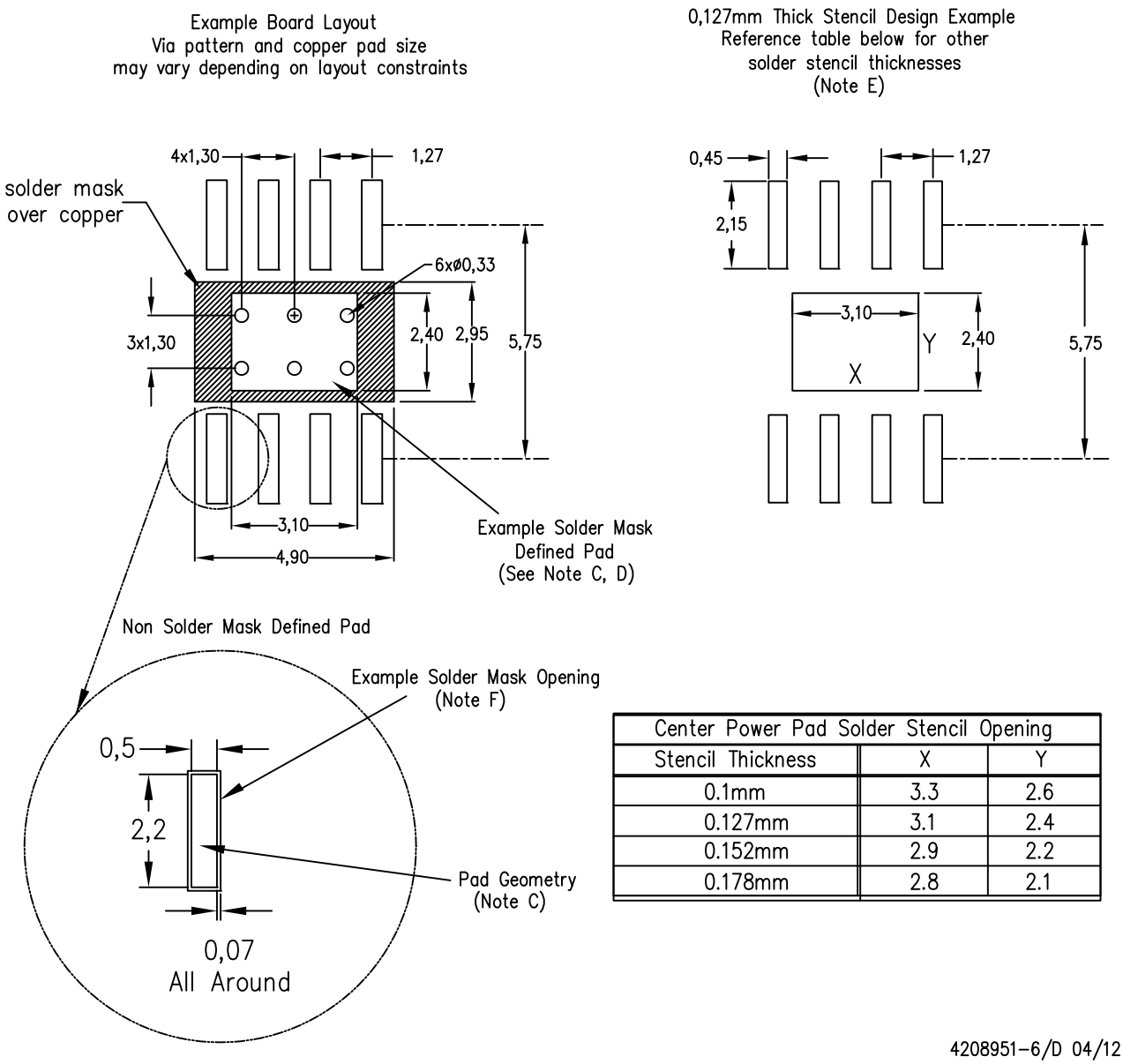
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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