

## DUAL INPUT BUS (2.5 V, 3.3 V) 9-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

### FEATURES

- Low Voltage Separate Power Bus
- 15-mΩ MOSFET Switches for High Efficiency at 9-A Continuous Output
- Adjustable Output Voltage
- Externally Compensated With 1% Internal Reference Accuracy
- Fast Transient Response
- Wide PWM Frequency: Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

### APPLICATIONS

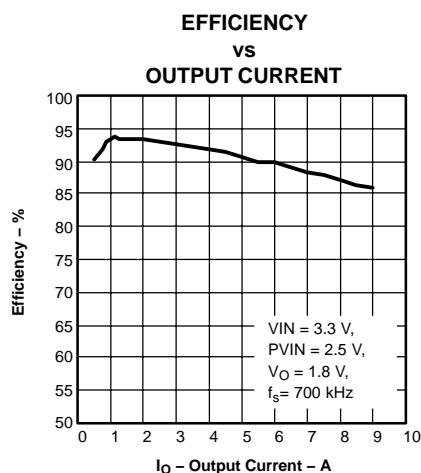
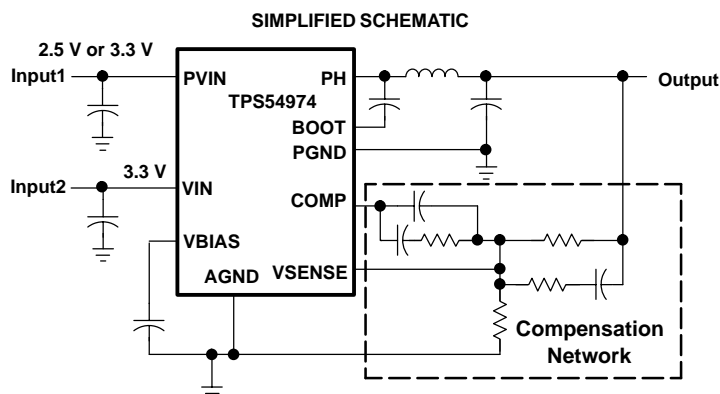
- Low-Voltage, High-Density Systems With Power Distributed at 2.5 V, 3.3 V Available
- Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure
- Portable Computing/Notebook PCs

### DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54974 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the VIN input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a power good output useful for processor/logic reset, fault signaling, and supply sequencing.

The TPS54974 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks.

### SIMPLIFIED SCHEMATIC



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# TPS54974

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

T <sub>A</sub>	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–40°C to 85°C	Adjustable down to 0.9 V	Plastic HTSSOP (PWP) <sup>(1)</sup>	TPS54974PWP

<sup>(1)</sup> The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54974PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

		TPS54974	UNIT
Input voltage range, V <sub>I</sub>	SS/ENA	−0.3 to 7	V
	RT	−0.3 to 6	
	VSENSE	−0.3 to 4	
	PVIN, VIN	−0.3 to 4.5	
	BOOT	−0.3 to 10	
Output voltage range, V <sub>O</sub>	VBIAS, COMP, PWRGD	−0.3 to 7	V
	PH	−0.6 to 6	
Source current, I <sub>O</sub>	PH	Internally limited	
	COMP, VBIAS	6	mA
Sink current, I <sub>S</sub>	PH	16	A
	COMP	6	mA
	SS/ENA, PWRGD	10	
Voltage differential	AGND to PGND	±0.3	V
Operating virtual junction temperature range, T <sub>J</sub>		−40 to 125	°C
Storage temperature, T <sub>stg</sub>		−65 to 150	°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		300	°C

<sup>(1)</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, VIN, V <sub>I</sub>	3		4	V
Power input voltage, PVIN	2.2	2.5	4.0	V
Operating junction temperature, T <sub>J</sub>	–40		125	°C

## DISSIPATION RATINGS<sup>(1)(2)</sup>

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T <sub>A</sub> = 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
28 Pin PWP with solder	14.4°C/W	6.94 W <sup>(3)</sup>	3.81 W	2.77 W
28 Pin PWP without solder	27.9°C/W	3.58 W	1.97 W	1.43 W

<sup>(1)</sup> For more information on the PWP package, refer to TI technical brief, literature number SLMA002.

<sup>(2)</sup> Test board conditions:

1. 3" x 3", 4 layers, thickness: 0.062"
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. 0.5 oz. copper ground planes on the 2 internal layers
5. 12 thermal vias (see “Recommended Land Pattern” in applications section of this data sheet)

<sup>(3)</sup> Maximum power dissipation may be limited by over current protection.

## ELECTRICAL CHARACTERISTICS

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 3\text{ V}$  to  $4\text{ V}$ ,  $PV_{IN} = 2.2\text{ V}$  to  $2.8\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY VOLTAGE, VIN							
Input voltage range, VIN			3.0		4.0	V	
Supply voltage range, PVIN		Output = 1.8 V	2.2	2.5	4.0	V	
I(Q)	Quiescent current	VIN	f <sub>s</sub> = 350 kHz, RT open, PH pin open, PVIN = 2.5 V		6.3	10.0	mA
			SHUTDOWN, SS/ENA = 0 V, PVIN = 2.5 V		1	1.4	
	PVIN	f <sub>s</sub> = 350 kHz, RT open, PH pin open, VIN = 3.3 V		4.0	7.0	mA	
		SHUTDOWN, SS/ENA = 0 V, VIN = 3.3 V		< 100		μA	
UNDER VOLTAGE LOCK OUT (VIN)							
Start threshold voltage, UVLO			2.95		3.0	V	
Stop threshold voltage, UVLO			2.70	2.80		V	
Hysteresis voltage, UVLO			0.14	0.16		V	
Rising and falling edge deglitch, UVLO <sup>(1)</sup>			2.5			μs	
BIAS VOLTAGE							
Output voltage, VBIAS		I(VBIAS) = 0	2.70	2.80	2.90	V	
Output current, VBIAS <sup>(2)</sup>			100			μA	
CUMULATIVE REFERENCE							
V <sub>ref</sub>	Accuracy		0.882	0.891	0.900	V	
REGULATION							
Line regulation <sup>(1)(3)</sup>		I <sub>L</sub> = 4.5 A, f <sub>s</sub> = 350 kHz, T <sub>J</sub> = 85°C	0.07			%/V	
Load regulation <sup>(1)(3)</sup>		I <sub>L</sub> = 0 A to 9 A, f <sub>s</sub> = 350 kHz, T <sub>J</sub> = 85°C	0.03			%/A	
OSCILLATOR							
Internally set—free running frequency		RT open <sup>(1)</sup>	280	350	420	kHz	
Externally set—free running frequency range		RT = 180 kΩ (1% resistor to AGND) <sup>(1)</sup>	252	280	308	kHz	
		RT = 100 kΩ (1% resistor to AGND)	460	500	540		
		RT = 68 kΩ (1% resistor to AGND) <sup>(1)</sup>	663	700	762		
Ramp valley <sup>(1)</sup>			0.75			V	
Ramp amplitude (peak-to-peak) <sup>(1)</sup>			1			V	
Minimum controllable on time <sup>(1)</sup>			200			ns	
Maximum duty cycle <sup>(1)</sup>			90%				

(1) Specified by design

(2) Static resistive loads only

(3) Specified by the circuit used in Figure 10

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## ELECTRICAL CHARACTERISTICS (continued)

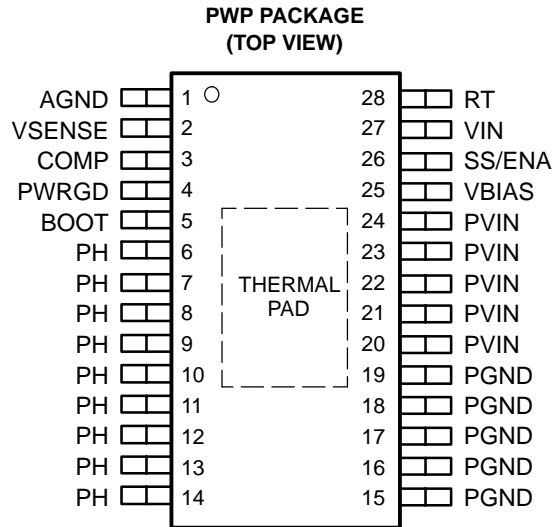
 $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 3\text{ V}$  to  $4\text{ V}$ ,  $PV_{IN} = 2.2\text{ V}$  to  $2.8\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ERROR AMPLIFIER</b>					
Error amplifier open loop voltage gain	1 k $\Omega$ COMP to AGND <sup>(1)</sup>	90	110		dB
Error amplifier unity gain bandwidth	Parallel 10 k $\Omega$ , 160 pF COMP to AGND <sup>(1)</sup>	3	5		MHz
Error amplifier common mode input voltage range	Powered by internal LDO <sup>(1)</sup>	0		V <sub>BIAS</sub>	V
Input bias current, V <sub>SENSE</sub>	V <sub>SENSE</sub> = V <sub>ref</sub>		60	250	nA
Output voltage slew rate (symmetric), COMP		1.0	1.4		V/ $\mu$ s
<b>PWM COMPARATOR</b>					
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive <sup>(1)</sup>		70	85	ns
<b>SLOW-START/ENABLE</b>					
Enable threshold voltage, SS/ENA		0.82	1.2	1.4	V
Enable hysteresis voltage, SS/ENA <sup>(1)</sup>			0.03		V
Falling edge deglitch, SS/ENA <sup>(1)</sup>			2.5		$\mu$ s
Internal slow-start time		2.6	3.35	4.1	ms
Charge current, SS/ENA	SS/ENA = 0 V	3	5	8	$\mu$ A
Discharge current, SS/ENA	SS/ENA = 0.2 V, V <sub>IN</sub> = 2.7 V, PV <sub>IN</sub> = 2.5 V	1.5	2.3	4.0	mA
<b>POWER GOOD</b>					
Power good threshold voltage	V <sub>SENSE</sub> falling		90		%V <sub>ref</sub>
Power good hysteresis voltage <sup>(1)</sup>			3		%V <sub>ref</sub>
Power good falling edge deglitch <sup>(1)</sup>			35		$\mu$ s
Output saturation voltage, PWRGD	I <sub>(sink)</sub> = 2.5 mA		0.18	0.3	V
Leakage current, PWRGD	V <sub>IN</sub> = 3.3 V, PV <sub>IN</sub> = 2.5 V			1	$\mu$ A
<b>CURRENT LIMIT</b>					
Current limit	V <sub>IN</sub> = 3.3 V, PV <sub>IN</sub> = 2.5 V <sup>(1)</sup> , Output shorted	11	15		A
Current limit leading edge blanking time <sup>(1)</sup>			100		ns
Current limit total response time <sup>(1)</sup>			200		ns
<b>THERMAL SHUTDOWN</b>					
Thermal shutdown trip point <sup>(1)</sup>		135	150	165	$^{\circ}\text{C}$
Thermal shutdown hysteresis <sup>(1)</sup>			10		$^{\circ}\text{C}$
<b>OUTPUT POWER MOSFETS</b>					
r <sub>DS(on)</sub> Power MOSFET switches	V <sub>IN</sub> = 3 V, PV <sub>IN</sub> = 2.5 V		15	30	m $\Omega$
	V <sub>IN</sub> = 3.6 V, PV <sub>IN</sub> = 2.5 V		14	28	

<sup>(1)</sup> Specified by design

<sup>(2)</sup> Static resistive loads only

<sup>(3)</sup> Specified by the circuit used in Figure 10



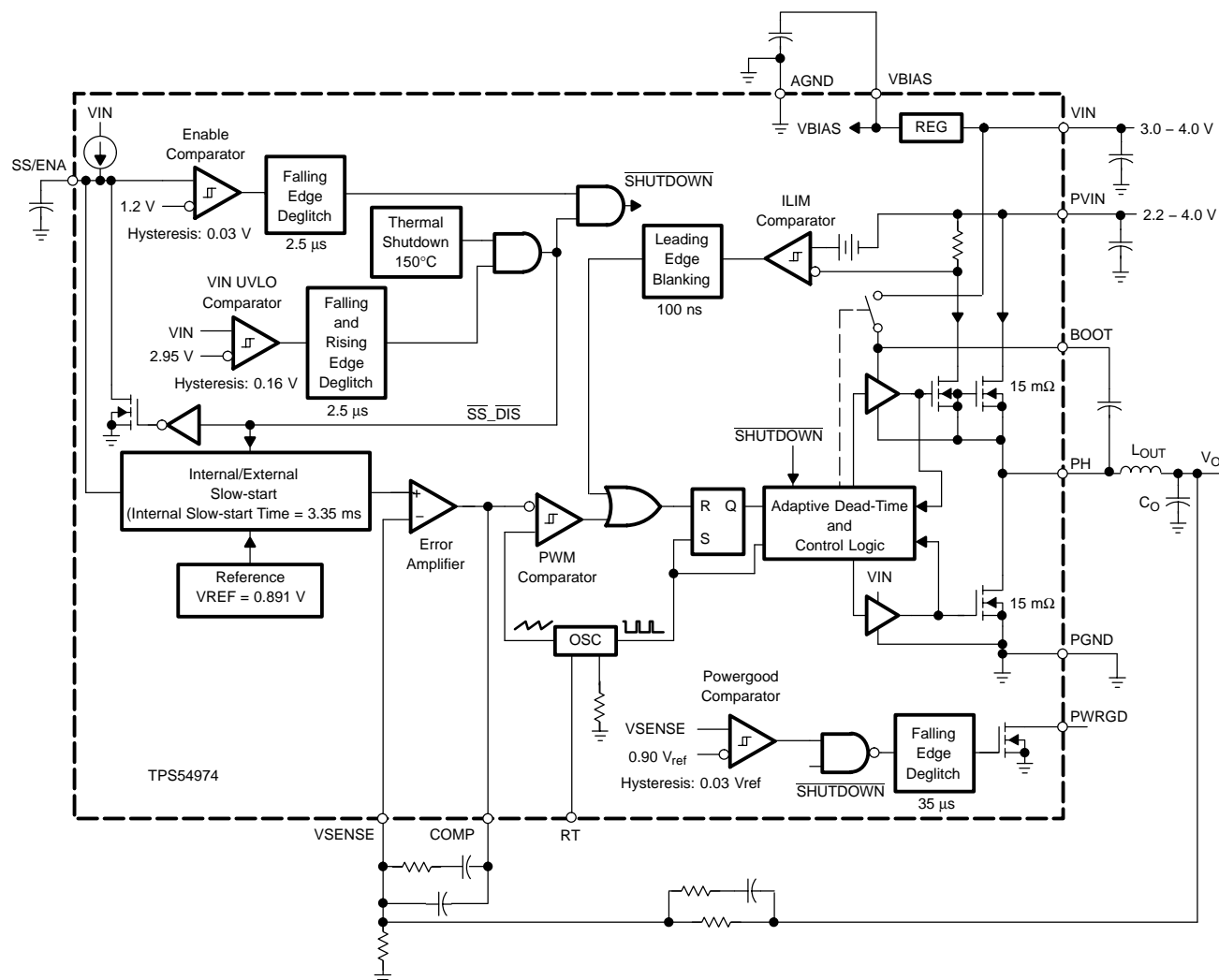
## TERMINAL FUNCTIONS

TERMINAL NAME	NO.	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, and RT resistor. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022-μF to 0.1-μF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
PGND	15–19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6–14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PVIN	20–24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10-μF ceramic capacitor.
PWRGD	4	Power good open drain output. High when VSENSE ≥ 90% V <sub>ref</sub> , otherwise PWRGD is low. Note that output is low when SS/ENA is low or the internal shutdown signal is active.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f <sub>s</sub> .
SS/ENA	26	Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high-quality, low-ESR 0.1-μF to 1.0-μF ceramic capacitor.
VIN	27	Input supply for the internal bias regulator. An external capacitor of 1 μF to be connected to the VIN pin.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

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## INTERNAL BLOCK DIAGRAM



## RELATED DC/DC PRODUCTS

- TPS40000—dc/dc controller
- TPS56300—dc/dc controller
- PT6600 series—9 A plugin modules
- TPS54910—dc/dc converter

## TYPICAL CHARACTERISTICS

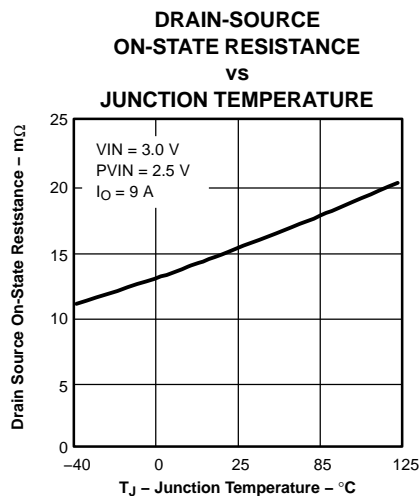


Figure 1

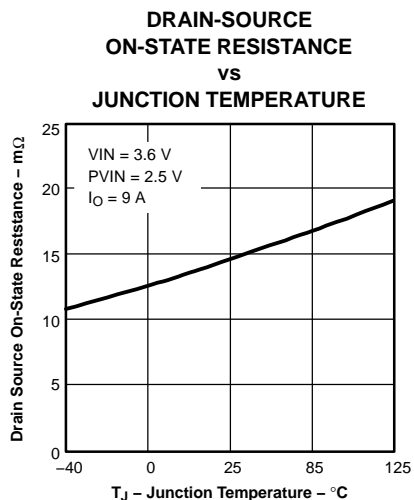


Figure 2

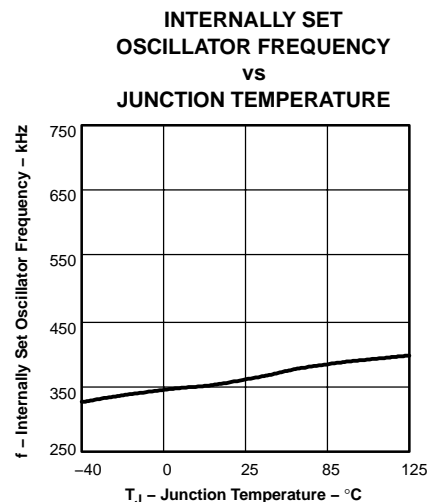


Figure 3

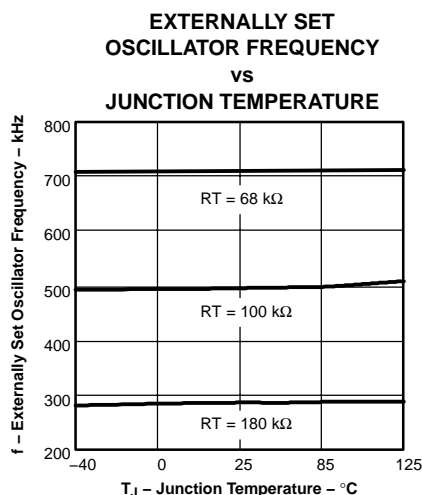


Figure 4

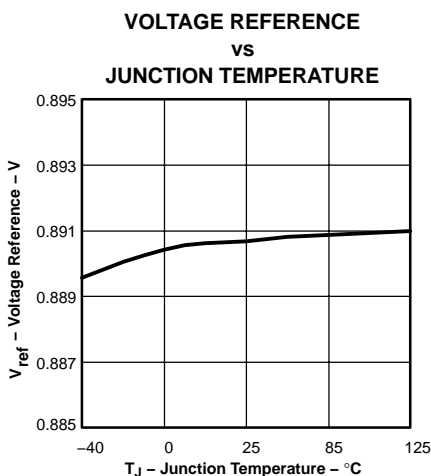


Figure 5

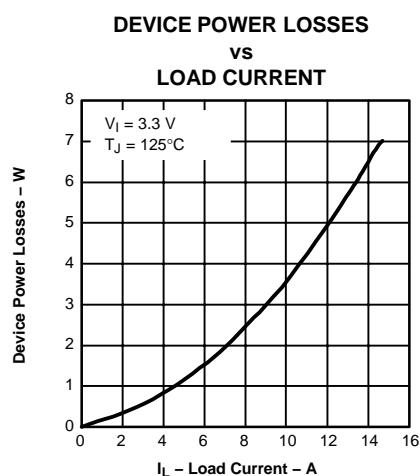


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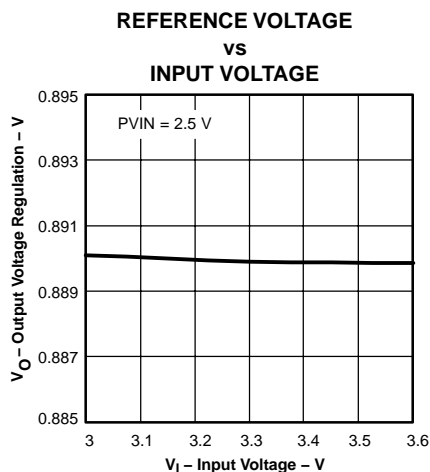


Figure 7

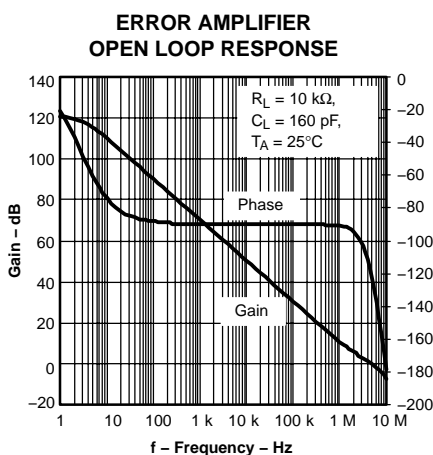


Figure 8

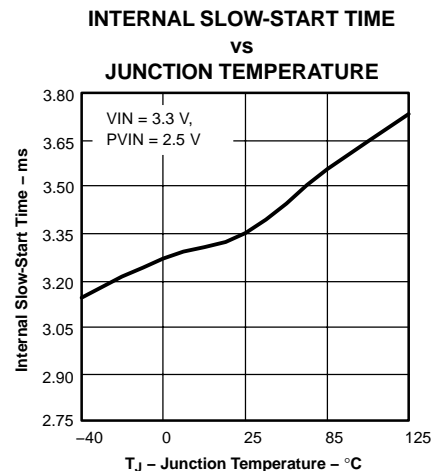


Figure 9

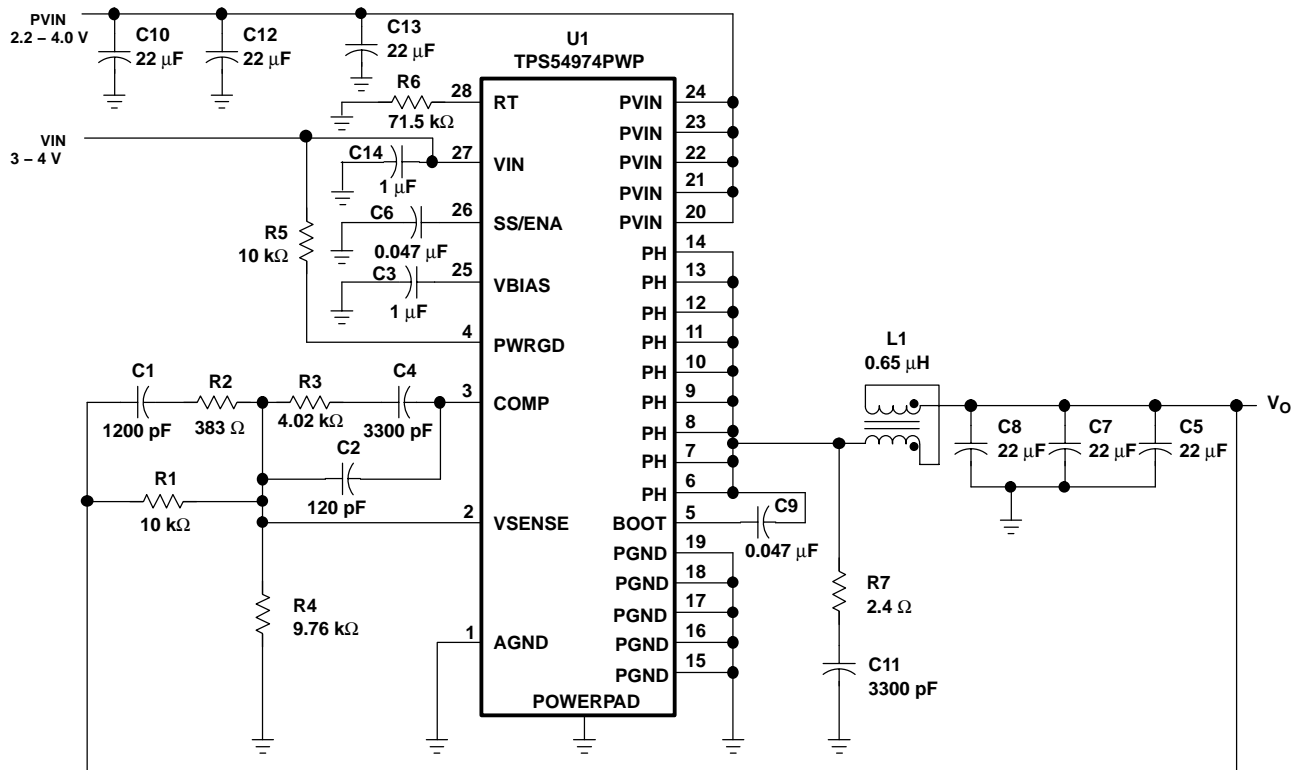
## TPS54974

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### APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54974 application. The TPS54974 (U1) can provide up to 9 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the exposed

thermal PowerPAD underneath the integrated circuit, TPS54974, package must be soldered to the printed-circuit board.



Analog and Power Grounds Are Tied at the Pad Under the Package of IC

Figure 10. Application Circuit

### COMPONENT SELECTION

The values for the components used in this design example were selected for best load transient response and small PCB area. Additional design information is available at [www.ti.com](http://www.ti.com).

### INPUT FILTER

The PVIN input voltage is nominally at 2.5 VDC. The input filter consists of three 22-μF ceramic capacitors (C10, C12, and C13) which must be located as close as possible to the PVIN and PGND pins or the device to provide high-frequency decoupling. Ripple current is carried in all three capacitors. The return path to PGND must be made so as to avoid introducing circulating currents in the output filter stage.

### FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times.

The resistor divider network of R1 and R4 sets the output voltage for the circuit at 1.8 V. R1 along with R2, R3, C1, C2, and C4 forms the loop compensation network for the circuit. For this design, a Type-3 topology is used.

### OPERATING FREQUENCY

In the application circuit, RT is grounded through a 71.5-kΩ resistor to select the operating frequency of 700 kHz. To set a different frequency, place a 68-kΩ to 180-kΩ resistor between RT (pin 28) and analog ground or leave RT floating to select the default of 350 kHz. The resistance can be approximated using the following equation:

$$R = \frac{500 \text{ kHz}}{\text{Switching Frequency}} \times 100 \text{ [k}\Omega\text{]} \quad (1)$$



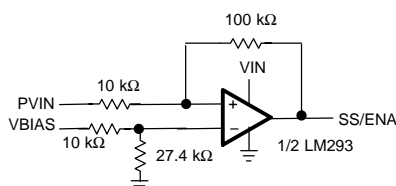
## OPERATING WITH SEPARATE PVIN

The TPS54974 is designed to operate with the power stage (high side and low side MOSFETs) with the PVIN input connected to a separate power source from VIN. The primary intended application has VIN connected to a 3.3-V bus and PVIN connected to a 2.5-V bus. The TPS54974 cannot be damaged by any sequencing of these voltages. However, the UVLO (see detailed description section) is referenced to the VIN input. There are some conditions that may cause undesirable operation.

If PVIN is absent when the VIN input is high, the slow-start is released, and the PWM circuit goes to maximum duty factor. When the PVIN input ramps up, the output of the TPS54974 follows the PVIN input until enough voltage is present to regulate to the proper output value.

### NOTE:

If the PVIN input is controlled via a fast bus switch, it results in a hard start condition and may damage the load (i.e., whatever is connected to the regulated output of the TPS54974). If a power good signal is not available from the 2.5-V power supply, one can be generated using a comparator and hold the SS/ENA pin low until the 2.5-V bus power is good. An example of this is shown in Figure 11. This circuit can also be used to prevent the TPS54974 output from following the PVIN input while the PVIN power supply is ramping up.



**Figure 11. Undervoltage Lockout Circuit for PVIN Using Open Collector or Open Drain Comparator**

PVIN and VIN can be tied together for 3.3-V bus operation.

## OUTPUT FILTER

The output filter is composed of a 0.65-μH inductor and 3 x 22-μF capacitor. The inductor is a low dc-resistance (.017 Ω) type, Pulse Engineering PA0277. The capacitors used are 22-μF, 6.3-V ceramic types with X5R dielectric. The feedback loop is compensated so that the unity gain frequency is approximately 75 kHz.

## MAXIMUM OUTPUT VOLTAGE

The maximum attainable output voltage is limited by the minimum voltage at the PVIN pin. Nominal maximum duty cycle is limited to 90% in the TPS54974, so maximum output voltage is:

$$V_{O(max)} = PVIN_{(min)} \times 0.9 \quad (2)$$

Care must be taken while operating when nominal conditions cause duty cycles near 90%. Load transients can require momentary increases in duty cycle. If the required duty cycle exceeds 90%, the output may fall out of regulation.

## GROUNDING AND POWERPAD LAYOUT

The TPS54974 has two internal grounds (analog and power). Inside the TPS54974, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54974, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes must tie together directly at the IC to reduce noise between the two grounds. The only components that must tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54974.

## LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3-inch by 3-inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013-inch diameter vias to avoid solder wicking through the vias.

Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

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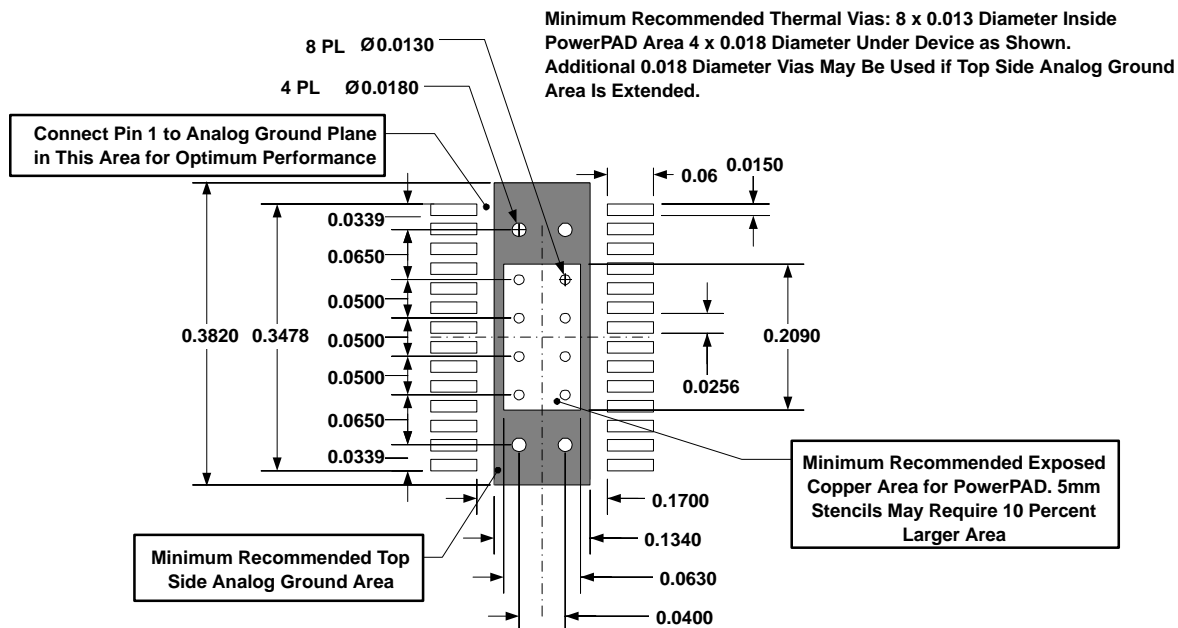


Figure 12. Recommended Land Pattern for 28-Pin PWP PowerPAD

## PERFORMANCE GRAPHS

Data shown is for the circuit of Figure 10. All data is for  $V_{IN} = 3.3\text{ V}$ ,  $PV_{IN} = 2.5\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $f_s = 700\text{ kHz}$ , and  $T_A = 25^\circ\text{C}$ , unless otherwise specified

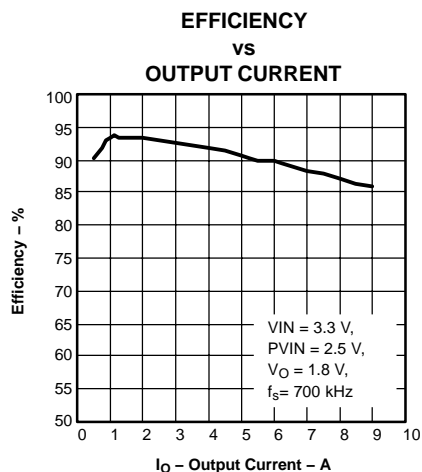


Figure 13

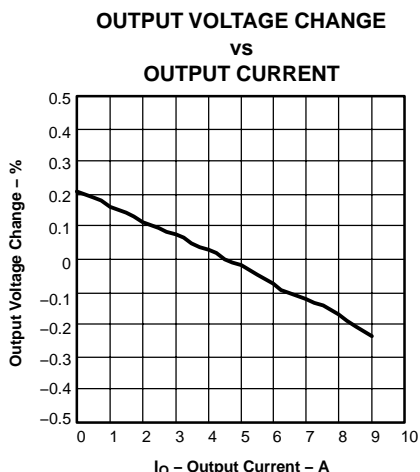


Figure 14

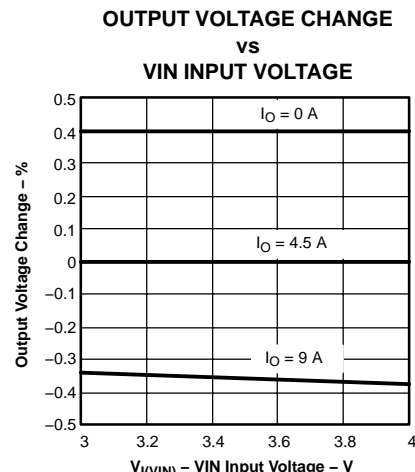


Figure 15

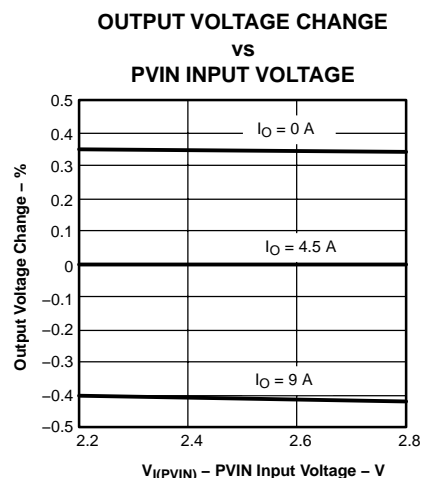


Figure 16

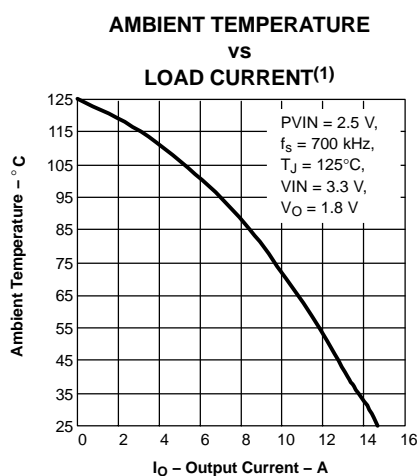


Figure 17

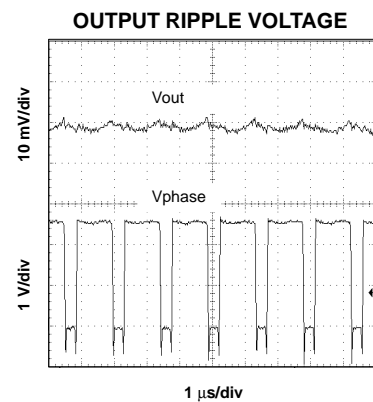


Figure 18

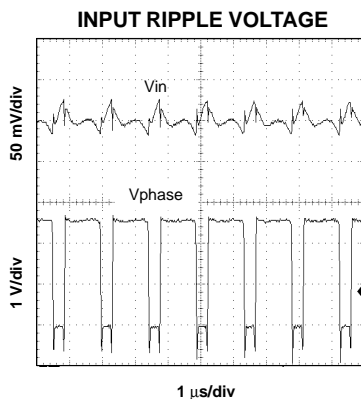


Figure 19

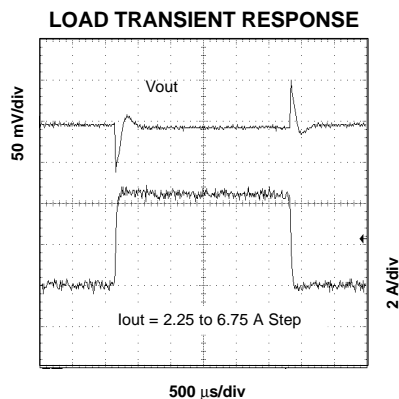


Figure 20

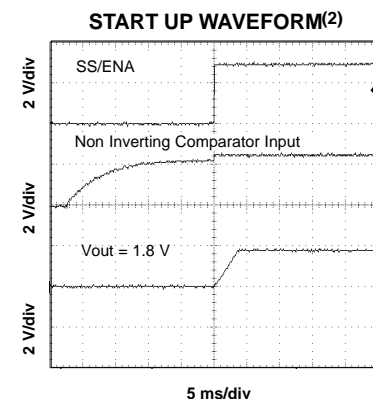


Figure 21

(1) Safe operating area is applicable to the test board conditions in the Dissipation Ratings

(2) Using the undervoltage lockout circuit of Figure 11

## DETAILED DESCRIPTION

### UNDERVOLTAGE LOCK OUT (UVLO)

The TPS54974 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-μs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN. UVLO with respect to VIN and not PVIN, see application note.

### SLOW-START/ENABLE (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start-up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-μs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise.

The second function of the SS/ENA pin provides an external means of extending the slow-start time with a low-value capacitor connected between SS/ENA and AGND.

Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2 \text{ V}}{5 \mu\text{A}} \quad (3)$$

Second, as the output becomes active, a brief ramp-up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7 \text{ V}}{5 \mu\text{A}} \quad (4)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp-up at the internal rate.

### VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits. VBIAS is derived from the VIN pin, see the internal block diagram on page 6.

### VOLTAGE REFERENCE

The voltage reference system produces a precise  $V_{ref}$  signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54974, since it cancels offset errors in the scale and error amplifier circuits.

### OSCILLATOR AND PWM RAMP

The oscillator frequency is set to an internally fixed value of 350 kHz. The oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100 \text{ k}\Omega}{R} \times 500 \text{ [kHz]} \quad (5)$$

### ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54974 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type-2 or Type-3 compensation can be employed using external compensation components.

## PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control-logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54974 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

## DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side

FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

## OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents current limit false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

## THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the slow-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

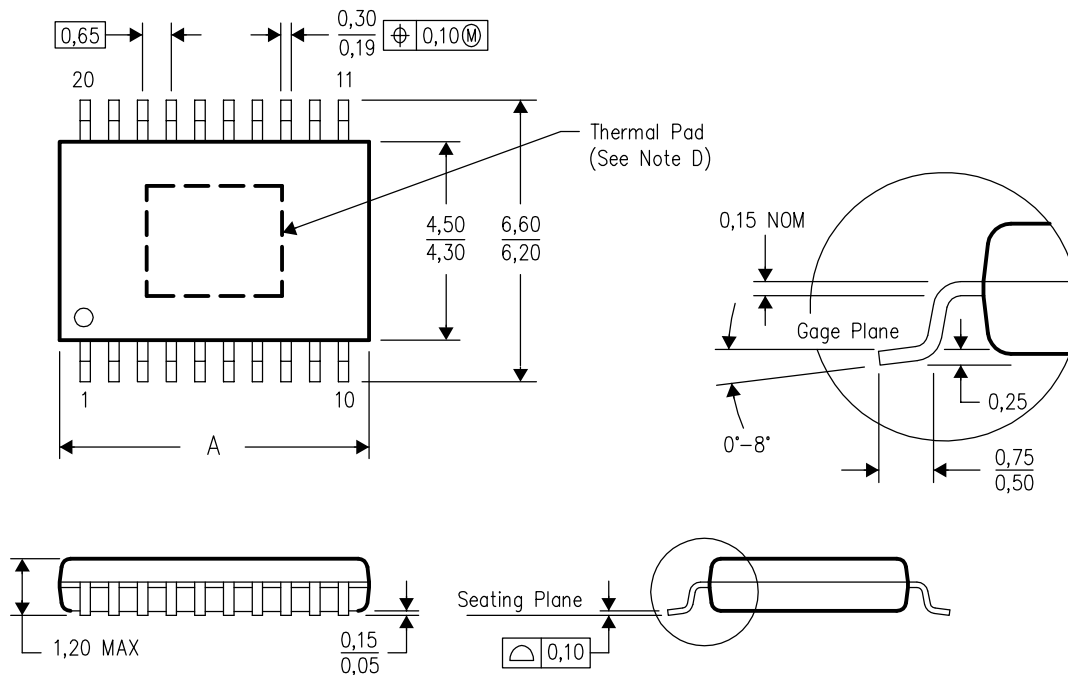
## POWER-GOOD (PWRGD)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or SS/ENA is low. When VIN ≥ UVLO threshold, SS/ENA ≥ enable threshold, and VSENSE > 90% of Vref, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of Vref and a 35 μs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

## PWP (R-PDSO-G\*\*)

## PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS **	14	16	20	24	28
DIM					
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Falls within JEDEC MO-153

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