Synchronous Switcher Controller With 2-A LDO for GPU Power

FEATURES

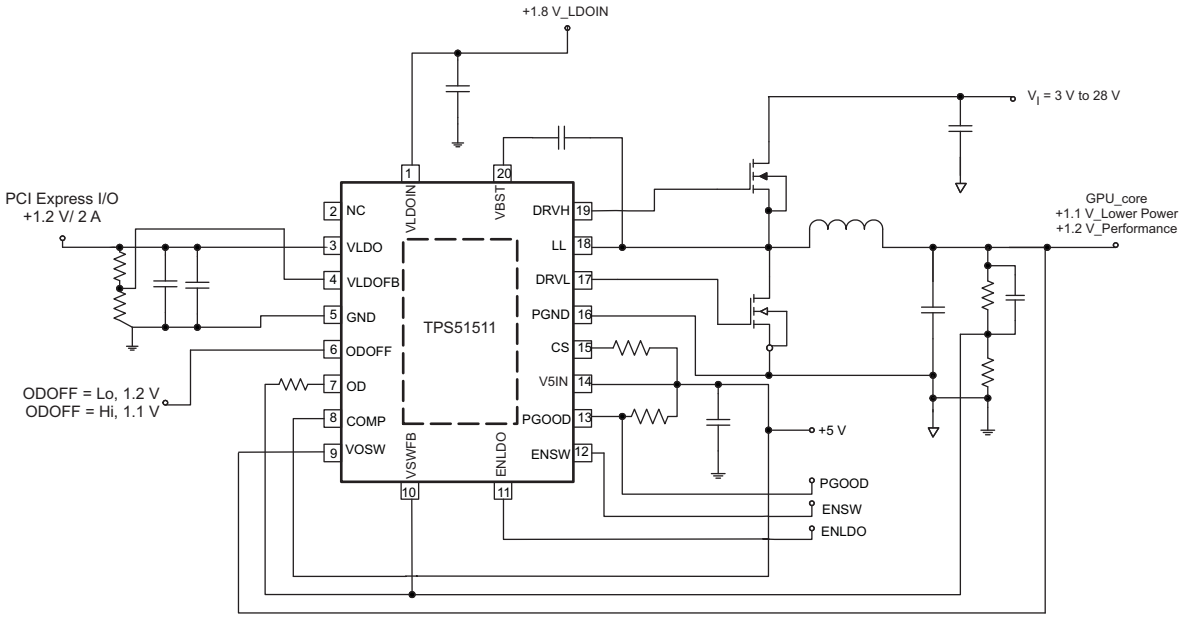
- **Switcher Controller:**
  - **Adjustable-Output Buck Converter, 0.75 V to 3.3 V**
  - **Wide Input Voltage Range: 3.0-V to 28-V**
  - **D-CAP™ Mode with 100-ns Load Step Response**
  - **Current Mode Option Supports Ceramic Output Capacitors**
  - **Current Sensing From $R_{DS(ON)}$ or Resistor**
  - **Internal Switch Supports Dynamic Output Voltage Change**
  - **Advanced PGOOD Mask Feature**
  - **Equipped With PGOOD, OVP and UVP**
  - **Output Discharge**
  - **5 V UVLO Protection**
- **LDO Regulator:**
  - **2-A LDO for GPU I/O Power**
  - **Input Range: Up to 5 V**
  - **Output Range: 0.75 V to 3.3 V**
  - **Requires Only 20-μF Ceramic Output Capacitor for LDO Output**
  - **Optional PGOOD**
  - **Output Discharge**
  - **Thermal Shutdown**

APPLICATIONS

- **GPU Power**
- **Notebook Computers**

DESCRIPTION

The TPS51511 is a 350-kHz D-CAP-mode synchronous switcher with a 2-A, source-only low drop-out (LDO) regulator. It is specifically designed for low cost/low noise/low external-component count power systems for GPU applications. The integrated 'OD' switch in the buck controller supports dynamic output voltage change. The current mode option of the synchronous buck converter can support pure output ceramic-capacitor applications. The open-drain LDO power-good signal can be accessed through the OD pin when it is needed in the application. The TPS51511 is available in the thermally-enhanced 20-pin QFN package, and is specified from –40°C to 85°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICES	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN
–40°C to 85°C	PLASTIC RHL	TPS51511RHLT	20	Small Tape-and-Reel	250	Green (RoHS and no Sb/Br)
		TPS51511RHLR		Tape-and-Reel	3000	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
Input voltage range(2)		VBST	–0.3 to 36	V
		VBST(3)	–0.3 to 6	V
		V5IN, VLDOIN	–0.3 to 6	V
		CS, VLDOFB, VOSW	–0.3 to 6	V
		ENSW, ENLDO, VSWFB, ODOFF	–0.3 to 6	V
		PGND	–0.3 to 0.3	V
Output voltage range (2)		DRVH	–1.0 to 36	V
		LL	–1.0 to 30	V
		DRVL	–0.3 to 6	V
		VLDO, OD, COMP, PGOOD	–0.3 to 6	V
θ_{JA}	Thermal information	Junction-to-Ambient thermal resistance	53.34	°C/W
θ_{JC}		Junction-to-PowerPAD thermal resistance	8.84	°C/W
T_A	Operating ambient temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage value is with respect to the LL terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V5IN	4.75	5.25	V
Voltage range	VBST, DRVH	–0.1	34	V
	LL	–0.6	28	
	VLDO, VLDOFB, VOSW	–0.1	3.6	
	PGND	–0.1	0.1	
	ENSW, ENLDO, ODOFF, PGOOD, CS, COMP, DRVL, OD, VSWFB, VLDOIN	–0.1	5.25	
T_A	Operating free-air temperature	–40	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{V5IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5IN1}	Supply current 1,V_{5IN}	T_A =25°C; No load, V_{ENSW}= V_{ENLDO} = 5 V, COMP connected to capacitor		0.8	2	mA
I_{V5IN2}	Supply current 2,V_{5IN}	T_A =25°C; No load, V_{ENSW}= 5,VENLDO = 0V, COMP connected to capacitor		300	600	µA
I_{V5IN3}	Supply current 3,V_{5IN}	T_A =25°C; No load, V_{ENSW} = 5 V, V_{ENLDO} = 0, V_{COMP} = 5 V		240	500	µA
$I_{V5INSDN}$	Shutdown current, V_{5IN}	T_A =25°C; No load, V_{ENSW} = V_{ENLDO} = 0 V		0.1	1.0	µA
$I_{VLDOIN1}$	Supply current1,VLDOIN	T_A =25°C; No load, V_{ENSW} = V_{ENLDO} = 5 V		1	15	µA
$I_{VLDOIN2}$	Supply current 2,VLDOIN	T_A =25°C; No load, V_{ENSW} = 0 V, $_{ENLDO}$ = 5 V,		0.1	15	µA
$I_{VLDOINSDN}$	Standby current, VLDOIN	T_A =25°C; No load, V_{ENSW} = V_{ENLDO} = 0 V		0.1	1	µA
LDO						
V_{LDOFB}	LDO feedback voltage	–40°C < T_A < 85°C V_{LDOIN} = 1.8 V, V_{VLDO} set to 1.2 V	745.6	757	768.3	mV
ΔV_{VLDO}	LDO load regulation	0 A < I_{LDO} < 2 A, V_{LDOIN} = 2.5 V(1), V_{VLDO} set to 1.2 V, 0°C < T_A < 85°C		30		mV
I_{LDOOC}	LDO current limit	V_{LDOIN} = 2.5 V(1), V_{LDO} = 1.2 V, C_{OUT} = 2×10 µF, Raise the output current until it is limited	2	2.5	3.5	A
$I_{VLDOFBBIAS}$	LDO feedback bias current	ENLDO = 5 V, VLDOIN = 1.8 V, VLDOFB = 0.8 V	–1	–0.2	1	µA
$I_{VLDOFBLK}$	LDO feedback leak current	ENLDO = 0 V, V_{LDOIN} = 1.8 V, VLDOFB = 0.8 V	–1		1	µA
$R_{DS(ON)}$	Series resistance	V_{VLDO} = 2.5 V, I_{VLDO} = 1 A; Reduce V_{LDOIN} until V_{VLDO} drops to 2.425 V, T_A = 25°C		0.18(2)		Ω
		V_{VLDO} = 1.8 V, I_{VLDO} = 1 A; Reduce V_{LDOIN} until V_{VLDO} drops to 1.746 V, T_A = 25°C		0.16(2)		
		V_{VLDO} = 1.2 V, I_{VLDO} = 1 A; Reduce V_{LDOIN} until V_{VLDO} drops to 1.164 V, T_A = 25°C		0.15(2)		
$I_{VLDODischg}$	VLDO discharge current	ENLDO = 0 V, VLDO = 0.5 V	10	17	40	mA
OPEN DRAIN SWITCH						
$V_{ODOFFth1}$	Open drain enable threshold voltage	Turn on threshold voltage	0.698	0.716	0.735	V
		Hysteresis		38		mV
$V_{ODOFFth2}$		Second threshold voltage		1.25		V
		Hysteresis		8		mV
$T_{ODOFFth1delay}$		Turn on threshold voltage ≥ Turn off threshold voltage		32		µs
R_{OD}	Open drain resistance	T_A = 25°C; V_{OD} = 0.5 V, V_{ODOFF} = 0 V		13	50	Ω
I_{ODLEAK}	OD switch current leakage	T_A = 25°C; V_{ODOFF} = 5 V	–1		1	µA
$I_{ODOFFBIAS}$	Open drain enable bias current	T_A = 25°C; V_{ODOFF} = 5 V	–1		1	

(1) Because of the voltage drop on the contact of the test fixture, V_{LDOIN} is set at 2.5 V.
(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{V5IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOSW OUTPUT						
V_{VSWFB}	VSWFB regulation voltage	T_A = 25°C	740.2	750	759.8	mV
		T_A = 0 to 85°C (3)	738.7	750	761.3	
		T_A = -40 to 85°C (3)	738.0	750	762.0	
R_{VOSW}	Input impedance, VOSW			750		kΩ
I_{VSWFB}	Input current, VSWFB	VSWFB = 0.78 V, COMP = open		–0.04		µA
		VSWFB = 0.78 V, COMP = 5 V		–0.06		µA
$I_{VOSWDischg}$	Discharge current, VOSW	ENSW = 0 V, VOSW = 0.5 V	8	15	35	mA
TRANSCONDUCTANCE AMPLIFIER						
gm	Gain	T_A = 25°C	240	300	360	µS
$I_{COMPSNK}$	COMP maximum sink current	ENLDO=0 V, ENSW=5 V, VSWFB=0 V, VOSW=1.94 V, COMP=1.28 V		13		µA
$I_{COMPSRC}$	COMP maximum source current	ENLDO=0 V, ENSW=5 V, VSWFB=0 V, VOSW=1.66 V, COMP=1.28 V		–13		µA
V_{COMPHI}	COMP high clamp voltage	ENLDO=0 V, ENSW=5 V, VSWFB=0 V, CS=0 V, VOSW=1.66 V	1.31	1.34	1.37	V
V_{COMPLO}	COMP low clamp voltage	ENLDO=0 V, ENSW=5 V, VSWFB=0V, CS=0 V, VOSW=1.94 V	1.18	1.21	1.24	V
DUTY CONTROL						
T_{ON}	Operation on time	V_{IN} = 12 V, VOSW = 1.8 V		400		ns
T_{ON0}	Startup on time	V_{IN} = 12 V, VOSW = 0 V		125		ns
T_{ONMIN}	Minimum on time	T_A = 25°C		100		ns
T_{OFFMIN}	Minimum off time	T_A = 25°C		350		ns
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = -100 mA		3	6	Ω
		Sink, I_{DRVH} = 100 mA		0.9	3	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = -100 mA		3	6	Ω
		Sink, I_{DRVL} = 100 mA		0.9	3	
T_D	Dead time	DRVH-off to DRVL-on (3)		10		ns
		DRVL-off to DRVH-on (3)		30		
INTERNAL BST DIODE						
V_{FBST}	Forward voltage	$V_{V5IN-VBST}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBST = 34 V, LL = 28 V, VOSW = 1.87 V, T_A = 25°C		0.1	1	µA
ZERO CURRNT COMPARATOR						
V_{ZC}	Zero current comparator offset		–10	0	10	mV

(3) Ensured by design. Not production tested.

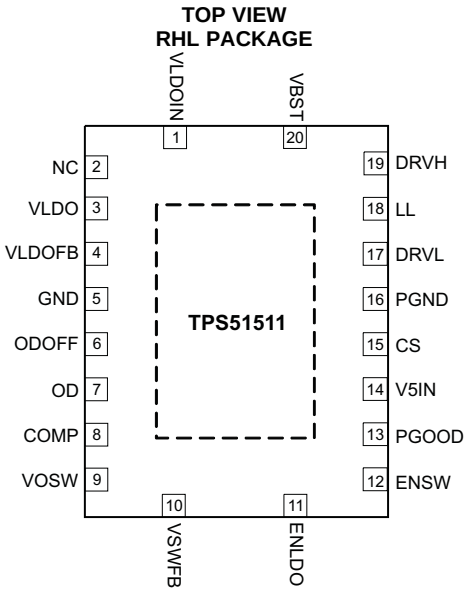
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{V5IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OCL}	Current limit threshold	$V_{PGND-CS}$ voltage, PGOOD = Hi, V_{CS} < 0.5 V	50	60	70	mV
		$V_{PGND-CS}$ voltage, PGOOD = Lo, V_{CS} < 0.5 V	20	30	40	
I_{TRIP}	CS sink current	V_{CS} > 4.5 V, PGOOD = Hi, T_A = 25°C	9	10	11	µA
		$V_{RDS(ON)CS}$ > 4.5 V, PGOOD = Lo, T_A = 25°C	4	5	6	
TC_{ITRIP}	TRIP current temperature coefficient	sense scheme, On the basis of 25°C		4500		ppm/°C
V_{OCLoff}	OCP comp. offset	($V_{V5IN-CS}$– $V_{PGND-LL}$) voltage, $V_{V5IN-CS}$ = 60 mV, V_{CS} > 4.5 V	–10	0	10	mV
V_{Rtrip}	Current limit threshold setting range	V_{5IN-CS} voltage(4)	30		150	mV
POWERGOOD COMPARATOR						
V_{TVoPG}	VOSW PG Threshold	PG out from low end	87%	90%	93%	
		PG out from high end	107%	110%	113%	
		PG hysteresis		5%		
I_{PGMAX}	PG Sink Current	VLDO = 0 V, VPGOOD = 0.5 V	2.5	7.5		mA
T_{PGDEL}	PGOOD Delay	Delay for PG in	80	130	200	µs
V_{VOSWTH}	VOSW threshold voltage for turning on PGOOD up limit and OVP feature	V_{OSW} = 1.5 V		1.36		V
	VOSW threshold hysteresis voltage for turning on PGOOD up limit and OVP feature			10		mV
UVLO/LOGIC THRESHOLD						
V_{UVV5IN}	V5IN UVLO threshold	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.15	0.225	0.3	
V_{IH}	High-level input voltage	ENLDO, ENSW	2.2			V
V_{IL}	Low-level input voltage	ENLDO, ENSW			0.3	V
V_{IHYS}	Hysteresis voltage	ENLDO, ENSW		0.2		V
I_{INLEAK}	Logic input leakage current	ENLDO, ENSW	–1		1	µA
$I_{INVSWFB}$	Input Leakage/Bias Current VSWFB -1 1		–1		1	µA
PROTECTION: UVP AND OVP						
V_{OVP}	VOSW OVP trip threshold	OVP detect	110%	115%	120%	
T_{OVPDEL}	VOSW OVP prop delay	See (4)		1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect		70%		
T_{UVPDEL}	Output UVP prop delay			32		clks
T_{UVPEN}	Output UVP enable delay			1007		clks
THERMAL SHUTDOWN						
T_{SDN}	Thermal SDN threshold	Shutdown temperature(4)		160		°C
		Hysteresis(4)		10		

(4) Ensured by design. Not production tested.

DEVICE INFORMATION



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VLDOIN	1	I	Input terminal of the LDO.
NC	2	–	Pin not used. No internal connection.
VLDO	3	O	Output terminal of the LDO. When LDO is turned off, the output capacitor is discharged by an internal FET.
VLDOFB	4	I	Feedback pin of the LDO. A voltage divider sets the LDO output voltage.
GND	5	–	Signal ground. Connect to negative terminal of the LDO output capacitor.
ODOFF	6	I	A comparator input. When this pin is tied to VLDOFB, OD acts as a PGOOD signal for the LDO. When connected to external logic, OD acts like a switch. See Table 1 for detailed information.
OD	7	I/O	The output of the multifuntional open-drain switch.
COMP	8	I/O	Output of the transconductance amplifier for phase compensation in current mode. Connect to V5IN to disable Gm amplifier and enable D-CAP mode.
VOSW	9	I/O	Switcher output voltage monitor. Input for on-time one-shot timer and advanced PGOOD masking comparator.
VSWFB	10	I	Feedback pin of the switcher. A voltage divider connected to this pin sets the switcher output voltage. A resistor connected between this pin and OD pin can be inserted in parallel with the low-side resistor of the voltage divider, according to the ODOFF input, to establish the dynamic voltage step. This terminal is also the input for the OVP, UVP and PGOOD comparators.
ENLDO	11	I	LDO-enable signal input.
ENSW	12	I	Switcher-enable signal input.
PGOOD	13	O	Power-good signal open-drain output. Pulled low when VSWFB voltage falls outside the target window comparator. The upper side of the window comparator will be masked if the VOSW volttage is lower than 1.36 V (typ.). Refer to the *Advance PGOOD Mask* section for details.
V5IN	14	I	5V Power supply input. This 5 V supplies internal control circuitry, LDO pass FET gate drive, VDRVH and VDRVL gate drivers.
CS	15	I/O	Current-sense comparator input (–) for resistor current-sense mode. If connected to 5VIN through a voltage-setting resistor, constant current sinks through this pin to set the OCL point for the $R_{DS(ON)}$ current-sense mode.
PGND	16	I/O	Ground for bottom MOSFET gate driver. Also current-sense comparator input (+).
DRVL	17	O	Rectifying (bottom) MOSFET gate-drive output.
LL	18	I/O	Switching (top) MOSFET gate driver return. Current sense comparator input (–) for $R_{DS(ON)}$ current-sense mode.
DRVH	19	O	Switching (top) MOSFET gate drive output
VBST	20	I/O	Switching (top) MOSFET driver bootstrap voltage input. Internally connected to V5IN through an PN diode.

TYPICAL CHARACTERISTICS

V5IN SUPPLY CURRENT vs TEMPERATURE

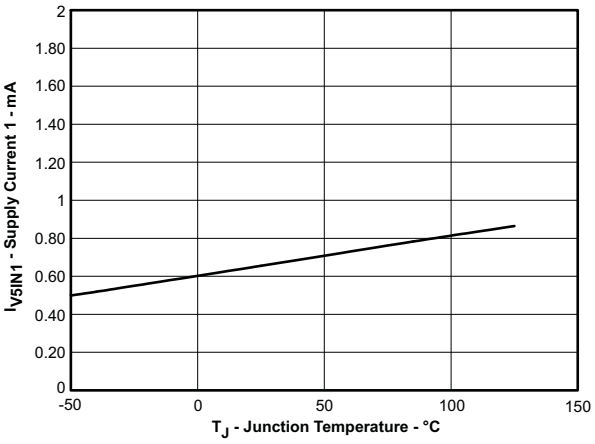


Figure 1.

V5IN SHUTDOWN CURRENT vs TEMPERATURE

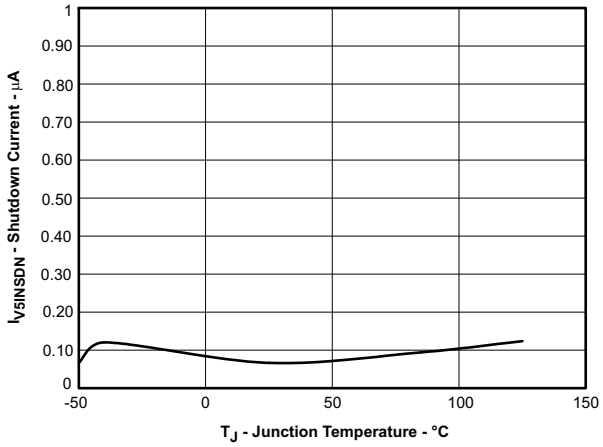


Figure 2.

VLDOIN SUPPLY CURRENT vs TEMPERATURE

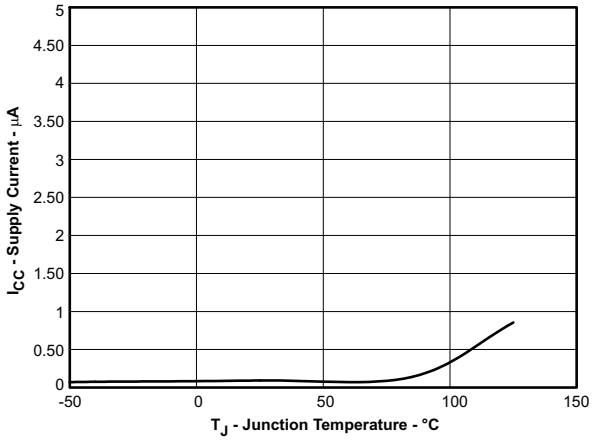


Figure 3.

CS CURRENT vs TEMPERATURE

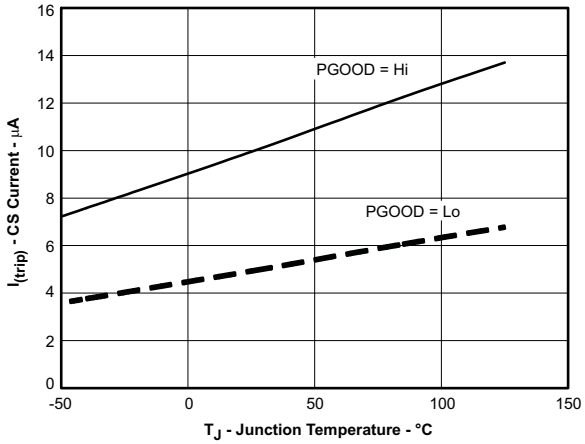


Figure 4.

VOSW DISCHARGE CURRENT vs TEMPERATURE

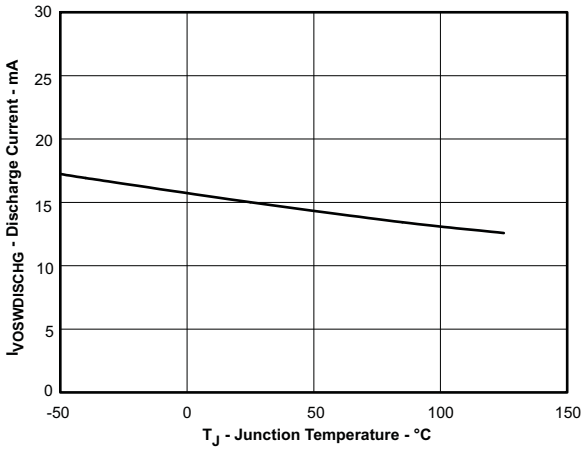


Figure 5.

VLDO DISCHARGE CURRENT vs TEMPERATURE

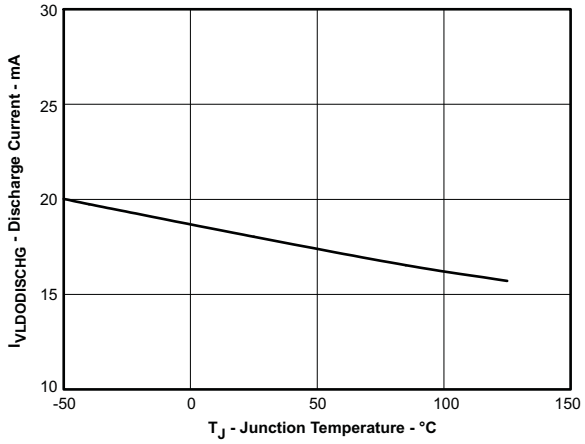


Figure 6.

TYPICAL CHARACTERISTICS (continued)

OVP, UVP THRESHOLD vs TEMPERATURE

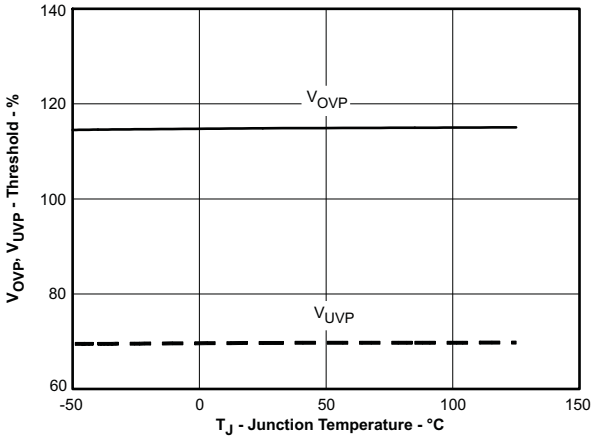


Figure 7.

SWITCHING FREQUENCY vs INPUT VOLTAGE

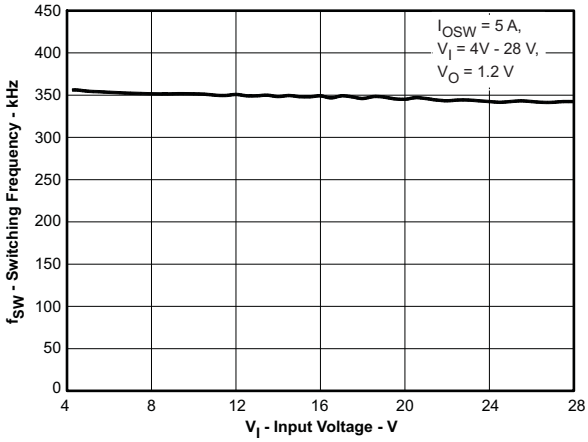


Figure 8.

SWITCHING FREQUENCY vs OUTPUT CURRENT

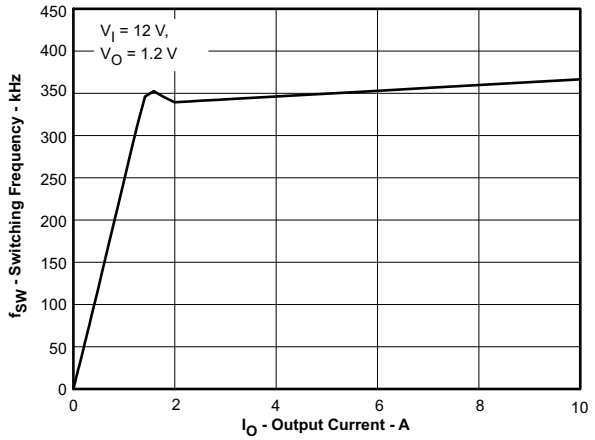


Figure 9.

VOSW LOAD REGULATION

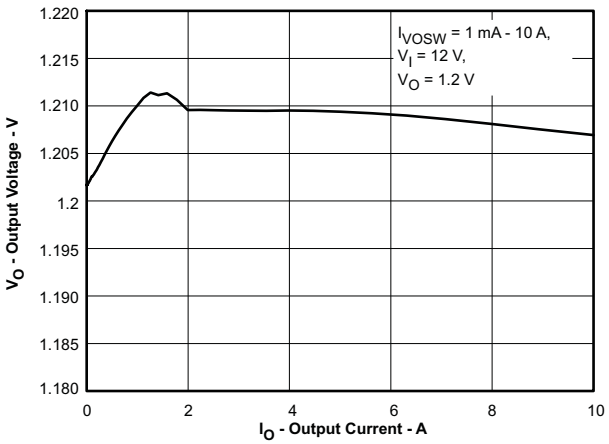


Figure 10.

VOSW LINE REGULATION

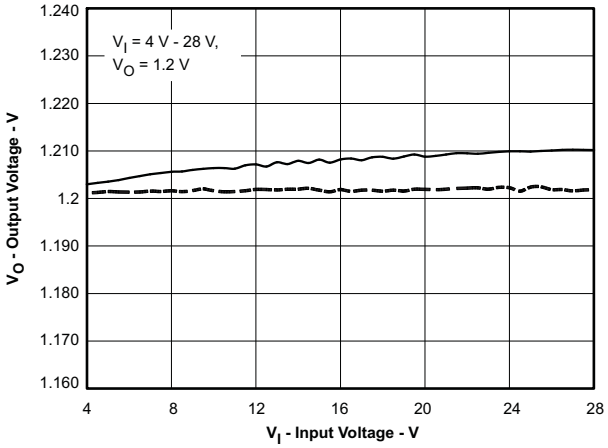


Figure 11.

LDO LOAD REGULATION AT 1.5V INPUT

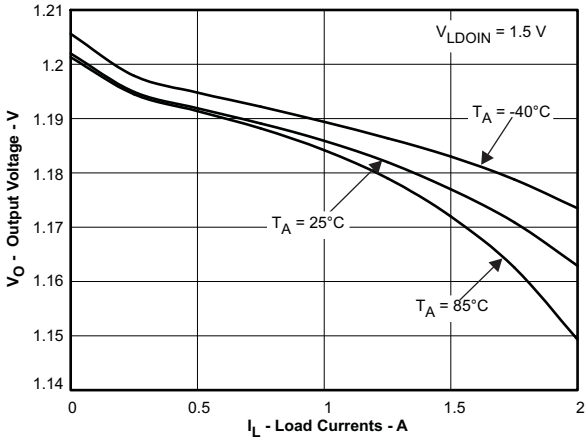


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LDO LOAD REGULATION AT 1.8V INPUT

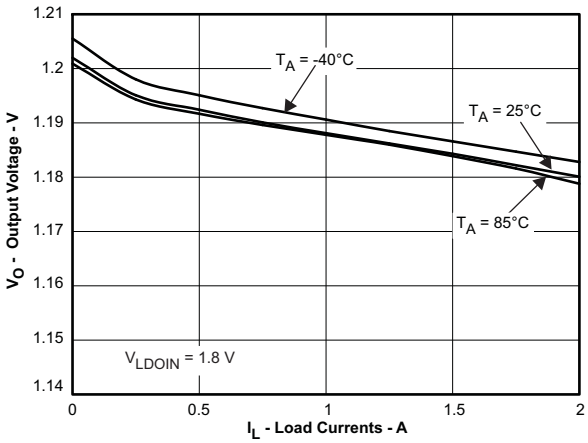


Figure 13.

VOSW EFFICIENCY

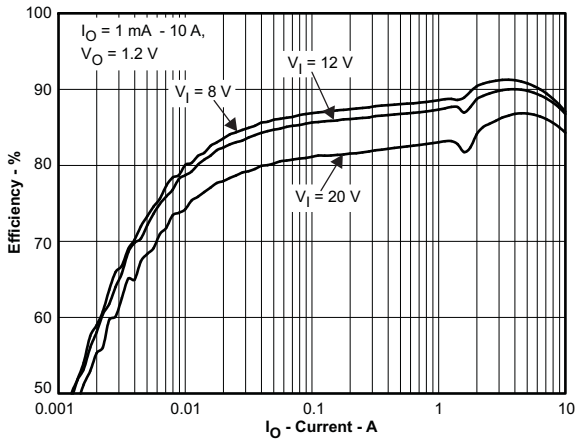


Figure 14.

RIPPLE WAVEFORMS, HEAVY LOAD CONDITION

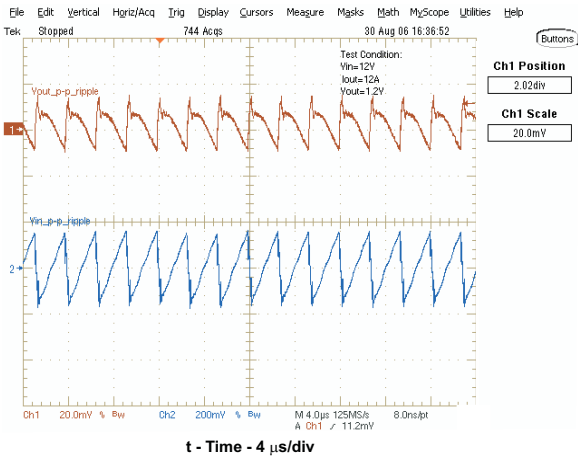


Figure 15.

VOSW LOAD TRANSIENT RESPONSE

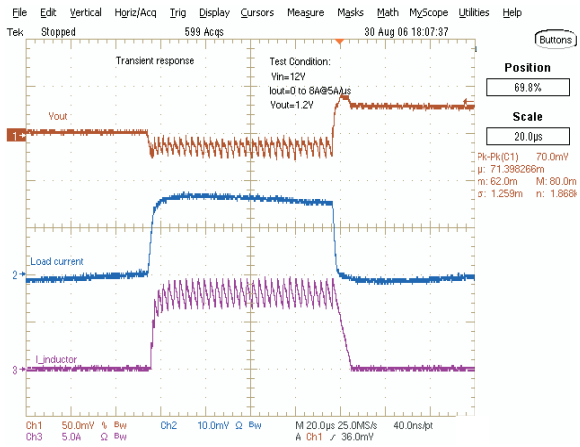


Figure 16.

VLDO LOAD TRANSIENT RESPONSE

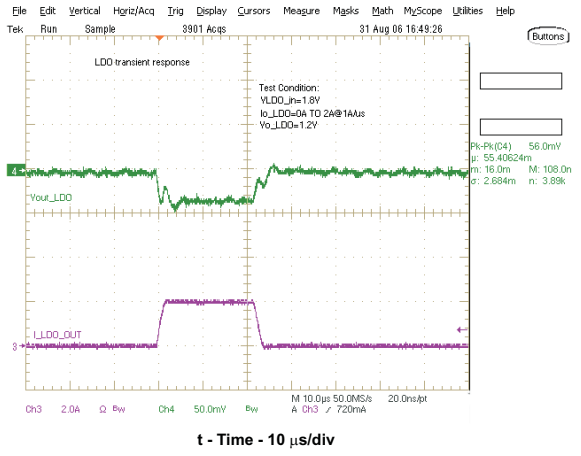


Figure 17.

VOSW START-UP WAVEFORMS

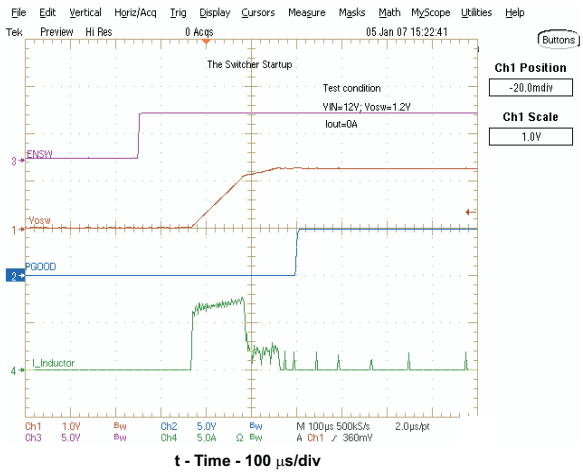


Figure 18.

TYPICAL CHARACTERISTICS (continued)

VOSW SHUT-DOWN WAVEFORMS

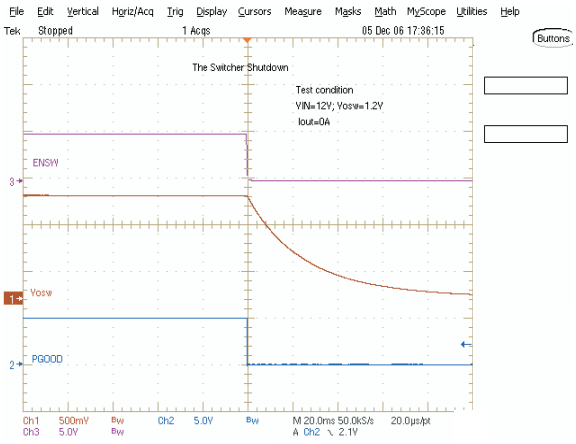


Figure 19.

VLDO START-UP WAVEFORMS

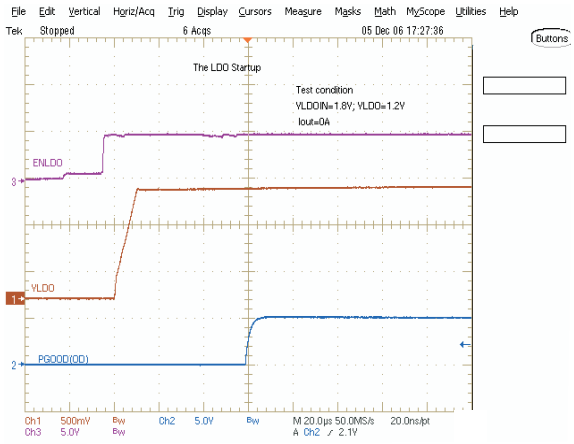


Figure 20.

VLDO SHUT-DOWN WAVEFORMS

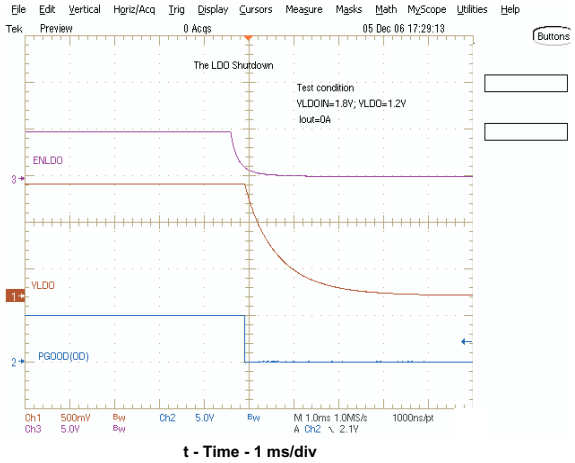


Figure 21.

VOSW BODE PLOT (CURRENT MODE)

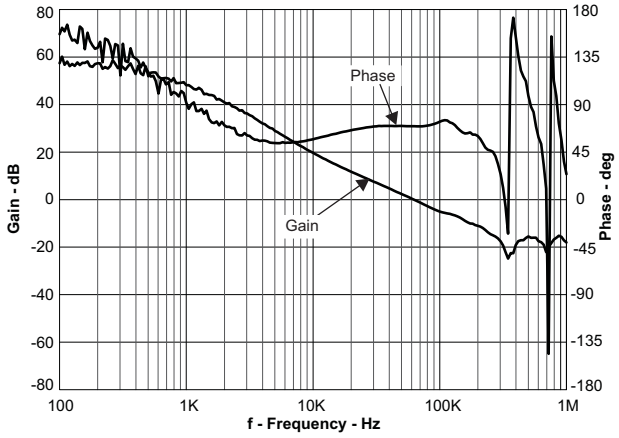


Figure 22.

DYNAMIC VOLTAGE STEP-UP WAVEFORMS

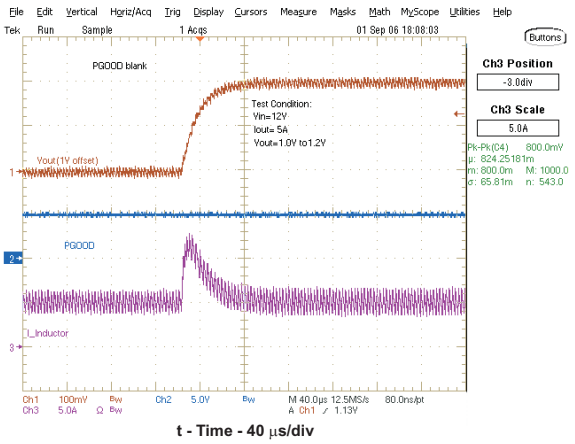


Figure 23.

DYNAMIC VOLTAGE STEP-DOWN WAVEFORMS

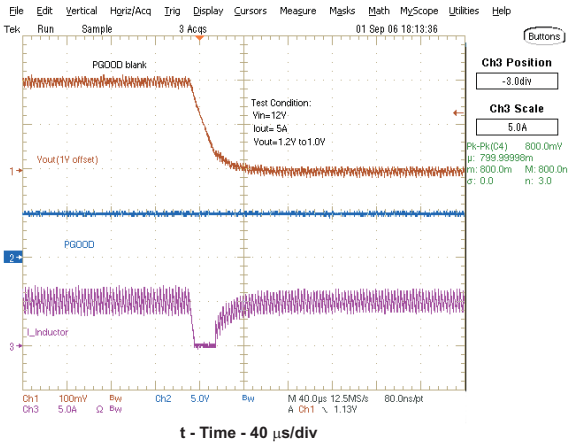
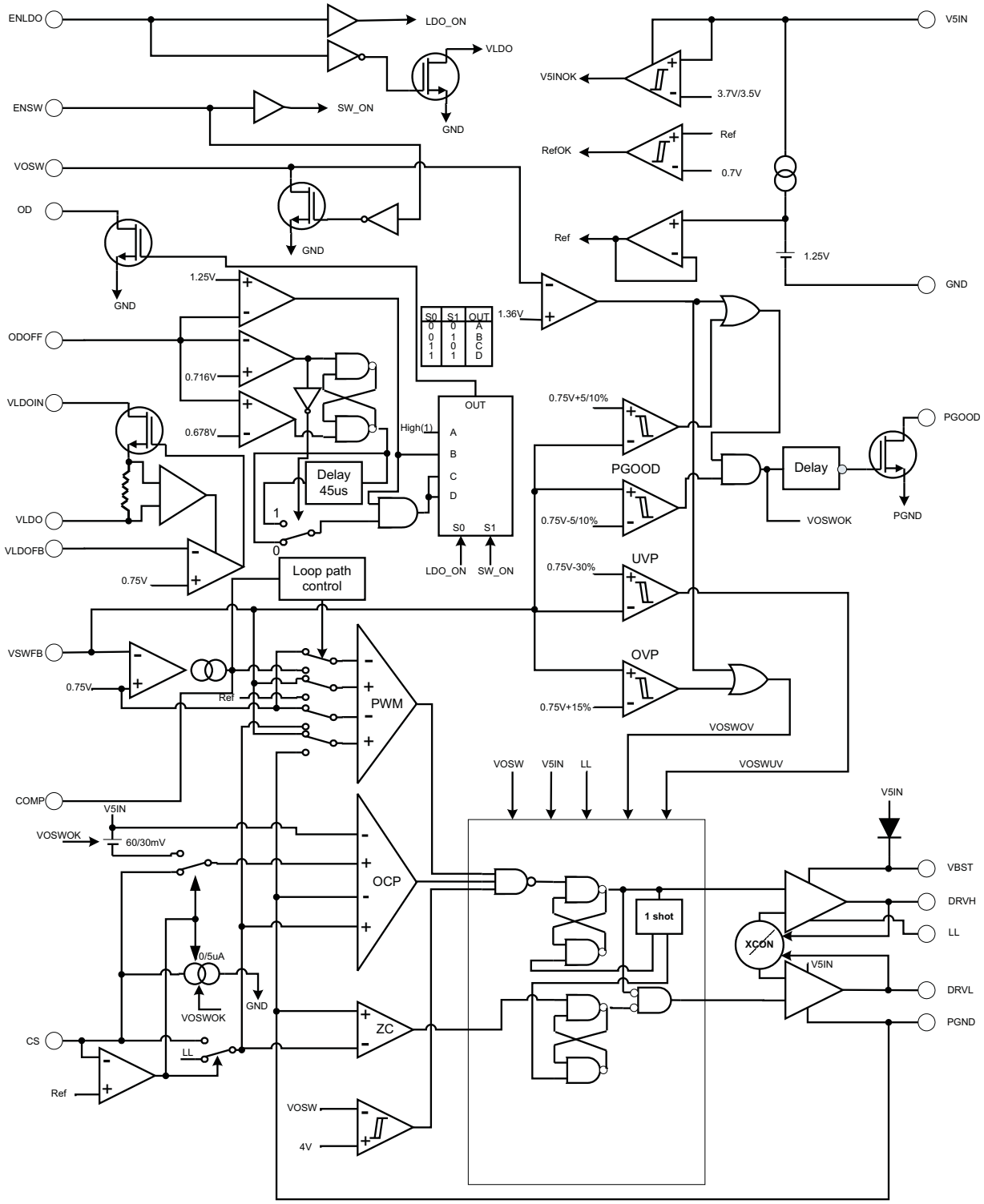


Figure 24.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

TPS51511 is an integrated power-management solution that combines a synchronous buck controller and a high-current, source-only, low-dropout linear regulator (LDO) in a small 20-pin QFN package. Each output provides voltages required by typical graphic-system applications. The switching-mode power supply portion employs external N-channel MOSFETs to provide high current for a GPU core. The output voltage is adjustable from 0.75 to 3.3 V with an external divider. The input voltage range of the switcher is 3 V to 28 V. The switcher uses adaptive on-time PWM under heavy load conditions, and automatically reduces the frequency under light loads to achieve excellent efficiency down to several mA. The output of the switcher is sensed by the VOSW pin to generate the on-time pulse, with the voltage of V_{IN} sensed by LL pin. The current sensing uses either the $R_{DS(ON)}$ of the external rectifying MOSFET for a low-cost, lossless solution, or a sense resistor placed in series to the rectifying MOSFET for applications needing a more accurate current limit.

The LDO can source up to 2 A DC current with only 20 μF (two 10 μF in parallel) ceramic output capacitors.

VOSW Switcher, Dual PWM Operation Modes

The main control loop of the switcher is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports two control schemes; a current mode and a proprietary D-CAP mode. D-CAP mode does not require an external compensation circuit, and is suitable for low external component count configurations using output capacitor(s) with an appropriate ESR value. Current-mode control has more flexibility, using an external compensation network, and can be used to achieve stable operation with very low-ESR capacitors such as ceramic capacitors.

These control modes are selected by the COMP terminal connection. If the COMP pin is connected to V5IN, the TPS51511 is in D-CAP Mode. If the COMP pin is connected to the RC compensation network, the device operates in current mode.

At the beginning of each cycle, the synchronous top MOSFET is turned on (*ON* state). This MOSFET is turned off (*OFF* state) after the internal one-shot timer expires. The on-time issued by this one-shot is proportional to the ratio of V_{OUT} to V_{IN}. In this way, the switching frequency can be kept reasonably constant over the input-voltage range, hence it is called adaptive on-time control (see PWM frequency and Adaptive On-time Control). The MOSFET is turned on again when the feedback information indicates insufficient output voltage and the inductor current is below the overcurrent limit. By repeating operation in this manner, the controller regulates the output voltage. The synchronous bottom, or the *rectifying* MOSFET, is turned on during each *OFF* state to minimize conduction loss. The rectifying MOSFET is turned off when the inductor current indicates zero voltage level. This enables seamless transition to the reduced frequency operation under light load conditions so that the high efficiency is maintained over the broad range of load currents.

In the current-mode control scheme, the transconductance amplifier generates a target current level corresponding to the voltage difference between the feedback point and the internal 750-mV reference. During the *OFF* state, the PWM comparator monitors the inductor-current signal as well as the target current level, and when the inductor-current signal goes lower than the target current level, the comparator asserts the *SET* signal, switching the system to the *ON* state. The voltage-feedback gain is adjustable outside the controller IC to support various types of output MOSFETs and capacitors. In the D-CAP Mode, the transconductance amplifier is disabled and the PWM comparator directly compares the feedback-point voltage to the internal 750-mV reference during the *OFF* state. When the feedback point becomes lower than the reference voltage, the comparator asserts the *SET* signal, triggering the *ON* state.

VOSW Switcher, Light Load Condition

TPS51511 automatically reduces the switching frequency under light load conditions to maintain high efficiency. This frequency reduction is achieved smoothly and without increasing the V_{OUT} ripple or affecting the load regulation.

As the output current decreases from a heavy load condition, the inductor current is also reduced and eventually comes to the point that its ripple-valley value decreases down to zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET will be turned off when this zero inductor current is detected. As the load current decreases further, the converter runs in discontinuous-conduction mode, and takes longer to discharge the output capacitor to the level that will issue the next *ON* cycle. The ON time is kept the same as that in the heavy load condition. Conversely, when the output current increases from a light load to a heavy load, the switching frequency increases to the constant 350 kHz as the inductor current reaches continuous conduction. The transition point between light and heavy-load operation $I_{OUT(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as follows;

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \quad (1)$$

Where f is the PWM switching frequency, 350 kHz.

The switching frequency versus the output current in the light load condition is a function of L, f, V_{IN} and V_{OUT}, but it decreases almost proportionally to the output current from the $I_{OUT(LL)}$ given above. For example, it will be 35 kHz at $I_{OUT(LL)}$/10 and 3.5 kHz at $I_{OUT(LL)}$/100.

Low-Side Driver

The low-side driver is designed to drive high current low $R_{DS(ON)}$ N-channel MOSFETs. The drive capability is represented by its internal resistance, 3 Ω for V5IN to DRVL, and 0.9 Ω for DRVL to PGND. A dead time to prevent shoot-through is internally generated between the top MOSFET off to bottom MOSFET on, and bottom MOSFET off to top MOSFET on. The 5-V bias voltage is delivered from V5IN supply.

The instantaneous drive current is supplied by an input capacitor connected between V5IN and GND. Add a ceramic capacitor with a value between 1.0 µF and 4.7 µF placed close to the V5IN pin to stabilize the 5-V output from any parasitic impedance from the supply. The average drive current is equal to the gate charge at V_{GS}=5 V condition, times the switching frequency. This gate-drive current as well as the high-side gate-drive current times 5 V accounts for the power that must be dissipated from the TPS51511 package.

High-Side Driver

The high-side driver is designed to drive high-current, low $R_{DS(ON)}$ N-channel MOSFET(s). It is configured as a floating driver, with the 5-V bias voltage delivered from the V5IN supply. The average drive current is also calculated by the gate charge at V_{GS}=5 V condition, times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBST and LL pins. The drive capability is represented by its internal resistance, 3 Ω for VBST to DRVH, and 0.9 Ω for DRVH to LL.

Current Sensing Scheme

To support both high-accuracy and low-cost current sensing applications, TPS51511 supports two different current sensing schemes; external-resistor sensing, and rectifying-MOSFET $R_{DS(ON)}$ sensing.

In the resistor-sensing scheme, an appropriate current-sensing resistor is connected between the source terminal of the rectifying MOSFET and PGND, and the CS pin is connected to the rectifying MOSFET source terminal node. The inductor current is monitored by the voltage between PGND pin and CS pin.

In the $R_{DS(ON)}$-sensing scheme, the CS pin is connected to the V5IN pin through the trip-voltage setting resistor R_{TRIP}. In this case, the CS terminal sinks the 10-µA I_{TRIP} current, and the trip level is set to the voltage across R_{TRIP}. The inductor current is monitored by the voltage between the PGND pin and the LL pin, so the LL pin is connected to the drain terminal of the rectifying MOSFET. I_{TRIP} has a 4500-ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$.

In either scheme, PGND is used as the positive current-sensing node, so PGND must be connected to the proper current-sensing device, i.e., the sense resistor or the source terminal of the rectifying MOSFET.

PWM Frequency and Adaptive On-Time Control

TPS51511 employs an adaptive on-time control scheme, and does not have a dedicated oscillator on board. However, the device runs with a fixed 350kHz pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage so that the duty-cycle ratio is kept the same as V_{OUT}/V_{IN} in the same cycle time. Although the TPS51511 does not have a pin connected to V_{IN}, the input voltage is monitored at the LL pin during the *ON* state. This reduces the pin count in order to make the part compact without sacrificing its performance. In order to secure minimum *ON* time during startup, the feed-forward feature from the output voltage is enabled after the output voltage becomes 750 mV or higher.

Soft-Start and Powergood (PGOOD)

The soft-start function of the switcher is achieved by ramping up the reference voltage and a two-stage current clamp. At the starting point, the reference voltage is set to 650 mV (87% of its target value), and the overcurrent threshold is set to half of the nominal value. When the UVP comparator detects an VOSW voltage greater than 80% of the target, the reference begins to ramp up and reaches 750 mV after 85 µs. 45 µs after the voltage becomes *good*, the power-good comparator releases the overcurrent threshold to the nominal value. TPS51511 turns off the power-good open-drain MOSFET when VOSW reaches the good state.

The soft-start function of the LDO is achieved by clamping the current during startup. The threshold of the current limit is set to 2.5 A (typical). TPS51511 has an independent window comparator for each output, but the PGOOD signal indicates only the status of VOSW. If a separate powergood signal is needed for the LDO, see *OD and ODOFF* for configuration details.

The soft-start durations, T_{VOSW}, T_{VLDO} are functions of output capacitances.

$$T_{VOSW} = \frac{2 \times C_{VOSW} \times V_{VOSW}}{I_{VOSWOCP}} + 80\ \mu s \tag{2}$$

Where, $I_{VOSWOCP}$ is the current limit value for the VOSW switcher calculated by Equation 5.

$$T_{VLDO} = \frac{C_{VLDO} \times V_{VLDO}}{I_{VLDOOCL}} \tag{3}$$

Where, $I_{VLDOOCL}$ = 2.5 A (typical).

In both equations, no load current during startup is assumed. Note that both the switcher and the LDO do not start up to target voltage with full load conditions.

Enable and Discharge

Both the switcher and LDO can be enabled by bringing the voltage on the ENSW and ENLDO pins above 2.2 V, and disabled by pulling the voltage of ENSW and ENLDO down to 0.3 V. Both the switcher and LDO have output-discharge feature. The output is discharged through an internal MOSFET when the channel is disabled. Discharge continues until the output voltage is discharged below 0.3 V. In UVP or OVP conditions of the switching power supply, the device is latched off and the discharge is enabled until the output voltage drops below 0.3 V.

Current Protection for VOSW

The switcher has cycle-by-cycle current-limit control. The inductor current is monitored during the *OFF* state, and the controller keeps the *OFF* state while the inductor current is larger than the overcurrent trip level. The trip level and current-sense scheme are determined by the CS pin connection (see *Current Sensing Scheme*). In the resistor sensing scheme, the trip level, V_{TRIP}, is a fixed value of 60 mV. In the $R_{DS(ON)}$ sensing scheme, the CS terminal sinks 10 μA and the trip level is set to the voltage across the R_{TRIP} resistor.

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times 10(\mu A) \quad (4)$$

Because the comparison is done during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{ocp}, can be calculated as follows;

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{TRIP}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (5)$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall. If the output voltage becomes less than power-good level, the V_{TRIP} level is cut in half, and the output voltage tends to be even lower. Eventually, it will end up crossing the undervoltage-protection threshold and be shut down.

Over/Under Voltage Protection for VOSW

The TPS51511 monitors the feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high, and the circuit latches the top MOSFET driver OFF and the bottom MOSFET driver ON. The TPS51511 also monitors the VOSW voltage directly, and if it becomes greater than 4 V, TPS51511 turns off the top MOSFET driver. When the feedback voltage becomes lower than 70% of the target voltage, the UVP-comparator output goes high, and an internal UVP delay counter starts. After 32 switching cycles, the TPS51511 latches OFF both top and bottom MOSFETs. This function is enabled after 1007 cycles from switcher startup to ensure proper startup.

V5IN UVLO Protection

TPS51511 has V5IN under voltage lock out protection (UVLO). When the V5IN voltage is lower than the UVLO threshold voltage, the switcher and LDO are shut off. This is a non-latching protection.

LDO Operation

The TPS51511 integrated LDO is a source-only 2- A LDO. It has a typical current limit of 2.5 A . It can be separately enabled via the ENLDO pin, and the output voltage is set via the external voltage divider. Only a 20 μF ceramic capacitor (2×10μF) is needed for this LDO. The transient response is very fast due to the wide bandwidth design of the LDO feedback loop.

The LDO has an internally fixed constant overcurrent limit of 2.5 A. This is a trailing current limit with no shutdown function.

Thermal Shutdown

The TPS51511 monitors its internal temperature. If the temperature exceeds the threshold value (typically 160°C), the switcher and LDO are shut off. This is a non-latching protection, and operation is resumed when the device is cooled down by approximately 10°C.

Dynamic Voltage Step, OD and ODOFF

OD and ODOFF are multifunction pins. By connecting the OD pin through a resistor to VSWFB, ODOFF is connected to an external control logic signal which can control OD to switch in and out this resistor in parallel with the bottom resistor of the voltage divider. This can dynamically change the switcher output voltage during operation. If the application requires a power-good signal for the LDO rather than switcher dynamic voltage control, OD and ODOFF can be configured to support the LDO power-good feature by connecting ODOFF to VLDOFB. In this mode, connect OD through a pullup resistor to the bias voltage (i.e. 5 V, 3.3 V) to act as the LDO power-good output. The functions of ODOFF and OD pin combinations related to the ENLDO and ENSW pin voltage levels are shown in Table 1.

Table 1. OD and ODOFF Functions

ENLDO	ENSW	ODOFF(1)	OD(2)	Applications(3)
Hi	X	> 1.25 V	Off	D
		0.716 V < ODOFF < 1.25 V and lasts longer than 45 µs	Off	D&G
		0.716 V < ODOFF < 1.25 V and lasts less than 45 µs	Keep State	G
		0.678 V < ODOFF < 0.716 V	Keep State	G
		< 0.678 V	On	D&G
Lo	Hi	> 1.25 V	Off	D
		< 1.25 V	On	D&G
Lo	Lo	X	On	G

(1) All voltages are typical values.
(2) "Keep state" means no state change with previous state, “On” means open drain MOSFET is turned on and OD is connected to ground through this MOSFET. “Off” means open drain MOSFET off.
(3) “D” stands for dynamic voltage change “G” stands for LDO PGOOD .

Advanced PGOOD Mask

The advanced PGOOD mask feature allows the switcher to dynamically change the output voltage while maintaining the PGOOD and OVP functions during the transition.

During the dynamic voltage change, if the output voltage is lower than 1.36 V (typ) the high-end PGOOD comparator and OVP comparator is masked. If the output voltage is set equal to or higher than 1.36 V (typ), the blanking circuit is disabled, and the high-end PGOOD threshold is set to 110%, and the OVP threshold is set to 115% of the output-voltage setting . When dynamic voltage change is implemented, a 1-nF ceramic capacitor must be added in parallel with the top resistor of the voltage divider as shown in Figure 27.

APPLICATION INFORMATION

LOOP COMPENSATION AND EXTERNAL PARTS SELECTION

Current Mode Operation

A buck converter using TPS51511 current mode operation can be partitioned into three portions, a voltage divider, an error amplifier and a switching modulator. By linearizing the switching modulator, we can derive the transfer function of the whole system. Since the current-mode scheme directly controls the inductor current, the modulator can be linearized as shown in Figure 25.

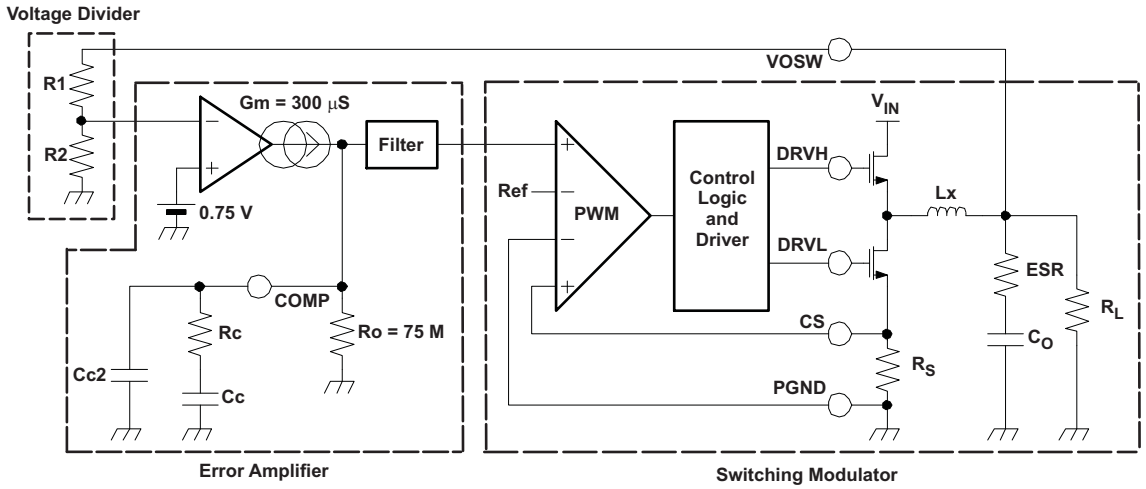


Figure 25. Simplified Current-Mode Functional Blocks

In this representation, the inductor is located inside the local feedback loop, and its inductance does not appear in the small-signal model. As a result, a modulated current source including the power inductor can be modeled

APPLICATION INFORMATION (continued)

as a current source with its transconductance of 1/Rs, and the output capacitor represents the modulator portion. This simplified model is applicable in the frequency space up to approximately half the switching frequency. Although the inductance has no influence in the small-signal model, it influences the large-signal model by limiting the slew rate of the current source. This means that the buck converter's load-transient response, one of the large signal behaviors, can be improved by using a smaller inductance without affecting loop stability.

The total open-loop transfer function of the whole system is given by

$$H(s) = H_1(s) \times H_2(s) \times H_3(s) \quad (6)$$

Assuming RL>>ESR, Ro>>Rc and Cc>>Cc2, the transfer function of each block is

$$H_1(s) = \frac{R_2}{(R_2 + R_1)} \quad (7)$$

$$H_2(s) = -Gm \times \frac{Ro(1 + s \times Cc \times Rc)}{(1 + s \times Cc \times Ro)(1 + s \times Cc2 \times Rc)} \quad (8)$$

$$H_3(s) = \frac{1 + s \times Co \times ESR}{1 + s \times Co \times RL} \times \frac{RL}{Rs} \quad (9)$$

There are three poles and two zeros in H(s). Each pole and zero is given by

$\omega_{p1} = 1/(Cc \times Ro)$ $\omega_{p2} = 1/(Co \times RL)$ $\omega_{p1} = 1/(Cc2 \times Rc)$

$\omega_{z1} = 1/(Cc \times Rc)$ $\omega_{z2} = 1/(Co \times ESR)$

Usually, each frequency of the poles and zeros is lower than the 0dB frequency, f_0. However, the f_0 should be kept under 1/3 of the switching frequency to avoid the effect of switching-circuit delay. The f_0 is given by Equation 10.

$$f_o = \frac{1}{2\pi} \times \frac{R_1}{R_1 + R_2} \times \frac{Gm}{Co} \times \frac{Rc}{Rs} = \frac{1}{2\pi} \times \frac{0.75}{Vout} \times \frac{Gm}{Co} \times \frac{Rc}{Rs} \quad (10)$$

Based on the small-signal analysis above, the external components can be selected by the following steps:

1. **Choose the inductor.**

The inductance value should be determined to give a ripple current of approximately 1/4 to 1/3 of the maximum output current.

$$L = \frac{1}{I_{IND(ripple)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (11)$$

The inductor also needs low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as follows.

$$I_{IND(peak)} = \frac{V_{trip}}{R_{DS(ON)}} + \frac{1}{L \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} \quad (12)$$

2. **Choose the rectifying (bottom) MOSFET.**

When the $R_{DS(ON)}$ sensing scheme is selected, the rectifying MOSFET's on-resistance is used as this Rs so that lower $R_{DS(ON)}$ does not always promise better performance. In order to clearly detect inductor current, minimum Rs recommended is to give 15 mV or larger ripple voltage with the inductor ripple current. This will provide smooth transitions from CCM to DCM or vice versa. The upper side of the $R_{DS(ON)}$ is of course restricted by the efficiency requirement, and usually this resistance affects efficiency more at high load conditions.

When using external-resistor current sensing, there is no restriction for low $R_{DS(ON)}$. However, the current sensing resistance Rs itself affects the efficiency.

3. **Choose the output capacitor(s).**

When using organic semiconductor capacitors (OS-CON) or specialty polymer capacitors (SP-CAP), the ESR

APPLICATION INFORMATION (continued)

to achieve required ripple value at stable state or transient load conditions will determine the number and size of capacitor(s) needed, and the resulting capacitance will then be enough to satisfy stable operation. The peak-to-peak ripple value can be estimated by ESR times the inductor ripple current for stable state, or ESR times the load-current step for a fast transient-load response.
Ceramic capacitors typically have ESR values small enough to meet the ripple requirement. On the other hand, transient undershoot and overshoot driven by output capacitance will become the key factor to determine the capacitance.

4. **Determine f_0 and calculate Rc** using Equation 13.

$$Rc \le 2\pi \times f_0 \times \frac{Vout}{0.75} \times \frac{Co}{Gm} \times Rs \quad (13)$$

Note that higher Rc shows faster transient response at the cost of instability. If the transient response is not enough even with a high Rc value, try increasing the output capacitance. Recommended f_0 is fosc/4. Then Rc can be derived by the next simplified equation.

$$Rc = 2.4 \times Vout \times Co[\mu F] \times Rs[m\Omega] \quad (14)$$

5. **Calculate Cc2.** The purpose of this capacitance is to cancel the zero caused by the output capacitor ESR. If ceramic capacitors are used, there is no need for Cc2.

$$\omega_{z2} = \frac{1}{(Co \times ESR)} = \omega_{p3} = \frac{1}{(Cc2 \times Rc)} \quad (15)$$

$$Cc2 = Co \times \frac{ESR}{Rc} \quad (16)$$

6. **Calculate Cc.** The purpose of Cc is to cut the DC component to obtain a high DC-feedback gain. However, because this causes phase delay, another zero to cancel this effect at f_0 frequency is needed. This zero, ω_{z1}, is determined by Cc and Rc. Recommended ω_{z1} is 10 times lower than the f_0 frequency.

$$f_{z1} = \frac{1}{2\pi \times Cc \times Rc} = \frac{f_0}{10} \quad (17)$$

$$Cc = \frac{10}{2\pi \times Rc \times f_0} \cong \frac{18}{Rc[k\Omega]} [nF] \quad (18)$$

7. **Determine the value of R1 and R2.** Recommended R2 value is from 10 kΩ to 100 kΩ. Determine R1 using Equation 19.

$$R_1 = \frac{Vout - 0.75}{0.75} \times R_2 \quad (19)$$

D-CAP™ Mode Operation

A buck converter system using D-CAP mode can be simplified as shown in Figure 26.

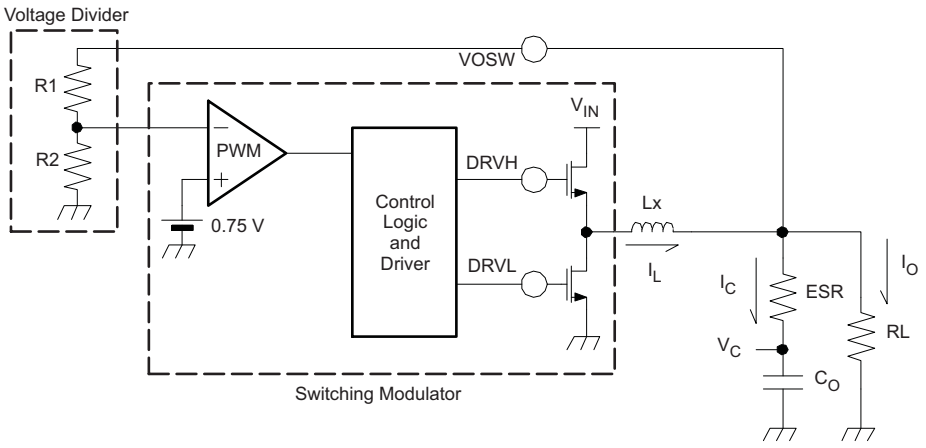


Figure 26. Simplified D-CAP Mode Buck Converter Functional Blocks

APPLICATION INFORMATION (continued)

The VOSW voltage is compared with the internal reference voltage from the divider resistors. The PWM comparator determines the timing to turn on the top MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increases.

To ensure loop stability, the 0dB frequency, f_0, defined below, should be lower than 1/3 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times Co} \leq \frac{f_{sw}}{3} \tag{20}$$

Because f_0 is determined solely by the output capacitor's characteristics, the loop stability of D-CAP Mode is determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have Co in the order of several-hundred µF and ESR values in the range of 10 mΩ. These will make f_0 approximately 100 kHz or less, and the loop will be stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this mode.

D-CAP mode provides many advantages such as ease-of-use, minimum external component count and extremely short response time. However, because it does not employ an error amplifier in the loop, a sufficient amount of feedback signal must be provided by the external circuit to reduce jitter level. A good layout which follows the layout considerations in this data sheet also can reduce the jitter level.

Components selection is much simpler in D-CAP mode.

1. Choose inductor.

   This section is the same as the current mode. Refer to the instructions in the *Current Mode Section*.

2. Choose output capacitor(s).

   Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

Thermal Design

The primary power dissipation of TPS51511 is generated from the LDO. The potential difference between VLDOIN and VLDO times LDO current gives the power dissipation, W_{DSRC},

$$W_{DSRC} = \left(V_{VLDOIN} - V_{VLDO}\right) \times I_{VLDO} \tag{21}$$

Another power consideration is the current used for internal control circuitry from the V5IN supply. V5IN supports both the internal circuitry and the external MOSFET drive current.

These powers need to be effectively dissipated from the package. Maximum power dissipation allowed to the package is calculated by,

$$V_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}} \tag{22}$$

Where:

$T_{J(max)}$ is 125°C
$T_{A(max)}$ is the maximum ambient temperature in the system
θ_{JA} is the thermal resistance from the silicon junction to the ambient

This thermal resistance strongly depends on the board layout. TPS51511 is assembled in a thermally enhanced PowerPAD package that has an exposed die pad underneath the body. For maximum thermal performance, this die pad must be attached to a ground trace via a thermal land on the PCB. This ground trace acts as a heat sink. The typical thermal resistance, 53.3°C/W, is achieved based on a 3,05 mm × 2,05 mm thermal land with 6 vias without air flow. It can be improved by using a larger thermal land and/or increasing the number of vias. Further information about PowerPAD™ and its recommended board layout is described in a Texas Instruments document, SLMA002. This document is available at www.TI.com.

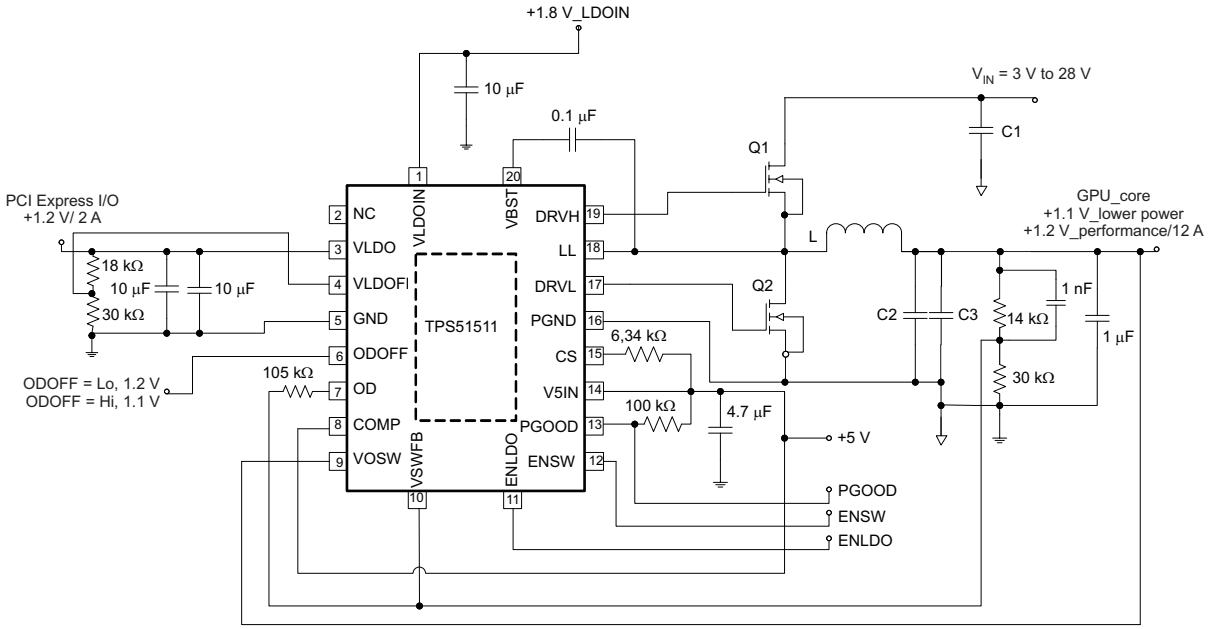
APPLICATION INFORMATION (continued)

Layout Considerations

Below are some points to be considered before the layout of TPS51511 design begins.

- The PCB trace defined as LL node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET, and the high voltage side of the inductor, should be as short and wide as possible.
- Consider adding a small snubber circuit consisting of a 3-Ωresistor and 1-nF capacitor between LL and PGND if a high frequency surge is observed on the LL voltage waveform.
- V5IN input capacitor, 1 µF - 4.7 µF, should be placed near the V5IN pin, within 0.1" (2,5 mm), if possible.
- All sensitive analog traces such as VOSW, VSWFB,VLDOFB and CS should be placed away from high-voltage switching nodes such as LL, DRVL or DRVH nodes to avoid coupling.
- An input bypass capacitor should be placed to VLDOIN as close as possible with short and wide connection.
- The output capacitor for VLDO should be placed close to the pin with short and wide connections in order to avoid additional ESR and/or ESL of the trace.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Using a wide trace for the component-side copper, connected to this thermal land, will help heat dissipation. Numerous vias of 0,33 mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation. Do NOT connect PGND to this thermal land underneath the package.

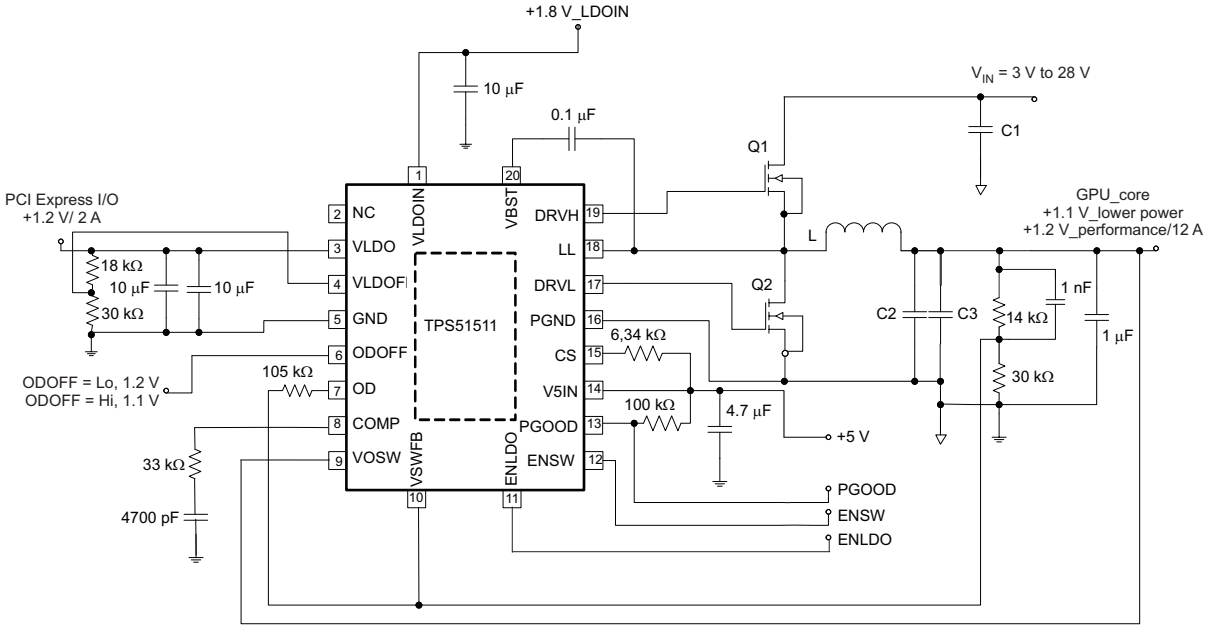
APPLICATION CIRCUITS



Symbol	Specification	Manufacturer	Part Number
L	1 µH	Vishay	IHLP5050
C1	3X10 µF	TDK	C3225X5R1E106M
C2	330 µF	Sanyo	2R5TPE330MC
C3	330 µF	Sanyo	2R5TPE330MC
Q1	30 V, 13 mΩ	IR	IRF7821
Q2	30 V, 5 mΩ	IR	IRF7832

Figure 27. D-CAP Mode, $R_{DS(ON)}$ Sensing, 1-Bit DAC for the Output Voltage Dynamic Change

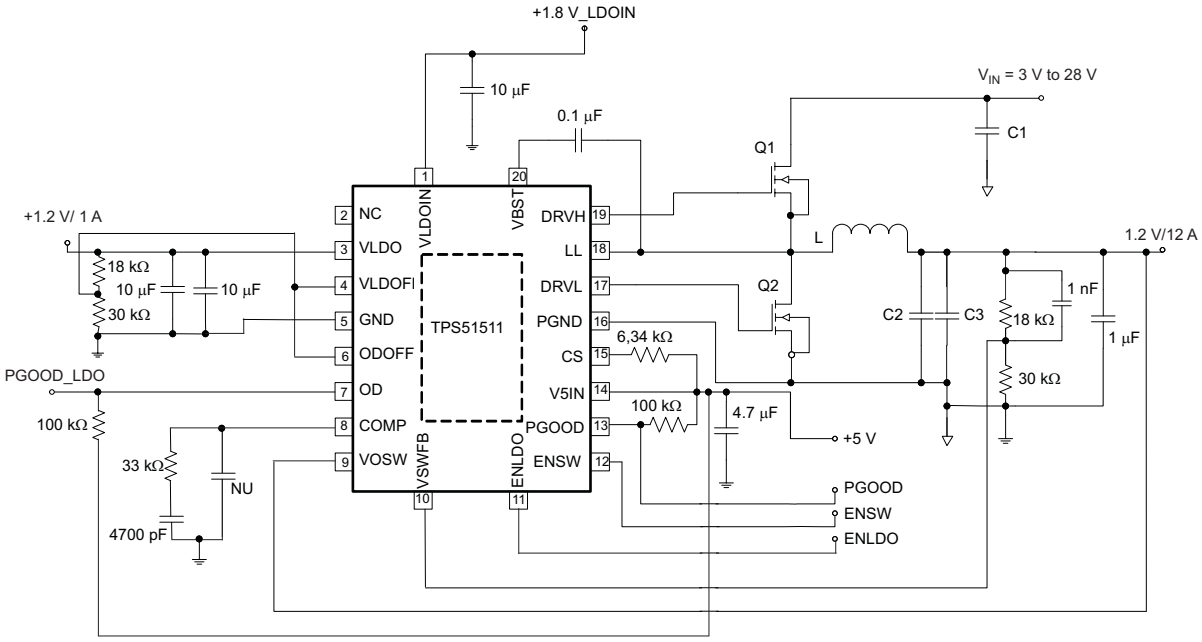
APPLICATION INFORMATION (continued)



Symbol	Specification	Manufacturer	Part Number
L	1 µH	Vishay	IHLP5050
C1	3X10 µF	TDK	C3225X5R1E106M
C2	47 µF	TDK	C3225X5R0J476K
C3	47 µF	TDK	C3225X5R0J476K
Q1	30 V, 13 mΩ	IR	IRF7821
Q2	30 V, 5 mΩ	IR	IRF7832

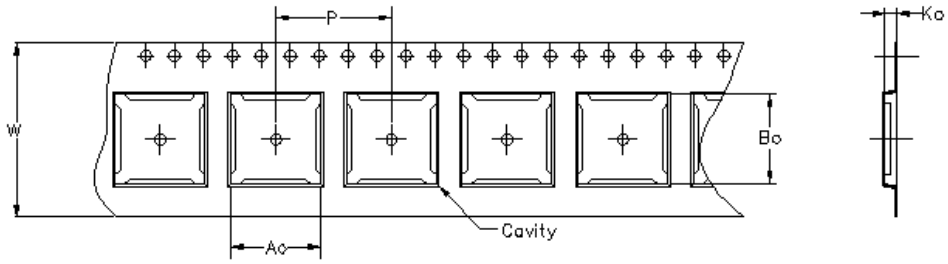
Figure 28. Current Mode, $R_{DS(ON)}$ Sensing, 1-Bit DAC for the Output Voltage Dynamic Change

APPLICATION INFORMATION (continued)



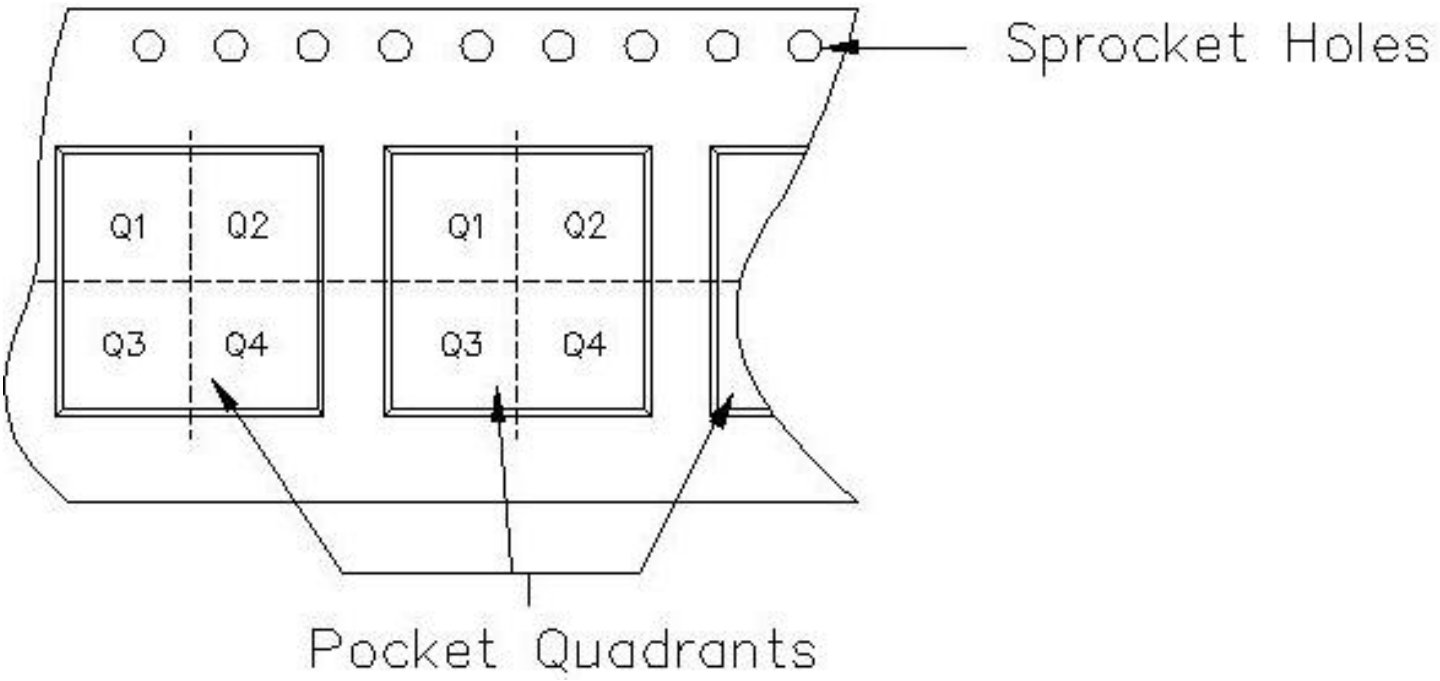
Symbol	Specification	Manufacturer	Part Number
L	1 µH	Vishay	IHLP5050
C1	3X10 µF	TDK	C3225X5R1E106M
C2	47 µF	TDK	C3225X5R0J476K
C3	47 µF	TDK	C3225X5R0J476K
Q1	30 V, 13 mΩ	IR	IRF7821
Q2	30 V, 5 mΩ	IR	IRF7832

Figure 29. Current Mode Single Switcher, OD and ODOFF Configure to Second PGOOD for LDO



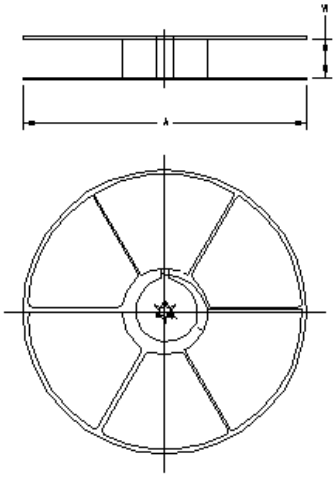
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



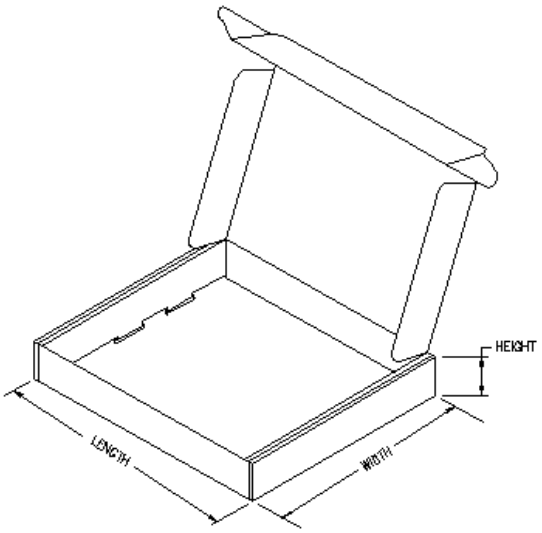
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51511RHLR	RHL	20	MLA	330	12	3.8	4.8	1.6	8	12	PKGORNT1TR-MSP
TPS51511RHLT	RHL	20	MLA	180	12	3.8	4.8	1.6	8	12	PKGORNT1TR-MSP

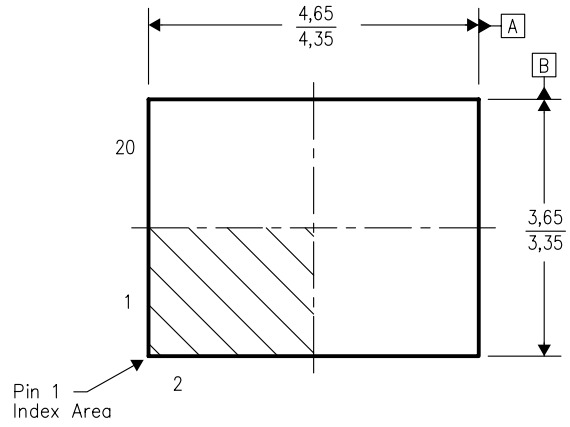


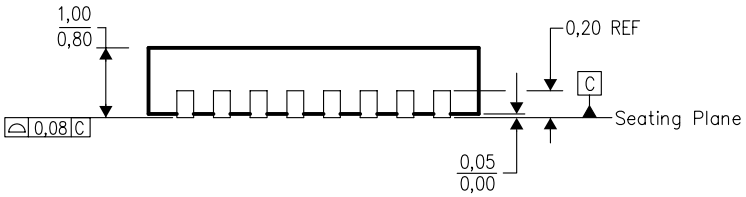
TAPE AND REEL BOX INFORMATION

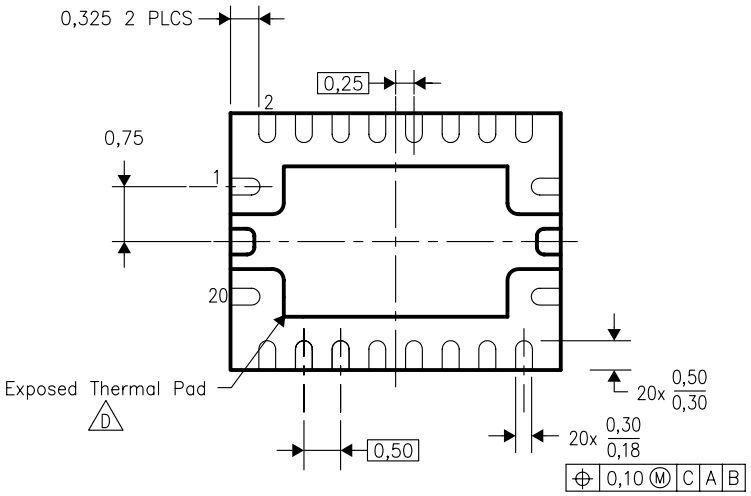
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS51511RHLR	RHL	20	MLA	346.0	346.0	29.0
TPS51511RHLT	RHL	20	MLA	190.0	212.7	31.75


HEIGHT
LENGTH
WIDTH

RHL (R–PQFP–N20) PLASTIC QUAD FLATPACK







4205346–2/C 12/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

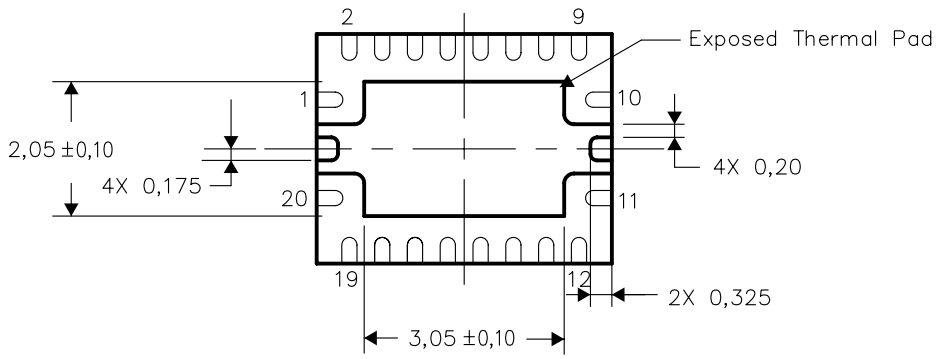
RHL (R–PQFP–N20)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

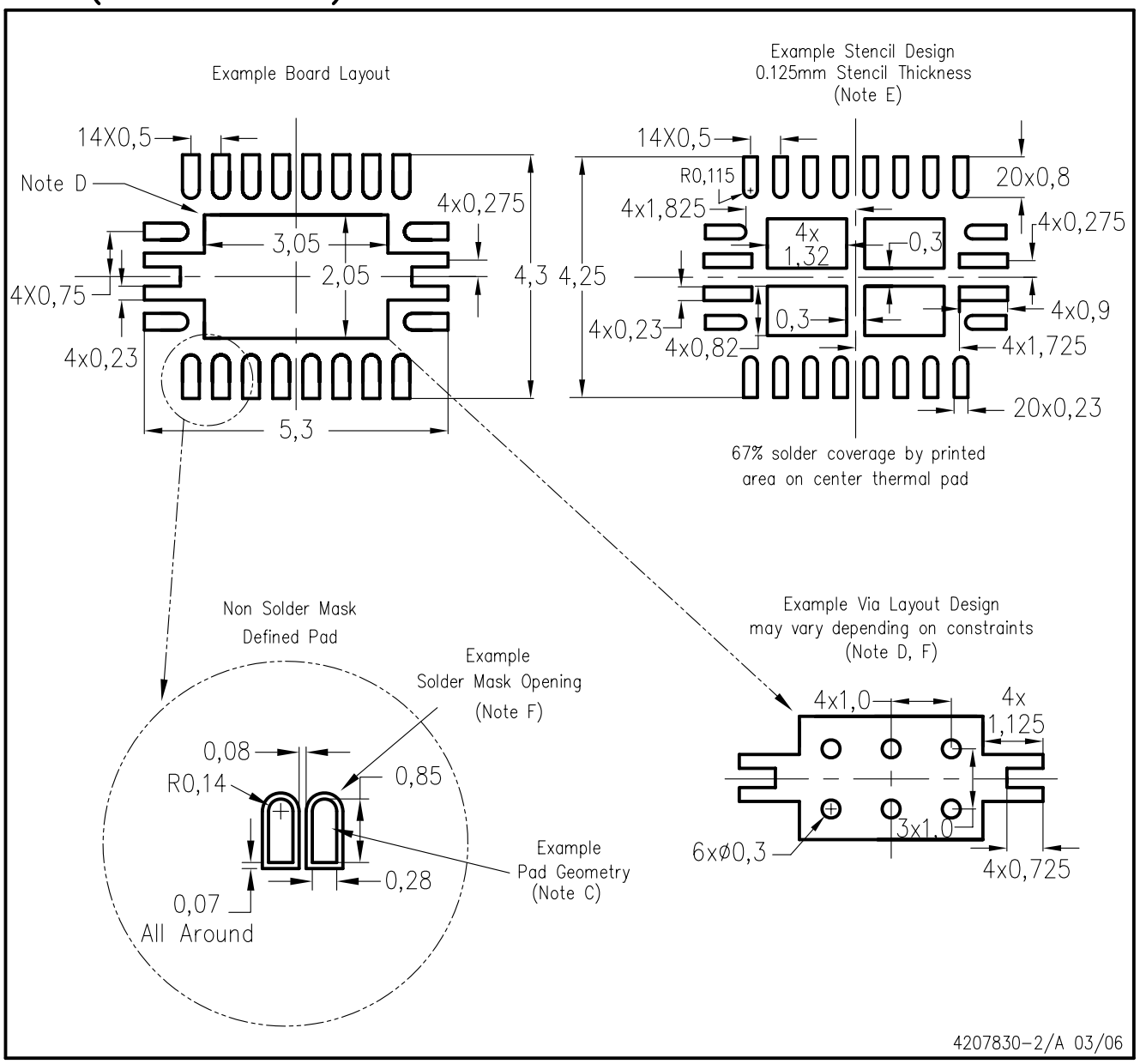


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHL (R–PQFP–N20)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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