HIGH-FREQUENCY MULTIPHASE CONTROLLER

Check for Samples: TPS40090-Q1

FEATURES

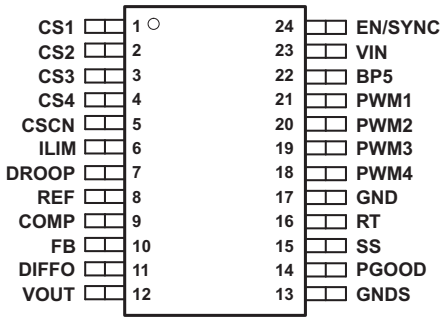
- **Qualified for Automotive Applications**
- **Two-, Three-, or Four-Phase Operation**
- **5-V to 15-V Operating Range**
- **Programmable Switching Frequency Up to 1-MHz/Phase**
- **Current Mode Control With Forced Current Sharing** (1)
- **1% Internal 0.7-V Reference**
- **Resistive Divider Set Output Voltage**
- **True Remote Sensing Differential Amplifier**
- **Resistive or DCR Current Sensing**
- **Current Sense Fault Protection**
- **Programmable Load Line**
- **Compatible with UCC37222 Predictive Gate Drive™ Technology Drivers**
- **24-Pin Space-Saving TSSOP Package**
- **Binary Outputs**

(1) Patent pending

APPLICATIONS

- **Internet Servers**
- **Network Equipment**
- **Telecommunications Equipment**
- **DC Power Distributed Systems**

PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS40090 is a two-, three-, or four-phase programmable synchronous buck controller that is optimized for low-voltage, high-current applications powered by a 5-V to 15-V distributed supply. A multi-phase converter offers several advantages over a single power stage including lower current ripple on the input and output capacitors, faster transient response to load steps, improved power handling capabilities, and higher system efficiency.

Each phase can be operated at a switching frequency up to 1-MHz, resulting in an effective ripple frequency of up to 4-MHz at the input and the output in a four-phase application. A two-phase design operates 180° out of phase, a three-phase design operates 120° out of phase, and a four-phase design operates 90° out of phase, as shown in Figure 1.

The number of phases is programmed by connecting the deactivated phase PWM output to the output of the internal 5-V LDO. In two-phase operation the even phase outputs should be deactivated.

The TPS40090 uses fixed frequency, peak current mode control with forced phase current balancing. When compared to voltage mode control, current mode results in a simplified feedback network and reduced input line sensitivity. Phase current is sensed by using either current sense resistors installed in series with output inductors or, for improved efficiency, by using the DCR (direct current resistance) of the filter inductors. The latter method involves generation of a current proportional signal with an R-C circuit (shown in Figure 11).

The R-C values are selected by matching the time constants of the R-C circuit and the inductor; R-C = L/DCR. With either current sense method, the current signal is amplified and superimposed on the amplified voltage error signal to provide current mode PWM control.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

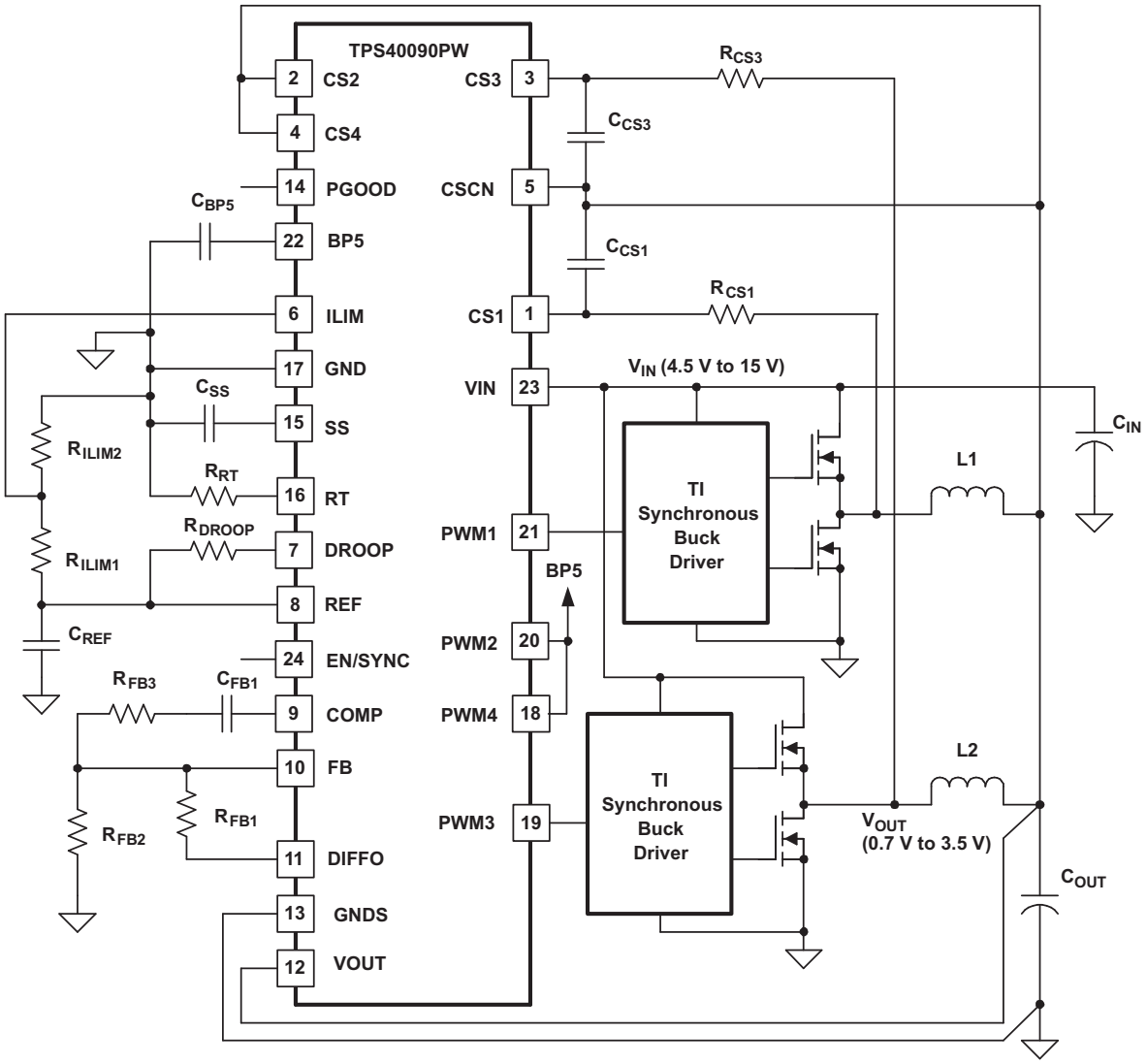
An output voltage droop can be programmed to improve the transient window and reduce size of the output filter. Other features include a single voltage operation, a true differential sense amplifier, a programmable current limit, soft-start, and a power good indicator.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Reel of 2000	TPS40090QPWRQ1	TPS40090Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SIMPLIFIED TWO-PHASE APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATING

over operating free-air temperature range unless otherwise noted(1)

V_{IN}	Input voltage range	EN/SYNC, VIN,	16.5 V
		CS1, CS2, CS3, CS4, CSCN, DROOP, FB, GNDS, ILIM, VOUT	–0.3 V to 6 V
V_{OUT}	Output voltage range	REF, COMP, DIFFO, PGOOD, SS, RT, PWM1, PWM2, PWM3, PWM4, BP5	–0.3 V to 6 V
T_J	Operating virtual-junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature		–65°C to 150°C
ESD	Electrostatic discharge protection, Human-Body Model (HBM)		1500 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage	4.5	15	V
T_J	Operating virtual-junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = 12 V, $R_{(RT)}$ = 64.9 kΩ, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Operating voltage range, VIN		4.5		15	V
V_{IN}	UVLO	Rising V_{IN}	4.25		4.45	V
V_{IN}	UVLO(1)	Falling V_{IN}	4.1		4.35	V
I_{IN}	Shutdown current, VIN			2	10	µA
I_{IN}	Quiescent current switching	Four channels, 400 kHz each, no load		4	6	mA
OSCILLATOR/SYNCHRONIZATION						
	Phase frequency accuracy	Four channels, R_{RT} = 64.9 kΩ	350	415	455	kHz
	Phase frequency set range(1)	Four channels	100		1200	kHz
	Synchronization frequency range(1)	Four channels	800		9600	kHz
	Synchronization input threshold(1)	Four channels		V_{BP5}/2		V
PWM						
	Maximum duty cycle per channel	4-phase operation		87.5		%
		2- and 3-phase operation		83.3		%
	Minimum duty cycle per channel(1)				0	%
	Minimum controllable on-time(1)			50	100	ns
ERROR AMPLIFIER						
	Feedback input voltage		0.690	0.700	0.707	V
	Feedback input bias current	V_{FB} = 0.7 V		25	150	nA
V_{OH}	High-level output voltage	I_{COMP} = –1 mA	2.5	2.9		V
V_{OL}	low-level output voltage	I_{COMP} = 1 mA		0.5	0.8	V
G_{BW}	Gain bandwidth(1)			5		MHz
A_{VOL}	Open loop gain(1)			90		dB
SOFT START						
I_{SS}	Soft-start source current		3.5	5	6	µA
V_{SS}	Soft-start clamp voltage		0.95	1.00	1.05	V

(1) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, $R_{(RT)}$ = 64.9 kΩ, T_J = T_A (unless otherwise noted)

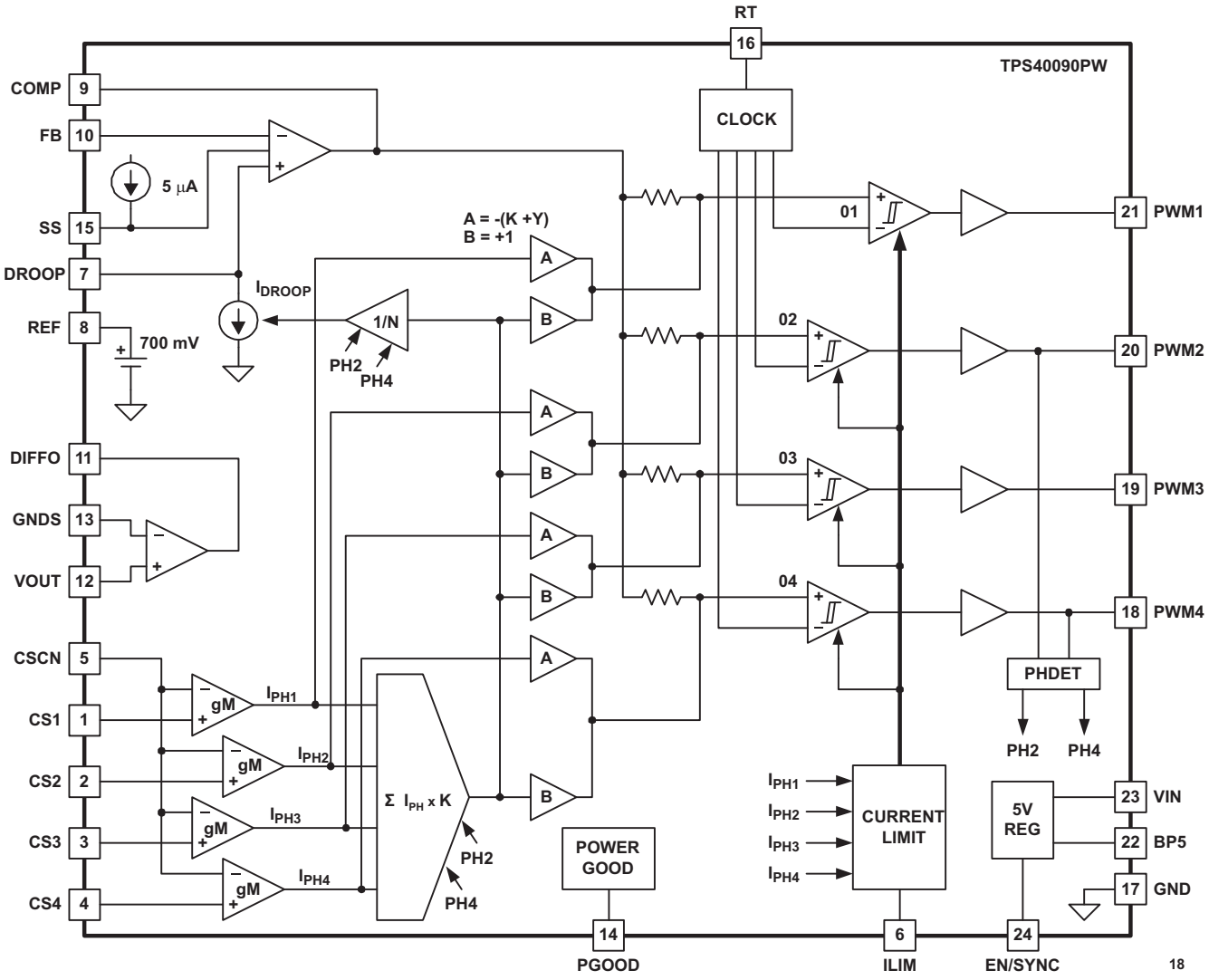
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE						
	Enable threshold voltage		0.8	2	2.5	V
	Enable voltage capability(2)				$V_{IN(max)}$	
PWM OUTPUT						
	PWM pullup resistance	I_{OH} = 5 mA		27	45	Ω
	PWM pulldown resistance	I_{OL} = 10 mA		27	45	
5-V REGULATOR						
V_{OUT}	Output voltage	External I_{LOAD} = 2 mA on BP5	4.8	5	5.2	V
	Pass device voltage drop	V_{IN} = 4.5 V, No external load on BP5			200	mV
	Short circuit current		8		30	mA
CURRENT SENSE AMPLIFIER						
	Gain transfer	–100 mV ≤ $V_{(CS)}$ ≤ 100 mV, V_{CSRTN} = 1.5 V	4.7	5.4	5.9	V/V
	Gain variance between phases	V_{CS} = 100 mV	–5		5	%
	Input offset variance at zero current	V_{CS} = 0 V	–7	0	8	mV
	Input common mode(2)		0		4	V
	Bandwidth(2)		18			MHz
	Maximum V_{CS} in regulation				200	mV
DIFFERENTIAL AMPLIFIER						
	Gain			1		V/V
	Gain tolerance	V_{OUT} 4 V vs 0.7 V, V_{GNDS} = 0 V	–0.5		0.5	%
CMRR	Common mode rejection ratio(2)	0.7 V ≤ V_{OUT} ≤ 4 V	60			dB
	Bandwidth(2)		5			MHz
RAMP						
	Ramp amplitude(2)		0.4	0.5	0.6	V
POWER GOOD						
	PGOOD high threshold	Reference to V_{REF}	10		14	%
	PGOOD low threshold	Reference to V_{REF}	–14		–10	%
V_{OL}	Low-level output voltage	I_{PGOOD} = 4 mA		0.35	0.60	V
I_{lkg}	PGOOD output leakage	V_{PGOOD} = 5 V		50	80	µA
OUTPUT OVERVOLTAGE/UNDERVOLTAGE FAULT						
V_{OV}	Overvoltage threshold voltage	V_{FBK} relative to V_{REF}	15		19	%
V_{UV}	Undervoltage threshold voltage	V_{FBK} relative to V_{REF}	–18		–14	%
LOAD LINE PROGRAMMING						
I_{DROOP}	Pulldown current on DROOP	4-phase, V_{CS} = 100 mV		40		µA

(2) Specified by design

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BP5	22	O	Output of an internal 5-V regulator. A 4.7-µF capacitor should be connected from this pin to ground. For 5-V applications, this pin should be connected to VDD.
COMP	9	O	Output of the error amplifier. The voltage at this pin determines the duty cycle for the PWM.
CS1	1	I	Used to sense the inductor current in the phases. Inductor current can be sensed with an external current sense resistor or by using an external circuit and the inductor's DC resistance. They are also used for overcurrent protection and forced current sharing between the phases.
CS2	2	I	
CS3	3	I	
CS4	4	I	
CSCN	5	I	Common point of current sense resistors or filter inductors
DIFFO	11	O	Output of the differential amplifier. The voltage at this pin represents the true output voltage without drops that result from high current in the PCB traces
DROOP	7	I	Used to program droop function. A resistor between this pin and the REF pin sets the desired droop value.
EN/SYNC	24	I	A logic high signal on this input enables the controller operation. A pulsing signal to this pin synchronizes the main oscillator to the rising edge of an external clock source. These pulses must be of higher frequency than the free running frequency of the main oscillator set by the resistor from the RT pin.
FB	10	I	Inverting input of the error amplifier. In closed loop operation, the voltage at this pin is the internal reference level of 700 mV. This pin is also used for the PGOOD and OVP comparators.
GND	17		Ground connection to the device.
GNDS	13	I	Inverting input of the differential amplifier. This pin should be connected to ground at the point of load.
ILIM	6	I	Used to set the cycle-by-cycle current limit threshold. If ILIM threshold is reached, the PWM cycle is terminated and the converter delivers limited current to the output. Under these conditions the undervoltage threshold is reached eventually and the controller enters the hiccup mode. The controller stays in hiccup mode for seven consecutive cycles. At the eighth cycle the controller attempts a full start-up sequence.
PGOOD	14	O	Power good indicator of the output voltage. This open-drain output connects to the supply via an external resistor.
PWM1	21	O	Phase shifted PWM outputs which control the external drivers. The high output signal commands a PWM cycle. The low output signal commands controlled conduction of the synchronous rectifiers. These pins are also used to program various operating modes as follows: for three-phase mode, PWM4 is connected to 5 V; for two-phase mode, PWM2 and PWM4 are connected to 5 V.
PWM2	20	O	
PWM3	19	O	
PWM4	18	O	
REF	8	O	Output of an internal 0.7-V reference voltage.
RT	16	I	Connecting a resistor from this pin to ground sets the oscillator frequency.
VIN	23	I	Power input for the chip. Decoupling of this pin is required.
VOUT	12	I	Noninverting input of the differential amplifier. This pin should be connected to VOUT at the point of load.
SS	15	I	Provides user programmable soft-start by means of a capacitor connected to the pin.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

Functional Description

The TPS40090 is a multiphase, synchronous, peak current mode, buck controller. The controller uses external gate drivers to operate N-channel power MOSFETs. The controller can be configured to operate in a two-, three-, or four-phase power supply.

The controller accepts current feedback signals from either current sense resistors placed in series with the filter inductors or current proportional signals derived from the inductors' DCR.

Other features include an LDO regulator with UVLO to provide single voltage operation, a differential input amplifier for precise output regulation, user programmable operation frequency for design flexibility, external synchronization capability, programmable pulse-by-pulse overcurrent protection, output overvoltage protection, and output undervoltage shutdown.

Differential Amplifier

The unity gain differential amplifier with high bandwidth allows improved regulation at a user-defined point and eases layout constraints. The output voltage is sensed between the VOUT and GNDS pins. The output voltage programming divider is connected to the output of the amplifier (DIFFO). The differential amplifier can be used only for output voltages lower then 3.3 V.

If there is no need for a differential amplifier, or if the output voltage required is higher than 3.3 V, the differential amplifier can be disabled by connecting the GNDS pin to the BP5 pin. The voltage programming divider in this case should be connected directly to the output of the converter.

Current Sensing and Balancing

The controller employs a peak current-mode control scheme, which naturally provides a certain degree of current balancing. With current mode, the level of current feedback should comply with certain guidelines depending on duty factor, known as *slope compensation* to avoid subharmonic instability. This requirement can prohibit achieving a higher degree of phase current balance. To avoid the controversy, a separate current loop that forces phase currents to match is added to the proprietary control scheme. This effectively provides high degree of current sharing independently of properties of controller's small signal response.

High-bandwidth current amplifiers can accept as an input voltage either voltage drop across dedicated precise current-sense resistors, or inductor's DCR voltage derived by an R-C network, or thermally compensated voltage derived from the inductor's DCR. The wide range of current-sense settings eases the cost and complexity constraints and provides performance superior to those found in controllers using low-side MOSFET current sensing.

Setting Controller Configuration

By default, the controller operates at four-phase configuration. The alternate number of active phases is programmed by connecting unused PWM outputs to BP5. (See Figure 1) For example, for three-phase operation, the unused fourth phase output, PWM4, should be connected to BP5. For two-phase operation, the second, PWM2, and the fourth, PWM4, outputs should be connected to BP5.

Power Up

Capacitors connected to the BP5 pin and the soft-start pin set the power-up time. When EN is high, the capacitor connected to the BP5 pin gets charged by the internal LDO as shown in Figure 2.

$$t_{BPS} = \frac{4.5 \times C_{BP5}}{8 \times 10^{-3}} \quad (1)$$

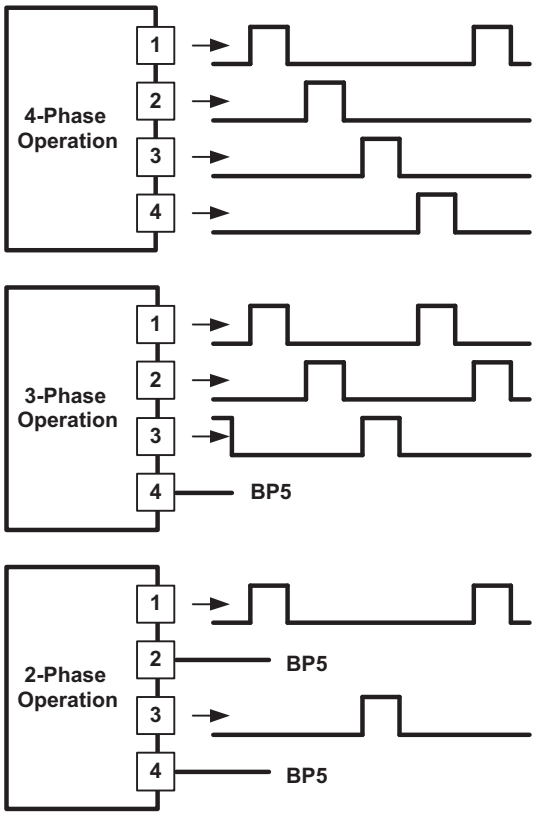


Figure 1. Programming Controller Configuration

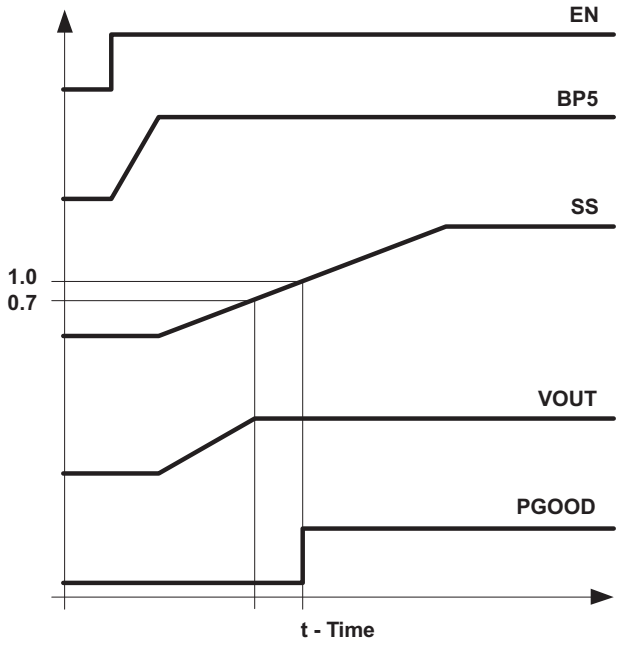


Figure 2. Power-Up Waveforms

When the BP5 pin voltage crosses its lower undervoltage threshold and the power-on reset function is cleared, the calibrated current source starts charging the soft start capacitor. The PGOOD pin is held low during the start up. The rising voltage across the capacitor serves as a reference for the error amplifier assuring start-up in a closed loop manner. When the soft start pin voltage reaches the level of the reference voltage V_{REF} = 0.7 V, the converter's output reaches the regulation point and further rise of the soft start voltage has no effect on the output.

$$t_{SS} = \frac{0.7 \times C_{SS}}{5 \times 10^{-6}} \quad (2)$$

When the soft-start voltage reaches level of 1 V, the power good (PGOOD) function is cleared and reported on the PGOOD pin. Normally, the PGOOD pin goes high at this moment. The time from when SS begins to rise to when PGOOD is reported is:

$$t_{PG} = 1.43 \times T_{SS} \quad (3)$$

Output Voltage Programming

The converter output voltage is programmed by the R1/R2 divider from the output of the differential amplifier. The center point of the divider is connected to the inverting output of the error amplifier (FB), as shown in Figure 5.

$$V_{OUT} = 0.7\ V \times \left(\frac{R1}{R2} + 1\right) \quad (4)$$

Current Sense Fault Protection

Multiphase controllers with forced current sharing are inherently sensitive to failure of a current sense component. In the event of such failure, the whole load current can be steered with catastrophic consequences into a single channel where the fault has happened. The dedicated circuit in the TPS40090 controller prevents it from starting up if any current sense pin is open or shorted to ground. The current-sense fault detection circuit is active only during device initialization, and it does not provide protection should a current-sense failure happen during normal operation.

Overvoltage Protection

If the voltage at the FB pin (V_{FB}) exceeds V_{REF} by more than 16%, the TPS40090 enters into an overvoltage state. In this condition, the output signals from the controller to the external drivers is pulled low, causing the drivers to force all of the upper MOSFETs to the OFF position and all the lower MOSFETs to the ON position. As soon as V_{FB} returns to regulation, the normal operating state resumes.

Overcurrent Protection

The overcurrent function monitors the voltage level separately on each current sense input and compares it to the voltage on the ILIM pin set by a divider from the controller's reference. In case a threshold of $V_{(ILIM)}/2.7$ is exceeded the PWM cycle on the associated phase is terminated. The voltage level on the ILIM pin is determined by the following expression:

$$V_{ILIM} = 2.7 \times I_{PH(max)} \times R_{CS} \tag{5}$$

$$I_{PH(max)} = I_{OUT} + \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}}$$

where:

- $I_{PH(max)}$ is a maximum value of the phase current allowed
- R_{CS} is a value of the current sense resistor used (6)

If the overcurrent condition continues, each phase's PWM cycle is terminated by the overcurrent signals. This puts a converter in a constant current mode with the output current programmed by the ILIM voltage. Eventually, the supply and demand equilibrium on the converter output fails and the output voltage declines. When the undervoltage threshold is reached, the converter enters a hiccup mode. The controller is stopped and the output is not regulated any more, the soft-start pin function changes. It now serves as a timing capacitor for a fault control circuit. The soft-start pin is periodically charged and discharged by the fault control circuit. After seven hiccup cycles expire, the controller attempts to restore normal operation. If the overload condition is not cleared, the controller stays in the hiccup mode indefinitely. In such conditions, the average current delivered to the load is roughly 1/8 of the set overcurrent value.

Undervoltage Protection

If the FB pin voltage falls lower than the undervoltage protection threshold (84.5%), the controller enters the hiccup mode as it is described in the Overcurrent Protection section.

Fault-Free Operation

If the SS pin voltage is prevented from rising above the 1-V threshold, the controller does not execute nor report most faults and the PGOOD output remains low. Only the overcurrent function and current-sense fault remain active. The overcurrent protection continues to terminate PWM cycle every time when the threshold is exceeded but the hiccup mode is not entered.

Setting the Switching Frequency

The clock frequency is programmed by the value of the timing resistor connected from the RT pin to ground.

$$R_{RT} = K_{PH} \times \left(39.2 \times 10^3 \times f_{PH}^{-1.041} - 7\right) \tag{7}$$

where:

K_{PH} is a coefficient that depends on the number of active phases. For two-phase and three-phase configurations, K_{PH}= 1.333. For four-phase configurations, K_{PH}= 1. f_{PH} is a single phase frequency, kHz. The RT resistor value is returned by the last expression in kΩ.

To calculate the output ripple frequency, use the following equation:

$$F_{RPL} = N_{PH} \times f_{PH}$$

where:

- N_{PH} is a number of phases used in the converter. (8)

The switching frequency of the controller can be synchronized to an external clock applied to the EN/SYNC pin. The external frequency should be somewhat higher than the free-running clock frequency for synchronization to take place.

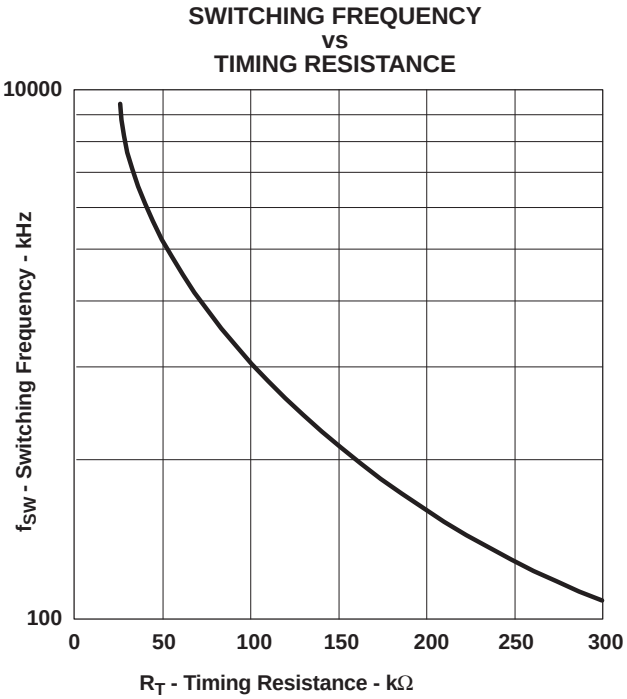


Figure 3.

Setting the Output Voltage Droop

In many applications, the output voltage of the converter is intentionally allowed to droop as load current increases. This approach (sometimes referred to as active load line programming) allows for better use of the regulation window and reduces the amount of the output capacitors required to handle the same load current step. A resistor from the REF pin to the DROOP pin sets the desired value of the output voltage droop.

$$R_{DROOP} = \frac{2500\ N_{PH} \times V_{DROOP}}{I_{OUT} \times R_{CS}} \times \frac{V_{REF}}{V_{OUT}} = \frac{2500\ N_{PH} \times V_{DROOP}}{V_{CS1} + V_{CS2} + V_{CS3} + V_{CS4}} \times \frac{R2}{R1 + R2} \quad (9)$$

where:

- V_{DROOP} is the value of droop at maximum load current I_{OUT}
- N_{PH} is number of phases
- R_{CS} is the current-sense resistor value
- 2500 Ω is the inversed value of transconductance from the current sense pins to DROOP(1)
- V_{CSx}, are the average voltages on the current sense pins

(1) I_{DROOP} is relatively linear vs V_{CS} and is typically 40 µA at V_{CS} = 100 mV. Above V_{CS} = 100 mV, I_{DROOP} becomes nonlinear, rolls off, and saturates to approximately 50 µA to 65 µA when V_{CS} > 200 mV (see Figure 6). Thus, above 100 mV, Equation 9 is not accurate.

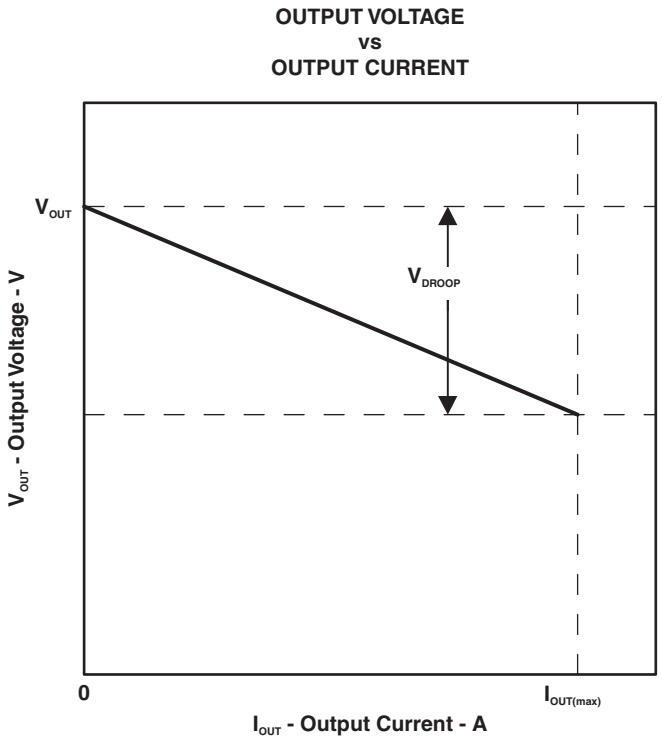


Figure 4.

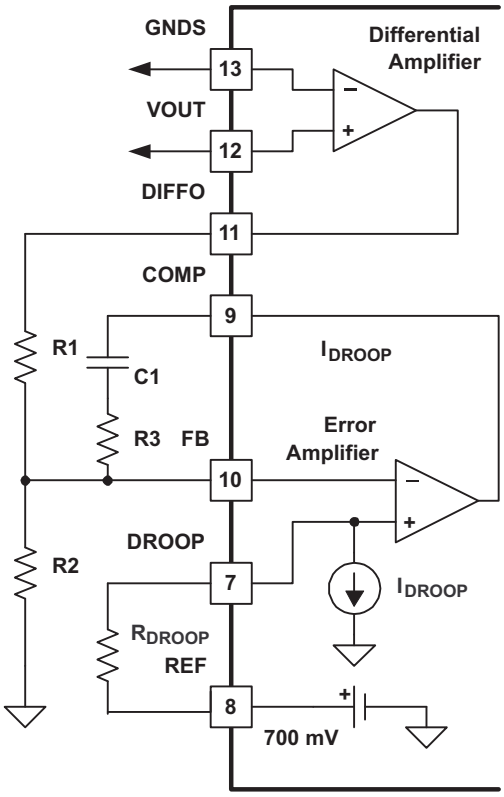


Figure 5.

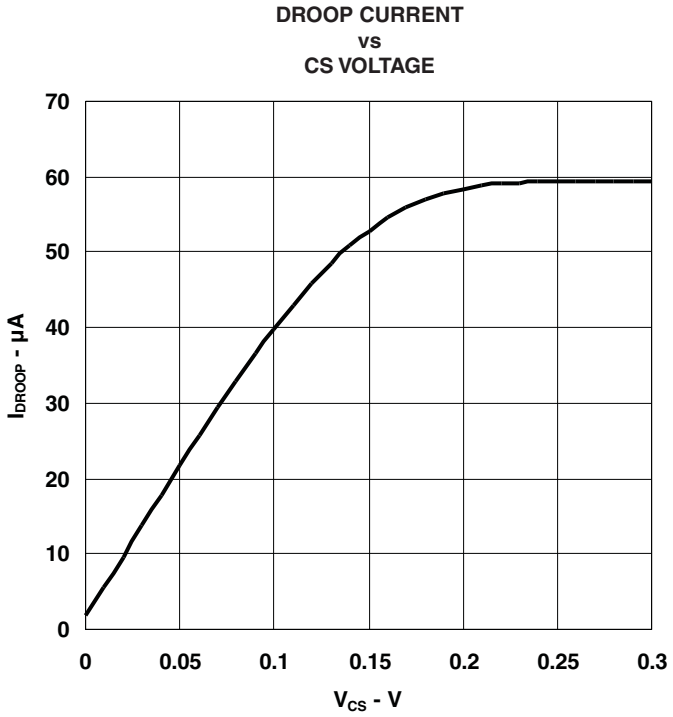


Figure 6.

Feedback Loop Compensation

The TPS40090 operates in a peak current mode and the converter exhibits a single pole response with ESR zero for which Type II compensation network is usually adequate, as shown in Figure 8.

The following equations show where the load pole and ESR zero calculations are situated.

$$f_{OP} = \frac{1}{2\pi \times R_{OUT} \times C_{OUT}} \qquad f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{10}$$

To achieve desired bandwidth the error amplifier must compensate for modulator gain loss on the crossover frequency and this is facilitated by placing the zero over the load pole. The ESR zero alters the modulator's -1 slope at higher frequencies. To compensate for that alteration, the pole in-error amplifier transfer function should be added at frequency of the ESR zero as shown in Figure 7.

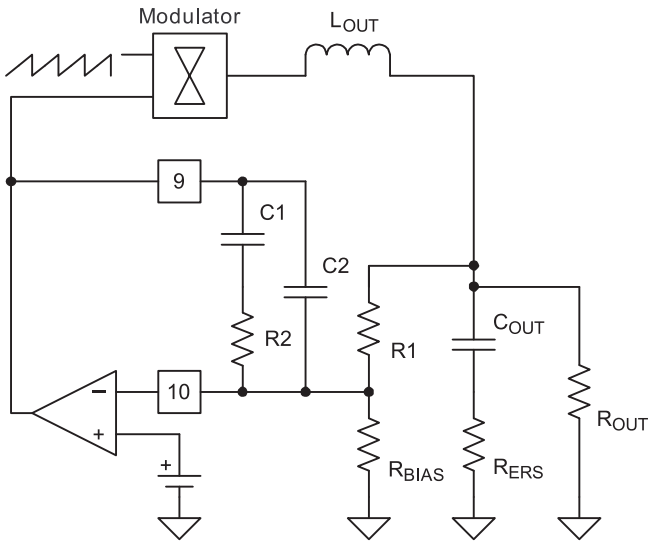


Figure 7.

The following equations help in choosing components of the error amplifier compensation network. Fixing the value of the resistor R1 first is recommended as it simplifies further adjustments of the output voltage without altering the compensation network.

$$R2 = R1 \times 10^{\left(\frac{-G_{OMAG}}{20}\right)}; \quad C1 = \frac{1}{\left(2\pi \times F_{OP} \times R2\right)}; \quad C2 = \frac{1}{\left(2\pi \times F_{ESRZ} \times R2\right)} \tag{11}$$

where:

- G_{OMAG} is the control to output gain at desired system crossover frequency.

Introduction of output voltage droop as a measure to reduce amount of filter capacitors changes the transfer function of the modulator as it is shown in the Figure 9.

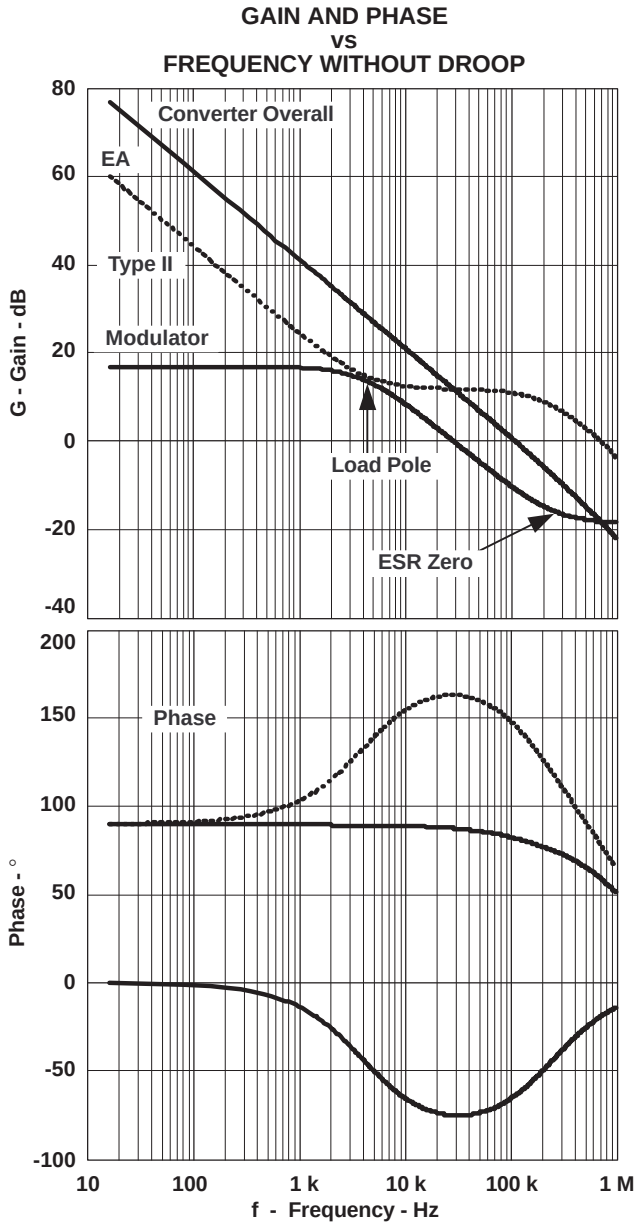

GAIN AND PHASE
vs
FREQUENCY WITHOUT DROOP
Converter Overall
EA
Type II
Modulator
Load Pole
ESR Zero
G - Gain - dB
80
60
40
20
0
-20
-40
Phase
Phase - °
200
150
100
50
0
-50
-100
10
100
1 k
10 k
100 k
1 M
f - Frequency - Hz

Figure 8.

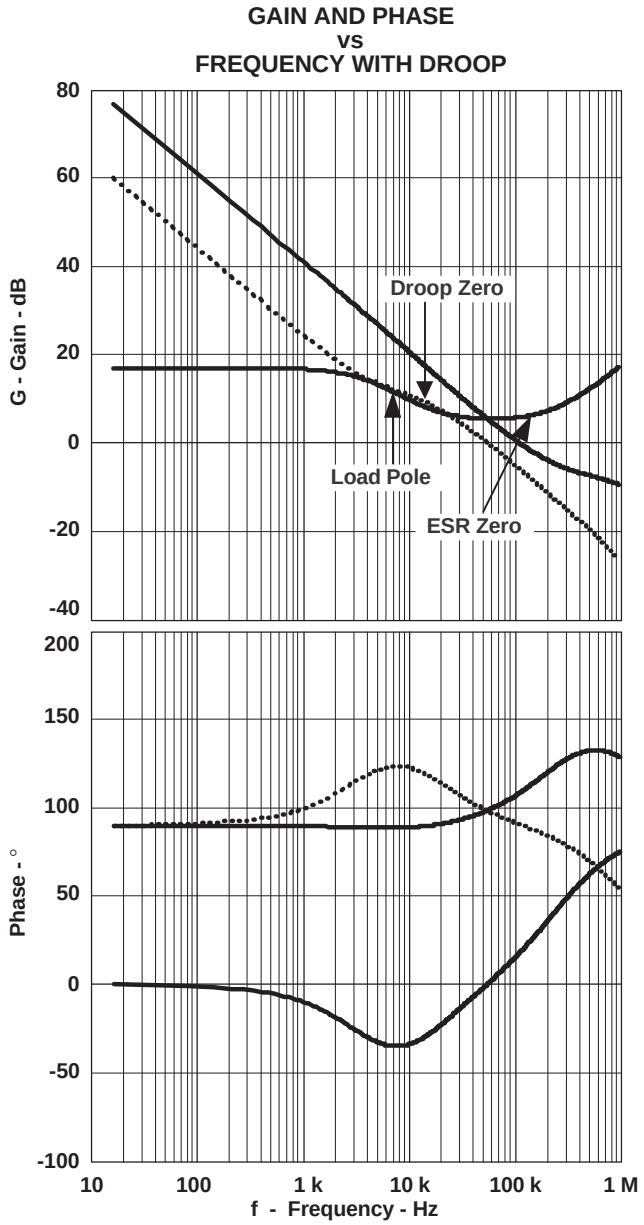


Figure 9.

The droop function, as well as the output capacitor ESR, introduces zero on some frequency left of the crossover point.

$$F_{DROOPZ} = \frac{1}{2\pi \left(\frac{V_{DROOP}}{I_{OUT(max)}} \right) \times C_{OUT}} \tag{12}$$

To compensate for this zero, pole on the same frequency should be added to the error amplifier transfer function. With Type II compensation network a new value for the capacitor C2 is required compared to the case without droop.

$$C2 = \frac{C1}{2\pi \times R2 \times C1 \times \left(F_{DROOPZ} - 1 \right)} \tag{13}$$

When attempting to close the feedback loop at frequency that is near the theoretical limit, use the above considerations as a first approximation and perform on bench measurements of closed loop parameters as effects of switching frequency proximity and finite bandwidth of voltage and current amplifiers may substantially alter them as it is shown in Figure 10.

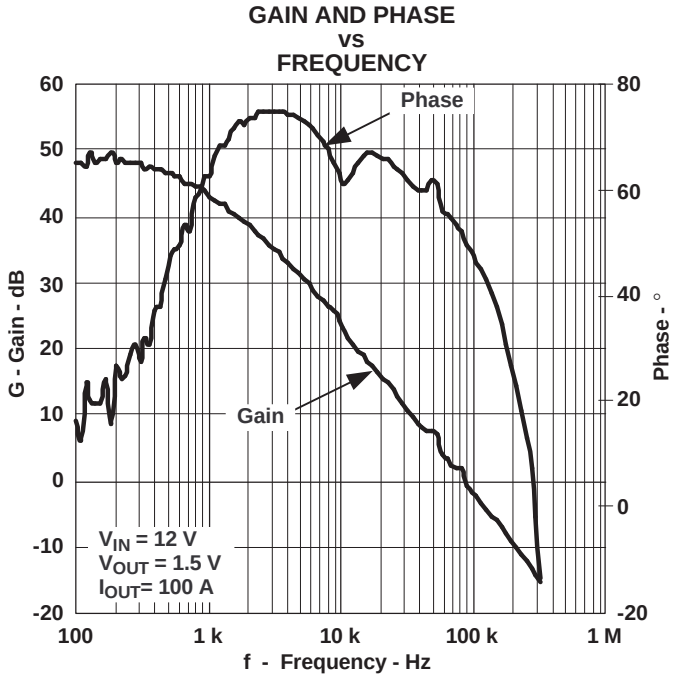


Figure 10.

Thermal Compensation of DCR Current Sensing

Inductor DCR current sensing is a known lossless technique to retrieve a current proportional signal. Equation 14 and Equation 15 show the calculation used to determine the DCR voltage drop for any given frequency. (See Figure 11)

$$V_{DCR} = \left(V_{IN} - V_{OUT}\right) \times \frac{DCR}{DCR + \omega \times L} \tag{14}$$

$$V_C = \left(V_{IN} - V_{OUT}\right) \times \frac{1}{\omega \times C \times \left(R + \frac{1}{\omega \times C}\right)} \tag{15}$$

Voltage across the capacitor is equal to voltage drop across the inductor DCR, $V_C = V_{DCR}$ when time constant of the inductor and the time constant of the R-C network are equal:

$$V_C = \frac{1}{\omega \times C \times \left(R + \frac{1}{\omega \times C}\right)} = \frac{DCR}{DCR + \omega \times L}; \quad \frac{L}{DCR} = R \times C; \quad \tau_{DCRL} = \tau_{RC} \tag{16}$$

The output signal generated by the network shown in Figure 11 is temperature dependant due to positive thermal coefficient of copper specific resistance as determined using Equation 17. The temperature variation of the inductor coil can exceed 100°C in a practical application leading to approximately 40% variation in the output signal and in turn, respectively move the overcurrent threshold and the load line.

$$K(T) = 1 + 0.0039 \times (T - 25) \tag{17}$$

The relatively simple network shown in Figure 12 (made of passive components including one NTC resistor) can provide almost complete compensation for copper thermal variations.

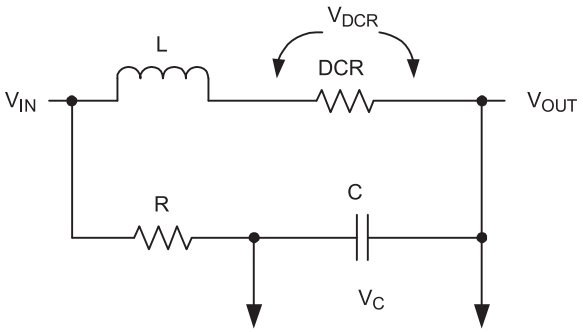


Figure 11.

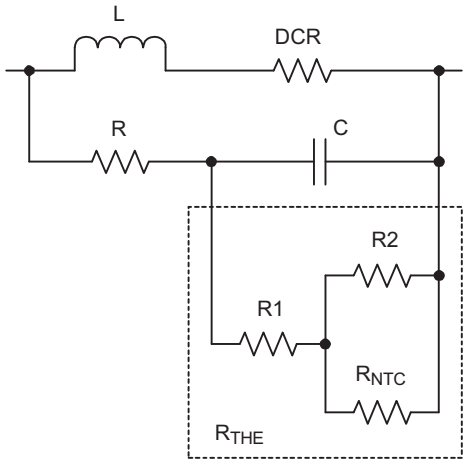


Figure 12.

The following algorithm and expressions help to determine components of the network.

1. Calculate the equivalent impedance of the network at 25°C that matches the inductor parameters in Equation 18. Use of COG type capacitors for this application is recommended. For example, for L = 0.4 µH, DCR = 1.22 mΩ, C = 10 nF; R_E = 33.3 kΩ. It is recommended to keep R_E < 50 kΩ as higher values may produce false triggering of the current sense fault protection.

$$R_E = \frac{\frac{L}{DCR}}{C} \tag{18}$$

2. It is necessary to set the network attenuation value $K_{DIV}(25)$ at 25°C. For example, $K_{DIV}(25)$ = 0.85. The attenuation values $K_{DIV}(25)$ > 0.9 produces higher values for NTC resistors that are harder to get from suppliers. Attenuation values lower 0.7 substantially reduce the network output signal.
3. Based on calculated R_E and $K_{DIV}(25)$ values, calculate and pick the closest standard value for the resistor R = $R_E/K_{DIV}(25)$. For the given example R = 33 kΩ/ 0.85 = 38.8 kΩ. The closest standard value from 1% line is R = 39.2 kΩ.
4. Pick two temperature values at which curve fitting is made. For example T1 = 50°C and T2 = 90°C.
5. Find the relative values of R_{THE} required on each of these temperatures.

$$R_{THE1} = \frac{R_{THE}(T1)}{R_{THE}(25)} \qquad R_{THE2} = \frac{R_{THE}(T2)}{R_{THE}(25)} \tag{19}$$

$$R_T = \frac{K_{DIV}(T)}{1 - K_{DIV}(T)} \times R \qquad K_{DIV}(T) = \frac{K_{DIV}(25)}{1 + 0.0039 \times (t - 25)} \tag{20}$$

For the given example R_{THE1}= 0.606, R_{THE2}=0.372.

6. From the NTC resistor datasheet get the relative resistance for resistors with desired curve. For the given example and curve 17 for NTHS NTC resistors from Vishay R_{NTC1}= 0.3507 and R_{NTC2}= 0.08652.
7. Calculate relative values for network resistors including the NTC resistor.

$$R1_R = \frac{\left(R_{NTC1} - R_{NTC2}\right) \times R_{E1} \times R_{E2} - R_{NTC1} \times R_{E2} \times \left(1 - R_{NTC2}\right) + R_{NTC2} \times R_{E1} \times \left(1 - R_{NTC1}\right)}{R_{NTC1} \times R_{E1} \times \left(1 - R_{NTC2}\right) - R_{NTC2} \times R_{E2} \times \left(1 - R_{NTC1}\right) - \left(R_{NTC1} - R_{NTC2}\right)} \quad (21)$$

$$R2_R = \left(1 - R_{NTC1}\right) \times \left[\frac{1}{1 - R1_R} - \frac{R_{NTC1}}{R_{E1} - R1_R}\right]^{-1} \quad (22)$$

$$RNTC_R = \left[\left(1 - R1_R\right)^{-1} - \left(R2_R\right)^{-1}\right]^{-1} \quad (23)$$

For the given example $R1_R$= 0.281, $R2_R$ = 2.079, and $RNTC_R$ = 1.1.

8. Calculate the absolute value of the NTC resistor as $R_{THE}(25)$. In given example R_{NTC} = 244.3 kΩ.
9. Find a standard value for the NTC resistor with chosen curve type. In case the close value does not exist in a desired form factor or curve type. Chose a different type of the NTC resistor and repeat steps 6 to 9. In the example, the NTC resistor with the part number NTHS0402N17N2503J with $R_{NTCS}(25)$ = 250 kΩ is close enough to the calculated value.
10. Calculate a scaling factor for the chosen NTC resistor as a ratio between selected and calculated NTC value and. In the example k = 1.023.

$$k = \frac{RNTC_S}{RNTC_C} \quad (24)$$

11. Calculate values of the remaining network resistors.

$$R1_C = R_{THE}(25) \times \left[\left((1 - k) + k \times R1_R\right)\right] \quad (25)$$

For the given example, $R1_C$= 58.7 kΩ and $R2_C$ = 472.8 kΩ. Pick the closest available 1% standard values: R1 = 39.2 kΩ, and R2 = 475 kΩ, thus completing the design of the thermally compensated network for the DCR current sensor.

Figure 13 illustrates the fit of the designed network to the required function.

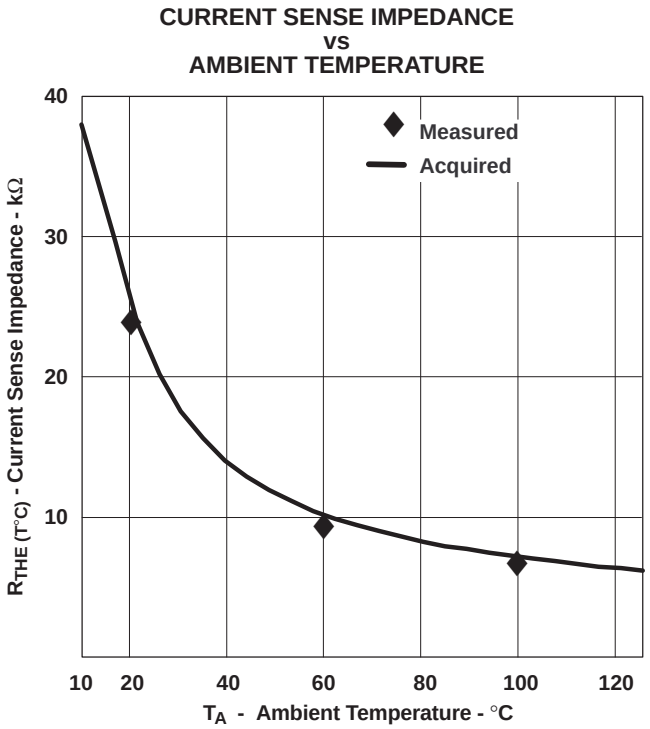


Figure 13.

Operation With Output Voltages Higher Than 3.3 V

The TPS40090 controllers are designed to operate in power supplies with output voltages ranging from 0.7 V to 3.3 V. To support higher output voltages, mainly in 12-V to 5-V power supplies, the BP5 voltage needs to be increased slightly to provide enough headroom to ensure linearity of current sense amplifiers. The simple circuit on Figure 14 shows a configuration that generates a 6-V voltage source to power the controller with increased bias voltage. Both the VIN and BP5 pins should be connected to this voltage source. The differential amplifier normally excessive for higher-output voltages can be disabled by connecting GNDS pin to the BP5 pin.

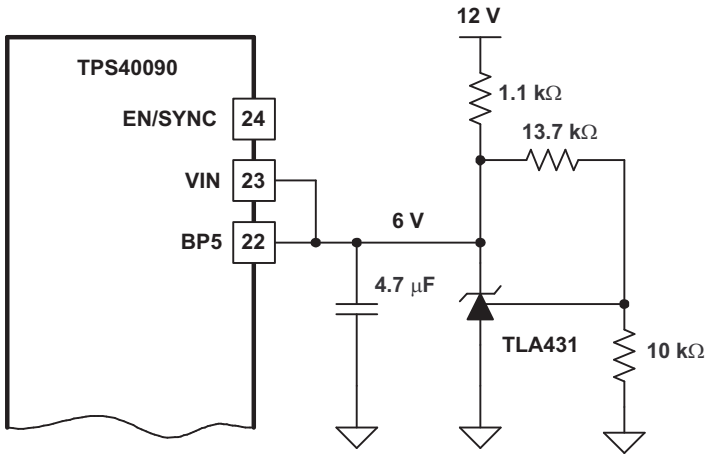


Figure 14. Biasing the TPS40090 With a 5-V Power Supply

Design Example

A design example is available in the TPS40090EVM-001 user's guide (SLUU175).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40090QPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS40090Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS40090-Q1 :

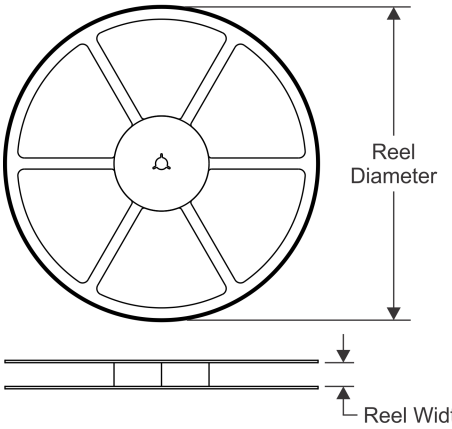
- Catalog: TPS40090

NOTE: Qualified Version Definitions:

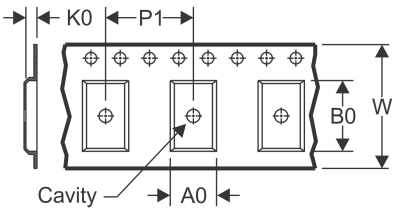
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

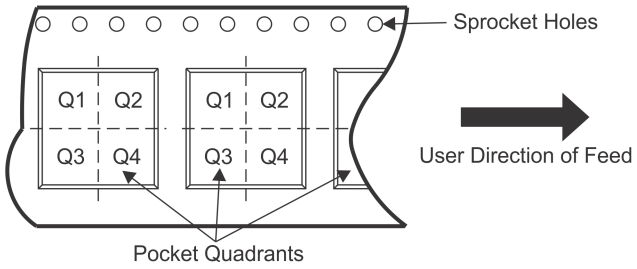


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

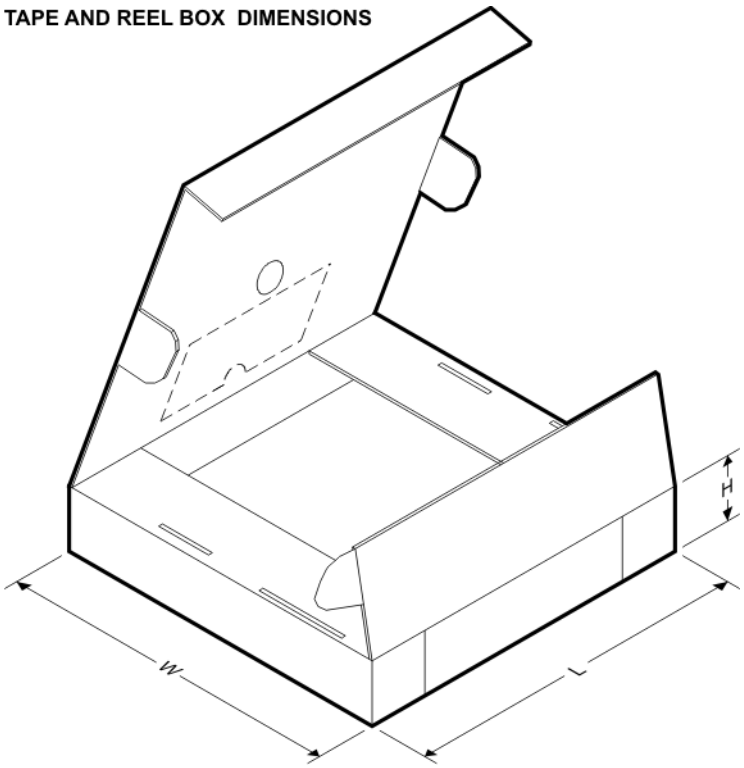
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40090QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

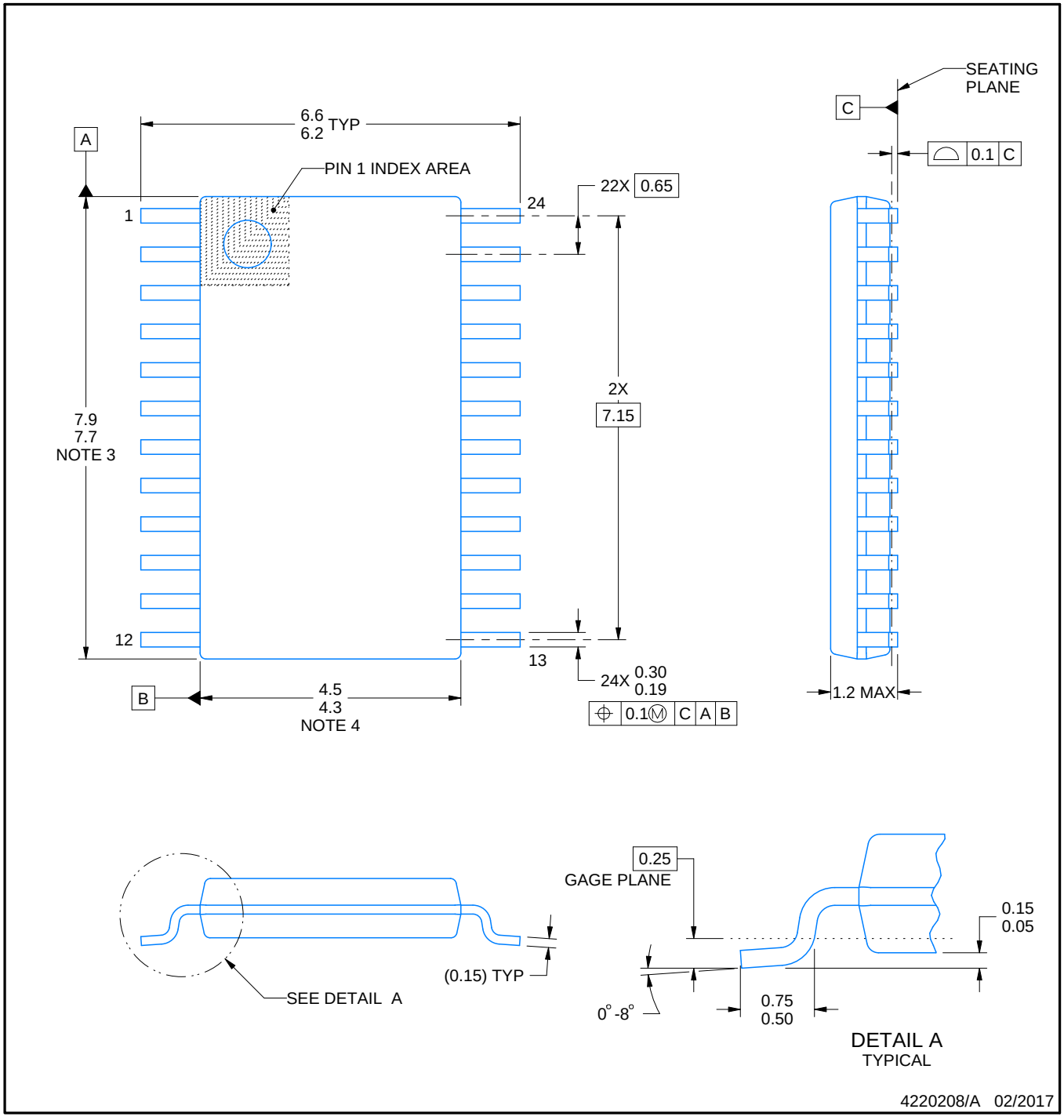
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40090QPWRQ1	TSSOP	PW	24	2000	853.0	449.0	35.0

PACKAGE OUTLINE

PW0024A

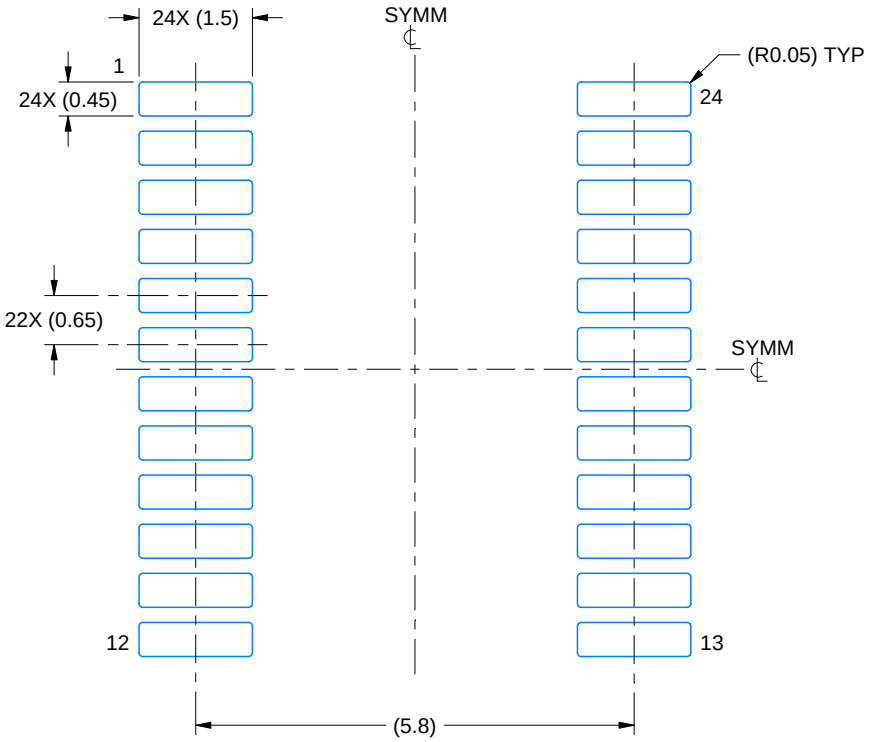
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

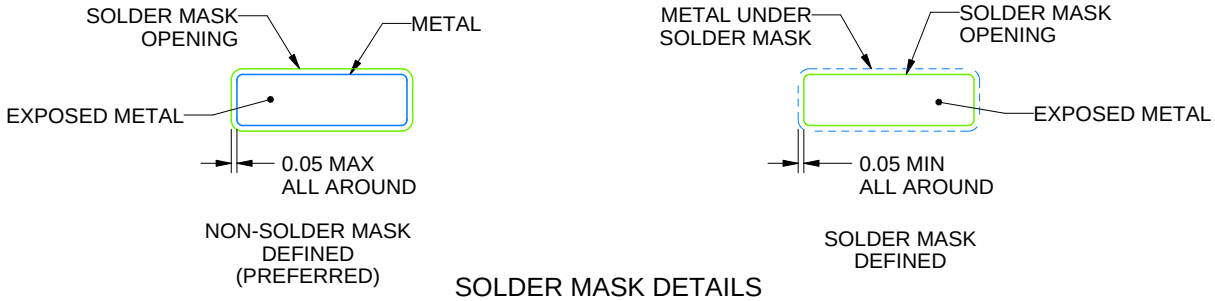


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

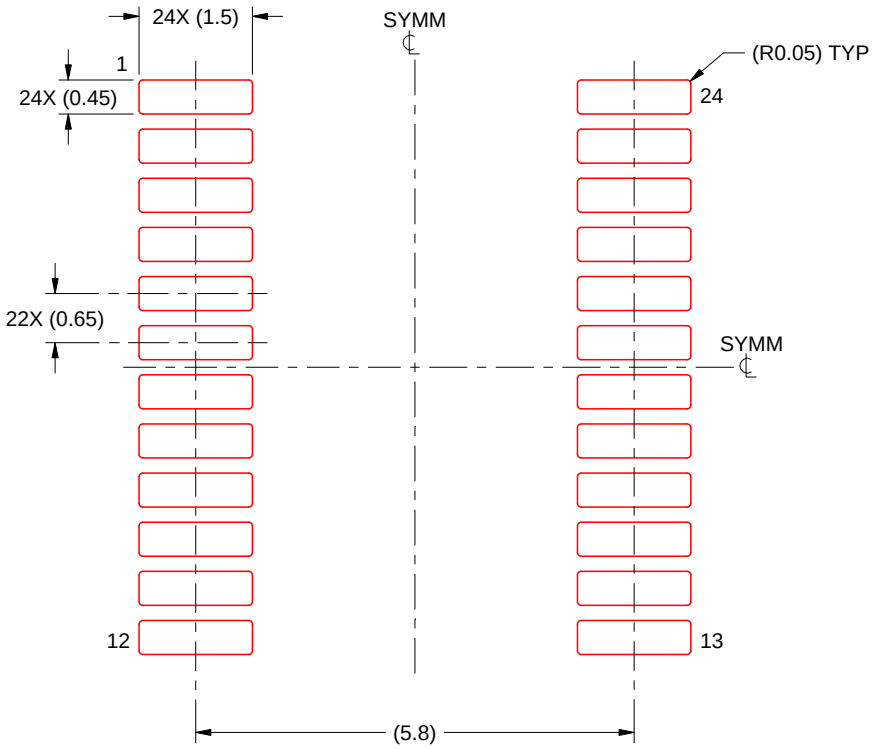


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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