**TEXAS INSTRUMENTS**

**TPS3813J25, TPS3813L30, TPS3813K33, TPS3813I50**

SLVS331H – DECEMBER 2000 – REVISED JULY 2016

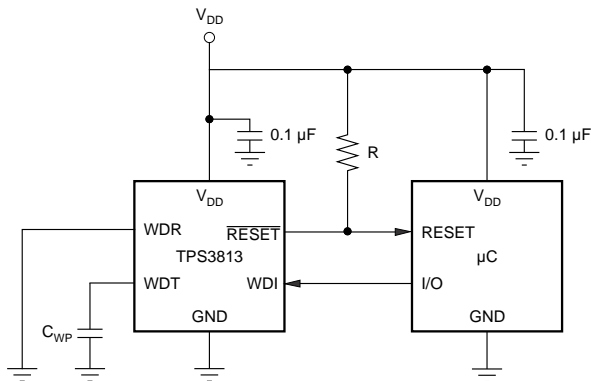# TPS3813xxx Family Processor Supervisory Circuits With Window-Watchdog

## 1 Features

- Window-Watchdog With Programmable Delay and Window Ratio
- 6-Pin SOT-23 Package
- Supply Current of 9 µA (Typical)
- Power-On Reset Generator With a Fixed Delay Time of 25 ms
- Precision Supply Voltage Monitor: 2.5 V, 3 V, 3.3 V, and 5 V
- Open-Drain Reset Output
- Temperature Range: –40°C to 85°C

## 2 Applications

- Applications Using DSPs, Microcontrollers, or Microprocessors
- Safety Critical Systems
- Automotive Systems
- Heating Systems

### Typical Operating Circuit



Copyright © 2016, Texas Instruments Incorporated

## 3 Description

The TPS3813xxx family of supervisory circuits provide circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power on, $\overline{\text{RESET}}$ is asserted when supply voltage ($V_{DD}$) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors $V_{DD}$ and keeps $\overline{\text{RESET}}$ active as long as $V_{DD}$ remains below the threshold voltage ($V_{IT}$). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_d = 25$ ms typical, starts after $V_{DD}$ has risen above the threshold voltage ($V_{IT}$). When the supply voltage drops below the threshold voltage ($V_{IT}$), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage ($V_{IT}$) set by an internal voltage divider.

For safety critical applications the TPS3813xxx family incorporates a so-called window-watchdog with programmable delay and window ratio. The upper limit of the watchdog time-out can be set by either connecting WDT to GND, $V_{DD}$, or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or $V_{DD}$. The supervised processor now needs to trigger the TPS3813xxx within this window not to assert a $\overline{\text{RESET}}$.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 6-pin SOT-23 package.

The TPS3813xxx devices are characterized for operation over a temperature range of –40°C to 85°C.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS3813xxx | SOT-23 (6) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

# 5 Device Comparison Table

| $T_A$[1] | DEVICE NAME | THRESHOLD VOLTAGE | MARKING |
|---|---|---|---|
| −40°C to +85°C | TPS3813J25DBV | 2.25 V | PCDI |
| | TPS3813L30DBV | 2.64 V | PEZI |
| | TPS3813K33DBV | 2.93 V | PFAI |
| | TPS3813I50DBV | 4.55 V | PFBI |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

# 6 Pin Configuration and Functions

**DBV Package**
**6-Pin SOT-23**
**Top View**

```
WDI  | 1      6 | RESET
GND  | 2      5 | WDR
WDT  | 3      4 | V_DD
```
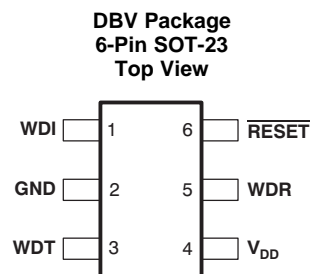
**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | WDI | I | Watchdog timer input. This input must be driven at all times and not left floating. |
| 2 | GND | I | Ground |
| 3 | WDT | I | Programmable watchdog delay input |
| 4 | $V_{DD}$ | I | Supply voltage and supervising input |
| 5 | WDR | I | Selectable watchdog window ratio input. This input must be tied to $V_{DD}$ or GND and not left floating. |
| 6 | RESET | O | Open-drain reset output |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[1]

|          |                                        | MIN  | MAX           | UNIT |
|----------|----------------------------------------|------|---------------|------|
| $V_{DD}$ | Supply voltage[2]                       |      | 7             | V    |
|          | RESET                                  | −0.3 | $V_{DD}$ + 0.3 | V    |
|          | All other pins [2]                      | −0.3 | 7             | V    |
| $I_{OL}$ | Maximum low output current             |      | 5             | mA   |
| $I_{OH}$ | Maximum high output current            |      | −5            | mA   |
| $I_{IK}$ | Input clamp current ($V_I$ < 0 or $V_I$ > $V_{DD}$) |      | ±20           | mA   |
| $I_{OK}$ | Output clamp current ($V_O$ < 0 or $V_O$ > $V_{DD}$) |      | ±20           | mA   |
|          | Continuous total power dissipation     |      | See *Dissipation Ratings* |      |
|          | Soldering temperature                  |      | 260           | °C   |
| $T_A$    | Operating free-air temperature         | −40  | 85            | °C   |
| $T_{stg}$ | Storage temperature                   | −65  | 150           | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than t = 1000h continuously.

## 7.2 ESD Ratings

|              |                        |                                                        | VALUE | UNIT |
|--------------|------------------------|--------------------------------------------------------|-------|------|
| $V_{(ESD)}$  | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]  | ±4000 | V    |
|              |                        | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1500 |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

At specified temperature range.

|                |                                       | MIN              | MAX              | UNIT |
|----------------|---------------------------------------|------------------|------------------|------|
| $V_{DD}$       | Supply voltage                        | 2                | 6                | V    |
| $V_I$          | Input voltage                         | 0                | $V_{DD}$ + 0.3   | V    |
| $V_{IH}$       | High-level input voltage              | 0.7 × $V_{DD}$   |                  | V    |
| $V_{IL}$       | Low-level input voltage               |                  | 0.3 × $V_{DD}$   | V    |
| Δt/ΔV          | Input transition rise and fall rate   |                  | 100              | ns/V |
| $t_w$          | Pulse width of WDI trigger pulse      | 50               |                  | ns   |
| $T_A$          | Operating free-air temperature        | −40              | 85               | °C   |

## 7.4 Thermal Information

|                |                                            | TPS3813xxx            |      |
|----------------|--------------------------------------------|-----------------------|------|
|                | **THERMAL METRIC**[1]                       | DBV (SOT-23)          | UNIT |
|                |                                            | 6 PINS                |      |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance    | 208.5                 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 123.3            | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance      | 37.2                  | °C/W |
| $\psi_{JT}$    | Junction-to-top characterization parameter | 14.6                  | °C/W |
| $\psi_{JB}$    | Junction-to-board characterization parameter | 36.3                | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a           | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Low-level output voltage | | $V_{DD}$ = 2 V to 6 V, $I_{OL}$ = 500 µA | | | | 0.2 | V |
| | | | $V_{DD}$ = 3.3 V $I_{OL}$ = 2 mA | | | | 0.4 | |
| | | | $V_{DD}$ = 6 V, $I_{OL}$ = 4 mA | | | | 0.4 | |
| $V_{POR}$ | Power up reset voltage [1] | | $V_{DD}$ ≥ 1.1 V, $I_{OL}$ = 50 µA | | | | 0.2 | V |
| $V_{IT}$ | Negative-going input threshold voltage [2] | TPS3813J25 | $T_A$ = –40°C to +85°C | | 2.2 | 2.25 | 2.3 | V |
| | | TPS3813L30 | | | 2.58 | 2.64 | 2.7 | |
| | | TPS3813K33 | | | 2.87 | 2.93 | 3 | |
| | | TPS3813I50 | | | 4.45 | 4.55 | 4.65 | |
| $V_{hys}$ | Hysteresis | TPS3813J25 | | | | 30 | | mV |
| | | TPS3813L30 | | | | 35 | | |
| | | TPS3813K33 | | | | 40 | | |
| | | TPS3813I50 | | | | 60 | | |
| $I_{IH}$ | High-level input current | WDI, WDR | WDI = $V_{DD}$ = 6 V, WDR = $V_{DD}$ = 6 V | | –25 | | 25 | nA |
| | | WDT | WDT = $V_{DD}$ = 6 V, $V_{DD}$ > $V_{IT}$, $\overline{RESET}$ = High | | –100 | | 100 | |
| $I_{IL}$ | Low-level input current | WDI, WDR | WDI = 0 V, WDR = 0 V, $V_{DD}$ = 6 V | | –25 | | 25 | |
| | | WDT | WDT = 0 V, $V_{DD}$ > $V_{IT}$, $\overline{RESET}$ = High | | –100 | | 100 | |
| $I_{OH}$ | High-level output current | | $V_{DD}$ = $V_{IT}$ + 0.2 V, $V_{OH}$ = $V_{DD}$ | | | | 25 | nA |
| $I_{DD}$ | Supply current | | $V_{DD}$ = 2-V output unconnected | | | 9 | 13 | µA |
| | | | $V_{DD}$ = 5-V output unconnected | | | 20 | 25 | |
| $C_i$ | Input capacitance | | $V_I$ = 0 V to $V_{DD}$ | | | 5 | | pF |

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_r$, $V_{DD}$ ≥ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) must be placed near to the supply terminals.

## 7.6 Timing Requirements

At $R_L$ = 1 MΩ, $C_L$ = 50 pF, and $T_A$ = –40°C to +85°C.

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_w$ | Pulse width at $V_{DD}$ | $V_{DD}$ = $V_{IT–}$ + 0.2 V, $V_{DD}$ = $V_{IT–}$ – 0.2 V | 3 | | | µs |

## 7.7 Switching Characteristics

At $R_L$ = 1 MΩ, $C_L$ = 50 pF, and $T_A$ = –40°C to +85°C.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time | | $V_{DD}$ ≥ $V_{IT}$ + 0.2 V, See Figure 1 | 20 | 25 | 30 | ms |
| $t_{t(out)}$ | Watchdog time-out | Upper limit | WDT = 0 V | 0.2 | 0.25 | 0.3 | s |
| | | | WDT = $V_{DD}$ | 2 | 2.5 | 3 | |
| | | | WDT = programmable [1] | | See [2] | | ms |
| | Watchdog window ratio | | WDR = 0 V, WDT = 0 V | | 1:31.8 | | |
| | | | WDR = 0 V, WDT = $V_{DD}$ | | 1:32 | | |
| | | | WDR = 0 V, WDT = programmable | | 1:25.8 | | |
| | | | WDR = $V_{DD}$, WDT = 0 V | | 1:124.9 | | |
| | | | WDR = $V_{DD}$, WDT = $V_{DD}$ | | 1:127.7 | | |
| | | | WDR = $V_{DD}$, WDT = programmable | | 1:64.5 | | |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $V_{DD}$ to $\overline{RESET}$ delay | $V_{IL}$ = $V_{IT}$ – 0.2 V, $V_{IH}$ = $V_{IT}$ + 0.2 V | | 30 | 50 | µs |

(1) 155 pF < $C_{(ext)}$ < 63 nF
(2) ($C_{(ext)}$ ÷ 15.55 pF + 1) × 6.25 ms

---

Product Folder Links: *TPS3813J25  TPS3813L30  TPS3813K33  TPS3813I50*

## 7.8 Dissipation Ratings

| PACKAGE | $T_A < 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 80°C$ POWER RATING |
|---|---|---|---|---|
| DBV | 437 mW | 3.5 mW/°C | 280 mW | 227 mW |



**Figure 1. Timing Diagram**
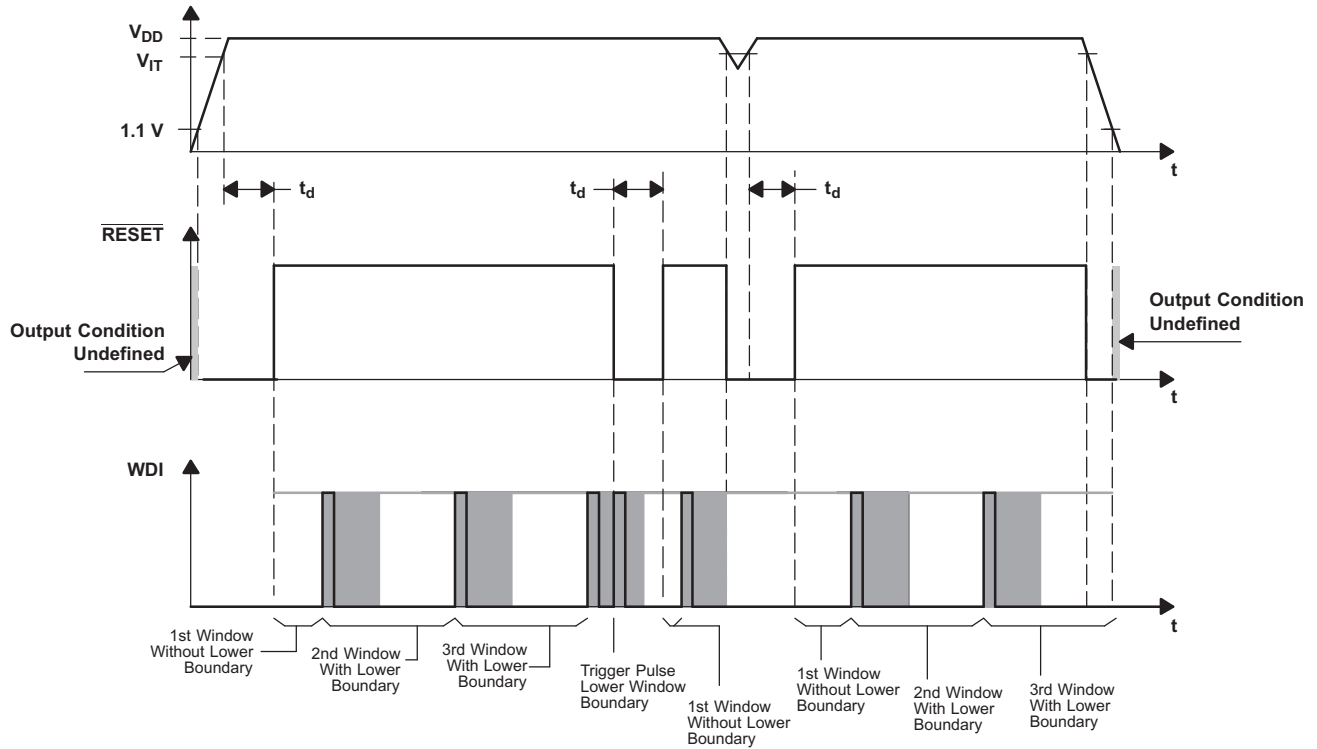
Product Folder Links: *TPS3813J25  TPS3813L30  TPS3813K33  TPS3813I50*

## 7.9 Typical Characteristics
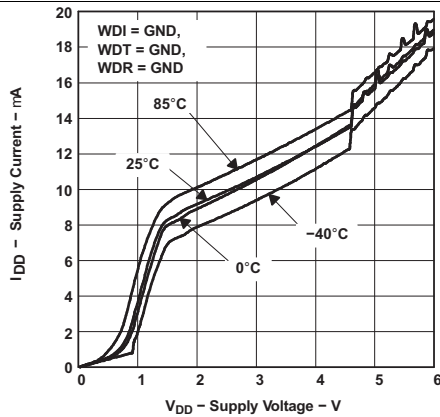


Figure 2. Supply Current vs Supply Voltage
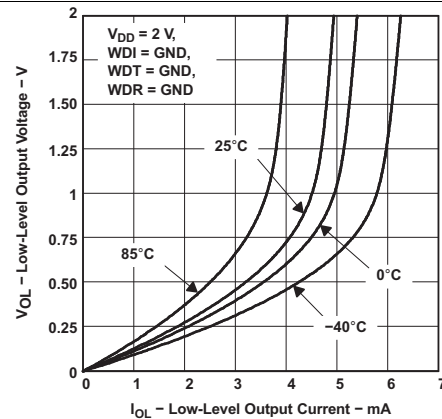
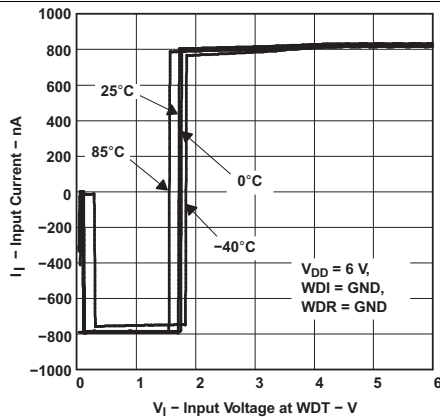Figure 3. Low-Level Output Voltage vs Low-Level Output Current
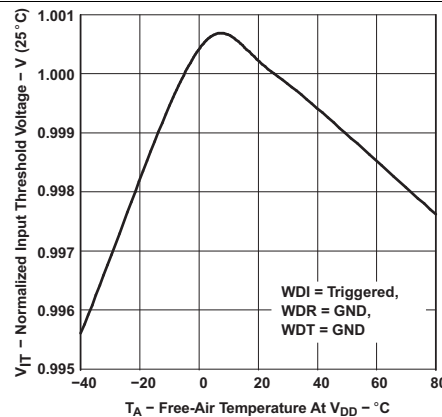
Figure 4. Input Current vs Input Voltage at WDT

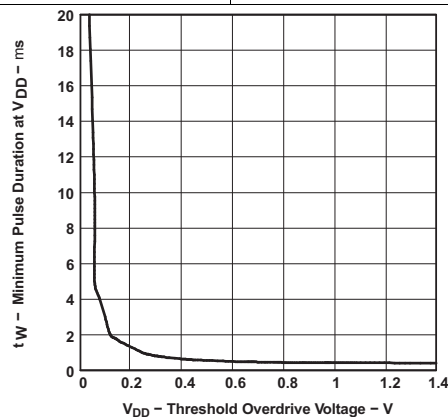Figure 5. Normalized Input Threshold Voltage vs Free-Air Temperature at VDD

Figure 6. Minimum Pulse Duration at $V_{DD}$ vs $V_{DD}$ Threshold Overdrive Voltage

Product Folder Links: *TPS3813J25  TPS3813L30  TPS3813K33  TPS3813I50*

# 8 Detailed Description

## 8.1 Overview

The TPS3813xxx family of supervisory circuits provide circuit initialization and timing supervision signals. During power on, $\overline{\text{RESET}}$ is asserted (low) when the supply voltage ($V_{DD}$) increases above 1.1 V. Thereafter, the supervisory circuit monitors $V_{DD}$ and keeps $\overline{\text{RESET}}$ low as long as $V_{DD}$ remains below the threshold voltage ($V_{IT}$). Once $V_{DD}$ increases above $V_{IT}$, an internal timer delays the deassertion of the output to allow for a proper system reset before $\overline{\text{RESET}}$ transitions to a high state. The delay time ($t_d$) is 25 ms typical and starts after $V_{DD}$ rises above the $V_{IT}$. When the supply voltage drops below $V_{IT}$, the output transitions low again. All the devices of this family have a fixed threshold voltage set by an internal voltage divider.

The TPS3813xxx family incorporates a so-called window-watchdog timer, which has a programmable delay and window ratio. The supervised processor must trigger the WDI pin of the TPS3813xxx within the user-programmable window to keep $\overline{\text{RESET}}$ from asserting. The upper limit of the watchdog time-out can be set by either connecting WDT to GND, $V_{DD}$, or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or $V_{DD}$.

## 8.2 Functional Block Diagram
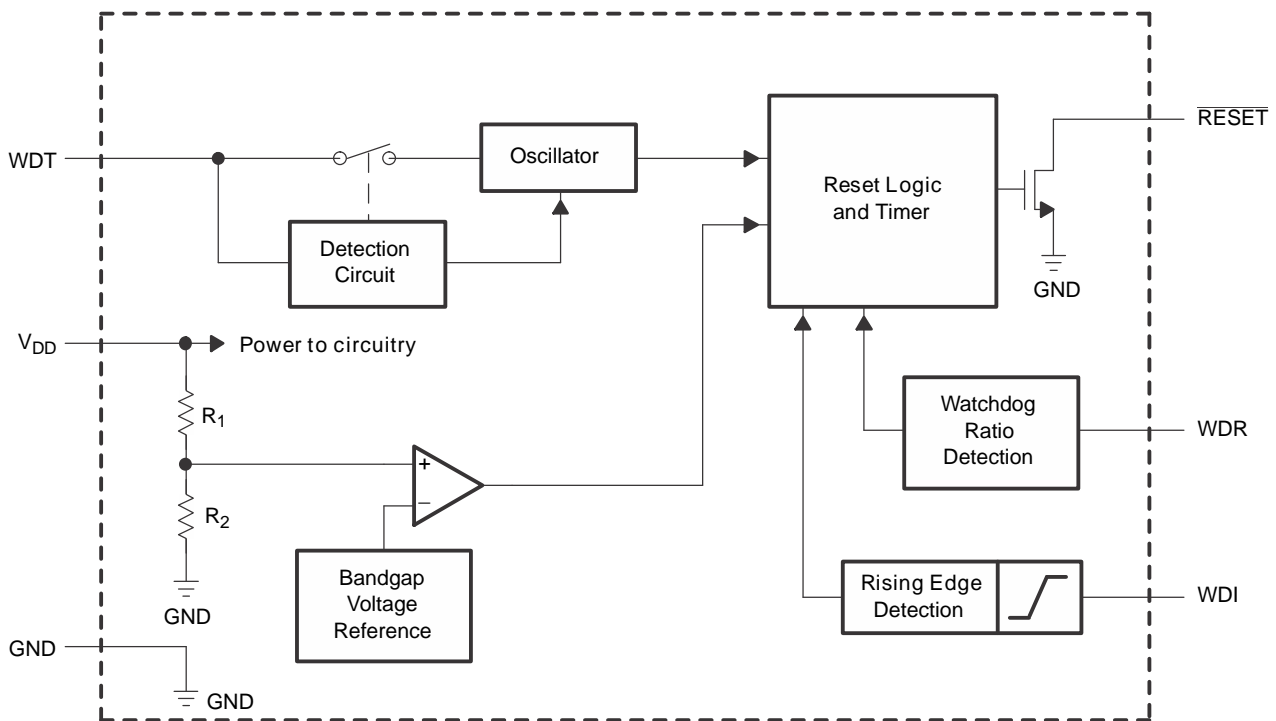


Copyright © 2016, Texas Instruments Incorporated

## 8.3 Feature Description

The TPS3813xxx family incorporates both a voltage supervisor and a window-watchdog timer into a single device. The device monitors the input voltage and the supervised processor must trigger the WDI pin of the TPS3813xxx within the user-programmable window to keep RESET from asserting.

## Feature Description (continued)

### 8.3.1 User-Programmable Watchdog Timer (WDI)

The TPS3813xxx family of devices have a watchdog timer that must be periodically triggered by either a positive or negative transition at the WDI pin to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$, $\overline{\text{RESET}}$ becomes asserts for the time period $t_d$. This event also reinitializes the watchdog timer. After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. After the first WDI low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses must fit into the configured window frame.

Both the upper and lower boundary of the window can be adjusted by the user. See *Programming* for more details on how to set the upper and lower boundaries of the window.

### 8.3.2 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$ remains high (deasserted) as long as $V_{DD}$ is above the threshold voltage ($V_{IT}$) and the user-programable watchdog timer criteria are met. If $V_{DD}$ falls below the $V_{IT}$ or if WDI is not triggered within the appropriate window, then RESET is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

When $V_{DD}$ is once again above $V_{IT}$, a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period ($t_d$) which is 25 ms typical. When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. RESET can be pulled up to any voltage up to 6 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor value and consider the required low-level output voltage ($V_{OL}$), the output capacitive loading, and the output leakage current.

## 8.4 Device Functional Modes

Table 1 summarizes the various functional modes of the device.

**Table 1. TPS3813xxx Function/Truth Table**

| $V_{DD}$ | WDI | $\overline{\text{RESET}}$ |
|---|---|---|
| $V_{DD} < V_{POR}$ | — | Undefined |
| $V_{POR} < V_{DD} < V_{IT}$ | — | L |
| $V_{DD} > V_{IT}$ | Outside window | L |
| $V_{DD} > V_{IT}$ | Inside window | H |

### 8.4.1 Normal Operation ($V_{DD} > V_{IT}$)

When $V_{DD}$ is greater than $V_{IT}$, the $\overline{\text{RESET}}$ signal is determined by the last WDI pulse.
- WDI pulse inside window: as long as pulses occur within the user-programmable window, the $\overline{\text{RESET}}$ signal remains high.
- WDI pulse outside window: if a pulse occurs outside the user-programmable window or not at all, the $\overline{\text{RESET}}$ signal goes low.

### 8.4.2 Above Power-On Reset But Less Than Threshold ($V_{POR} < V_{DD} < V_{IT}$)

When the voltage on $V_{DD}$ is less than the $V_{IT}$ voltage, and greater than the power-on reset voltage ($V_{POR}$), the $\overline{\text{RESET}}$ signal is asserted regardless of the WDI signal.

### 8.4.3 Below Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on $V_{DD}$ is lower than $V_{POR}$, the device does not have enough voltage to internally pull the asserted output low, and $\overline{\text{RESET}}$ is undefined and must not be relied upon for proper device function.

Product Folder Links: *TPS3813J25  TPS3813L30  TPS3813K33  TPS3813I50*

## 8.5 Programming

### 8.5.1 Implementing Window-Watchdog Settings

There are two ways to configure the watchdog timer window the most flexible is to connect a capacitor to WDT to set the upper boundary of the window watchdog while connecting WDR to either $V_{DD}$ or GND, thus setting the lower boundary. The other way to configure the timing is by wiring the WDT and WDR pin to either $V_{DD}$ or GND. By hardwiring the pins to either $V_{DD}$ or GND there are four different timings available; these settings are listed in Table 2.

**Table 2. Cap-Free Timer Settings**

| SELECTED OPERATION MODE | | WINDOW FRAME | LOWER WINDOW FRAME |
|---|---|---|---|
| WDT = 0 V | WDR = 0 V | Max = 0.3 s | Max = 9.46 ms |
| | | Typ = 0.25 s | Typ = 7.86 ms |
| | | Min = 0.2 s | Min = 6.27 ms |
| | WDR = $V_{DD}$ | Max = 0.3 s | Max = 2.43 ms |
| | | Typ = 0.25 s | Typ = 2 ms |
| | | Min = 0.2 s | Min = 1.58 ms |
| WDT = $V_{DD}$ | WDR = 0 V | Max = 3 s | Max = 93.8 ms |
| | | Typ = 2.5 s | Typ = 78.2 ms |
| | | Min = 2 s | Min = 62.5 ms |
| | WDR = $V_{DD}$ | Max = 3 s | Max = 23.5 ms |
| | | Typ = 2.5 s | Typ = 19.6 ms |
| | | Min = 2 s | Min = 15.6 ms |

To visualize the values named in the table, a timing diagram was prepared. It is used to describe the upper and lower boundary settings. For an application, the important boundaries are the $t_{boundary,max}$ and $t_{window,min}$. Within these values, the watchdog timer must be retriggered to avoid a time-out condition or a boundary violation in the event of a trigger pulse in the lower boundary. The values in the table above are typical and worst-case conditions. They are valid over the whole temperature range of –40°C to +85°C.

In the shaded area of Figure 7, it cannot be predicted if the device detects a violation or not and release a reset. This is also the case between the boundary tolerance of $t_{boundary,min}$ and $t_{boundary,max}$ as well as between $t_{window,min}$ and $t_{window,max}$. It is important to set up the trigger pulses accordingly to avoid violations in these areas.
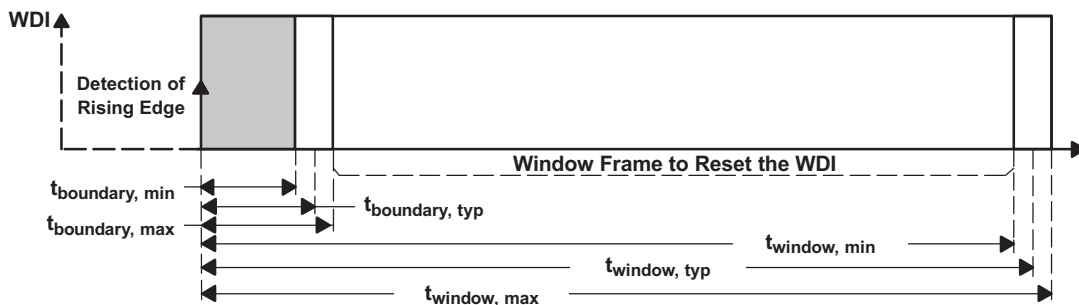


**Figure 7. Upper and Lower Boundary Visualization**

### 8.5.2 Programmable Window-Watchdog by Using an External Capacitor

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. They must have low ESR and low tolerances because the tolerances have to be considered if the calculations are performed. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the $t_{boundary,max}$ and $t_{window,min}$. The trigger pulse has to fit into this window frame.

The external capacitor must have a value between a minimum of 155 pF and a maximum of 63 nF.

**Table 3. Setting Upper Window Using External Capacitor**

| SELECTED OPERATION MODE | | WINDOW FRAME |
|---|---|---|
| WDT = external capacitor $C_{(ext)}$ | WDR = 0 V and WDR = $V_{DD}$ | $t_{window,max} = 1.25 \times t_{window,typ}$ |
| | | $t_{window,min} = 0.75 \times t_{window,typ}$ |

$$t_{window,typ} = \left( \frac{C_{(ext)}}{15.55 \text{ pF}} + 1 \right) \times 6.25 \text{ ms}$$

(1)

### 8.5.3 Lower Boundary Calculation

The lower boundary can be calculated based on the values given in *Switching Characteristics*. Additionally, facts must be considered to verify that the lower boundary is where it is expected. Because the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin is considered at the next internal clock cycle. This happens regardless of the external source. Because the shift between internal and external clock is not known, it is best to consider the worst-case condition for calculating this value.

**Table 4. Setting Lower Boundary Using External Cap**

| SELECTED OPERATION MODE | | LOWER BOUNDARY OF FRAME |
|---|---|---|
| WDT = external capacitor $C_{(ext)}$ | WDR = 0 V | $t_{boundary,max} = t_{window,max} / 23.5$ |
| | | $t_{boundary,typ} = t_{window,typ} / 25.8$ |
| | | $t_{boundary,min} = t_{window,min} / 28.7$ |
| | WDR = $V_{DD}$ | $t_{boundary,max} = t_{window,max} / 51.6$ |
| | | $t_{boundary,typ} = t_{window,typ} / 64.5$ |
| | | $t_{boundary,min} = t_{window,min} / 92.7$ |

### 8.5.4 Watchdog Software Considerations

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, TI recommends that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses must be set to different timings inside the window frame to release a defined reset, if the program must hang in any subroutine. This allows the window watchdog to detect time-outs of the trigger pulse, as well as pulses that distort the lower boundary.

### 8.5.5 Power-Up Considerations

Many microcontrollers use general-purpose input and output (GPIO) pins that can be programmed to be either inputs or outputs. During power-up, these I/O pins are typically configured as inputs. If a GPIO pin is used to drive the WDI input pin of the TPS3813xxx, then a pulldown resistor (shown as R2 in Figure 8) must be added to keep the WDI pin from floating during power up.

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TPS3813xxx is a voltage supervisor that incorporates a window-watchdog timer, allowing for comprehensive supervision of microcontrollers and other similar devices. The TPS3813xxx can be operated from a VDD rail of 2 V to 6 V with a user-programmable watchdog time-out from 0.25 s to 2.5 s. The following sections describe how to properly use this device, depending on the requirements of the final application.

## 9.2 Typical Application

A typical application example (see Figure 8) is used to describe the function of the watchdog in more detail.

To configure the window watchdog function, two pins are provided by the TPS3813xxx. These pins set the window time-out and ratio.

The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. It can be configured in two different frame sizes.
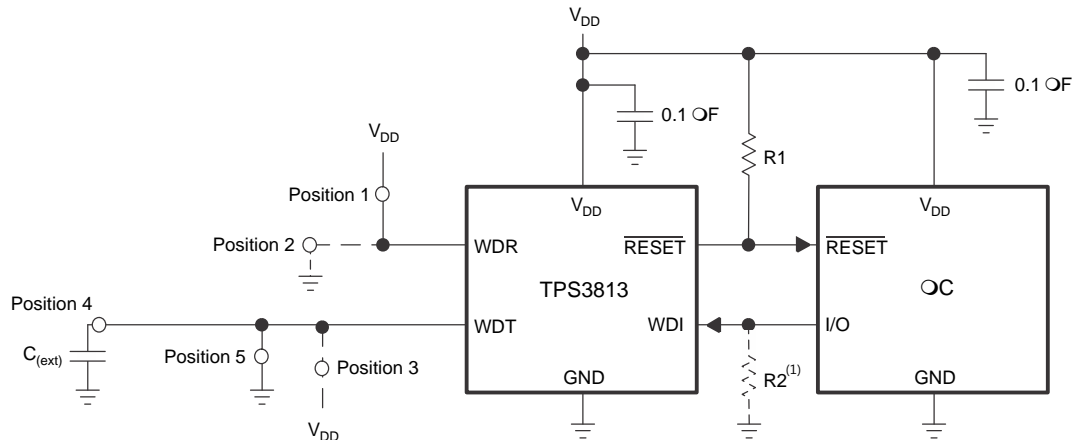


Copyright © 2016, Texas Instruments Incorporated

(1)  Use this pulldown resistor if a GPIO pin is used to drive the WDI input pin of the TPS3813xxx to keep the WDI pin from floating during power up.

**Figure 8. Application Example**

### 9.2.1 Design Requirements

The TPS3813xxx $\overline{RESET}$ output can be used to drive the $\overline{RESET}$ pin of a microcontroller to initiate a reset event. The $\overline{RESET}$ pin of the TPS3813xxx can be pulled high with a 1-MΩ resistor; the watchdog window timing is controlled by the WDT and WDR pins, and is set depending on the reset requirement times of the microprocessor.

### 9.2.2 Detailed Design Procedure

If the window watchdog ratio pin (WDR) is set to $V_{DD}$, Position 1 in Figure 8, then the lower window frame is a value based on a ratio calculation of the overall window time-out size: For the watchdog time-out pin (WDT) connected to GND, it is a ratio of 1:124.9, for WDT connected to $V_{DD}$, it is a ratio of 1:127.7, and for an external capacitor connected to WDT, it is a ratio of 1:64.5.

Product Folder Links: *TPS3813J25  TPS3813L30  TPS3813K33  TPS3813I50*

## Typical Application (continued)

If the window watchdog ratio pin (WDR) is set to GND, Position 2, the lower window frame is a value based on a ratio calculation of the overall window time-out size: For the watchdog time-out pin (WDT) connected to GND, it is a ratio of 1:31.8, for WDT connected to $V_{DD}$ it is 1:32, and for an external capacitor connected to WDT it is 1:25.8.

The watchdog time-out can be set in two fixed timings of 0.25 seconds and 2.5 seconds for the window or can by programmed by connecting a external capacitor with a low leakage current at WDT.

Example: If the watchdog time-out pin (WDT) is connected to $V_{DD}$, the time-out is 2.5 seconds. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to $V_{DD}$, the lower boundary is 19.6 ms.
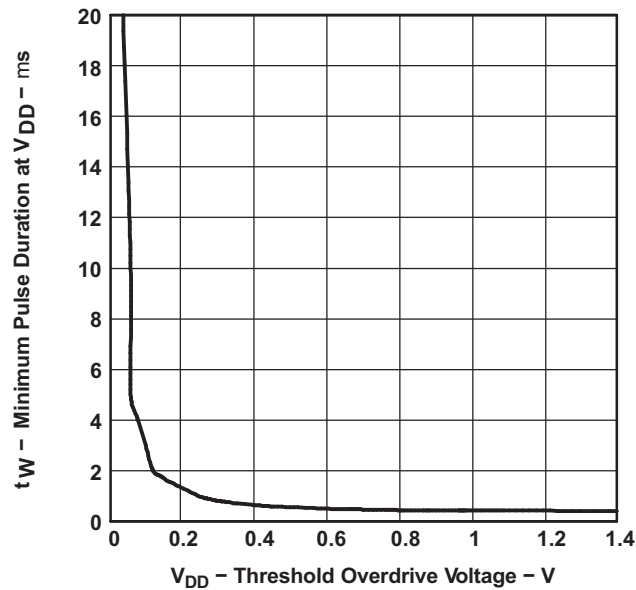
### 9.2.3  Application Curve



**Figure 9.  Minimum Pulse Duration at $V_{DD}$ vs $V_{DD}$ Threshold Overdrive Voltage**

## 10   Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 2 V to 6 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

In applications where the WDI input may experience a negative voltage while $V_{DD}$ is ramping from 0 V to 0.8 V, the $V_{DD}$ slew rate in this range must be greater than 10 V/s. A negative voltage on the WDI input along with a slew rate less than 10 V/s could result in a greatly reduced watchdog window time and reset output delay time.

## 11   Layout

### 11.1   Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic bypass capacitor near the VDD pin.
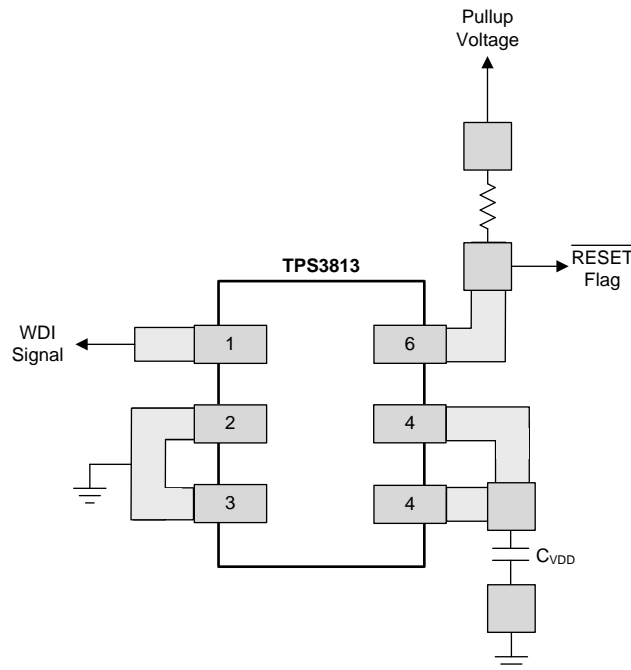
### 11.2   Layout Example



**Figure 10.  TPS3813xxx Layout Example**

Product Folder Links: *TPS3813J25  TPS3813L30  TPS3813K33  TPS3813I50*

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS3813J25 | Click here | Click here | Click here | Click here | Click here |
| TPS3813L30 | Click here | Click here | Click here | Click here | Click here |
| TPS3813K33 | Click here | Click here | Click here | Click here | Click here |
| TPS3813I50 | Click here | Click here | Click here | Click here | Click here |

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TEXAS INSTRUMENTS

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3813I50DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PFBI | Samples |
| TPS3813I50DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PFBI | Samples |
| TPS3813J25DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCDI | Samples |
| TPS3813J25DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCDI | Samples |
| TPS3813J25DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCDI | Samples |
| TPS3813K33DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PFAI | Samples |
| TPS3813K33DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PFAI | Samples |
| TPS3813K33DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PFAI | Samples |
| TPS3813K33DBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PFAI | Samples |
| TPS3813L30DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PEZI | Samples |
| TPS3813L30DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PEZI | Samples |
| TPS3813L30DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PEZI | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
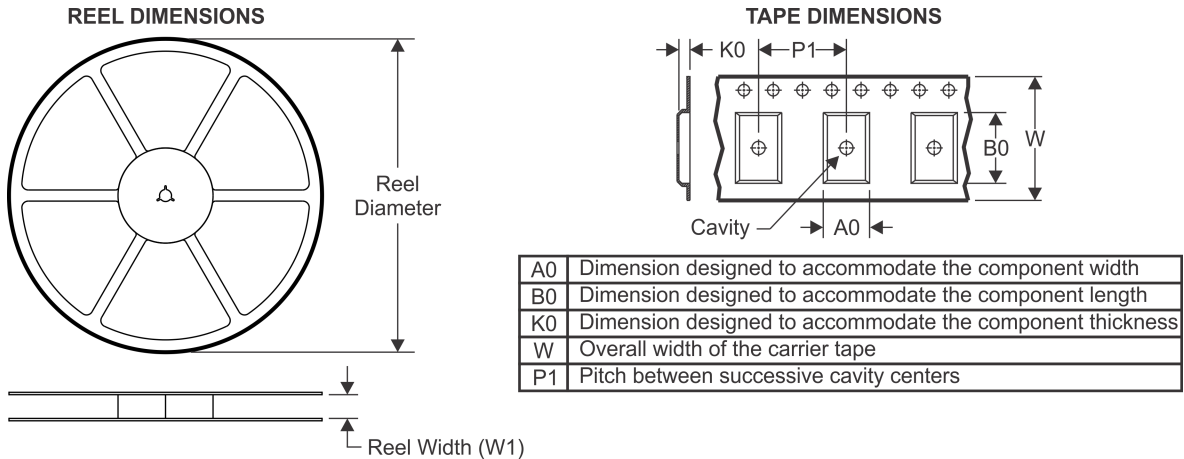
**OTHER QUALIFIED VERSIONS OF TPS3813 :**

- Automotive: TPS3813-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3813I50DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813I50DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813J25DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813J25DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813K33DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813K33DBVR | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3813K33DBVT | SOT-23 | DBV | 6 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3813K33DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813L30DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3813L30DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3813I50DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3813I50DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3813J25DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3813J25DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3813K33DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3813K33DBVR | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3813K33DBVT | SOT-23 | DBV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS3813K33DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3813L30DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3813L30DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |

3.0
2.6

1.75
1.45

B

A

PIN 1
INDEX AREA

1

2X 0.95

1.9

2

3

6

5

4

3.05
2.75

6X 0.50
0.25

⊕ 0.2 Ⓜ C A B

C

◻ 0.1 C

1.45 MAX

(1.1)

0.15 TYP
0.00

0.25
GAGE PLANE

0.22 TYP
0.08

8°
0°
TYP

0.6 TYP
0.3

SEATING PLANE
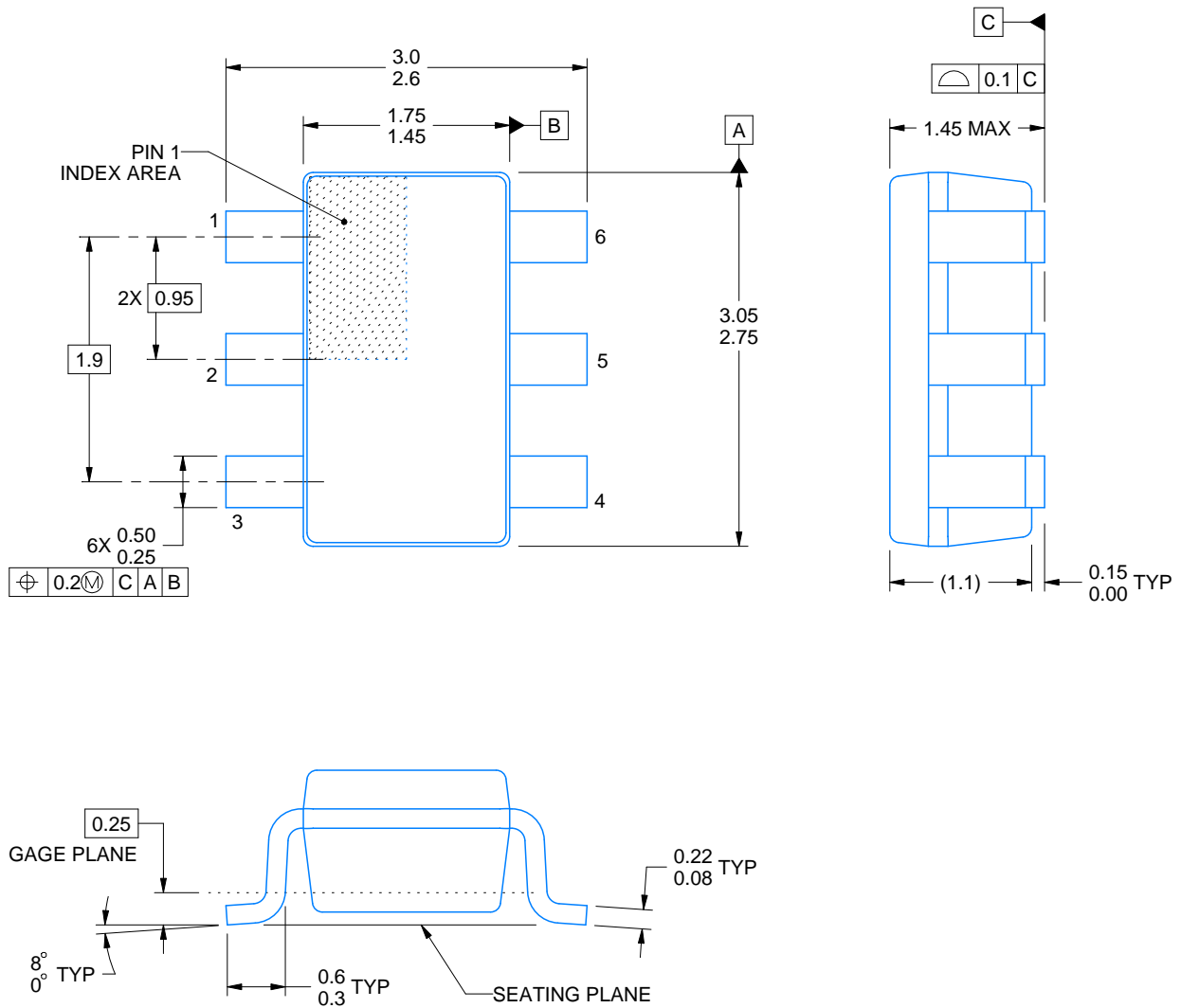
4214840/B   03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

**TEXAS INSTRUMENTS**
www.ti.com

6X (1.1)

PKG ℄

1

6X (0.6)

6

SYMM ℄

2

5

2X (0.95)

3

4

(R0.05) TYP

(2.6)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED
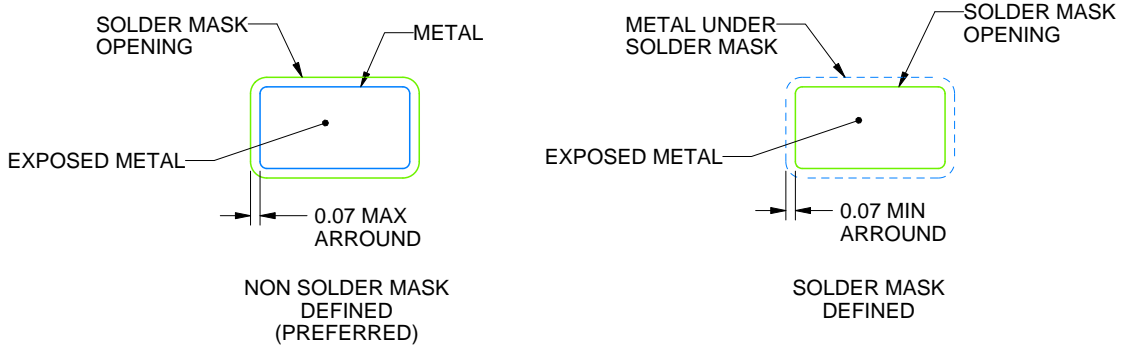
**SOLDER MASK DETAILS**

4214840/B   03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

6X (1.1)

1

6X (0.6)

2

2X(0.95)

3

6

SYMM

5

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B   03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.