SLVS367A − MARCH 2001 − REVISED JUNE 2001

SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DRIVE REGULATOR

FEATURES

- **Integrated Drive Regulator (4 V to 14 V)**
- **Adjustable/Adaptive Dead-Time Control**
- **4-A Peak current at VDRV of 14 V**
- **10-V to 15-V Supply Voltage Range**
- **TTL-Compatible Inputs**
- **Internal Schottky Diode Reduces Part Count**
- **Synchronous or Nonsynchronous Operation**
- **Inverting and Noninverting Options**
- **TSSOP PowerPad™ Package for Excellent Thermal Performance**

APPLICATIONS

- **Single or Multiphase Synchronous-Buck Power Supplies**
- **High-Current DC/DC Power Modules**

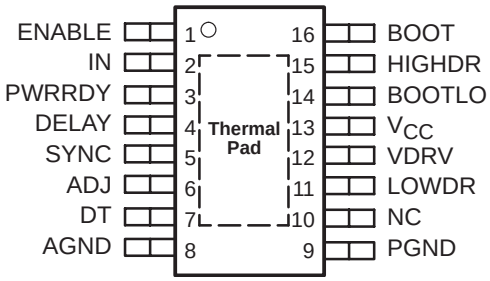
DESCRIPTION

The TPS2838/39/48/49 devices are MOSFET drivers designed for high-performance synchronous power supplies. The drivers can source and sink up to 4-A peak current at a 14-V drive voltage. These are ideal devices to use with power supply controllers that do not have on-chip drivers. The low-side driver is capable of driving loads of 3.3 nF in 10-ns rise/fall times and has 40-ns propagation delays at room temperature.

The MOSFET drivers have an integrated 150-mA regulator, so the gate drive voltage can be optimized for specific MOSFETs. The TPS2848 and TPS2849 have a fixed 8-V drive regulator, while the TPS2838/39 allow the drive regulator to be adjusted from 4 V to 14 V by selection of two external resistors.

The devices feature VDRV to PGND shoot-through protection with adaptive/adjustable deadtime control. The deadtime, for turning on the high-side FET from LOWDR transitioning low, is adjustable with an external capacitor on the DELAY pin. This allows compensation for the effect the gate resistor has on the synchronous FET turn off. The adaptive deadtime prevents the turning on of the low-side FET until the voltage on the BOOTLO pin falls below a threshold after the high-side FET stops conducting. The high-side drive can be configured as a ground referenced driver or a floating bootstrap driver. The internal Schottky diode minimizes the size and number of external components needed for the bootstrap driver circuit. Only one external ceramic capacitor is required to configure the bootstrap driver.

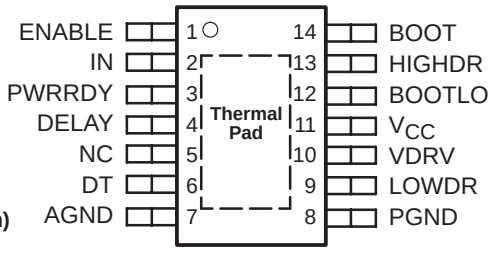
TPS2838, TPS2839
PWP PACKAGE
(TOP VIEW)



ACTUAL SIZE
(5,1 mm x 6,6 mm)

ACTUAL SIZE
(5,1 mm x 6,6 mm)

TPS2848, TPS2849
PWP PACKAGE
(TOP VIEW)



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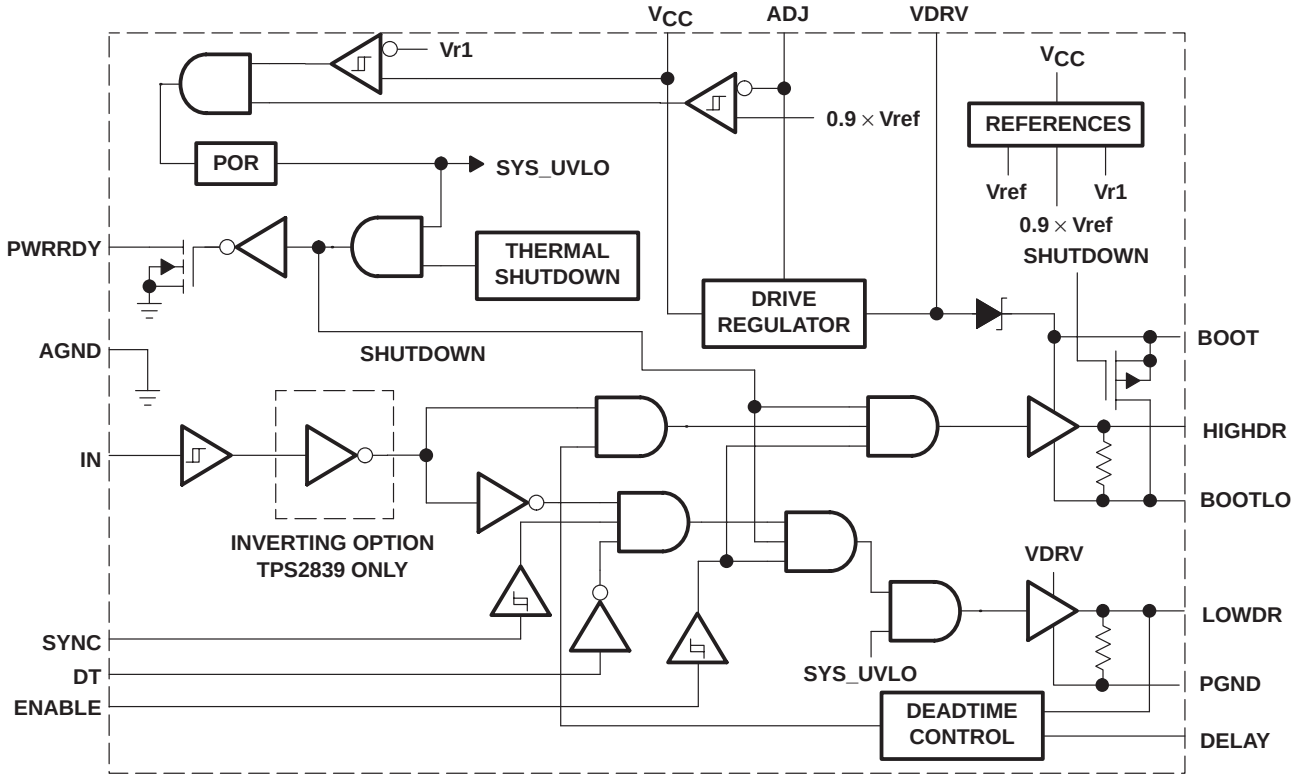
description (continued)

The SYNC pin can be used regardless of load to disable the synchronous FET driver and operate the power supply nonsynchronously.

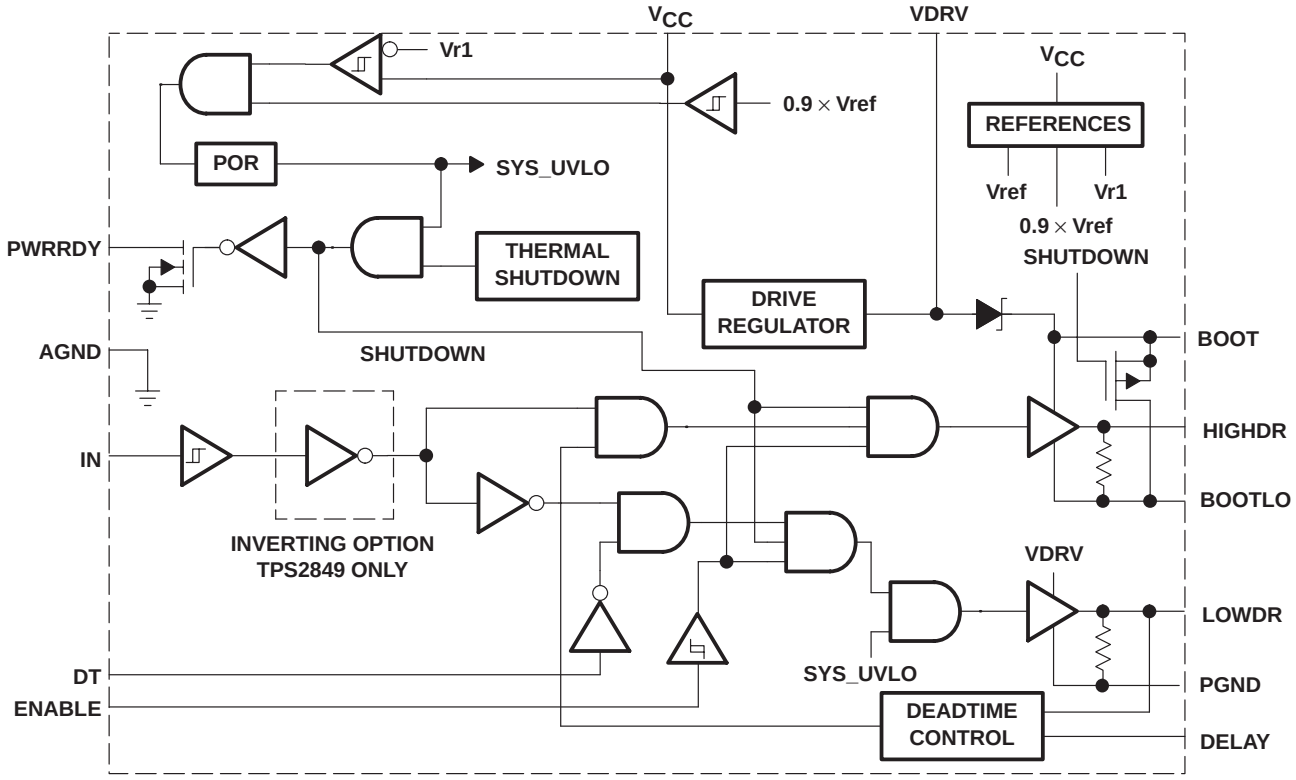
A power ready/undervoltage lockout function outputs the status of the V_{CC}-pin voltage and driver regulator output on the open-drain PWRRDY pin. This feature can be used to enable a controller's output once the V_{CC} voltage reaches the threshold and the regulator output is stable. This function ensures both FET drivers are off when the V_{CC} voltage is below the voltage threshold.

The TPS2838/39/48/49 devices are offered in the thermally enhanced 14-pin and 16-pin PowerPAD TSSOP package. The PowerPAD package features an exposed leadframe on the bottom that can be soldered to the printed-circuit board to improve thermal efficiency. The TPS2838/48 are noninverting control logic while the TPS2839/49 drivers are inverting control logic.

functional block diagram (TPS2838, TPS2839)



functional block diagram (TPS2848, TPS2849)



Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.		
	TPS283x	TPS284x	
ADJ	6	—	Adjust. The adjust pin is the feedback pin for the drive regulator (TPS283X only)
AGND	8	7	Analog ground
BOOT	16	14	Bootstrap. A capacitor is connected between the BOOT and BOOTLO pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 μF and 1 μF.
BOOTLO	14	12	Boot low. This pin connects to the junction of the high-side and low-side MOSFETs.
DELAY	4	4	Delay. Connecting a capacitor between this pin and ground adjusts the deadtime for high-side driver
DT	7	6	Deadtime control. Connect DT to the junction of the high-side and low-side MOSFETs
ENABLE	1	1	Enable. If ENABLE is low, both drivers are off.
HIGHDR	15	13	High drive. This pin is the output drive for the high-side power MOSFET.
IN	2	2	Input. This pin is the input signal to the MOSFET drivers.
LOWDR	11	9	Low drive. This pin is the output drive for the low-side power MOSFET.
NC	10	5	No internal connection
PGND	9	8	Power ground. This pin is connected to the FET power ground.
PWRRDY	3	3	Power ready. This open-drain pin indicates a power good for VDRV and V_{CC}.
SYNC	5	—	Synchronous rectifier enable. If SYNC is low, the low-side driver is always off; if SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
V_{CC}	13	11	Input power supply. It is recommended that a capacitor (minimum 1 μF) be connected from V_{CC} to PGND. Note that V_{CC} must be 2 V higher than VDRV.
VDRV	12	10	Drive regulator output voltage. It is recommended that a capacitor (minimum 1 μF) be connected from VDRV to PGND. Note that V_{CC} must be 2 V higher than VDRV.

detailed description

low-side driver

The low-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 4 A, source and sink.

high-side driver

The high-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 4 A minimum, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating-bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

dead-time (DT) control

Dead-time control prevents shoot-through current from flowing through the main power FETs during switching transitions by controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (BOOTLO) is low. The TTL-compatible DT terminal connects to the junction of the power FETs.

ENABLE

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low. ENABLE is a TTL-compatible digital terminal.

detailed description (continued)

IN

The IN terminal is a TTL-compatible digital terminal that is the input control signal for the drivers. The TPS2838/48 have noninverting inputs; the TPS2839/49 have inverting inputs. On the TPS2838 and TPS2848, a high on IN results in a high on HIGHDR. On the TPS2839 and TPS2849, a high on IN results in a low on HIGHDR.

SYNC (TPS283x only)

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off. SYNC is a TTL-compatible digital terminal.

PWRRDY

Depicts the status of the V_{CC} pin voltage and the driver regulator output on the open-drain PWRRDY pin.

DELAY

Adjustable high-side turnon delay from from when the low-side FET is turned off.

ADJ (TPS283x only)

Input for adjusting the driver regulator output. See the *application information* section for the adjustment formula.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.3 V to 16 V
Input voltage range:	ADJ	−0.3 V to 7 V
	BOOT to PGND (high-side driver ON)	−0.3 V to 30 V
	BOOTLO to PGND	−0.3 V to 16 V
	BOOT to BOOTLO	−0.3 V to 16 V
	ENABLE, IN, and SYNC	−0.3 V to 16 V
	VDRV, PWRRDY, and DELAY	−0.3 V to 16 V
	DT	−0.3 V to 16 V
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		−40°C to 125°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to PGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
14-pin PWP with solder‡	2668	26.68 mW/°C	1467	1067
14-pin PWP without solder‡	1024	10.24 mW/°C	563	409
16-pin PWP with solder‡	2739	27.39 mW/°C	1506	1095
16-pin PWP without solder‡	1108	11.08 mW/°C	609	443

JUNCTION-CASE THERMAL RESISTANCE TABLE

14-pin PWP	Junction-case thermal resistance	2.07 °C/W
16-pin PWP	Junction-case thermal resistance	2.07 °C/W

‡ Test Board Conditions:
1. Thickness: 0.062″
2. 3″ × 3″ (for packages < 27 mm long)
3. 4″ × 4″ (for packages > 27 mm long)
4. 2-oz copper traces located on the top of the board (0,071 mm thick)
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1-oz copper (0,036 mm thick)
7. Thermal vias, 0,33 mm diameter, 1,5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief literature number SLMA002.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		10		15	V
Input voltage, V_I	BOOT to PGND	10		29	V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Quiescent current	$V_{(ENABLE)}$ = Low,	V_{CC} = 13 V			425	µA
		$V_{(ENABLE)}$ = High,	V_{CC} = 13 V			1	mA

NOTE 2: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

dead-time control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH(LOWDR)}$	LOWDR high-level input voltage	Over full VDRV range See Note 2	50			%VDRV
$V_{IL(LOWDR)}$	LOWDR low-level input voltage	Over full VDRV range See Note 2			1	V
$V_{IH(DT)}$	DT high-level input voltage	Over full V_{CC} range	2			V
$V_{IL(DT)}$	DT low-level input voltage	Over full V_{CC} range			1	V
	Deadtime delay	$V_{(VDRV)}$ = 4 V to 14 V See Note 2	0.5	1	1.5	ns/pF
	Driver nonoverlap time (DT to LOWDR)	$V_{(VDRV)}$ = 4.5 V, T_J = 25°C, See Note 2	30		150	ns
		$V_{(VDRV)}$ = 14.5 V, T_J = 25°C, See Note 2	30		100	ns
	Driver nonoverlap time (LOWDR to HIGHDR)	$V_{(VDRV)}$ = 4.5 V, T_J = 25°C, $C_{L(Delay)}$ = 50 pF See Note 2	75		180	ns
		$V_{(VDRV)}$ = 14.5 V, T_J = 25°C, $C_{L(Delay)}$ = 50 pF See Note 2	58		125	
	Driver nonoverlap time (LOWDR to HIGHDR)	$V_{(VDRV)}$ = 4.5 V, T_J = 25°C, $C_{L(Delay)}$ = 0 pF See Note 2	50		125	ns
		$V_{(VDRV)}$ = 14.5 V, T_J = 25°C, $C_{L(Delay)}$ = 0 pF See Note 2	30		100	

NOTE 2: Ensured by design, not production tested.

high-side driver

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Peak output current	$V_{(BOOT)} - V_{(BOOTLO)}$ = 4 V, See Note 2	$V_{(HIGHDR)}$ = 0.5 V (src)	1	1.3		A
			$V_{(HIGHDR)}$ = 4 V (sink)	2	2.4		
		$V_{(BOOT)} - V_{(BOOTLO)}$ = 8 V, See Note 2	$V_{(HIGHDR)}$ = 0.5 V (src)	2	2.4		
			$V_{(HIGHDR)}$ = 8 V (sink)	2	3.3		
		$V_{(BOOT)} - V_{(BOOTLO)}$ = 14 V, See Note 2	$V_{(HIGHDR)}$ = 0.5 V (src)	2	3.9		
			$V_{(HIGHDR)}$ = 14 V (sink)	2	4.4		
r_o	Output resistance	$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V T_J = 25°C	$V_{(HIGHDR)}$ = 4 V (src)			45	Ω
			$V_{(HIGHDR)}$ = 0.5 V (sink)			6	
		$V_{(BOOT)} - V_{(BOOTLO)}$ = 7.5 V, T_J = 25°C	$V_{(HIGHDR)}$ = 7 V (src)			26	
			$V_{(HIGHDR)}$ = 0.5 V (sink)			5	
		$V_{(BOOT)} - V_{(BOOTLO)}$ = 11.5 V, T_J = 25°C	$V_{(HIGHDR)}$ = 11 V (src)			20	
			$V_{(HIGHDR)}$ = 0.5 V (sink)			4	
	HIGHDRV-to-BOOTLO resistor				250		kΩ
t_r/t_f	Rise and fall time (see Notes 2 and 3)	C_L = 3.3 nF, $V_{(BOOTLO)}$ = GND, T_J = 125°C	$V_{(BOOT)}$= 4 V			85	ns
			$V_{(BOOT)}$= 8 V			70	
			$V_{(BOOT)}$= 14 V			65	
		C_L = 10 nF, $V_{(BOOTLO)}$ = GND, T_J = 125°C	$V_{(BOOT)}$= 4 V			170	
			$V_{(BOOT)}$= 8 V			140	
			$V_{(BOOT)}$= 14 V			100	
t_{PHL}	Propagation delay time, HIGHDR going low (excluding deadtime)	$V_{(BOOTLO)}$ = GND, T_J = 125°C, See Notes 2 and 3	$V_{(BOOT)}$ = 4 V			120	ns
			$V_{(BOOT)}$= 8 V			100	
			$V_{(BOOT)}$= 14 V			80	

NOTES: 2: Ensured by design, not production tested.

3. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $r_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

low-side driver

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Peak output current	$V_{(VDRV)}$ = 4 V, T_J = 25°C, See Note 2	$V_{(LOWDR)}$ = 0.5 V (src)	1	1.6		A
			$V_{(LOWDR)}$ = 4 V (sink)	2	2.4		
		$V_{(VDRV)}$ = 8 V, T_J = 25°C, See Note 2	$V_{(HIGHDR)}$ = 0.5 V (src)	2	2.4		
			$V_{(HIGHDR)}$ = 8 V (sink)	2	3.3		
		$V_{(VDRV)}$ = 14 V (src), T_J = 25°C, See Note 2	$V_{(HIGHDR)}$ = 0.5 V (src)	2	3.9		
			$V_{(HIGHDR)}$ = 14 V (sink)	2	4.4		
r_o	Output resistance	$V_{(VDRV)}$ = 4.5 V, T_J = 25°C	$V_{(LOWDR)}$ = 4 V (src)			30	Ω
			$V_{(LOWDR)}$ = 0.5 V (sink)			8	
		$V_{(VDRV)}$ = 7.5 V, T_J = 25°C	$V_{(LOWDR)}$ = 7 V (src)			25	
			$V_{(LOWDR)}$ = 0.5 V (sink)			7	
		$V_{(VDRV)}$= 11.5 V, T_J = 25°C	$V_{(LOWDR)}$ = 11 V (src)			22	
			$V_{(LOWDR)}$ = 0.5 V (sink)			6	
	LOWDR-to-PGND resistor				250		kΩ
t_r/t_f	Rise and fall time	C_L = 3.3 nF, T_J = 125°C, See Note 2	$V_{(VDRV)}$ = 4 V			60	ns
			$V_{(VDRV)}$ = 8 V			50	
			$V_{(VDRV)}$ = 14 V			40	
		C_L = 10 nF, T_J = 125°C, See Note 2	$V_{(VDRV)}$ = 4 V			110	
			$V_{(VDRV)}$ = 8 V			100	
			$V_{(VDRV)}$ = 14 V			80	
t_{PLH}	Propagation delay time, LOWDR going high (excluding deadtime)	T_J = 125°C, See Notes 2 and 3	$V_{(VDRV)}$ = 4 V			110	ns
			$V_{(VDRV)}$ = 8 V			90	ns
			$V_{(VDRV)}$ = 14 V			80	ns

NOTES: 2: Ensured by design, not production tested.
3: The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $r_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

V_{CC} undervoltage lockout

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Start threshold voltage				10.3	V
	Stop threshold voltage		7.5			V
V_{hys}	Hysteresis voltage		1	1.5		V
t_{pd}	Propagation delay time	50-mV overdrive, See Note 2		300	1000	ns
t_d	Falling-edge delay time	See Note 2	2		5	us

NOTE 2: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 12 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

digital control (IN, ENABLE, SYNC)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	IN	Over full V_{CC} range	2			V
		ENABLE, SYNC	Over full V_{CC} range	2.2			V
V_{IL}	Low-level input voltage	IN	Over full V_{CC} range			1	V
		ENABLE, SYNC	Over full V_{CC} range			1	V
	ENABLE propagation delay time		See Note 2	2		7	µs

NOTE 2: Ensured by design, not production tested.

thermal shutdown

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal shutdown	See Note 2	155	170	185	°C
t_d	Falling edge delay time	See Note 2	10		20	µs

NOTE 2: Ensured by design, not production tested.

drive regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Recommended output voltage		4		14	V
V_O	Output voltage	V_{CC} = 10 V to 15 V, I_O = 5 mA to 150 mA	−2		2	%nom
V_{ref}	Reference voltage	V_{CC} = 10 V to 15 V		1.235		V
	Dropout voltage	V_{CC} = 10 V, I_O = 150 mA See Note 2		1000	1100	mV
	Line regulation	V_{CC} = 10 V to 15 V, I_O = 5 mA		0.2		%/V
	Load regulation	V_{CC} = 10 V, I_O = 5 mA to 150 mA		2		%
	Current limit	V_{CC} = 8 V		0.5	0.6	A
	PWRRDY saturation voltage	I_O = 5 mA			0.8	V
I_{lkg}	Leakage current	$V_{I(PWRRDY)}$ = 4.5 V			1	µA

drive regulator undervoltage lockout

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Start threshold voltage	See Note 2			85	%Vref
	Stop threshold voltage	See Note 2	80			%Vref
V_{hys}	Hysteresis voltage	See Note 2	2.5	5		%Vref
t_{pd}	Propagation delay time	50-mV overdrive, See Note 2		300	1000	ns
	Falling-edge delay time	See Note 2	2		5	µs
	Power on reset time	See Note 2		100	1000	µs

NOTE 2: Ensured by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

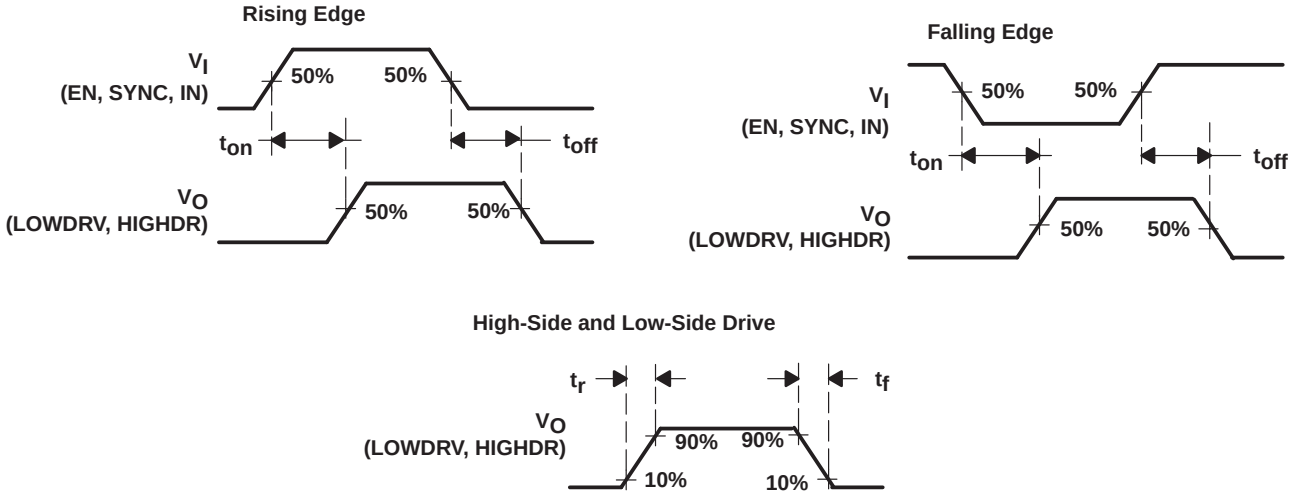


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS

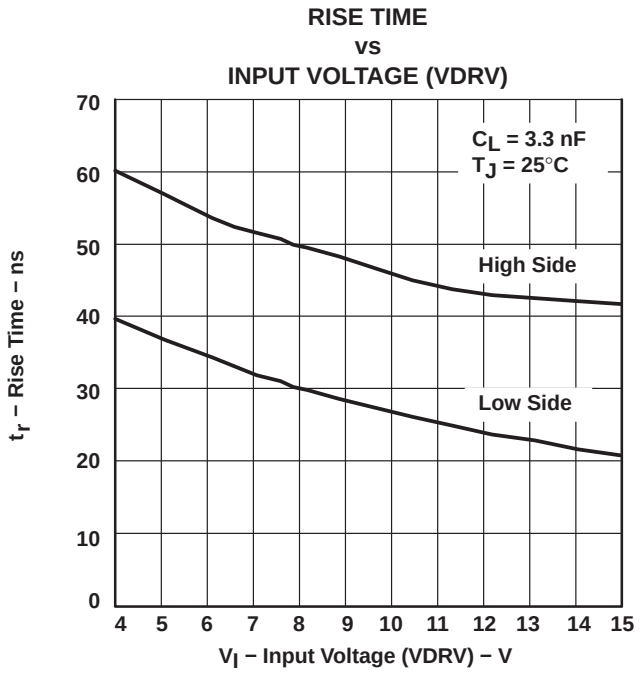


Figure 2

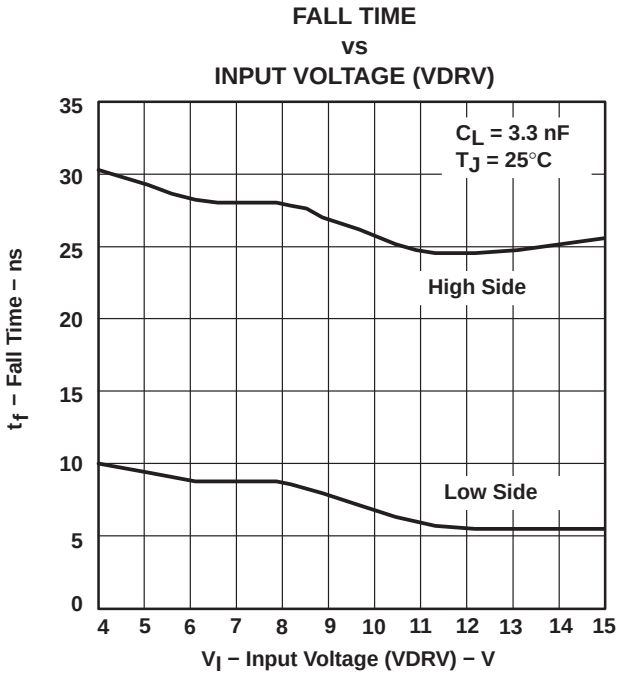


Figure 3

TYPICAL CHARACTERISTICS

RISE TIME
vs
JUNCTION TEMPERATURE

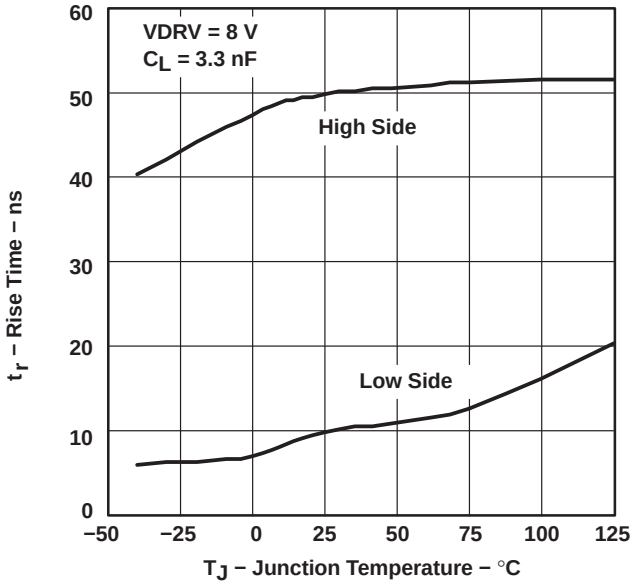


Figure 4

FALL TIME
vs
JUNCTION TEMPERATURE

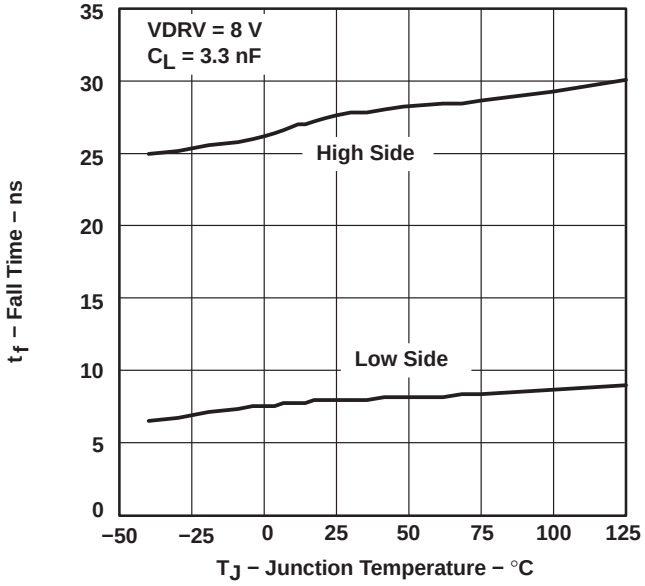


Figure 5

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
INPUT VOLTAGE (VDRV)

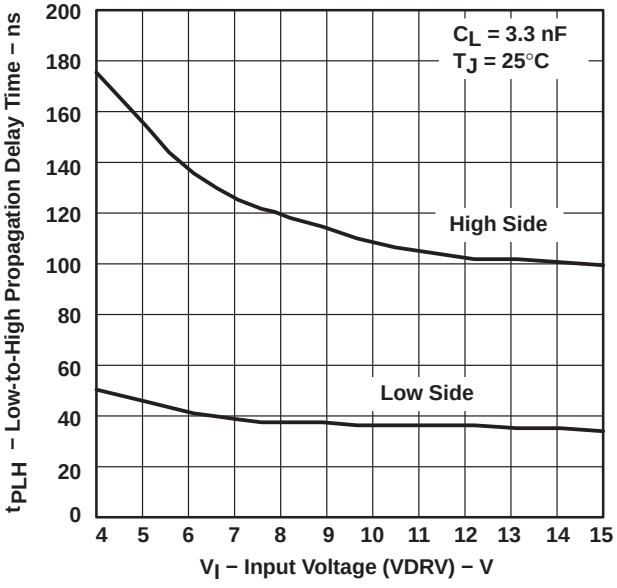


Figure 6

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
INPUT VOLTAGE (VDRV)

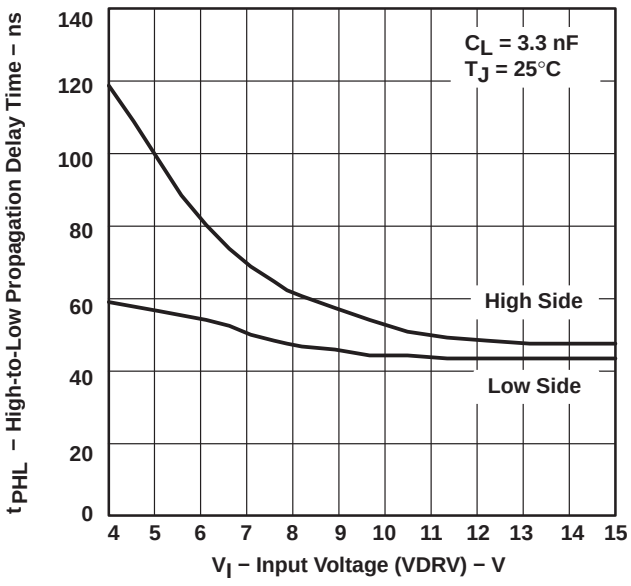


Figure 7

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME vs JUNCTION TEMPERATURE

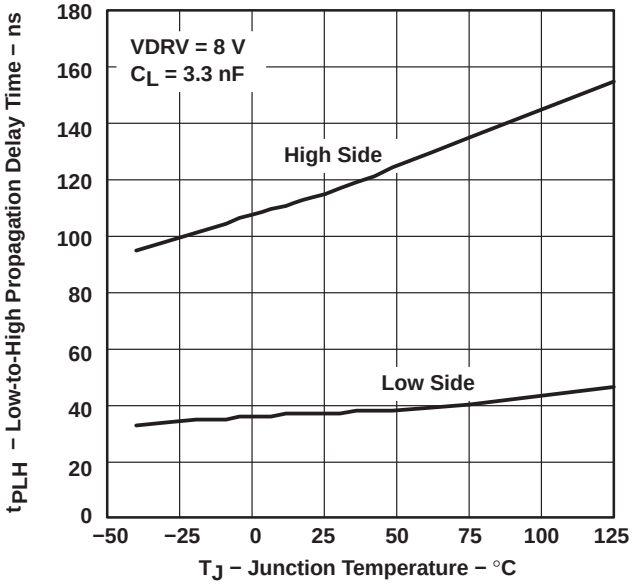


Figure 8

HIGH-TO-LOW PROPAGATION DELAY TIME vs JUNCTION TEMPERATURE

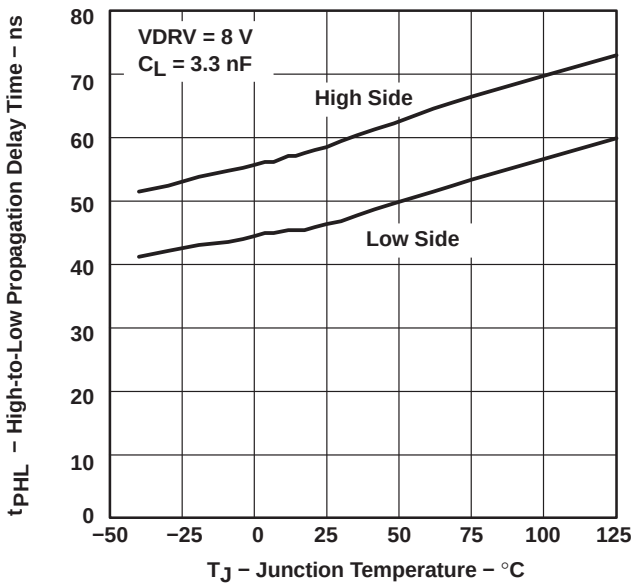


Figure 9

DRIVER-OUTPUT RISE TIME vs LOAD CAPACITANCE

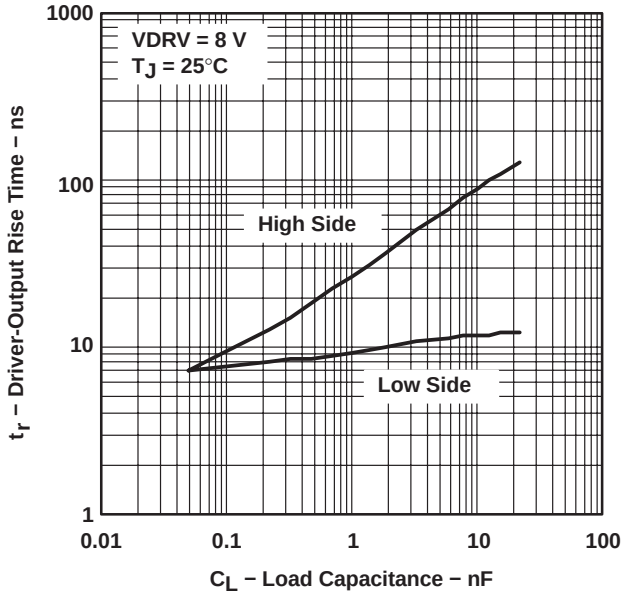


Figure 10

DRIVER-OUTPUT FALL TIME vs LOAD CAPACITANCE

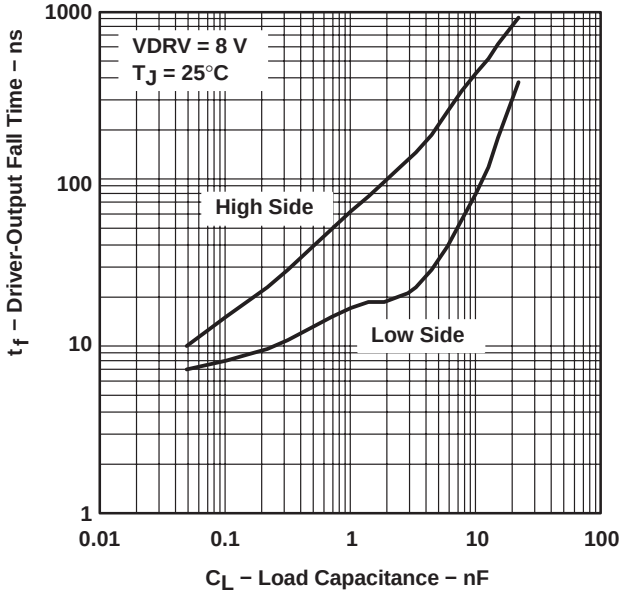


Figure 11

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
INPUT VOLTAGE (VDRV)

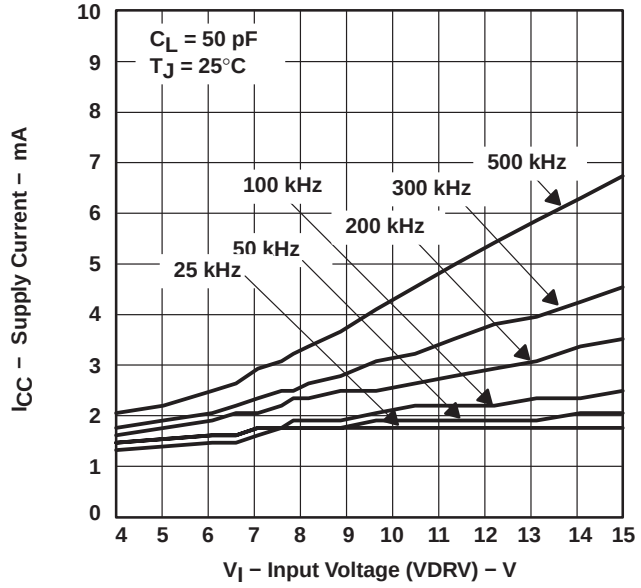


Figure 12

SUPPLY CURRENT
vs
INPUT VOLTAGE (VDRV)

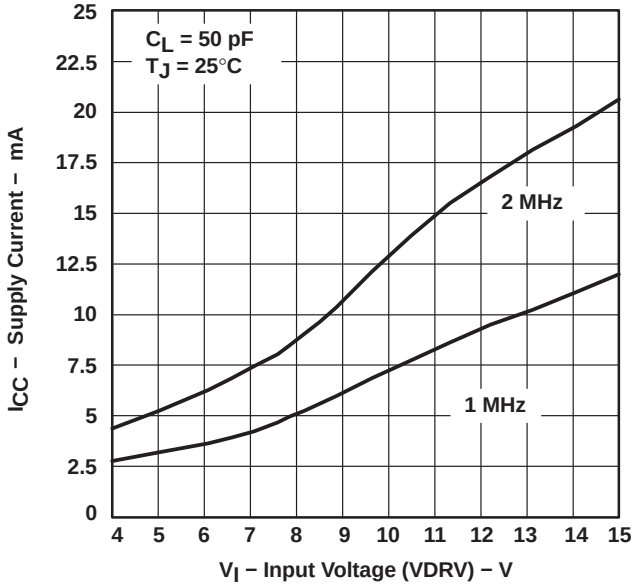


Figure 13

PEAK SOURCE CURRENT
vs
INPUT VOLTAGE (VDRV)

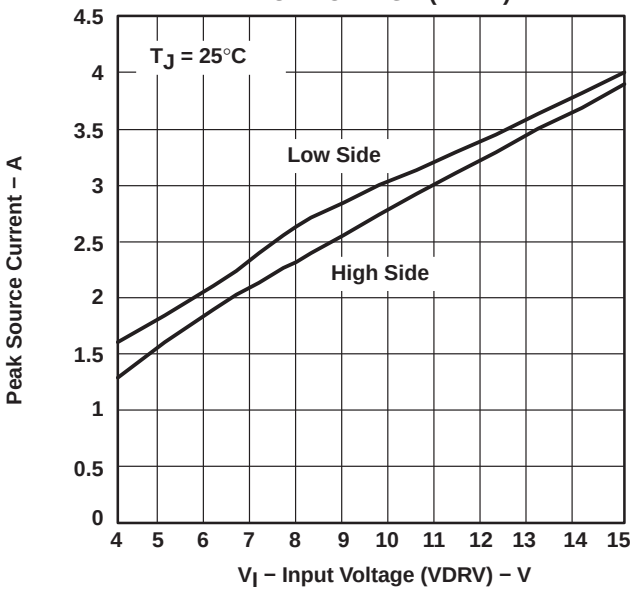


Figure 14

PEAK SINK CURRENT
vs
INPUT VOLTAGE (VDRV)

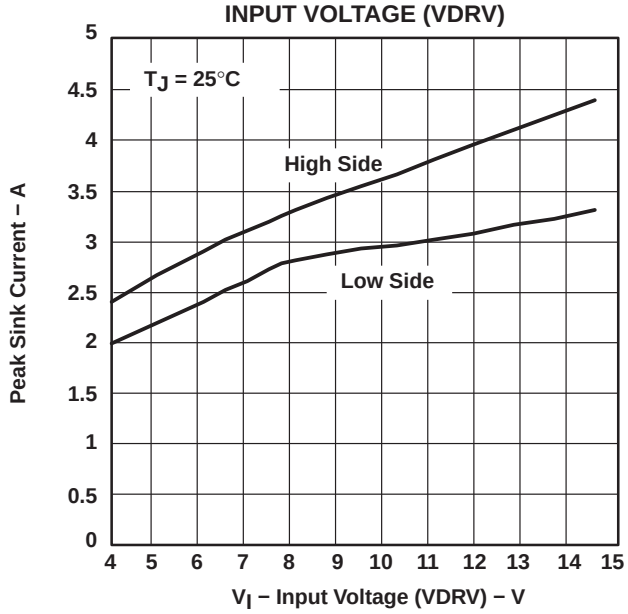


Figure 15

TYPICAL CHARACTERISTICS

START/STOP V_{CC} UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

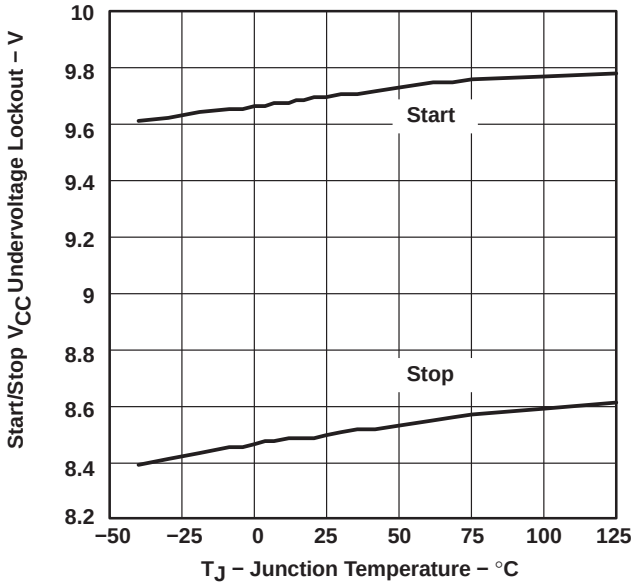


Figure 16

BOOTSTRAP SCHOTTKY DIODE
INPUT CURRENT
vs
OUTPUT VOLTAGE

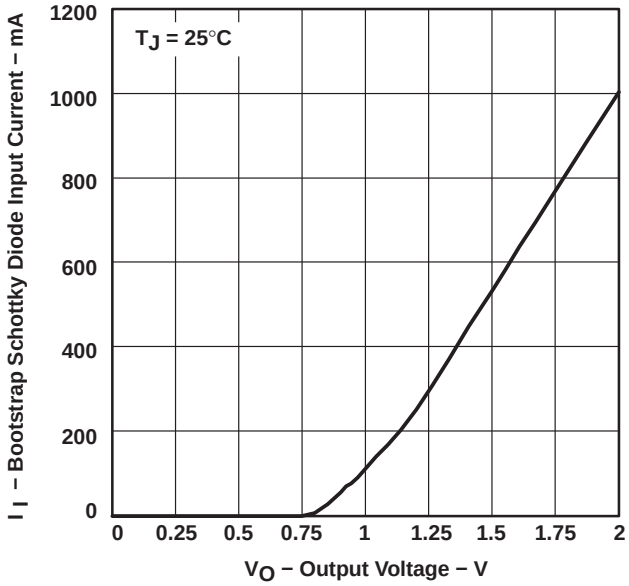


Figure 17

DELAY TIME (DEAD TIME)
vs
INPUT VOLTAGE (VDRV)

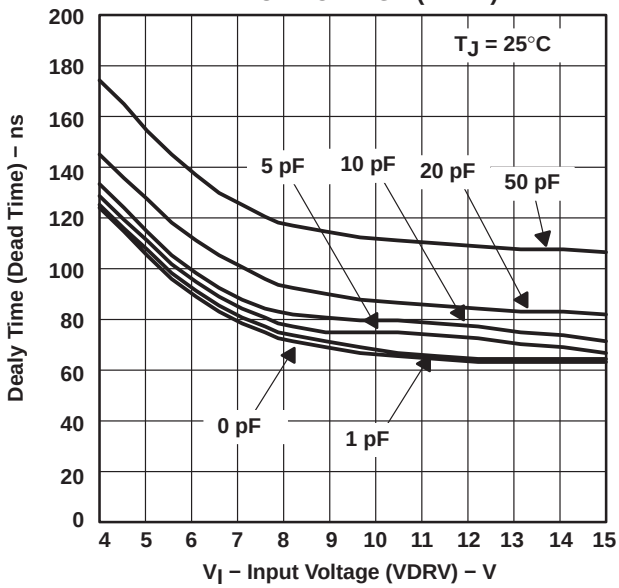


Figure 18

DELAY TIME
vs
JUNCTION TEMPERATURE

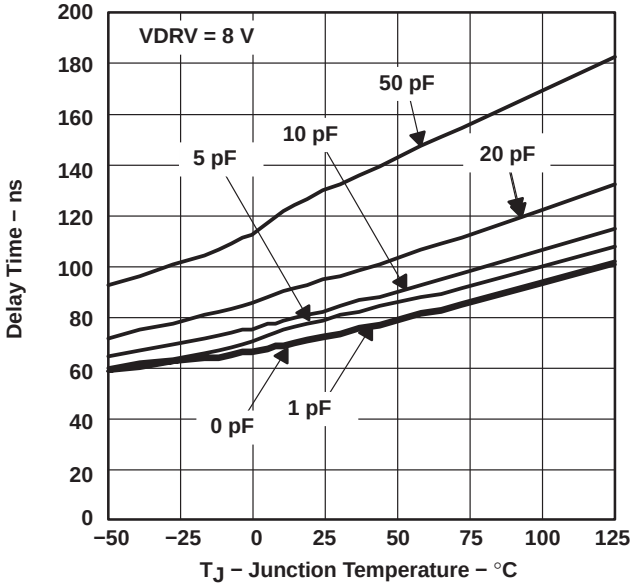


Figure 19

TYPICAL CHARACTERISTICS

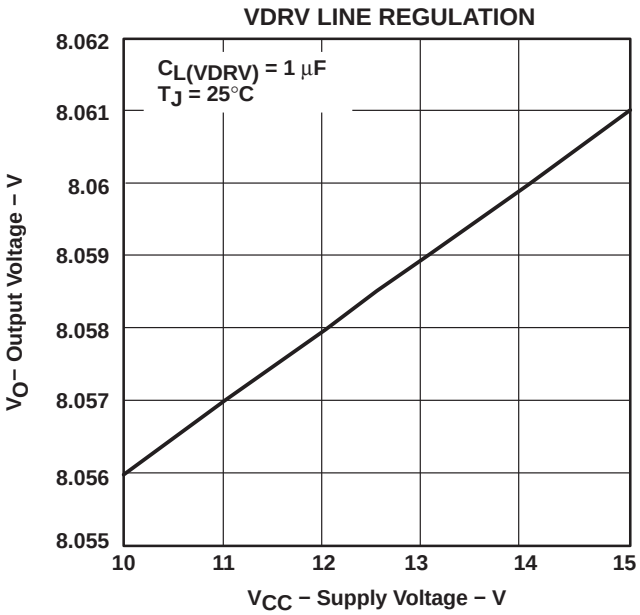


Figure 20

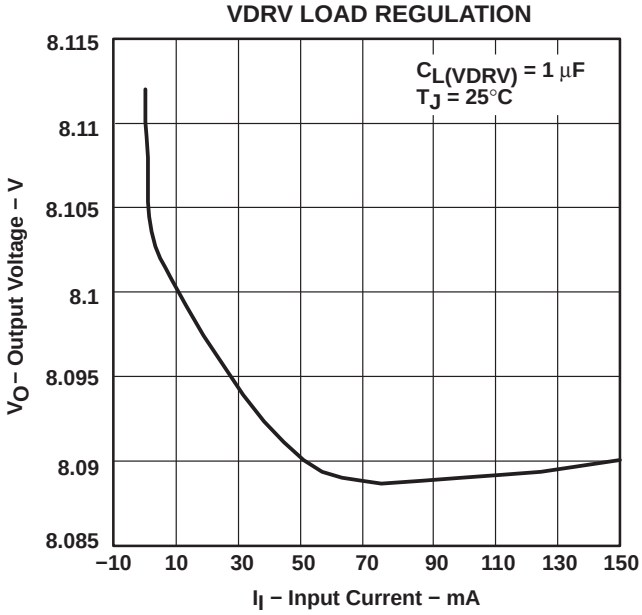
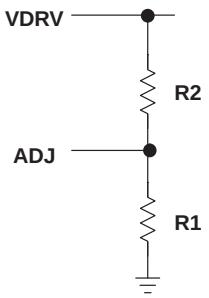


Figure 21

APPLICATION INFORMATION

Figure 22 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001ACD pulse-width-modulation (PWM) controller and a TPS2838 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3-A continuous load. The converter achieves an efficiency of 94% for V_{IN} = 5 V, I_L=1 A, and 93% for V_{IN} = 5 V, I_L = 3 A.

R1 (kΩ)	R2 (kΩ)	VDRV Voltage (V)
30	67	4
30	91	5
30	165	8
30	261	12
30	322	14.5



To set the regulator voltage (TPS2838/39) use the following equation:

$$R2 = \left(\frac{R1}{1.235} \times VDRV\right) - R1$$

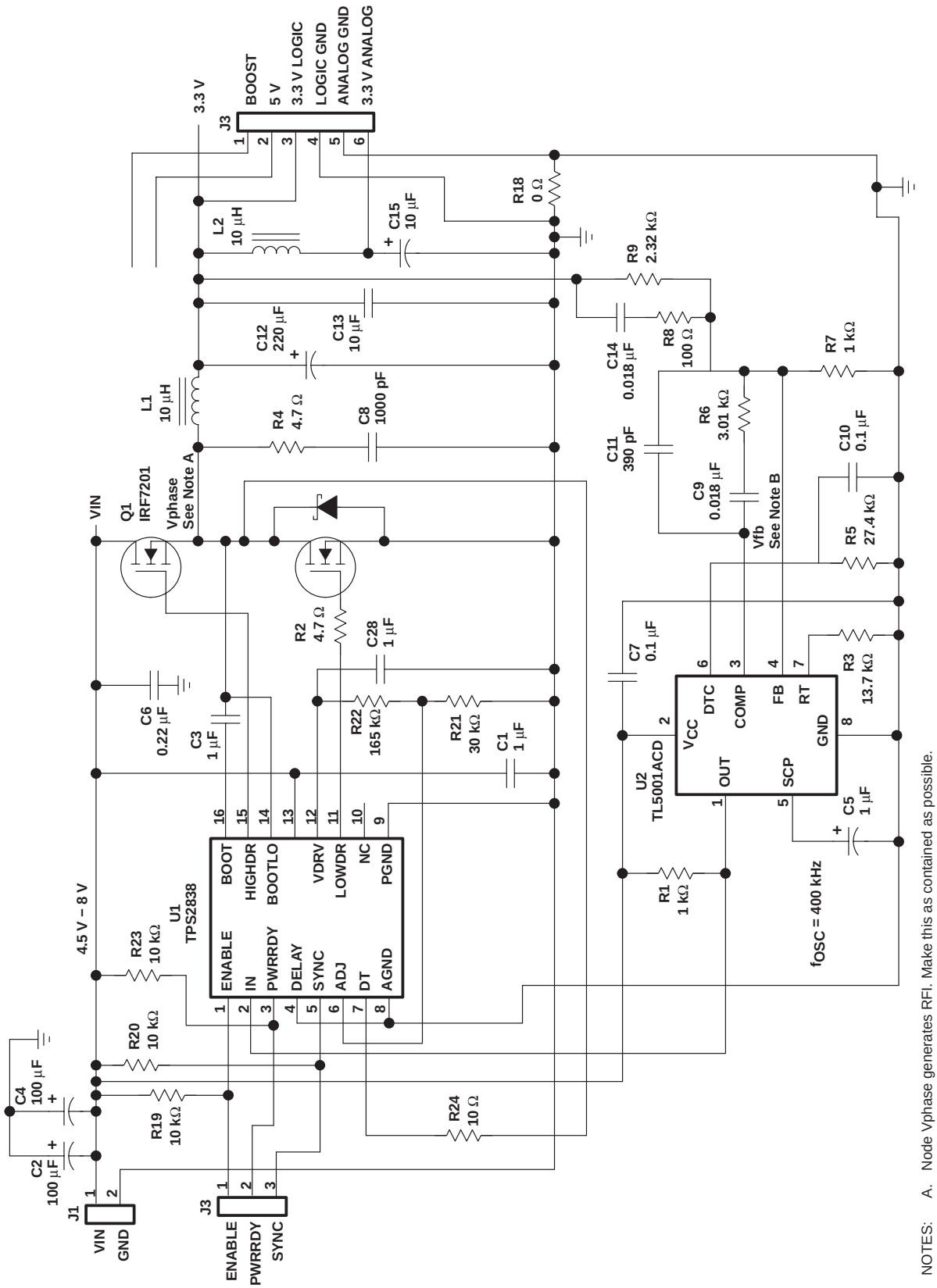


Figure 22. 3.3-V 3-A Synchronous-Buck Converter Circuit

NOTES: A. Node Vphase generates RFI. Make this as contained as possible.
B. Node Vphase is very sensitive. Make this as short as possible.

APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A). This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have other EMI problems and the power supply will be relatively free of noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2838PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2838	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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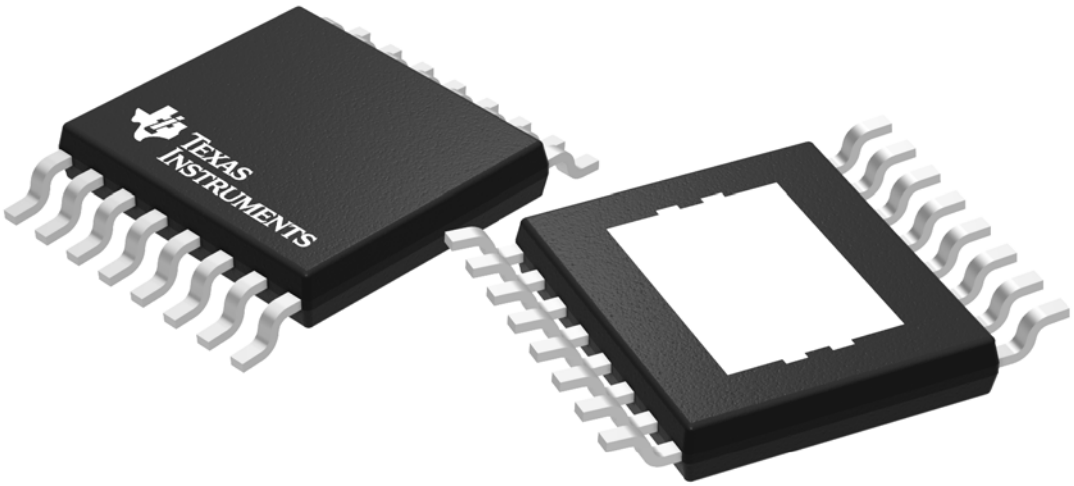
PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

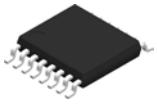
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

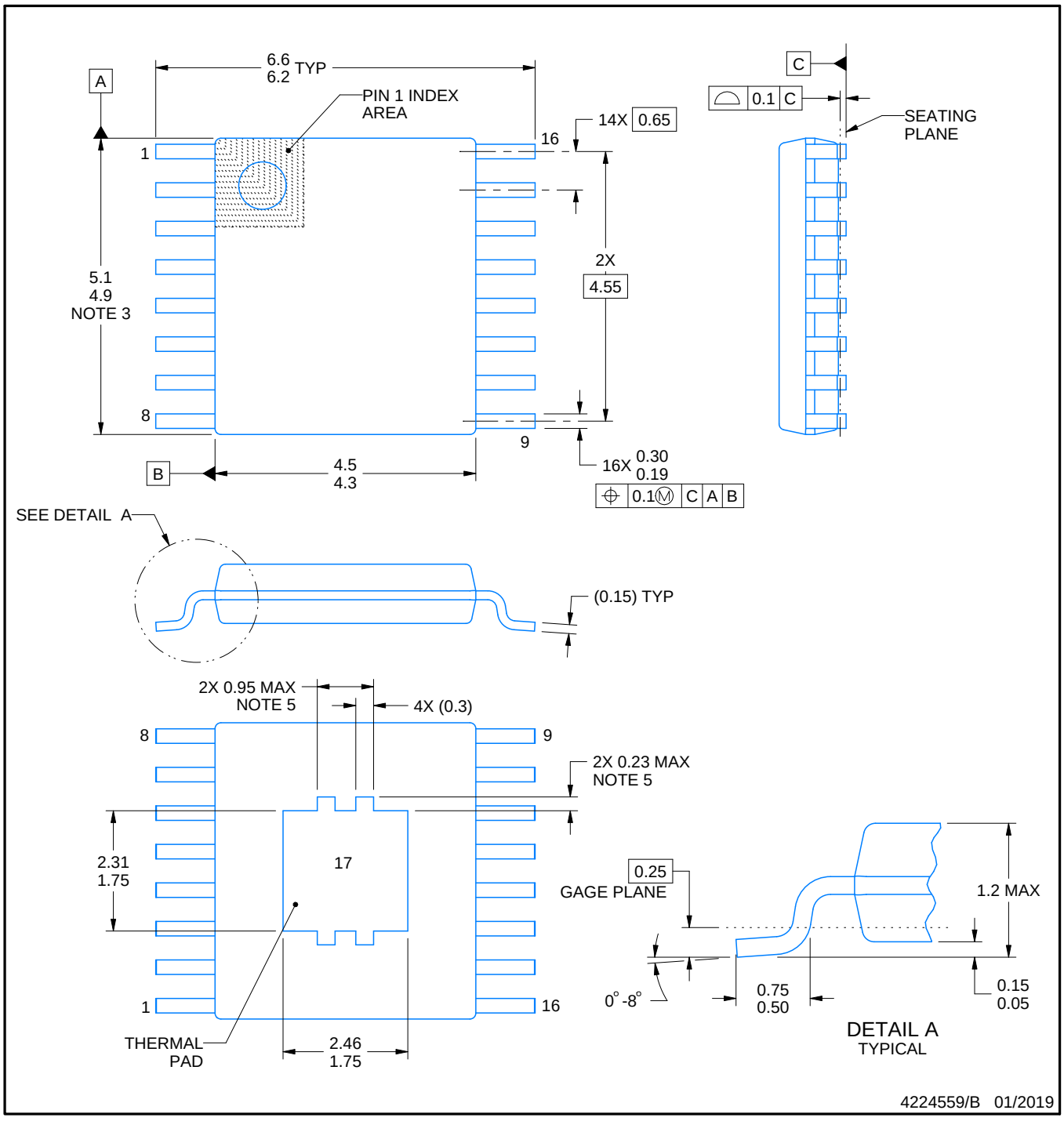
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

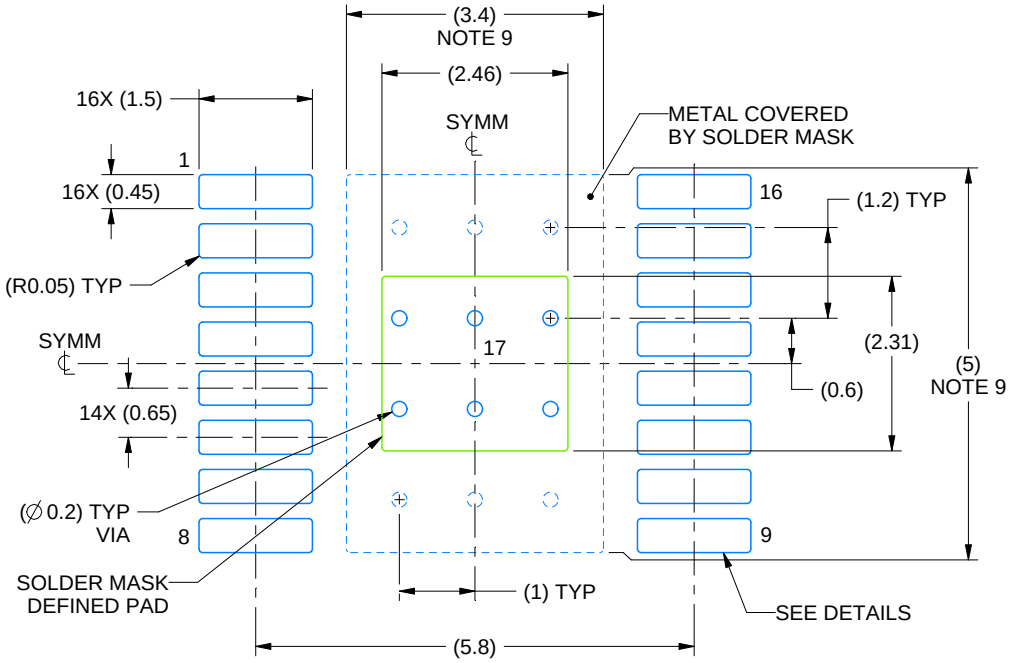
SMALL OUTLINE PACKAGE



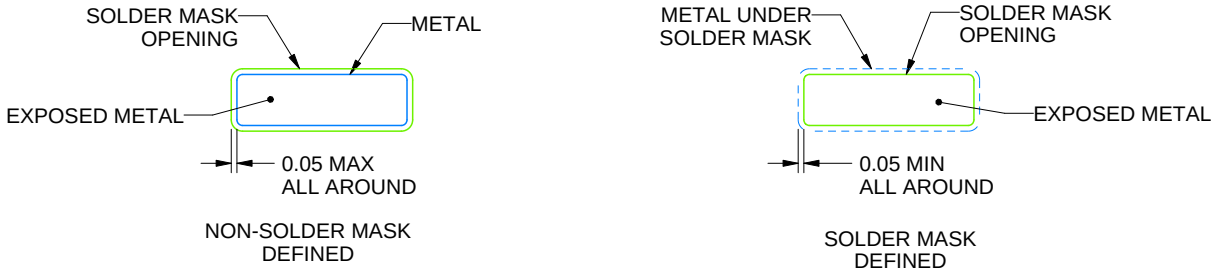
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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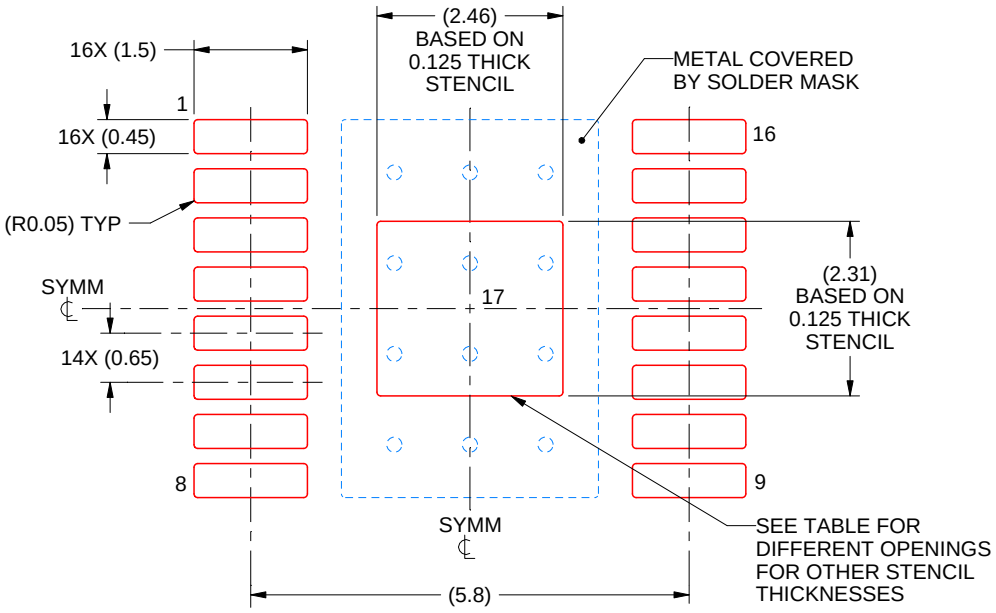
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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