Dual Channel Squib Drivers

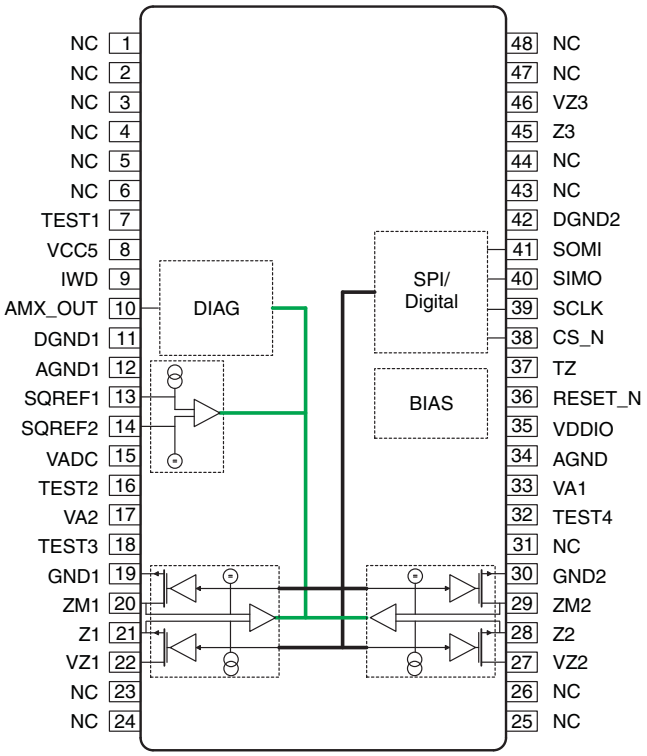
Check for Samples: TPIC71002-Q1

FEATURES

- **Two-Channel Squib Drivers For Airbag Application**
- **Loop Diagnostics Monitor and Reporting**
- **Two Logic Inputs Providing Independent Safety Logic for Enabling/Disabling Deployment**
- **Two Independent Thermally Protected High-Side Drivers that Can Source Deployment or Diagnostic Current Level to Each Squib Load**
- **Two Independent Avalanche Voltage and Thermally Protected Low-Side Drivers that can Sink Deployment or Diagnostic Current Level from Each Squib Load**
- **Each Output Capable of 1.2 A/1.75 A Firing Current for Typical 2 ms/0.5 ms**
- **SPI Slave Interface for Serial Bus Communication with Parity Check**
- **Firing VZx Voltage Range 10V to 35V, Transients up to 40 V**
- **Programmable Firing Time up to 8.2 ms**
- **Common Load Current Settings for All Deployment Loops, Using Registers**
- **Individual Firing Current Timer Limit Set for Each Deployment Loop, Using Registers**
- **Firing Current Timer to Monitor Firing Current Over Deployment Time for Each Deployment Loop**
- **Independent Switch Control for Both High- And Low-Side Switches**
- **Diagnostic Mode for Fault Checking**
- **Internal Fault Monitoring for Safe Operation**
- **Multiplexable Output Buffer for Analog Voltage Measurements**
- **Use of External Clamping Devices on Squib Pins is Not Required to Protect the Deployment ASIC Against Substrate Injection Effects During Deployment Due to Dynamic Shorts to Ground**
- **External Pin Connection to the Microprocessor ADC Supply for Ratio-Metric Squib Resistance Measurement**
- **40-V Pin Capability on All Pins (Except GNDx, AGND, DGND, V_{CC5}, V_{DDIO}, AMX_OUT)**
- **Operating Ambient Temperature Range: –40°C to 105°C**
- **Thermally Enhanced 48-Pin TSSOP DCA PowerPad™ Package**

APPLICATIONS

- **Squib Drivers for Airbag Application**



DESCRIPTION

The TPIC71002 is a two-channel squib driver for airbag deployment in automotive applications. Each channel consists of a high side and a low side switches with independent control logic for protection against inadvertent deployment. Both the high and the low side switches have internal current limits and over-temperature protection.

The IC registers are used for two channel configuration, control and status monitoring. To prevent inadvertent deployment, the high and the low side switches are turned on only if the proper configuration sequence is used, two independent arming/safing inputs are active and multiple inputs to the deploy controller logic are at the correct level. The registers are programmed using a serial communication interface.

To prevent excessive power dissipation the maximum active ON time for each channel is limited by programmable Firing Time Out Timer. In addition, a current limit register is used to program the maximum current through the switches during a deployment. The current limitation on the low side switch is larger than the corresponding high side switch. During deployment, the low side switch will be fully enhanced and operates in R_{DS_ON} mode and the high side switch will be in the current regulation mode.

IC diagnostic functions monitor deployment pin voltages to facilitate high-side switch test, low-side switch test, squib resistance measurements, squib leakage measurement to battery or ground or leakage between any squib channels. The squib leakage measurement does not require the squib load to be present and covers both Zx and ZMx pins. Diagnostic information is communicated through the AMX_OUT pin (for analog signals) and SPI mapped status registers (for status signals latched in digital core).

The high-side and low-side squib drivers have a diagnostic level current limit and a deployment level current limit. The default current limit for high-side and low-side squib drivers is the diagnostic level current limit. The high-side switch deployment current limit for all high-side drivers can be set to either 1.2 A min or 1.75 A min (see Table 1) through SPI mapped registers and device EEPROM settings (see Table 2). The low-side switch deployment current limit is not programmable and is fixed to a level greater than the high-side driver current limit. The ON time duration for each individual squib driver can be programmed through SPI mapped registers.

The deployment sequence requires a specific set of software commands combined with external hardware arming/safing logic inputs (TZ=H, IWD=L) to provide deployment capability. The turn-on sequence of the high-side and low-side drivers is software controlled via SPI commands. The turn-off procedure is automatically controlled by the deployment ASIC for the high side drivers, while the low side drivers turn-off procedure can be controlled by the deployment ASIC or by software via SPI commands. After the programmed ON time deployment has been achieved, the high-side driver is deactivated first. It is followed by the low-side driver deactivation after approximately 100usec (in case of hardware control turn-off sequence device configuration), or after SPI command for low side driver turn-off has been received from an external microcontroller (in case of software control turn-off sequence device configuration).

The RESET_N is an active low input reset signal. This input is driven high (by the power supply unit and/or the external µC) once the external voltage supplies are within the specified limits. The external microcontroller is required to configure and control device through the serial communication interface. Reliable software is critical for the system operation.

Table 1. Potential Deployment Settings for Typical Firing Current

FIRING VOLTAGE	MAXIMUM AVERAGE FIRING VOLTAGE BETWEEN VZX AND ZX PINS TO ACHIEVE DEPLOYMENT	TYPICAL FIRING CURRENT	DWELL (FIRING) TIME
35 V	32.56 V	1.2 A	2 ms(1)
35 V	35.0 V	1.75 A	0.5 ms(1)

(1) For programming desired dwell (firing) time

Extended deployment duration activates the over-temperature protection circuit and terminates deployment. If short-to-ground condition occurs during deployment, 35-V firing voltage is completely dropped across the HS_FET, thereby thermal shut down protection kicks in to protect the device.

Table 2. Potential Deployment Settings for Maximum Firing Current

FIRING VOLTAGE	MAXIMUM AVERAGE FIRING VOLTAGE BETWEEN VZX AND ZX PINS TO ACHIEVE DEPLOYMENT	MAX FIRING CURRENT(1)	DWELL (FIRING)TIME
35 V	30 V	2.6 A (for 1.75 A current setting)	0.7 ms(2)
35 V	31 V	2. 0 A (for 1.2 A current setting)	2.0 ms(2)

(1) The max firing current levels are set through device EEPROM setting
(2) For programming desired dwell (firing) time

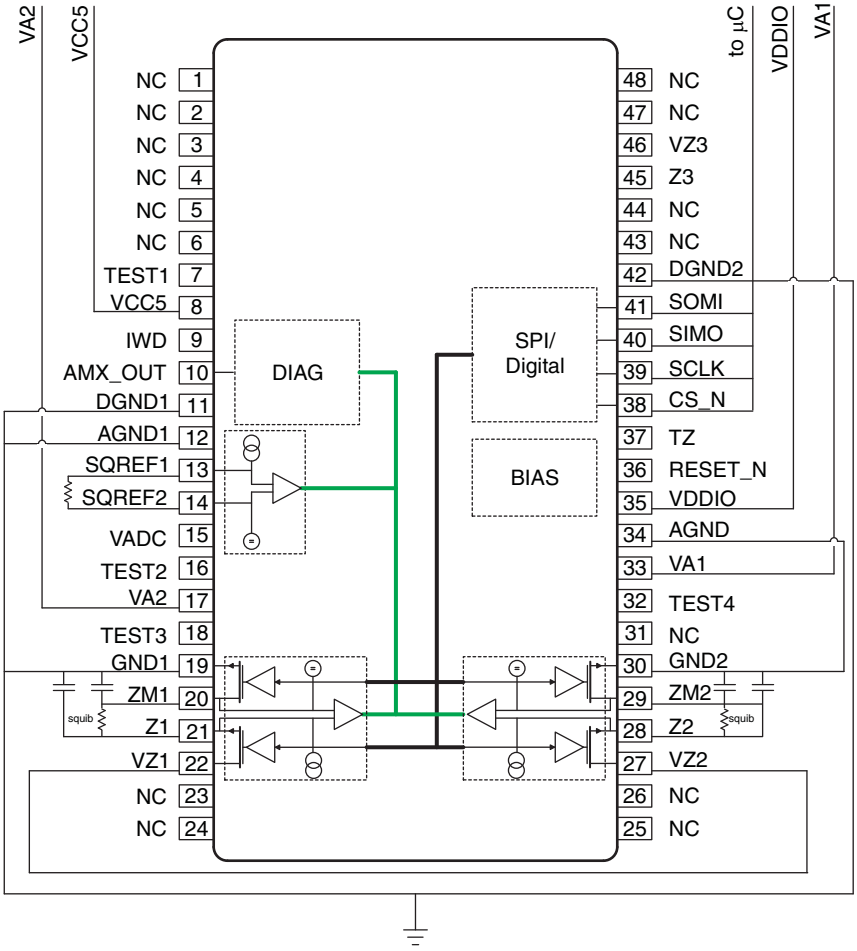


Figure 1. Functional Block Diagram

For the full version of this document, please contact msamktg@list.ti.com .

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC71002TDCARQ1	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPIC71002T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

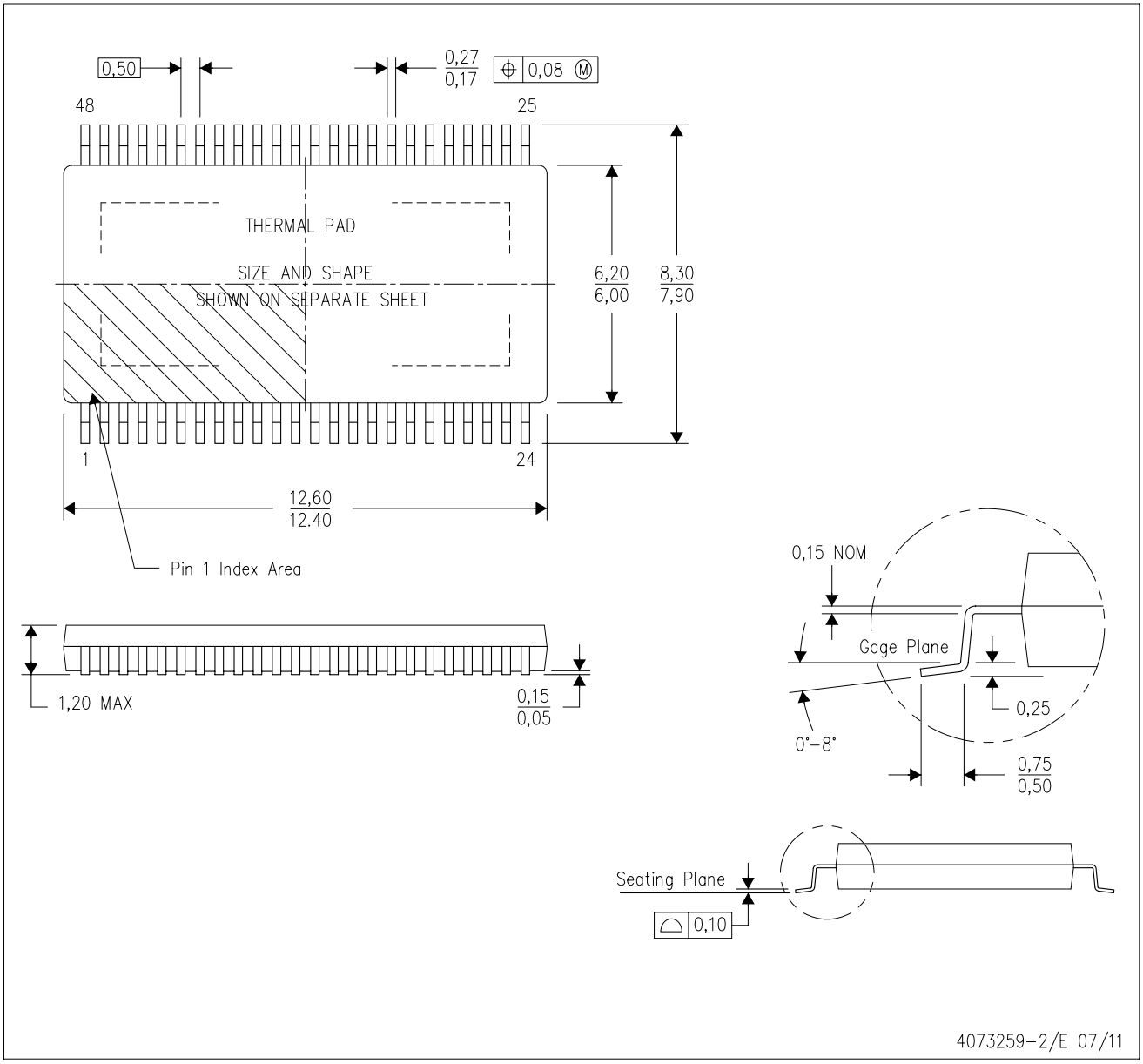
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

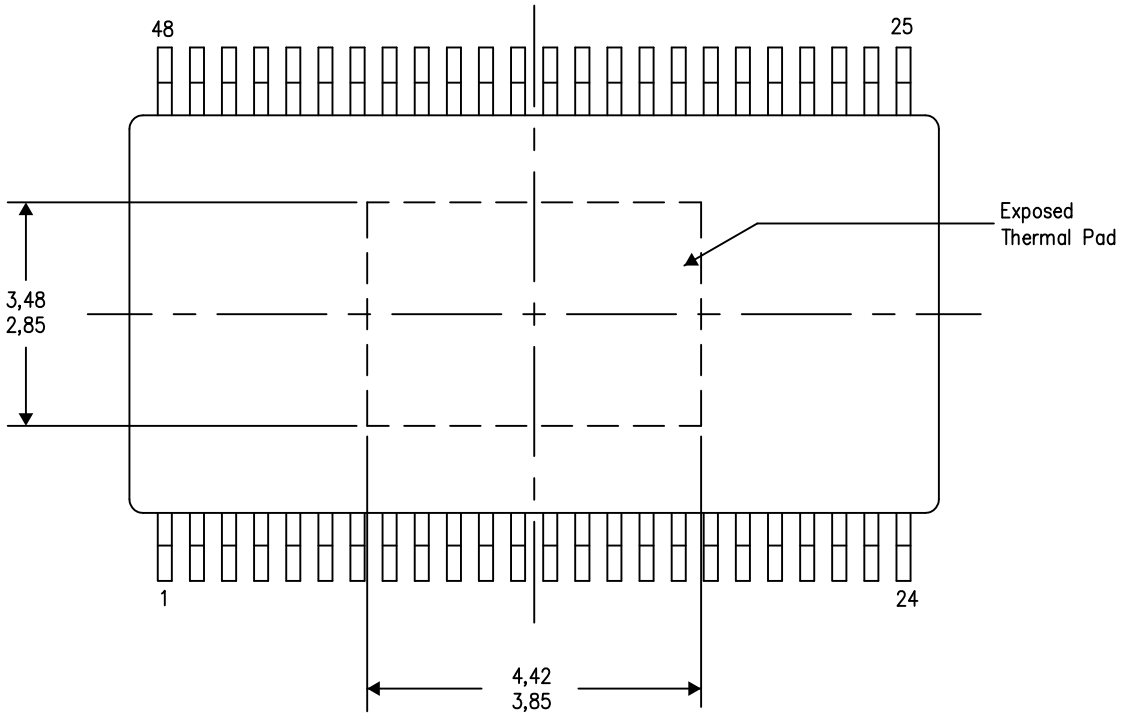
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

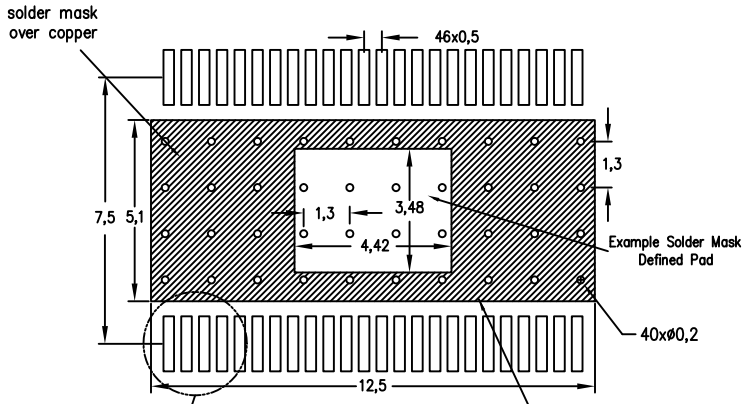
4206320–3/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

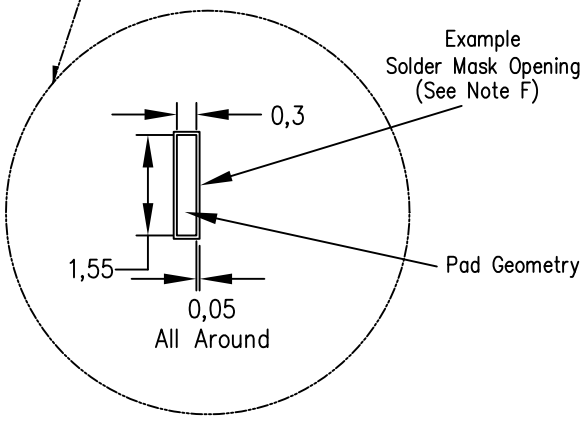
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

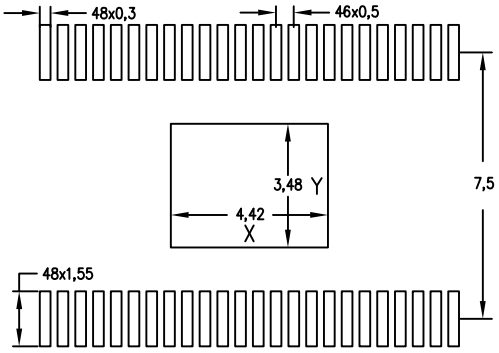


Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.98	3.92
0.127mm	4.42	3.48
0.152mm	4.04	3.18
0.178mm	3.73	2.94

4208546–2/H 11/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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