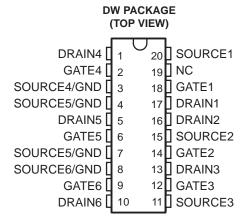
- Low r<sub>DS(on)</sub> . . . 0.4 Ω Typ
- High-Voltage Output . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Fast Commutation Speed

## description

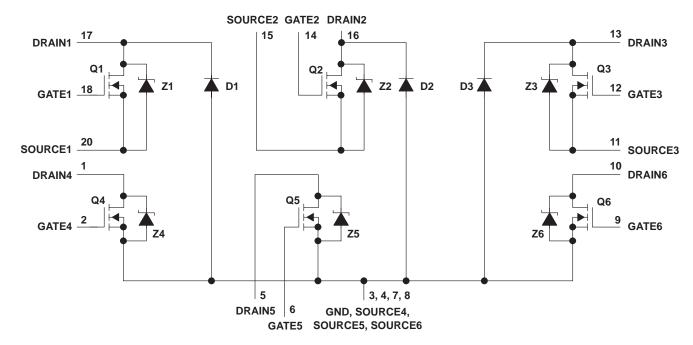
The TPIC5621L is a monolithic logic-level power DMOS-transistor array that consists of six N-channel enhancement-mode DMOS transistors, three of which are configured with a common source.

The TPIC5621L is offered in a wide-body surface-mount (DW) package and is characterized for operation over the case temperature range of -40°C to 125°C.



NC - No internal connection

## schematic



## TPIC5621L SIX-OUTPUT POWER DMOS ARRAY

SLIS033 - JUNE 1994

## absolute maximum ratings over operating case temperature range (unless otherwise noted)<sup>†</sup>

Drain-to-source voltage, V <sub>DS</sub> 60 V
Source-to-GND voltage (Q1, Q2, and Q3)
Drain-to-GND voltage (Q1, Q2, and Q3)
Drain-to-GND voltage (Q4, Q5, and Q6)
Gate-to-source voltage range, V <sub>GS</sub> ±20 \
Continuous drain current, each output, T <sub>C</sub> = 25°C
Continuous source-to-drain diode current, T <sub>C</sub> = 25°C
Pulsed drain current, I <sub>max</sub> , T <sub>C</sub> = 25°C (each output, see Note 1 and Figure 15)
Single-pulse avalanche energy, E <sub>AS</sub> , T <sub>C</sub> = 25°C (see Figures 4, 15 and 16)
Continuous total dissipation (see Figure 15) See Dissipation Rating Table
Operating virtual junction temperature range, T <sub>J</sub> –40°C to 150°C
Operating case temperature range, T <sub>C</sub> –40°C to 125°C
Storage temperature range –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms and duty cycle = 2%.

## **DISSIPATION RATING TABLE**

PACKAGE	T <sub>C</sub> ≤ 25°C	DERATING FACTOR	T <sub>C</sub> = 125°C
	POWER RATING	ABOVE T <sub>C</sub> = 25°C	POWER RATING
DW	1389 mW	11.1 mW/°C	279 mW

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## electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST COND	ITIONS	MIN	TYP	MAX	UNIT
V <sub>(BR)DSX</sub>	Drain-to-source breakdown voltage	$I_D = 250 \mu\text{A},$	$V_{GS} = 0$	60			V
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	I <sub>D</sub> = 1 mA, See Figure 5	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
V <sub>(BR)</sub>	Reverse drain-to-GND breakdown voltage (across D1, D2, and D3)	Drain-to-GND curren	t = 250 μA	100			V
V <sub>DS(on)</sub>	Drain-to-source on-state voltage	I <sub>D</sub> = 1 A, See Notes 2 and 3	V <sub>G</sub> S = 5 V,		0.4	0.48	V
VF(SD)	Forward on-state voltage, source-to-drain	I <sub>S</sub> = 1 A, V <sub>GS</sub> = 0 (Z1, Z2, Z3, See Notes 2 and 3 and			0.9	1.1	V
٧ <sub>F</sub>	Forward on-state voltage, GND-to-drain	I <sub>D</sub> = 1 A (D1, D2, D3), See Notes 2 and 3			4.6		V
I <sub>DSS</sub>	Zero-gate-voltage drain current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0	$T_C = 25^{\circ}C$		0.05	1 10 μΑ	^
			T <sub>C</sub> = 125°C		0.5		μΑ
I <sub>GSSF</sub>	Forward gate current, drain short circuited to source	$V_{GS} = 16 V$ ,	$V_{DS} = 0$		10	100	nA
IGSSR	Reverse gate current, drain short circuited to source	V <sub>SG</sub> = 16 V,	V <sub>DS</sub> = 0		10	100	nA
	Laslane surrent dusin to CNID	V <sub>DGND</sub> = 48 V	T <sub>C</sub> = 25°C		0.05	1	^
likg	Leakage current, drain-to-GND	(D1, D2, D3)	T <sub>C</sub> = 125°C	0.5		10	μΑ
<b>"</b> ( )	Static drain-to-source on-state resistance	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1 A,	T <sub>C</sub> = 25°C		0.4	0.48	Ω
rDS(on)	Static drain-to-source on-state resistance	See Notes 2 and 3 and Figures 6 and 7	T <sub>C</sub> = 125°C		0.65	0.68	22
9fs	Forward transconductance	V <sub>DS</sub> = 15 V, See Notes 2 and 3 ar	I <sub>D</sub> = 0.5 A, nd Figure 9	1	1.29	1.45	S
C <sub>iss</sub>	Short-circuit input capacitance, common source				190	240	
C <sub>oss</sub>	Short-circuit output capacitance, common source	$V_{DS} = 25 \text{ V},$	$V_{GS} = 0$ ,		100	125	pF
C <sub>rss</sub>	Short-circuit reverse transfer capacitance, common source	f = 1 MHz,	See Figure 11		40	50	þг

NOTES: 2. Technique should limit  $T_J - T_C$  to  $10^{\circ}C$  maximum.

## source-to-drain and GND-to-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER	T	MIN	TYP	MAX	UNIT		
		Z1, Z2, Z3		65				
t <sub>rr</sub>	t <sub>rr</sub> Reverse recovery time	$I_S = 0.5 \text{ A},$ $V_{DS} = 48 \text{ V},$ $V_{GS} = 0,$ $di/dt = 100 \text{ A}/\mu\text{s},$ See Figures 1 and 14		Z4, Z5, Z6		150		ns
			D1, D2, D3		200			
			$dI/dt = 100 A/\mu s$ ,	Z1, Z2, Z3		0.06		
QRR Total diode charge	J. 11		Z4, Z5, Z6		0.3		μС	
				D1, D2, D3		0.7		

<sup>3.</sup> These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

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## resistive-load switching characteristics, T<sub>C</sub> = 25°C

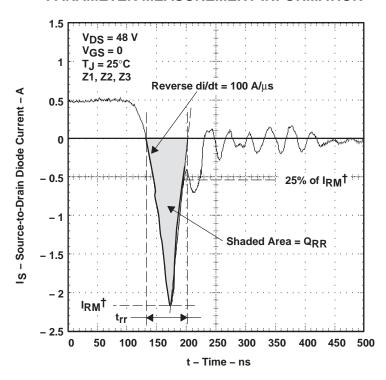
	PARAMETER	TEST CONDITIONS				TYP	MAX	UNIT		
t <sub>d</sub> (on)	Turn-on delay time					9	18			
td(off)	Turn-off delay time	$V_{DD} = 25 \text{ V},  R_L = 50 \Omega,$	$R_L = 50 \Omega$ ,	t <sub>en</sub> = 10 ns,		20	40			
t <sub>r</sub>	Rise time	$t_{dis} = 10 \text{ ns},$				21	42	ns		
tf	Fall time					25	50			
Qg	Total gate charge					3.1	3.7			
Q <sub>gs(th)</sub>	Threshold gate-to-source charge	V <sub>DS</sub> = 48 V, See Figure 3	V <sub>DS</sub> = 48 V, See Figure 3		$I_D = 0.5 A,$	$V_{GS} = 5 V$ ,		0.5	0.6	nC
Q <sub>gd</sub>	Gate-to-drain charge	gara a				1.9	2.3			
L <sub>D</sub>	Internal drain inductance					5		nH		
LS	Internal source inductance					5		пп		
Rg	Internal gate resistance					0.25		Ω		

## thermal resistance

	PARAMETER	R TEST CONDITIONS				UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (see Note 4)	All autoute with equal power		90		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power		27		C/VV

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

## PARAMETER MEASUREMENT INFORMATION

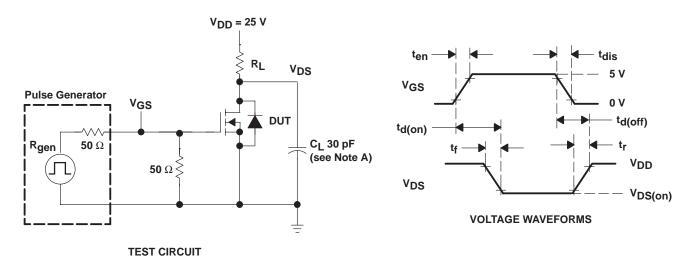


<sup>†</sup>I<sub>RM</sub> = maximum recovery current

NOTE A: The above waveform is representative of Z4, Z5, Z6, D1, D2, and D3 in shape only.

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

## PARAMETER MEASUREMENT INFORMATION



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms

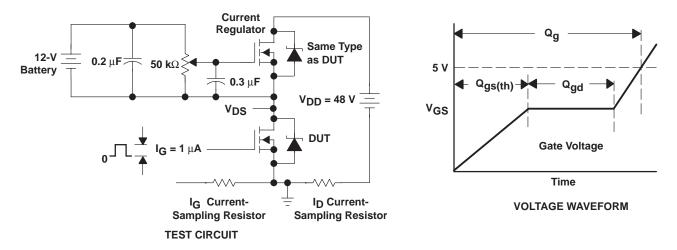
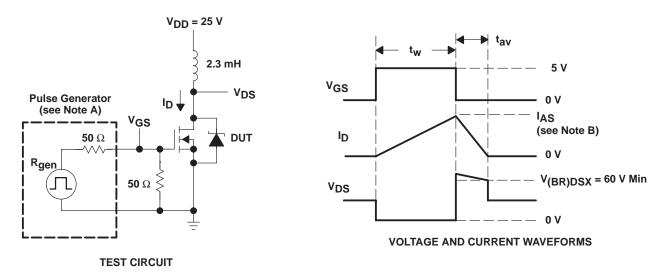


Figure 3. Gate-Charge Test Circuit and Voltage Waveform

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:  $t_r \le 10$  ns,  $t_f \le 10$  ns,  $t_{O} = 50 \Omega$ .

B. Input pulse duration  $(t_W)$  is increased until peak current  $I_{AS} = 3 A$ .

Energy test level is defined as  $E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 18 \text{ mJ}.$ 

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

## **TYPICAL CHARACTERISTICS**

8.0

 $I_D = 1 A$ 

**-** 40 - 20

# GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE $\begin{array}{c} 2.5 \\ \hline \\ 0.5 \\ \hline \\ 0.5 \\ \hline \\ 0.40-20 \\ \hline \end{array}$

Figure 5

0.7 V<sub>GS</sub> = 4.5 V

V<sub>GS</sub> = 4.5 V

V<sub>GS</sub> = 5 V

V<sub>GS</sub> = 5 V

0.1 0.1

40 60

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

JUNCTION TEMPERATURE

Figure 6

T<sub>J</sub> - Junction Temperature - °C

80 100 120 140 160

## **TYPICAL CHARACTERISTICS**

## STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

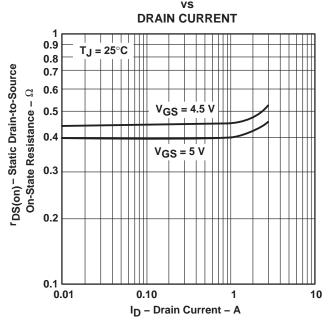


Figure 7

# D- Drain-to-Source Current - A

DRAIN-TO-SOURCE CURRENT vs
DRAIN-TO-SOURCE VOLTAGE

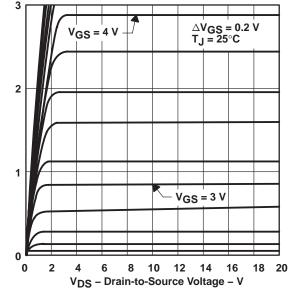


Figure 8

## DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

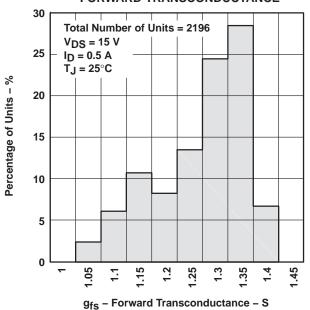


Figure 9

## DRAIN-TO-SOURCE CURRENT vs

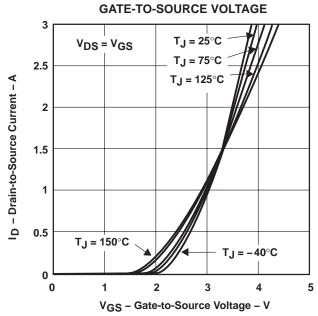


Figure 10

## **TYPICAL CHARACTERISTICS**

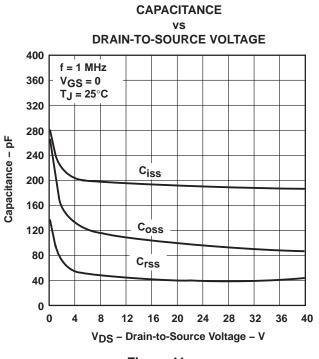


Figure 11

## DRAIN-TO-SOURCE AND GATE-TO-SOURCE VOLTAGE

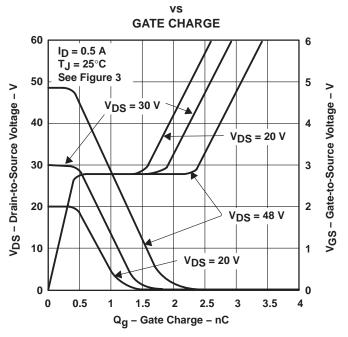


Figure 13

# SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

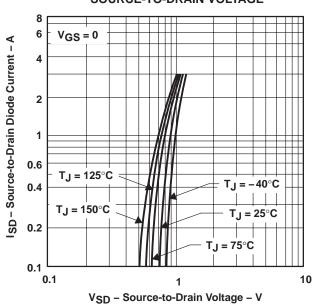


Figure 12

## **REVERSE RECOVERY TIME**

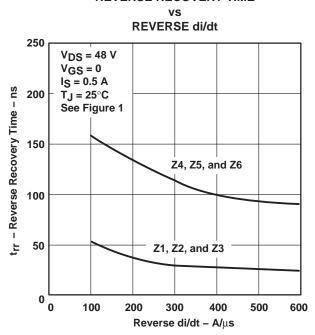
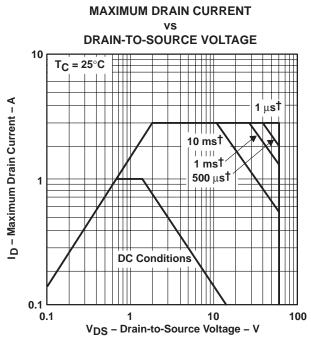


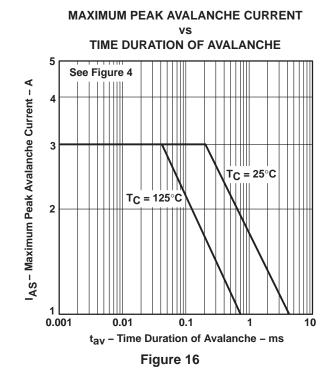
Figure 14

## THERMAL INFORMATION



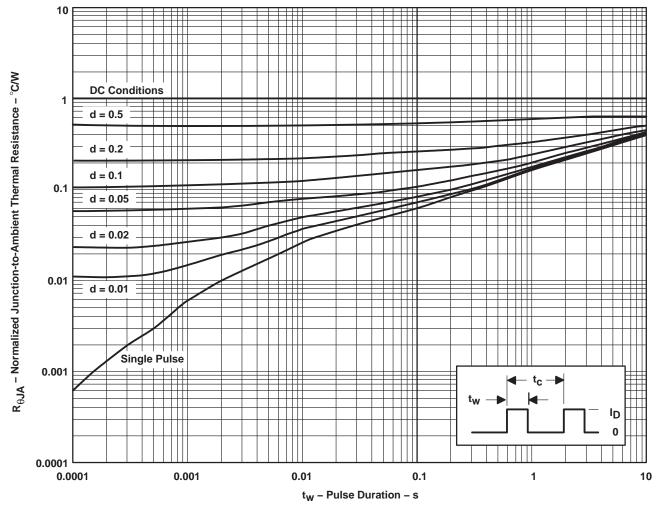
†Less than 2% duty cycle

Figure 15



## THERMAL INFORMATION

# NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE† vs PULSE DURATION



† Device mounted on FR4 printed-circuit board with no heat sink

 $\begin{aligned} \text{NOTES:} \quad & Z_{\theta A}(t) = \text{r(t)} \ R_{\theta J A} \\ & t_W = \text{pulse duration} \\ & t_C = \text{cycle time} \\ & d = \text{duty cycle} = t_W/t_C \end{aligned}$ 

Figure 17



## PACKAGE OPTION ADDENDUM

8-Apr-2005

## **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPIC5621LDW	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



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