TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅣ)

TPCT4203

Lithium-Ion Battery Applications (1Cell)

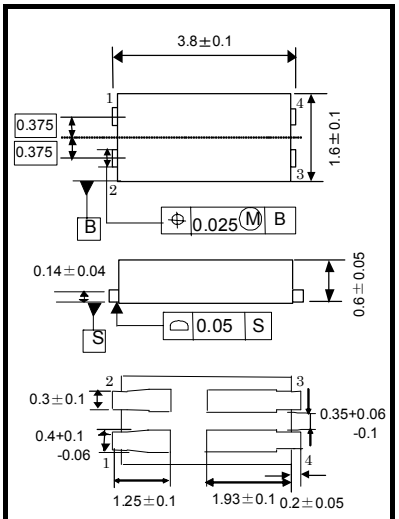
- Lead(Pb)-Free
- Small footprint due to a small and thin package
- Low source-source ON-resistance: $R_{SS\ (ON)}$ = 25.5 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 18 S (typ.)
- Low leakage current: I_{SSS} = 10 μA (max) (V_{SS} = 20 V)
- Enhancement mode: V_{th} = 0.5 to 1.2 V (V_{SS} = 10 V, I_S = 200 μA)
- Common drain

Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
Source-source voltage			V_{SSS}	20	V
Gate-source voltage			V_{GSS}	±12	V
Source current	DC	(Note 1)	I_S	6	A
	Pulse	(Note 1)	I_{SP}	24	
Power dissipation (t = 10 s)		(Note 2a, 3)	P_D	1.47	W
Power dissipation (t = 10 s)		(Note 2b, 3)	P_D	0.47	W
Single-pulse avalanche energy		(Note 4)	E_{AS}	46.8	mJ
Avalanche current			I_{AR}	6	A
Repetitive avalanche energy		(Note 2a, 5)	E_{AR}	0.058	mJ
Channel temperature			T_{ch}	150	°C
Storage temperature range			T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

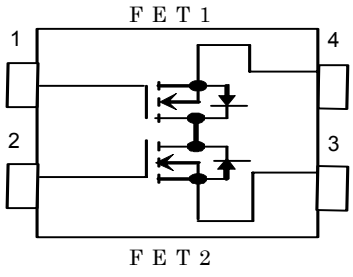
Unit: mm



1.GATE 1	3.SOURCE 2
2.GATE 2	4.SOURCE 1
JEDEC	—
JEITA	—
TOSHIBA	2-2V1A

Weight: 9.7 mg (typ.)

Circuit Configuration



⚠ WARNING

【Handling Precaution for Power MOSFET in use of Protection Circuit for Battery Pack】

Flame-retardant resins of UL94-V0 flammability class are used in packages, however, they are not noncombustible.

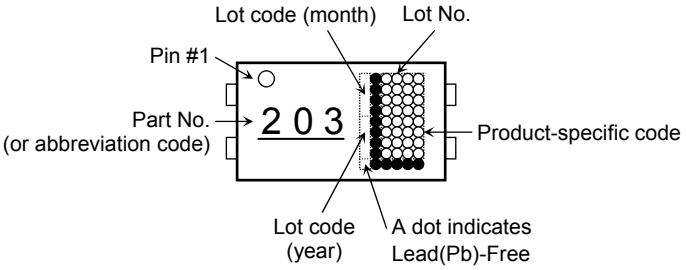
Use a unit, for example PTC Thermistor, which can shut off the power supply if a short-circuit occurs. If the power supply is not shut off on the occurring short-circuit, a large short-circuit current will flow continuously, which may cause the device to catch fire or smoke. The product listed in this document is intended for usage in Lithium Ion Battery charge and discharge control application. So it is responsible for customer when using the product in the different application.

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a, 3)	$R_{th\ (ch\text{-}a)}$	85	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b, 3)	$R_{th\ (ch\text{-}a)}$	266	°C/W

This transistor is an electrostatic-sensitive device. Handle with care.

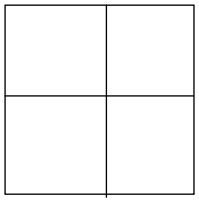
Marking (Note 6)



Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:

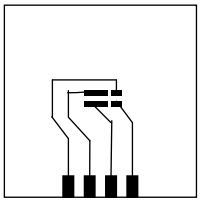
(a) Device mounted on a glass-epoxy board



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(a)

(b) Device mounted on a glass-epoxy board



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(b)

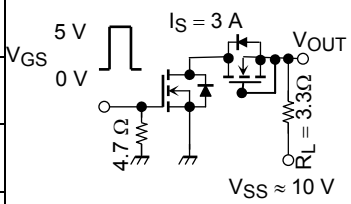
Note 3: The power dissipation and thermal resistance values are shown for both the FETs.

Note 4: V_{SS} = 16 V, T_{ch} = 25°C (initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 6 A

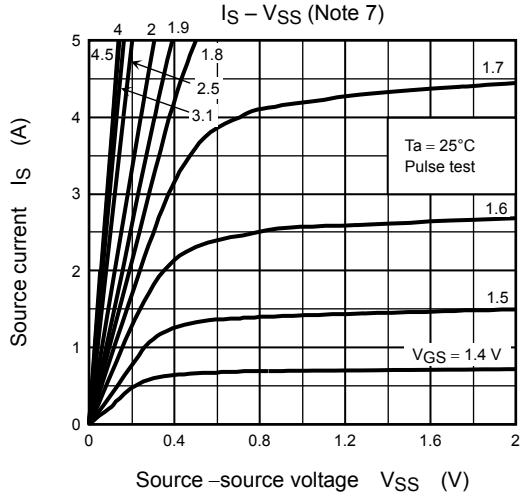
Note 5: Repetitive rating: pulse width is limited by max channel temperature.

Note 6: The circle "○" on the upper left of the marking indicates Pin 1.

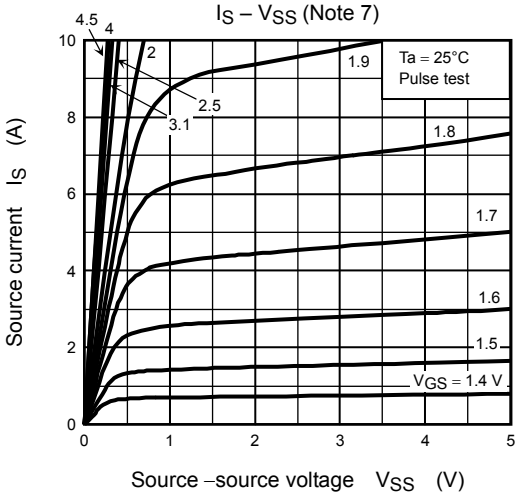
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±12 V, V_{SS} = 0 V (Note 8)	—	—	±100	nA
Source cutoff current		I_{SSS}	V_{SS} = 20 V, V_{GS} = 0 V (Note 8)	—	—	10	μA
Source -source breakdown voltage		$V_{(BR)\ SSS}$	I_S = 10 mA, V_{GS} = 0 V (Note 8)	20	—	—	V
		$V_{(BR)\ SSX}$	I_S = 10 mA, V_{GS} = −12 V (Note 8)	8	—	—	
Gate threshold voltage		V_{th}	V_{SS} = 10 V, I_S = 200μA (Note 8)	0.5	—	1.2	V
Source -source ON-resistance		$R_{SS(ON)}$	V_{GS} = 2.5 V, I_S = 3 A (Note 7)	28	37	49	mΩ
			V_{GS} = 4.0 V, I_S = 3 A (Note 7)	21	27	32	
			V_{GS} = 4.5 V, I_S = 3 A (Note 7)	19	25.5	31	
Forward transfer admittance		$\|Y_{fs}\|$	V_{SS} = 10 V, I_S = 3 A (Note 8)	9	18	—	S
Input capacitance		C_{iss}	V_{SS} = 10 V, V_{GS} = 0 V, f = 1 MHz (Note 8)	—	790	—	pF
Reverse transfer capacitance		C_{rss}		—	120	—	
Output capacitance		C_{oss}		—	190	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs (Note 8)	—	40	—	ns
	Turn-on time	t_{on}		—	60	—	
	Fall time	t_f		—	90	—	
	Turn-off time	t_{off}		—	190	—	
Total gate charge		Q_g	V_{SS} ≈ 16 V, V_{GS} = 5 V, I_S = 6 A (Note 8)	—	11	—	nC
Gate-source charge 1		Q_{gs1}		—	2.5	—	
Diode (source-source) forward voltage		V_{SSF}	I_{SR} = 6 A, V_{GS} = 0 V (Note 9)	—	—	−1.2	V

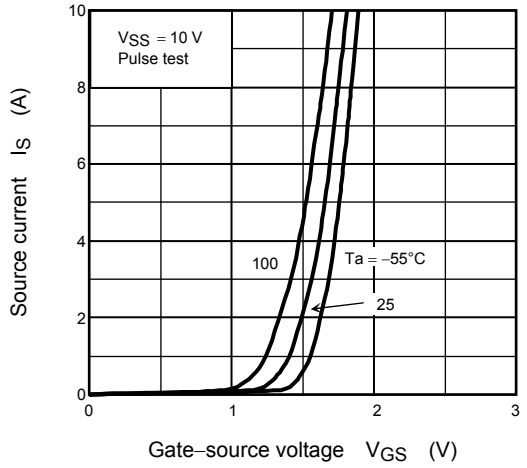
$I_S - V_{SS}$ (Note 7)



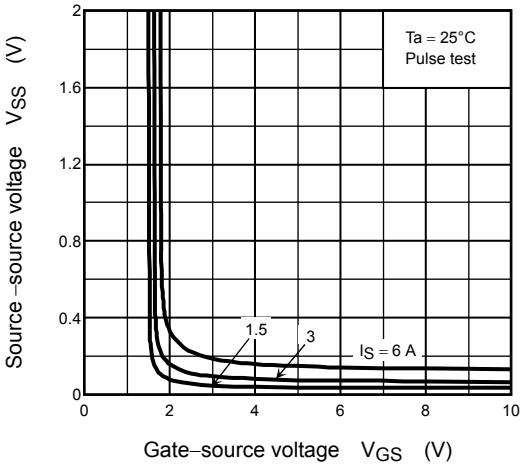
$I_S - V_{SS}$ (Note 7)



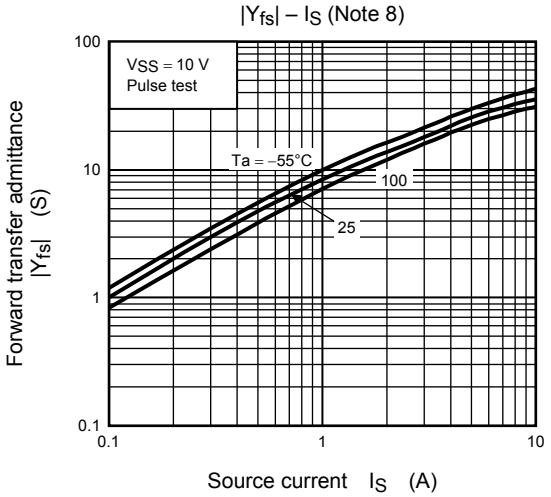
$I_S - V_{GS}$ (Note 8)



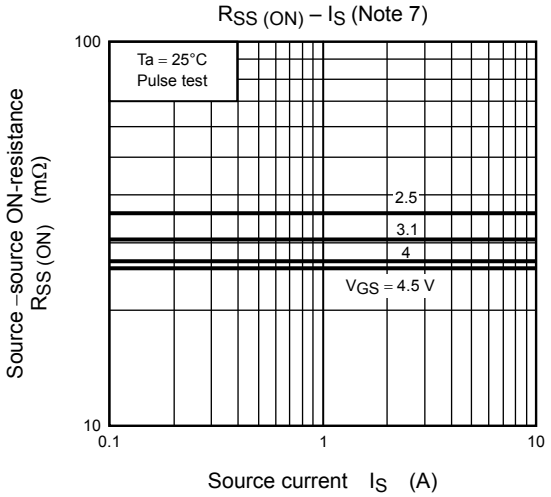
$V_{SS} - V_{GS}$ (Note 7)



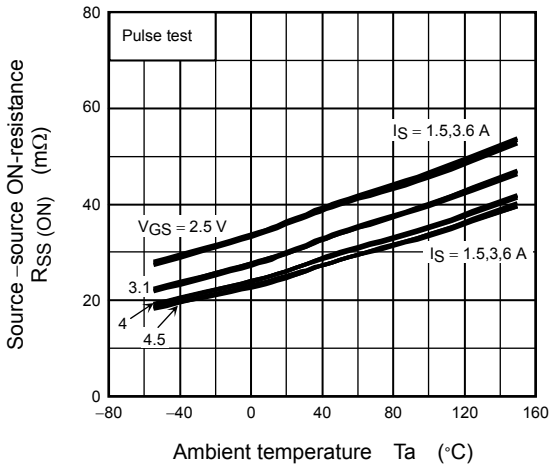
$|Y_{fs}| - I_S$ (Note 8)



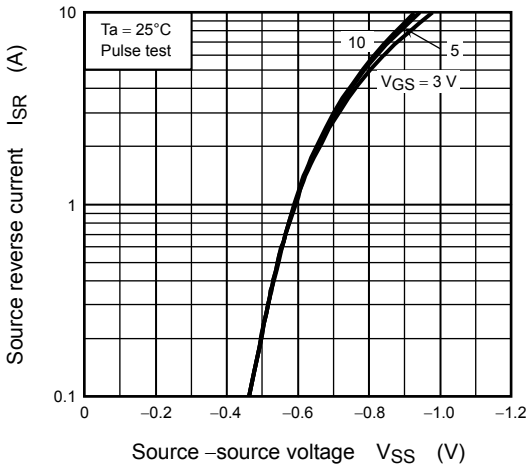
$R_{SS\ (ON)} - I_S$ (Note 7)



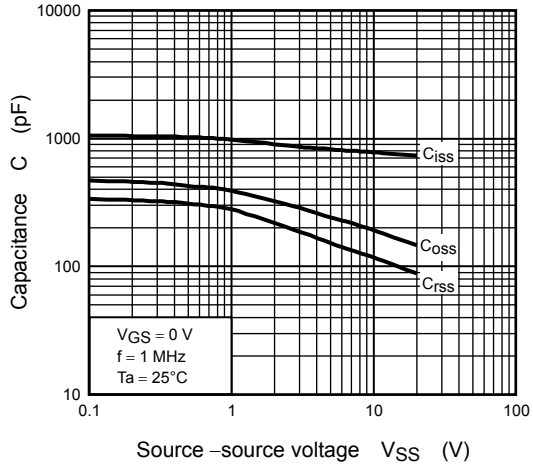
$R_{SS\ (ON)}$ – Ta (Note 7)



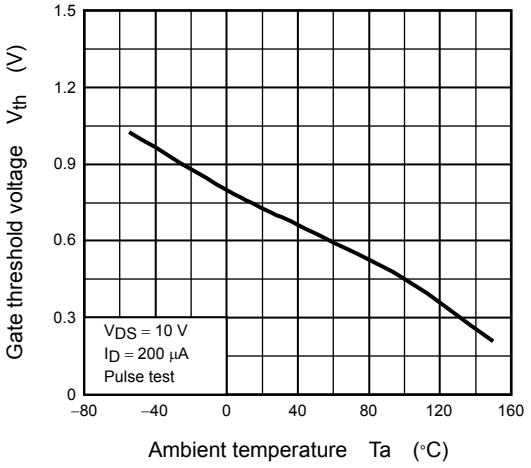
I_{SR} – V_{SS} (Note 10)



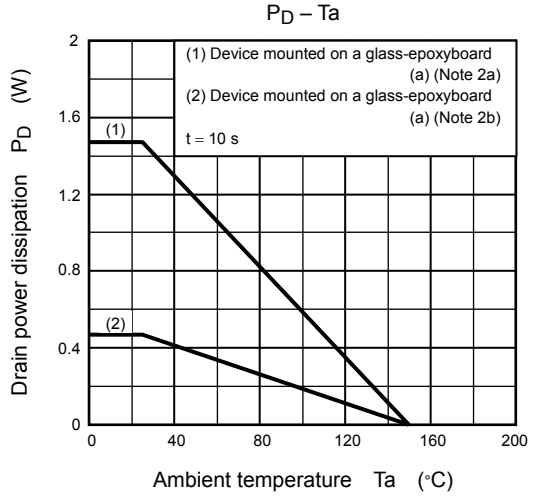
Capacitance – V_{SS} (Note 8)



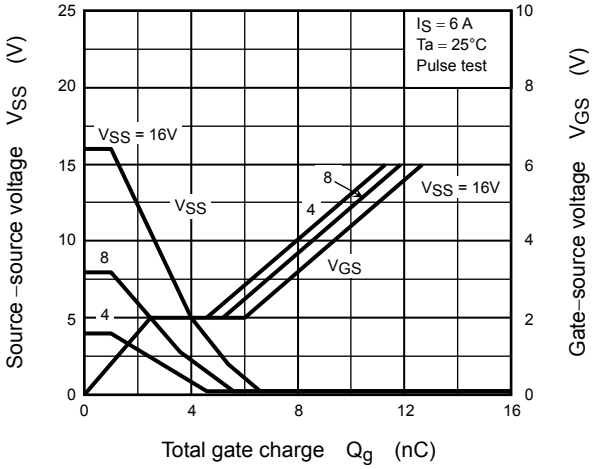
V_{th} – Ta (Note 8)

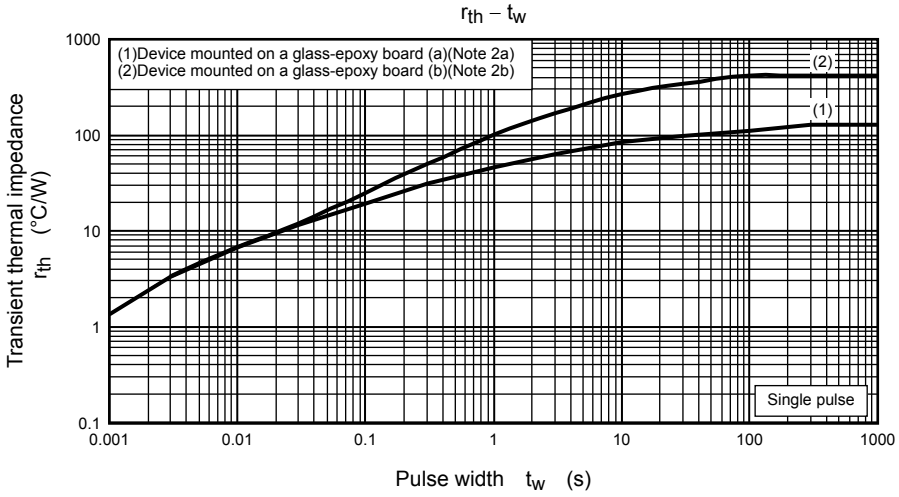


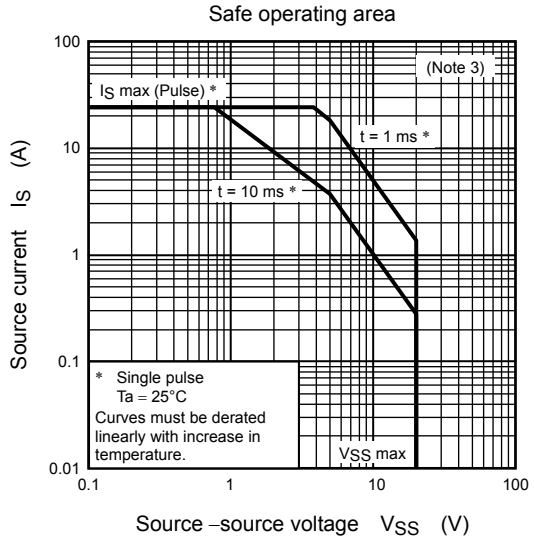
P_D – Ta



Dynamic input/outputcharacteristics (Note 8)







Note 7: Gate 1 and Gate 2 are connected to the same gate voltage (V_{GS}).

Note 8: FET1 measurement: Gate 2 and Source 2 are shorted together.

FET2 measurement: Gate 1 and Source 1 are shorted together.

Note 9: FET1 measurement: 4.5V (V_{GS}) is applied to Gate 2.

FET2 measurement: 4.5V (V_{GS}) is applied to Gate 1.

Note 10: FET1 measurement: Gate 1 and Source 1 are shorted together, V_{GS} is applied across Gate 2 and Source 2.

FET2 measurement: Gate 2 and Source 2 are shorted together, V_{GS} is applied across Gate 1 and Source 1.

Note11: 【Mounting condition】

The TPCT4203 should be soldered onto a pc board with up to two reflow passes at the recommended reflow conditions. The second reflow process should be performed within two weeks after the first reflow process.

【Manual repair after reflow soldering】

The package leads that have not been soldered properly may be repaired at most once per lead using a soldering iron. Care should be taken so that stress is not applied to the device, especially to the base of a lead, during the repair process.

・infrared reflow soldering

(1) It is recommended to heat the top and bottom of the device with far- and mid-infrared rays. (See Figure 1.)

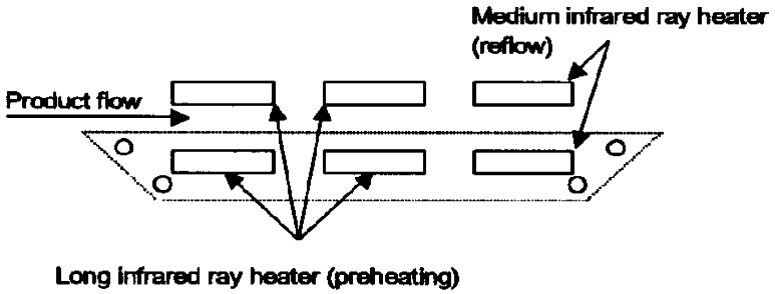


Figure 1. Heating the top and bottom of the device with far- and mid-infrared rays

(2) Examples of recommended reflow temperature profile

Figure 2 shows the recommended temperature profile for using eutectic solder. Figure 3 shows the recommended temperature profile for using lead (Pb)-free solder.

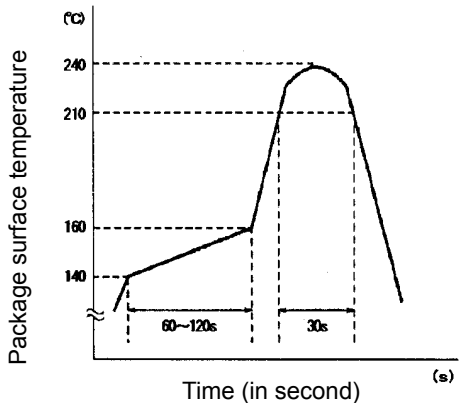


Figure 2. Recommended temperature profile for eutectic solder

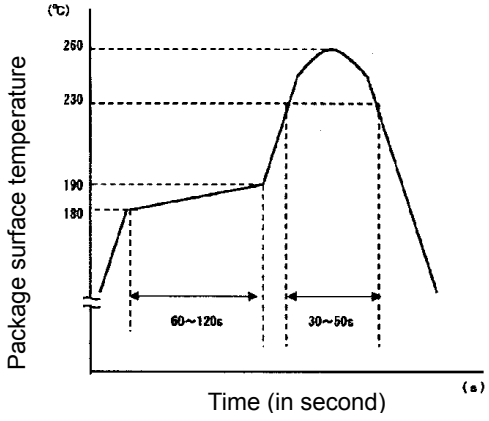


Figure 3. Recommended temperature profile for lead(Pb)-free solder

・ Hot-air reflow soldering

For the recommended temperature profiles, see Figures 2 and 3.

・ Using a soldering iron (for both eutectic and lead (Pb)-free solder)

Complete soldering within ten seconds for iron temperatures of up to 260°C or within three seconds for iron temperatures of up to 350°C.

Each lead may be heated at most once.

Note12:(1) 【Mechanical stress】

The TPCT4203 is very small and thin. Excessive mechanical stress may damage the package and/or chip. To avoid damage to the device, the distortion factor should be kept below 2000με or within the shaded area in Figure 4. Keep in mind that the stress applied to the device varies, depending on the shape, material, trace patterns, parts layout and other conditions of the pc board. Thus the integrity of the device should be tested on the actual application board. In addition, the end product should provide adequate headroom above the top (marking) side of the TPCT4203 so that no mechanical stress will be applied to it.

The distortion factor (ε) is given by: $\varepsilon = 6hS / (L * L)$

h: Board thickness S = Bend L = Support-to-support distance

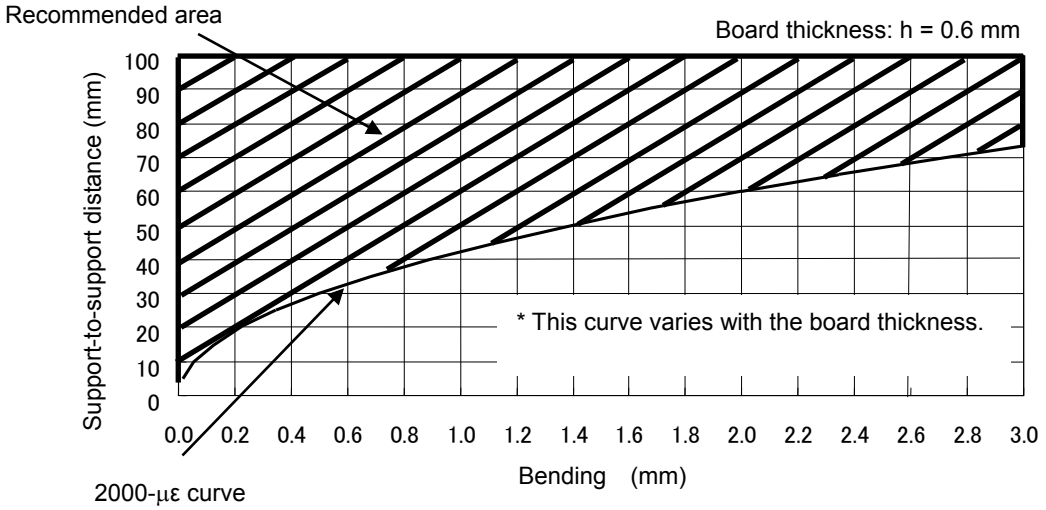


Figure 4. Support-to-support distance vs. bending

Test method (reference standard JEITA ED-4702A):

The test board is placed on supports with the TPCT4204 face-down. The supports are placed with a distance of 31 mm as shown in Figure 5 below. Stress is applied to the test board as shown in Figure 6.

Test board: FR-4 glass epoxy board (JIC C 6484) measuring 36 mm × 6 mm × 0.6 mm

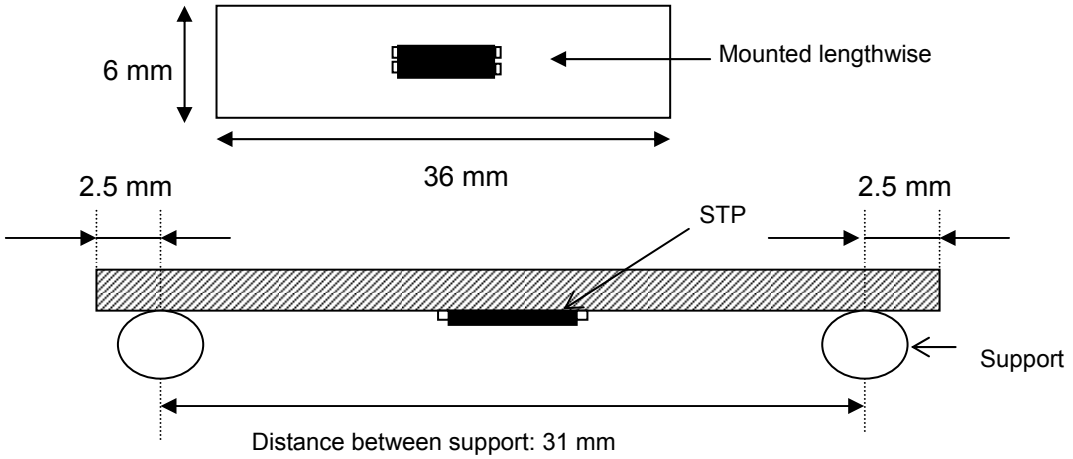


Figure 5. Placement

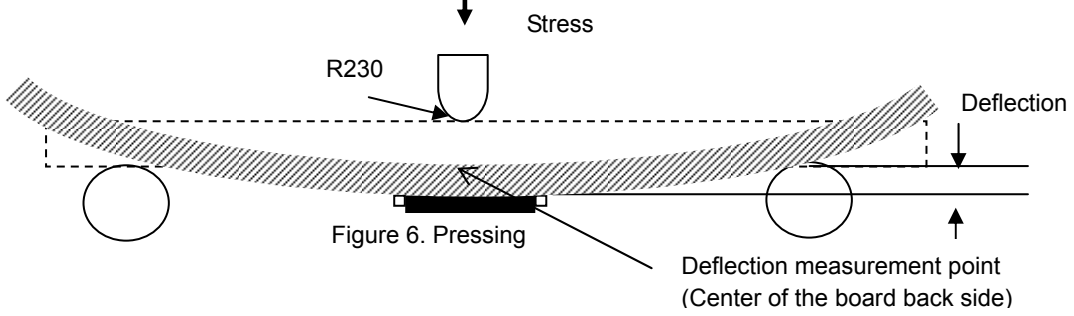


Figure 6. Pressing

(2) A rigid pc board with a thickness of 0.4 mm or more should be used for actual applications.

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20070701-EN GENERAL

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