High-Side NFET Driver for 48-V Battery Pack

Features

- Support Back-to-Back NMOS for Charging and Discharging Controlling in the Battery Pack
- Support PFET for Limiting Current as Pre-Charge with Depleted Battery or as Pre-Discharge for the Output Capacitor
- Independent Digital Control Input for CHG FET, DSG FET, PFET, and Charger Pump
- Scalable External Capacitor to Support Multi-FETs in Parallels
- Integrated Pack Voltage Divider Switch for Host Measuring
- Support Common or Separated Charge and Discharge Path Configuration
- Current in Normal Mode: 60 μA
  Current in Shutdown Mode: less than 9 μA at maximum
- TSSOP16 Package

Applications

- Ebikes, Escooters, Emotorcycles
- UPS and Energy Storage Systems
- Base-Station Battery Systems
- 12-V to 48-V Battery Packs

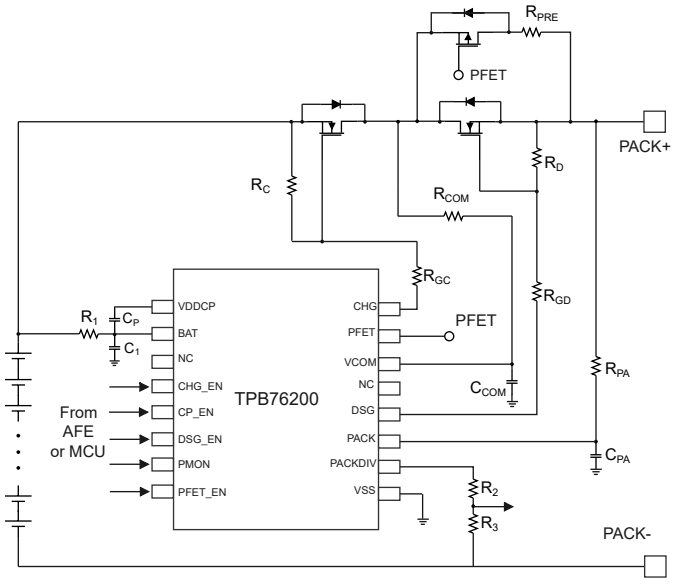
Description

The TPB76200 device is a high-side NFET driver integrated with a charge pump for a 48-V battery pack. It improves the safety of the battery pack by disconnecting the charging or discharging path at the battery-positive terminator. It avoids high-voltage broking communication ports by continuous ground. The device has a pre-charge or pre-discharge FET control. It can be used as a pre-charge FET control to charge a depleted battery and to slow the inrush current when a large bulk capacitor load is connected to the battery pack.

The independent enable inputs allow CHG and DSG FETs to be controlled by the battery pack analog front-end device or microcontroller.

The TPB76200 device is compatible with TPB76016, which is a 17-cell battery pack analog front-end device.

Typical Application Circuit



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Product Family Table

Order Number	Marking	Package	MSL
TPB76200-TS3R	7620	TSSOP-16	3

Revision History

Date	Revision	Notes
2023-10-30	Rev.A.0	Initial release.

Pin Configuration and Functions

TPB76200
TSSOP16 Package
Top View

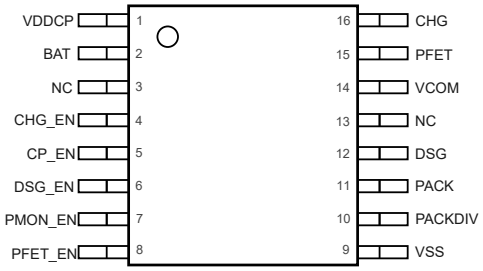


Table 1. Pin Functions: TPB76200

Pin No.	Name	I/O	Description
1	VDDCP	O	Charge pump output. Must connect a capacitor to BAT pin. Do not connect load on this pin.
2	BAT	I	Battery pack voltage input.
3	NC	-	No connect. Leave this pin floating
4	CHG_EN	I	Enable pin for CHG output.
5	CP_EN	I	Enable pin for charge pump
6	DSG_EN	I	Enable pin for DSG output
7	PMON_EN	I	Enable pin for pack monitor. It connects the PACK pin to PACKDIV pin through internal switch.
8	PFET_EN	I	Enable pin for precharge FET or predischarge FET.
9	VSS	G	Ground.
10	PACKDIV	O	Pack voltage divider pull-up voltage.
11	PACK	I	Pack voltage input/
12	DSG	O	Discharge FET gate driver output.
13	NC	-	No connect. Leave this pin floating
14	VCOM	P	Power supply.
15	PFET	O	Precharge or Predischarge FET gate driver output.
16	CHG	O	Charge FET gate driver output.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Input Voltage	BAT, PACK, VCOM	−0.3	100	V
	CHG_EN, DSG_EN, PFET_EN, PMON_EN, CP_EN	−0.3	15	V
Output Voltage	CHG, DSG, PFET, PACKDIV, VDDCP	−0.3	100	V
T_J	Maximum Junction Temperature	−40	125	°C
T_A	Operating Temperature Range	−40	85	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	0		75	V
V_{PACK}	Pack Voltage	0		75	V
V_{COM}	Input Voltage of Power Supply (it is the minimum voltage of V_{BAT} and V_{PACK})	8		75	V
V_{IN}	Input Voltage of CHG_EN, DSG_EN, PFET_EN, PMON_EN, CP_EN pins	0		14	V
C_{VDDCP}	Charge Pump Capacitor		1		μF

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP-16	115	50	°C/W

Electrical Characteristics

All test conditions: V_{BAT} = 48 V, T_A = +25°C, MIN and MAX values are tested with V_{BAT} = 8 V to 75 V with TA = −40°C to 85°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current						
I_{NOR}	Normal Mode Current, from COM and BAT pin.	C_{VDDCP} = 10nF, V_{BAT} = 8 V, C_L = 10 nF		36	60	μA
		C_{VDDCP} = 10nF, V_{BAT} = 48 V, C_L = 10 nF		38	60	μA
I_{SD}	Sum of Current of V_{COM}, V_{BAT}	Shutdown mode, PACK = 0 V, BAT = 8 V		5	9	μA
$V_{OP,MIN}$	Minimal Operation Voltage		8			V
Charge Pump						
V_{CP}	Charge Pump Voltage	No load, CP_EN = High, V_{VDDCP} – V_{BAT}	9		14	V
t_{CP}	Charge Pump Boot up Time from Zero Voltage	C_{VDDCP} = 470 nF, 10% to 90% of V_{CP}		100		ms
Input Control Pins						
V_{IL}	Digital Low Input Level for CHG_EN, DSG_EN, PFET_EN, CP_EN, PMON_EN				0.58	V
V_{IH}	Digital High Input Level for CHG_EN, DSG_EN, PFET_EN, CP_EN, PMON_EN		1.2			V
Charge FET Driver						
V_{CHGON}	CHG Gate Drive on Voltage	C_L = 10 nF, CHG_EN = High, V_{BAT} = V_{PACK}, V_{CHG} – V_{BAT}	9	12	14	V
R_{CHGON}	CHG Gate Driver on Resistance	V_{VDDCP} – V_{BAT} = 12 V, CHG_EN = High, V_{BAT} = V_{PACK}		1		kΩ
R_{CHGOFF}	CHG Gate Driver off Resistance	V_{VDDCP} – V_{BAT} = 12 V, CHG_EN = Low, V_{BAT} = V_{PACK}		0.3		kΩ
Discharge FET Driver						
V_{DSGON}	DSG Gate Driver on Voltage	C_L = 10 nF, DSG_EN = High, V_{BAT} = V_{PACK}, V_{DSG} – V_{BAT}	9	12	14	V
R_{DSGON}	DSG Gate Driver on Resistance	V_{VDDCP} – V_{BAT} = 12 V, CHG_EN = High, V_{BAT} = V_{PACK}		3.6		kΩ
R_{DSGOFF}	DSG Gate Driver off Resistance	V_{VDDCP} – V_{BAT} = 12 V, CHG_EN = Low, V_{BAT} = V_{PACK}		1.2		kΩ
Pre FET Driver						

Parameter		Conditions	Min	Typ	Max	Unit
V_{PFETON}	PFET Gate Driver on Voltage for PMOSFET	V_{PACK} > 17 V, V_{BAT} < V_{PACK}, V_{COM} - V_{PFET}	5	12	14	V
R_{PD}	PFET Gate Driver on Resistance	V_{PACK}> 17 V, V_{BAT} < V_{PACK}, V_{COM} - V_{PFET}		16		kΩ
Pack Monitor						
$R_{PMONFET}$	On Resistance of Internal FET between PACK Pin and PACKDIV Pin	PMON_EN = High		2.5		kΩ
Timing Requirements						
t_{CHGON}	CHG on Rise Time + Propagation Delay	C_L = 10 nF, (20% of CHG_EN from Low to High) to (80% of V_{CHGON}), CP_EN = High (charge pump is already on)		20	45	μs
t_{CHGOFF}	CHG off Fall Time + Propagation Delay	C_L = 10 nF, (80% of CHG_EN from High to Low) to (20% of V_{CHGON}), CHG_EN = High to Low		7	25	μs
t_{DSGON}	DSG on Rise Time + Propagation Delay	C_L = 10 nF, (20% of DSG_EN from Low to High) to (80%of V_{DSGON}), CP_EN = High, (Charge pump is already on)		70	100	μs
t_{DSGOFF}	DSG off Fall Time + Propagation Delay	C_L = 10 nF, (80% of DSG_EN from High to Low) to (20% of V_{DSGOFF})		20	25	μs
t_{PFETON}	PFET Turn-on Time + Propagation Delay	C_L = 1 nF, (20% of PFET_EN from High to Low) to (80% of V_{PFETON})		40	95	μs
$t_{PFETOFF}$	PFET Turn-off Time + Propagation Delay	C_L = 1 nF, (20% of PFET_EN from High to Low) to (80% of V_{PFETON})		20	60	μs

Typical Performance Characteristics

All test conditions: V_{BAT} = 48 V, unless otherwise noted.

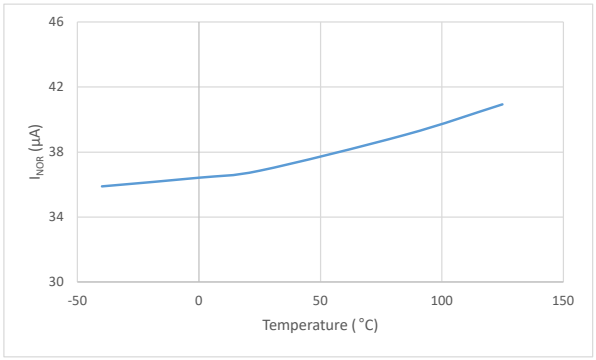


Figure 1. Normal Mode Current vs Temperature

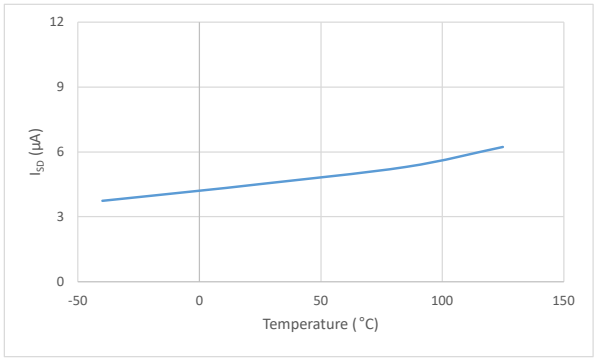


Figure 2. Shutdown Mode Current vs Temperature

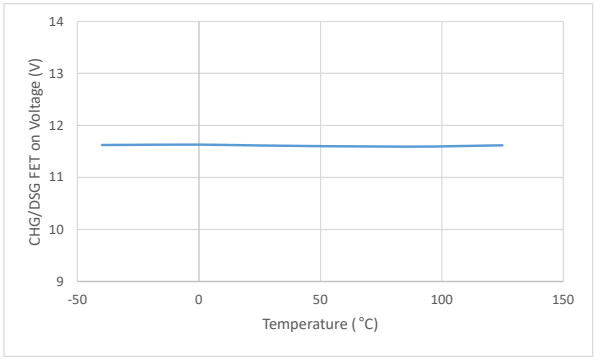


Figure 3. CHG/DSG FET on Voltage vs Temperature

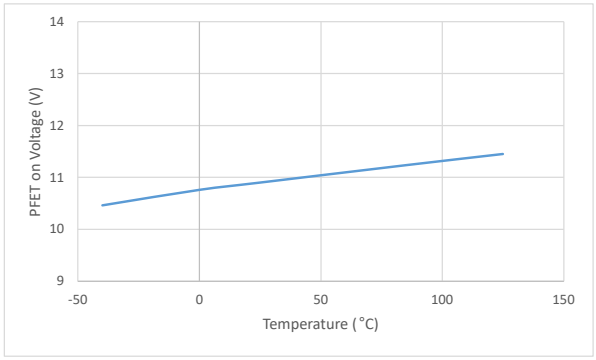


Figure 4. PFET on Voltage vs Temperature

Detailed Description

Overview

The TPB76200 device is a high-side, N-channel MOSFET driver for high-voltage system, like battery-pack systems, to implement a high-side protection.

The TPB76200 implements independent control on charging and discharging via the digital enable pins. The device has integrated charge pump which is enabled by the CP_EN pin. The enable pins, CHG_EN, DSG_EN, and PFET_EN control the CHG, DSG, and PFET driver respectively. These enable inputs can be connected to low-side driver outputs of AFE like TPB76016 or a general-purpose microcontroller.

In normal operation, when CHG_EN and DSG_EN are enabled, the CHG and DSG FET are turned on to connect the battery to PACK+. When CHG_EN and DSG_EN are disabled, the CHG and DSG FET are turned off to disconnect the battery to PACK+.

To charge a deeply depleted battery pack, a lower charging current is needed, which can be implemented by enabling PFET_EN to provide a pre charge path to battery pack. The PFET driver can be used to drive a pre-discharge FET to slow the inrush current when a big bulk capacitor load is connected to the battery pack.

The TPB76200 also has PACK+ voltage measurement, which is enabled by the PMON_EN pin. When it is enabled, the PACK+ voltage is connected to the PACKDIV pin which is connected to an external resistor divider to scale down the PACK+ voltage. The system can use the scaled-down PACK+ voltage for charger detection or advanced charging control.

Functional Block Diagram

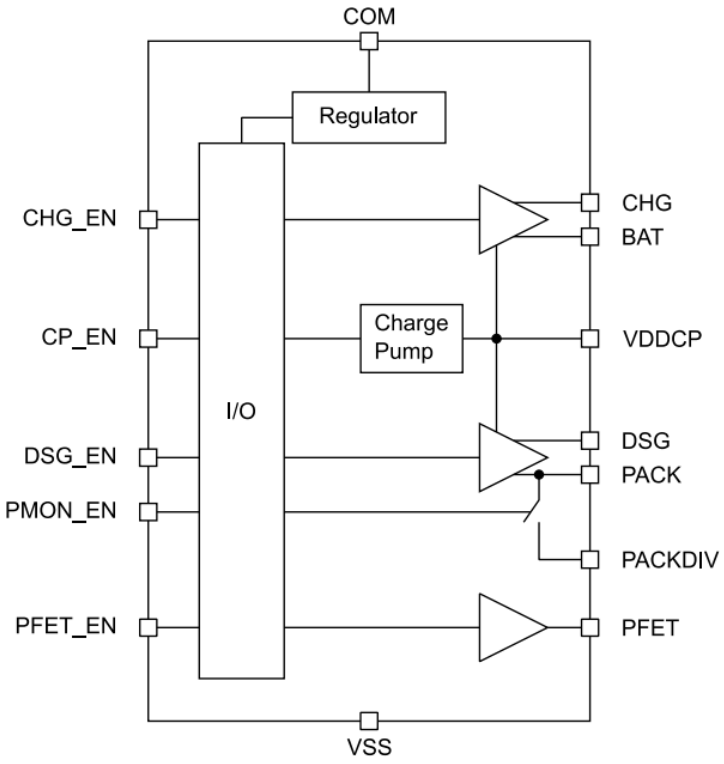


Figure 5. Functional Block Diagram

Feature Description

Charge Pump Control

The TPB76200 has an integrated charge pump, which needs a capacitor between the VDDCP pin and the BAT pin to ensure proper function. If more FETs are in parallel, the capacitor needs to be scaled up, which results in longer t_{CP}. The charge pump is controlled by CP_EN. When CP_EN is high, the charge pump voltage starts to ramp up, once the charge pump voltage is above the UVLO level, about 9 V above V_{BAT}, the charge pump is considered on. The charge pump voltage should continuously ramp to the V_{CP} level.

The charge charge pump can also be controlled by CHG_EN or DSG_EN even if the CP_EN pin is disabled. If the CHG_EN and/or DSG_EN is enabled, the CHG and/or DSG voltage starts to turn on after the charge pump voltage is above the UVLO level, and ramp up along the charge pump voltage to the V_{CP} level. The CHG and DSG turn off if the charge pump voltage falls below UVLO.

CHG and DSG Control

The CHG_EN and DSG_EN provide direct control of the CHG and DSG pins. The input levels of these pins are low enough to work with MCUs or to allow direct control from AFE FET driver. This gives a flexible option to design the system configuration. Table 2 shows the CHG and DSG pin status with respect to the CP_EN, CHG_EN, and DSG_EN.

Table 2. TCHG and DSG with Respect to CP_EN, CHG_EN, and DSG_EN

CP_EN	CHG_EN	DSG_EN	CHARGE PUMP	CHG	DSG
Lo	Lo	Lo	OFF	OFF	OFF
Lo	Lo	Hi	ON	OFF	ON
Lo	Hi	Lo	ON	ON	OFF
Lo	Hi	Hi	ON	ON	ON
Hi	Lo	Lo	ON	OFF	OFF
Hi	Lo	Hi	ON	OFF	ON
Hi	Hi	Lo	ON	ON	OFF
Hi	Hi	Hi	ON	ON	ON

PFET Control

The PFET_EN controls the PFET pin, which is a P-channel MOSFET driver and doesn't require charge pump. The PFET output driver is designed to drive an PMOSFET. The PFET driver provides an option of implementing a separated charging path with a PMOSFET to charge the battery deeply depleted, or the PFET driver can be constructed as a separated discharging path to charge the capacitor of loading. A resistor should be added in series to the PMOSFET to limit the charging or discharging current.

Pack Monitor Control

The TPB76200 provides pack voltage monitor function by the PMON pin which controls an internal switch to connect the PACK+ voltage to the PACKDIV pin, an external resistor divider is connected to the PACKDIV pin to scale down the PACK+ voltage into a measureable range of an MCU.The internal switch has an on resistance of $R_{PMONFET}$. To reduce power consumption, the PMON should be enabled only when the PACK+ voltage measurement is needed.

Function Modes

The TPB76200 has normal mode and shutdown mode. In normal mode, the charge pump is turned on, the CHG and DSG outputs are driven to V_{BAT} + V_{VDDCP}. In shutdown mode, the TPB76200 is completely powered down, all the controls inputs are driven low, and the outputs are driven low.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPB76200 device is a high-side NMOSFET driver with integrated charge pump. The device can convert a low-side battery protection system into a high-side protection system or receive enable signal from microcontroller to implement high-side protection. The device provides independent enables to control charge and discharge of a battery pack.

Typical Application

Figure 6 shows the typical application schematic of the TPB76200.

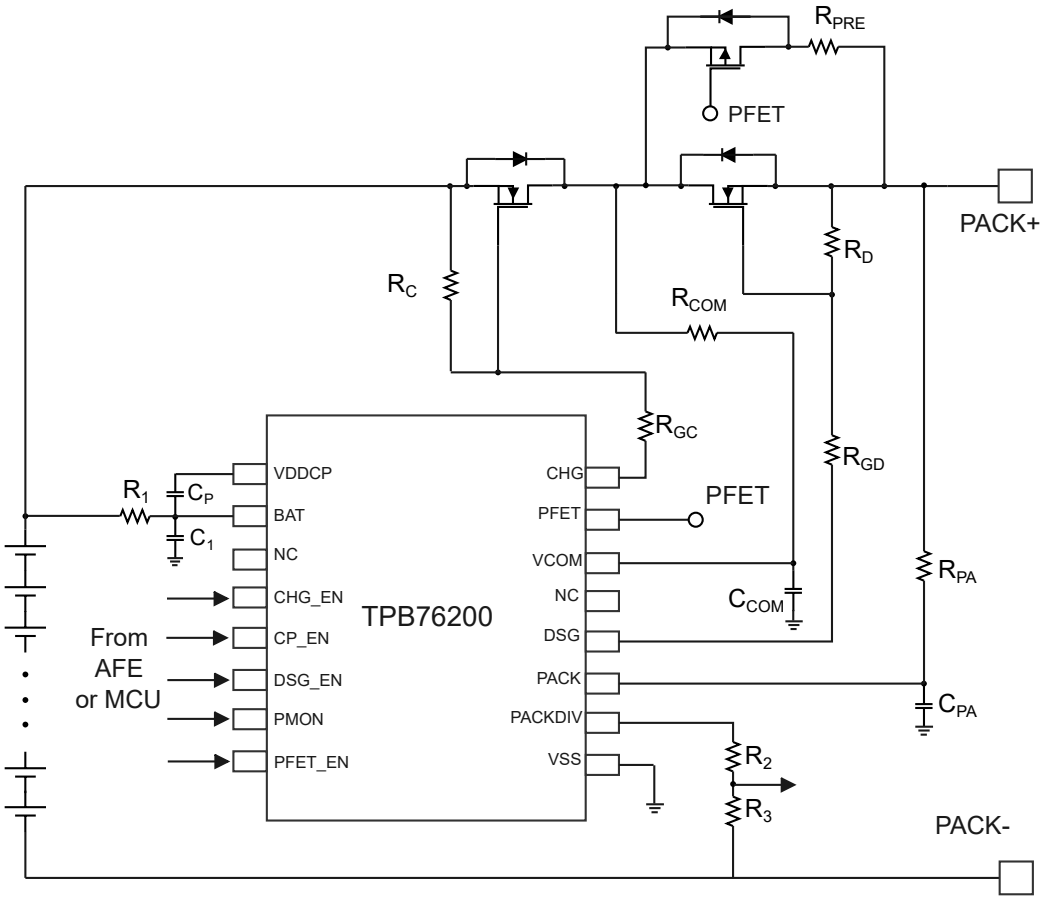
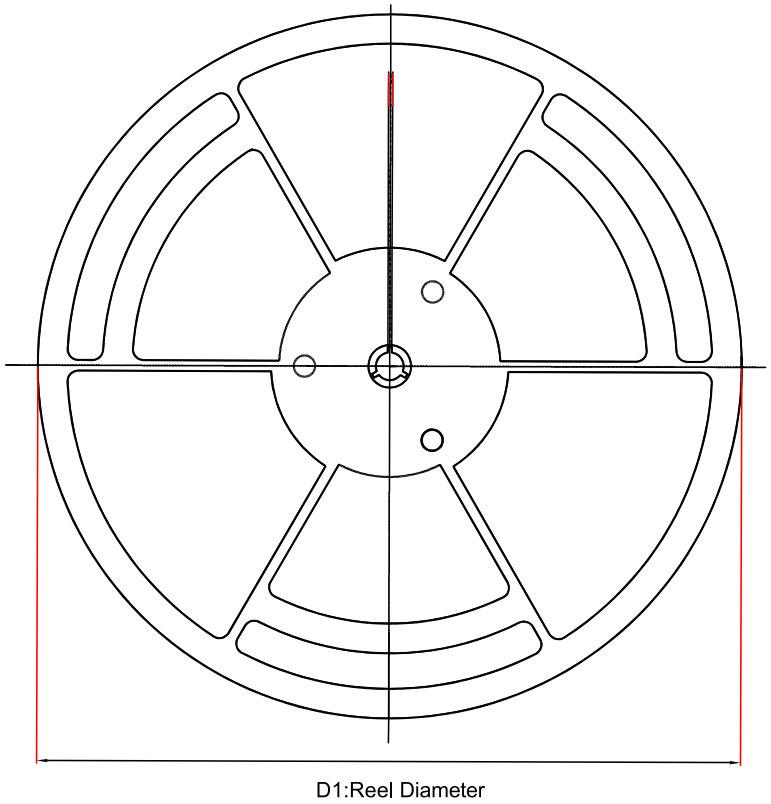
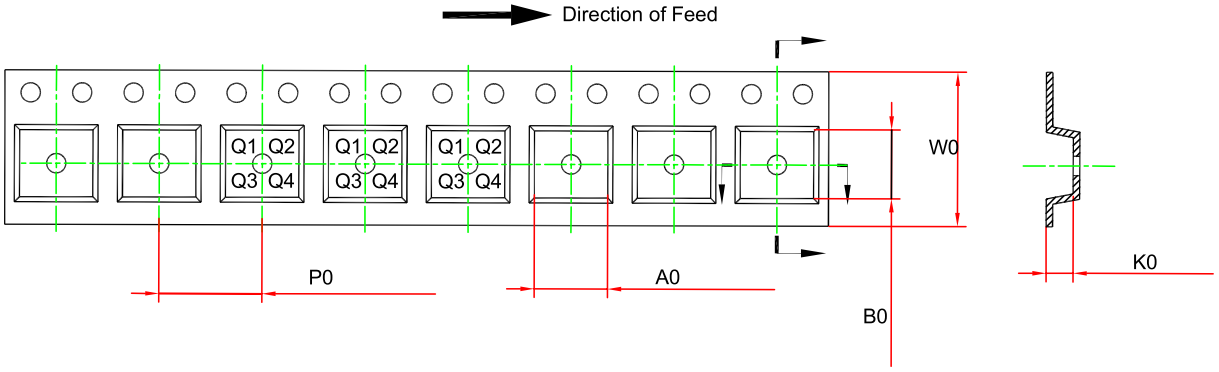


Figure 6. Typical Application Circuit

Tape and Reel Information



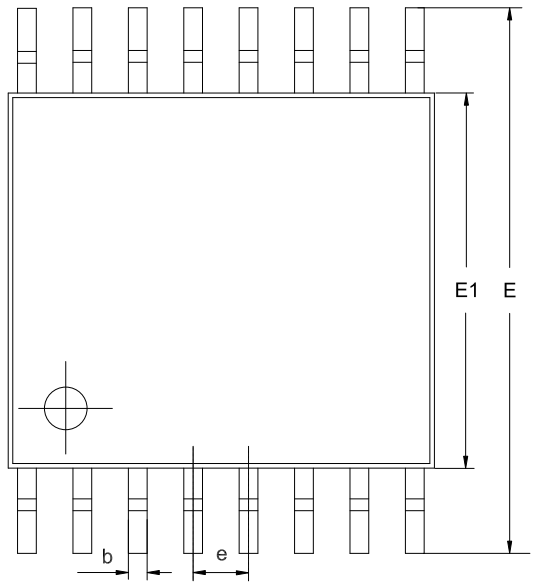


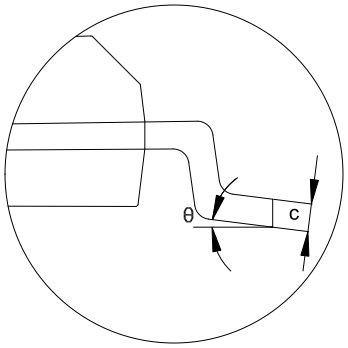
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPB76200-TS3R	TSSOP-16	330.0	17.6	6.8	5.5	1.5	8.0	12.0	Q1

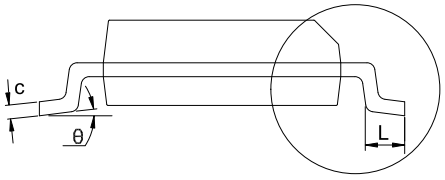
Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPB76200-TS3R	−40 to 125°C	TSSOP16	7620	3	3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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