4s High Accuracy Secondary Hardware Protector With CTL and LDO

Features

- Maximum Voltage Input 28V
- Wide Operation Voltage Range from 4V to 24V
- Low Current Consumption
  - Normal Mode 4μA at +25°C
  - Shutdown Mode 0.4μA at +25°C
- High Accuracy Voltage Detection Circuit for each cell
  - Programmable Overcharge Threshold Voltage from 4.1V to 4.8V in 50mV step
  - Overcharge Threshold Accuracy ±20mV (+25°C)
  - Overcharge Threshold Accuracy ±25mV (-10°C to +60°C)
  - Overcharge Hysteresis Voltage −380mV
- Internal Delay Timer for Overcharge
  - Selectable Overcharge Detection Delay Time 2s, 4s, 6s, and 8s
  - Selectable Delay Time for Shutdown 2s, 4s, 6s, and 8s
- High CO Pull Up Voltage
  - Selectable CMOS Active High or Low output
- Test Mode to Shorten Mass Production Time
- Integrated Linear Regulator
  - Selectable LDO Output 3.0V, and 3.3V
  - LDO output Cut off Voltage 2.5V
  - Output Current 2mA
  - Short Circuit Protector

Applications

- Notebook
- Portable Equipment

Description

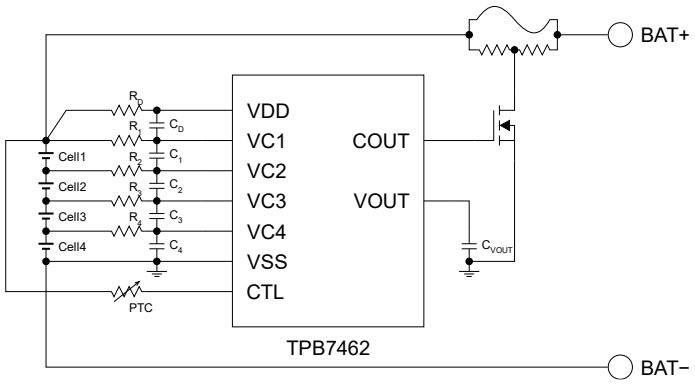
The TPB7462 series is a secondary overcharge hardware protector for 2s, 3s, or 4s lithium-ion battery packs

TPB7462 series provides high accuracy overcharge threshold to avoid the safety risk from battery pack. It also provides the CTL pin to directly control output or connect PTC (Positive Temperature Coefficient) resistor to monitor overtemperature of battery pack.

The TPB7462 integrates a LDO for powering external circuit with extremely low leakage current.

TPB7462 is available in WDFN2x2-8 package. Its operation temperature range is from −40°C to +85°C.

Typical Application Circuit



Product Name Rule

TPB7462 X X X - DFGR

Function Selection

	CTL Function at Shutdown	Timer Reset Delay Function	COUT	VOUT
A	Disable	Disable	Active High	3.0V
B	Enable	Disable	Active High	3.0V
C	Disable	Enable	Active High	3.0V
D	Enable	Enable	Active High	3.0V
E	Disable	Disable	Active High	3.3V
F	Enable	Disable	Active High	3.3V
G	Disable	Enable	Active High	3.3V
H	Enable	Enable	Active High	3.3V

Delay Time Selection

	Overvoltage Delay Time	Shutdown Delay Time
A	2s	2s
B	2s	4s
C	2s	6s
D	2s	8s
E	4s	2s
F	4s	4s
G	4s	6s
H	4s	8s
I	6s	2s
J	6s	4s
K	6s	6s
L	6s	8s
M	8s	2s
N	8s	4s
O	8s	6s
P	8s	8s

Overvoltage Threshold Selection

	Overvoltage Threshold
A	4.800V
B	4.750V
C	4.700V
D	4.650V
E	4.600V
F	4.550V
G	4.500V
H	4.450V
I	4.400V
J	4.350V
K	4.300V
L	4.250V

Table of Contents

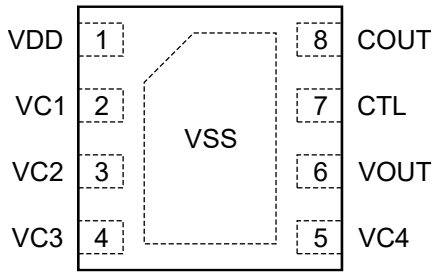
Revision History

Date	Revision	Notes
2022-04-06	Rev.A.0	First Release Version
2022-05-23	Rev.A.1	Update I_{SD} test condition

Pin Configuration and Functions

WDFN2x2-8

Top View



Pin Functions

Pin		I/O	Description
No.	Name		
1	VDD	I	Power Supply. Connect a 0.1μF capacitor to ground.
2	VC1	I	Voltage Sense Input of Positive Terminator of 1st Cell.
3	VC2	I	Voltage Sense Input of Positive Terminator of 2nd Cell and Negative Terminator of 1st Cell.
4	VC3	I	Voltage Sense Input of Positive Terminator of 3rd Cell and Negative Terminator of 2nd Cell.
5	VC4	I	Voltage Sense Input of Positive Terminator of 4th Cell and Negative Terminator of 3rd Cell.
6	VOUT	O	Voltage Regulator Output.
7	CTL	I	Control Pin for COUT.
8	COUT	O	FET Control. CMOS Output Active High or Active Low, NCH Open Drain Active High
9	Exposed Pad		Ground and Voltage Sense Input of Negative Terminator of 4th Cell.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage	VDD to VSS	−0.3	28	V
Sense Input Voltage	VDD to VC1	−0.3	6.5	V
	VCn+1 to VCn, n=1,2,3	−0.3	6.5	V
	VC4 to VSS	−0.3	6.5	V
VCO	COUT Output Voltage to VSS	−0.3	6.5	V
VOUT	VOUT Output Voltage to VSS	−0.3	6.5	V
VCTL	CTL Pin Input Voltage	−0.3	28	V
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	–45	85	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		300	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001(1)	2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002(2)	1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
WDFN2X2-8	TBD	TBD	°C/W

Electrical Characteristics

All test condition is T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overcharge and Shutdown Threshold						
V_{OTA}	Overcharge threshold accuracy	TA = 25°C	−20		20	mV
		TA = −20°C to 60°C	−25		25	mV
		TA = −40°C to 85°C	-35		35	mV
V_{HYS}	Overcharge Hysteresis Voltage			-0.38		V
V_{SD}	Shutdown Voltage Threshold	TA = 25°C	2.35	2.50	2.65	V
		TA = −40°C to 85°C	2.30		2.70	V
V_{SDR}	Shutdown Release Voltage	TA = 25°C	2.65	2.80	3.00	V
V_{TM}	Test Mode Transition Threshold				4	V
Input Voltage and Current						
V_{DD}	Operation Voltage		4		24	V
I_{DD}	Supply Current at Normal Mode	VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 3.8V, n = 1 to 3			4	µA
I_{SD}	Supply Current at Shutdown Mode	VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 2V, n = 1 to 3			0.4	µA
I_{VCn}	Input Current of VCn Pin, n = 2 to 4	VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 3.8V, n = 1 to 3			0.3	µA
	Input Current of VC1 Pin, n = 1				2	µA
I_{CTL}	Input Current of CTL	VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 4.0V, n = 1 to 3, V_{CTL} = 16V	1.2	1.6	2.4	µA
		VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 2.0V, n = 1 to 3, V_{CTL} = 8V, CTL Enable at Shutdown	0.6	0.8	1.2	µA
		VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 3.8V, n = 1 to 3, V_{CTL} = 8V, CTL Disable at Shutdown	0.35		0.35	µA
Delay Time						
t_{OV}	Overcharge Delay Time		t_{OV}x0.8	t_{OV}	t_{OV}x1.2	
t_{OVR}	Overcharge Release Time		12.8	16	19.2	ms
t_{SD}	Shutdown Delay Time		t_{SD}x0.8	t_{SD}	t_{SD}x1.2	
t_{TR}	Overcharge Delay Timer Reset Delay Time			0.38		ms
t_{OVF}	Overcharge Delay Time in Test Mode		$\frac{0.8}{128}\times t_{OV}$	$\frac{1}{128}\times t_{OV}$	$\frac{1.2}{128}\times t_{OV}$	
t_{tst}	Transition Time to Test Mode				40	ms
t_{CTL}	CTL Pin Response Time				3	ms

***Note: (1)** 100% tested at TA=25°C.

Electrical Characteristics (Continued)

All test condition is T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
COUT Output Voltage						
V_{COL}	COUT Pin ON Voltage	I_{OL} = 50μA, VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = V_{OV} − 0.1V, n = 1 to 3		0.08	0.5	V
V_{COH1}	COUT Pin ON Voltage 1	I_{OH} = −1μA, VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 4.7V, n = 1 to 3	4.0	4.7	5.4	V
V_{COH2}	COUT Pin ON Voltage 2	I_{OH} = −1mA, VDD = VC1, VC4-VSS = V_{Cn}-V_{Cn+1} = 4.7V, n = 1 to 3	V_{COH1}–0.5V	V_{COH1}–0.1V		V
Voltage Regulator Output						
V_{OUT}	VR Output Voltage	V_{DD} = 5.1V to 25V. I_{OUT} = 10μA	2.94	3.0	3.06	V
I_{OUT}	VR Output Current	V_{DD} = 5.1V to 25V			2	mA
CTL Input Voltage						
V_{IH}	CTL Pin Input Voltage, High		V_{DD}−0.8			V
V_{IL}	CTL Pin Input Voltage, Low				V_{DD}−2.0	V

***Note: (1)** 100% tested at T_A = 25°C.

Typical Performance Characteristics

All test condition: TA = +25°C, unless otherwise noted.

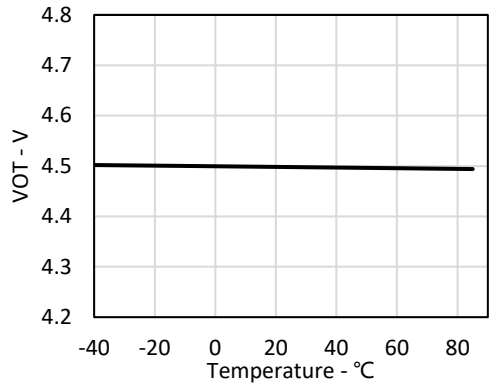


Figure 1 Overvoltage Threshold (4.5V) vs Temperature

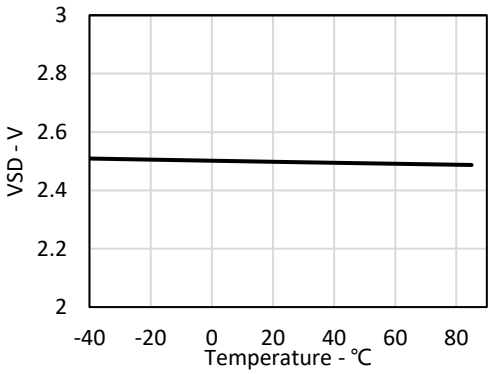


Figure 2 Shutdown Voltage Threshold V_{SD} vs Temperature

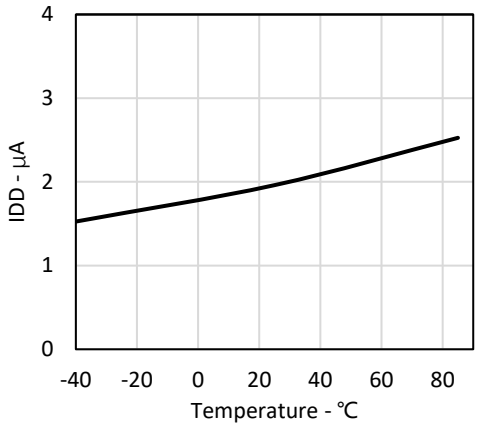


Figure 3 IDD Current vs Temperature at VDD=3.8V

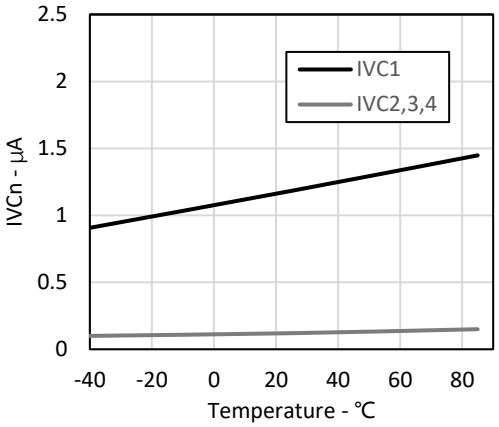


Figure 4 IVCn vs Temperature

Detailed Description

Overview

The TPB7462 series is a secondary overcharge hardware protector for 2s, 3s, or 4s lithium-ion battery packs. It provides high accuracy overcharge threshold to avoid the safety risk from battery pack. It also provides the CTL pin to directly control output or connect PTC (Positive Temperature Coefficient) resistor to monitor overtemperature of battery pack.

The TPB7462 integrates a LDO for powering external circuit with extremely low leakage current.

Feature Description

Overcharge Detection

The TPB7462 monitors VC1 to VC2, VC2 to VC3, VC3 to VC4, and VC4 to VSS voltage for over voltage protection. When the voltage of any cell exceeds V_{OT} during charging and lasts for equal to or longer than overcharge delay time (t_{OV}), COUT pin turns to H. This is called overcharge protection mode. COUT pin drives the connecting FET to provide charge control and a second protection.

Once all the cell voltages are lower than V_{OT} + V_{HYS} and last for overcharge release time (t_{OVR}), the overcharge is released, COUT pin turns to L, the TPB7462 enters normal state.

Overcharge Timer Reset

When an overcharge release noise that forces all the cell voltages temporarily below the overcharge detection voltage (V_{OT}) during the overcharge delay time (t_{OV}) counting period, the overcharge delay time will be continuously counted if the period of overcharge release noise is shorter than the overcharge delay timer reset time (t_{TR}). Otherwise, counting of t_{OV} will be reset if the period of overcharge release noise is equal to or longer than t_{TR}. After that, when V_{OT} has been exceeded, counting t_{OV} resumes. Disabling of overcharge timer reset function is user selectable.

Shutdown Detection

The TPB7462 monitors VC1 to VC2, VC2 to VC3, VC3 to VC4, and VC4 to VSS voltage for shutdown protection. When all the cell voltages are less than the V_{SD} during discharging and last for equal to or longer than shutdown delay time (t_{SD}), VOUT pin turns to L. Once the voltage of any cell exceeds V_{SDR}, TPB7462 enters normal mode and VOUT pin becomes to H.

CTL Function

The TPB7462 has a CTL pin to control the output of the COUT.

Table 1. Control via CTL Pin

CTL pin	COUT	
	Active High	Active Low
“H”	Normal state	Normal state
“Open”	“H”	“L”
“L”	“H”	“L”
“L” to “H”	--	--
“H” to “L”	--	--

COUT output active high/low is user selectable. Enabling/ disabling of CTL control function in the shutdown state is user selectable.

Timing

Overcharge detection

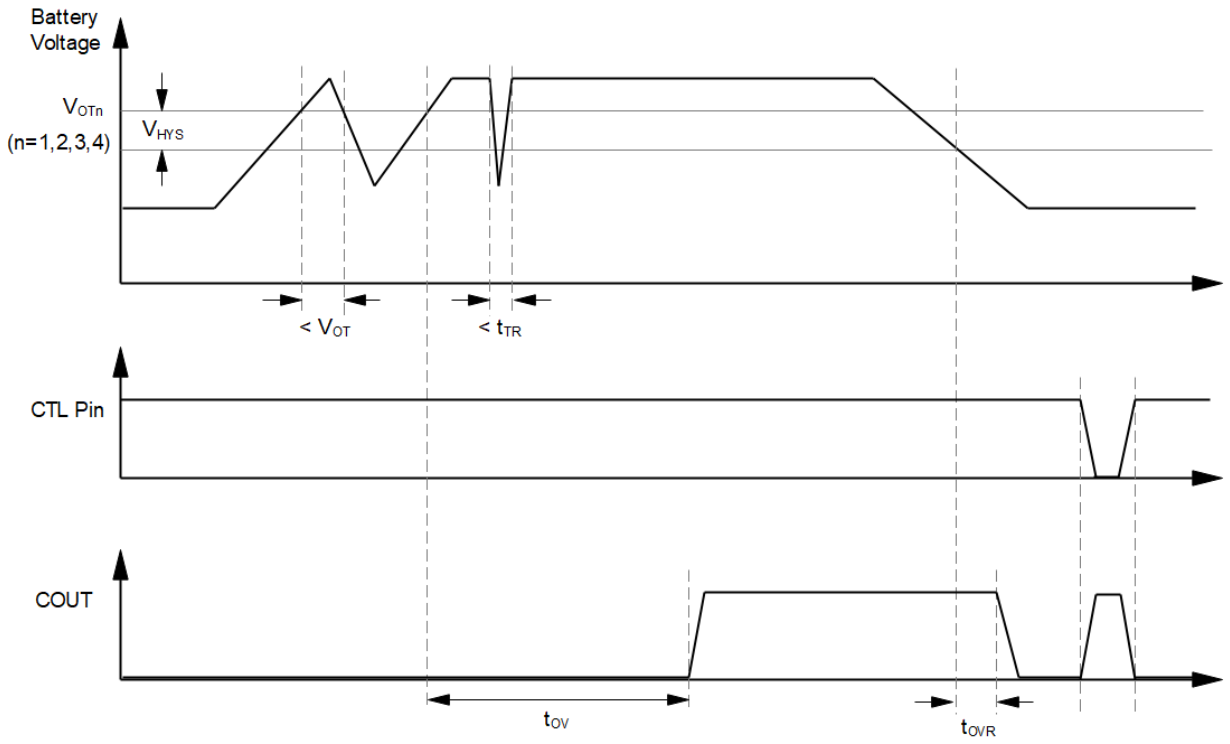


Figure 5 Timing for Overcharge

Overcharge Timer Reset

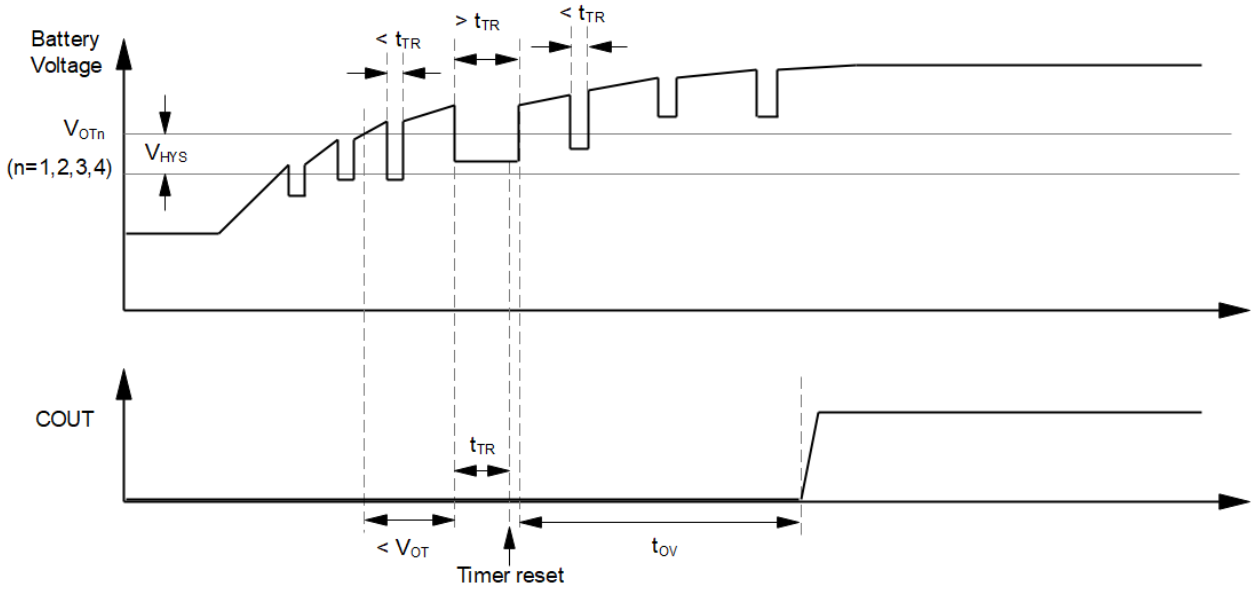


Figure 6 Timing for Overcharge Timer Reset

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPB7462 series monitors the overcharge voltage of battery for 2s, 3s, or 4s lithium-ion battery packs and controls the charging path through COUT when overcharge is detected. It also provides the CTL pin to directly control output or connect PTC resistor to monitor temperature of battery packs. The TPB7462 returns to normal state when abnormal events are disappeared.

Typical Application

Figure 7 shows the typical application schematic of the TPB7462.

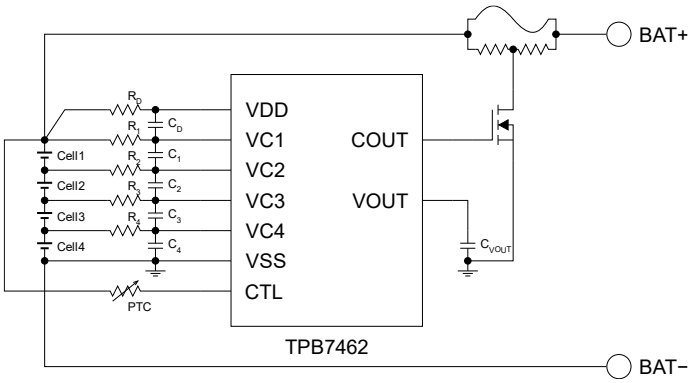


Figure 7 TPB7462 Typical Application Circuit

Symbol	Description	Recommend Value	Unit
R_1, R_2, R_3, R_4	Voltage monitor filter resistor	1	kΩ
C_P, C_1, C_2, C_3, C_4	Voltage monitor filter capacitor	0.1	μF
R_P	Supply voltage filter resistor	100	Ω
C_P	Supply voltage filter capacitor	0.1	μF
CVOUT	Regulator output capacitor	0.1	μF

Layout

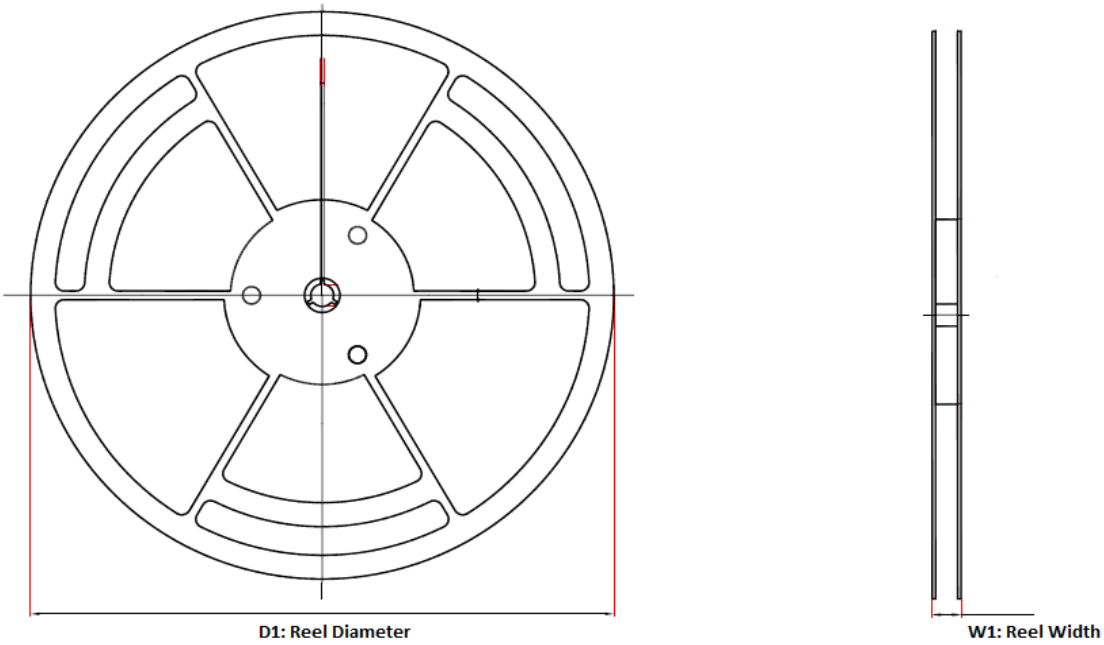
Layout Guideline

Both filter capacitors and output capacitor must be placed to the device pins as close as possible.

It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible. To get the best thermal performance, thermal vis should be placed under and around the exposed pad with enough number and size.

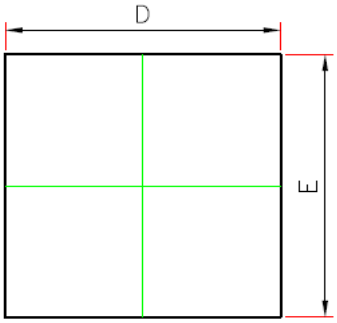
Tape and Reel Information



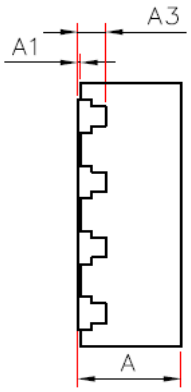
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPB7462GGA-DFGR	DFN2X2-8	180	13.1	2.3	2.3	1.1	4	8	Q1

Package Outline Dimensions

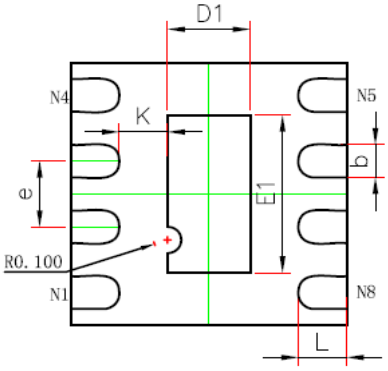
DFN2X2-8



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.500	0.700	0.020	0.028
E1	1.100	1.300	0.043	0.051
k	0.350REF.		0.014REF.	
b	0.200	0.300	0.008	0.012
e	0.500BSC.		0.020BSC.	
L	0.274	0.426	0.011	0.017

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPB7462GGA-DFGR	–40 to 85°C	DFN2X2-8	2NA	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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