

TP65H030G4PRS

650V SuperGaN® GaN FET in TOLT (source tab)

Description

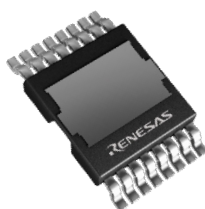
The TP65H030G4PRS 650V, 30mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

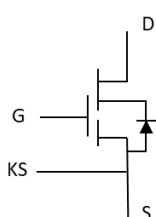
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with a 4V threshold voltage with no negative gate drive required
- Enables high-efficiency, high power density, and reliable power conversion
- Facilitates cost-effective GaN adoption reducing system size, weight, and costs

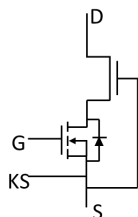
Product and Schematic Diagrams



TP65H030G4PRS TOLT



Cascode Schematic Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Zero reverse recovery charge
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Applications

- AI datacenter and telecom power supplies
- E-mobility charging
- PV inverter
- UPS
- BESS



Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum ^[1]	41
Q_{OSS} (nC) typical	135
Q_G (nC) typical	24.5

1. Dynamic $R_{DS(on)}$ (see Figure 20 and Figure 21)

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Thermal Specifications	4
2.3 Circuit Implementation	5
2.4 Electrical Specifications – Forward Device	6
2.5 Electrical Specifications – Reverse Device	7
3. Typical Performance Graphs	8
4. Test Circuits and Waveforms	12
5. Package Outline Drawings	13
6. Design Considerations	14
7. Related Information	14
8. Ordering Information	14
9. Revision History	14
A. ECAD Design Information	15

Figures

Figure 1. Pin Assignments	3
Figure 2. Simplified Half-Bridge Schematic	5
Figure 3. Typical Output Characteristics, $T_J = 25^\circ\text{C}$	8
Figure 4. Typical Output Characteristics, $T_J = 150^\circ\text{C}$	8
Figure 5. Typical Transfer Characteristics	8
Figure 6. Normalized On-Resistance	8
Figure 7. Typical Capacitance	9
Figure 8. Typical C_{OSS} Stored Energy	9
Figure 9. Typical Q_{OSS}	9
Figure 10. Typical Gate Charge	9
Figure 11. Power Dissipation	10
Figure 12. Current Derating	10
Figure 13. Forward Characteristics of Rev. Diode	10
Figure 14. Transient Thermal Resistance	10
Figure 15. Safe Operating Area $T_C = 25^\circ\text{C}$	11
Figure 16. Switching Time Test Circuit	12
Figure 17. Switching Time Waveform	12
Figure 18. Diode Characteristics Test Circuit	12
Figure 19. Diode Recovery Waveform	12
Figure 20. Dynamic $R_{DS(on)eff}$ Test Circuit	12
Figure 21. Dynamic $R_{DS(on)eff}$ Waveform	12

1. Pin Information

1.1 Pin Assignments

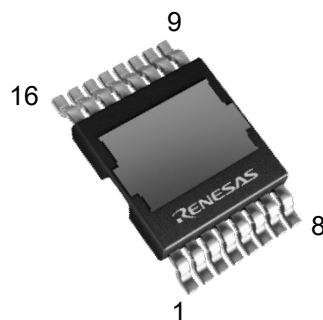


Figure 1. Pin Assignments

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 3, 4, 5, 6, 7, 8	D	Drain.
9	G	Gate.
10	KS	Kelvin Source.
11, 12, 13, 14, 15, 16	S	Source.

2. Specifications

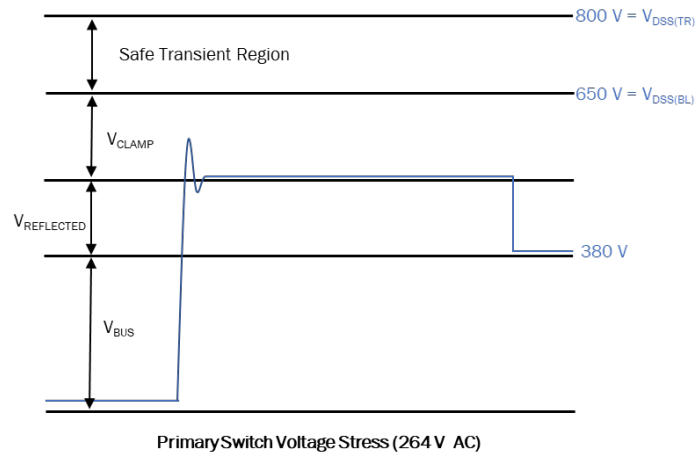
2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$ unless otherwise stated.

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	-	650	V
$V_{DSS(TR)}, \text{non-repetitive}$	Transient drain to source voltage, non-repetitive ^[1]	-	800	
$V_{DSS(TR)}, \text{repetitive}$	Transient drain to source voltage, repetitive ^[2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at $T_c = 25^\circ\text{C}$	-	192	W
I_D	Continuous drain current at $T_c = 25^\circ\text{C}$ ^[3]	-	55.7	A
	Continuous drain current at $T_c = 100^\circ\text{C}$ ^[3]	-	35	A
I_{DM}	Pulsed drain current (pulse width: 10 μs)	-	230	A
T_J	Operating temperature junction	-55	+150	$^\circ\text{C}$
T_S	Storage temperature	-55	+150	$^\circ\text{C}$
T_{SOLD}	Reflow soldering temperature ^[4]	-	260	$^\circ\text{C}$

1. In off-state, spike duration < 30 μs , non-repetitive.
2. Off-state, spike duration < 5 μs .
3. For increased stability at high current operation, see [Circuit Implementation](#).
4. Reflow MSL3.



2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\theta JC}$	Junction-to-case	0.65	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-ambient	40	

2.3 Circuit Implementation

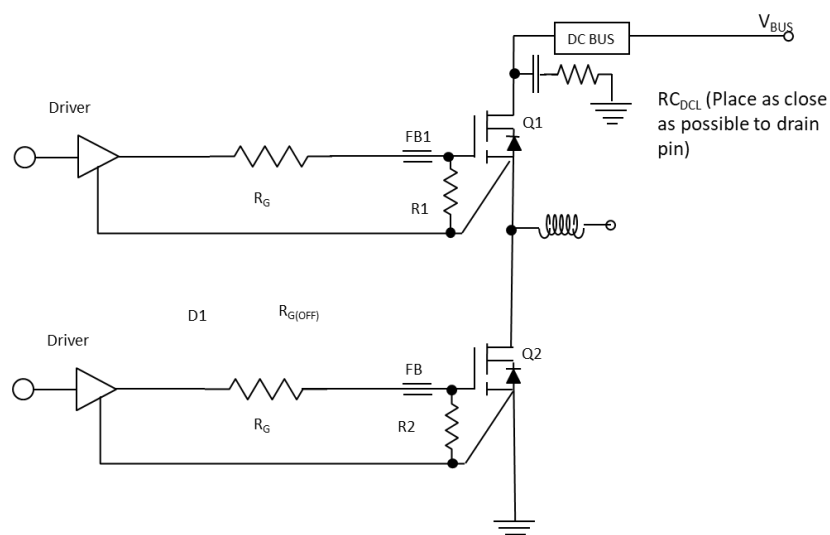


Figure 2. Simplified Half-Bridge Schematic

Recommended gate drive: (0V, 12V) with $R_{G(tot)} = 30\Omega$ ^[1]

Gate Ferrite Bead (FB1)	Recommended DC Link RC Snubber (RC_{DCL}) ^[2]
120 Ω at 100MHz	10nF + 2.3 Ω

1. For bridge topologies only.
2. Place RC_{DCL} as close as possible to the drain pin.

For additional driver configurations/options, see application note [Recommended External Circuitry for Renesas GaN FETs](#).

2.4 Electrical Specifications – Forward Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	$V_{GS} = 0V$	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1mA$	3.3	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-6.5	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance ^[1]	$V_{GS} = 12V, I_D = 30A, T_J = 25^\circ\text{C}$	-	30	41	mΩ
		$V_{GS} = 12V, I_D = 30A, T_J = 150^\circ\text{C}$	-	62	-	
I_{DSS}	Drain-to-source leakage current	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	3	30	μA
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	-	20	-	
I_{GSS}	Gate-to-source forward leakage current	$V_{GS} = 20V$	-	-	400	nA
	Gate-to-source reverse leakage current	$V_{GS} = -20V$	-	-	-400	
C_{iss}	Input capacitance	$V_{GS} = 0V, V_{DS} = 400V, f = 1MHz$	-	1500	-	pF
C_{oss}	Output capacitance		-	127	-	
C_{rss}	Reverse transfer capacitance		-	4.6	-	
$C_{O(er)}$	Output capacitance, energy related ^[2]	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	183	-	pF
$C_{O(tr)}$	Output capacitance, time related ^[3]		-	339	-	
Q_G	Total gate charge	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 12V, I_D = 30A$	-	24.5	-	nC
Q_{GS}	Gate-source charge		-	8.4	-	
Q_{GD}	Gate-drain charge		-	6.6	-	
Q_{oss}	Output charge	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$	-	135	-	nC
$t_{D(on)}$	Turn-on delay	$V_{DS} = 400V, V_{GS} = 0V \text{ to } 12V, R_{G(on)} = 10\Omega, R_{G(off)} = 30\Omega, I_D = 30A, Z_{FB} = 180\Omega \text{ at } 100MHz$ (see Figure 16)	-	26.4	-	ns
t_R	Rise time		-	6.4	-	
$t_{D(off)}$	Turn-off delay		-	63.6	-	
t_F	Fall time		-	5.2	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 20 and Figure 21 for conditions.
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

2.5 Electrical Specifications – Reverse Device

$T_J = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	$V_{GS} = 0V$, $T_C = 100^\circ\text{C}$, $\leq 25\%$ duty cycle	-	-	32	A
V_{SD}	Reverse voltage ^[1]	$V_{GS} = 0V$, $I_S = 32A$	-	1.8	-	V
		$V_{GS} = 0V$, $I_S = 16A$	-	1.3	-	
t_{RR}	Reverse recovery time	$I_S = 10A$, $V_{DD} = 400V$, $di/dt = 1000A/\mu s$	-	36	-	ns
Q_{RR}	Reverse recovery charge ^[2]		-	0	-	nC

1. Includes dynamic $R_{DS(on)}$ effect.
2. Excludes Q_{oss} .

3. Typical Performance Graphs

$T_c = 25^{\circ}\text{C}$ unless otherwise stated.

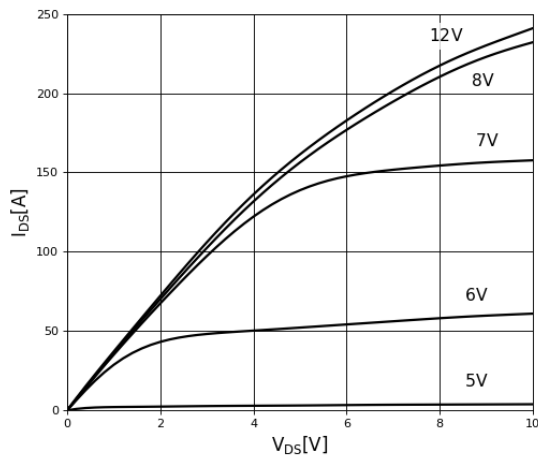


Figure 3. Typical Output Characteristics, $T_J = 25^{\circ}\text{C}$
Parameter: V_{GS}

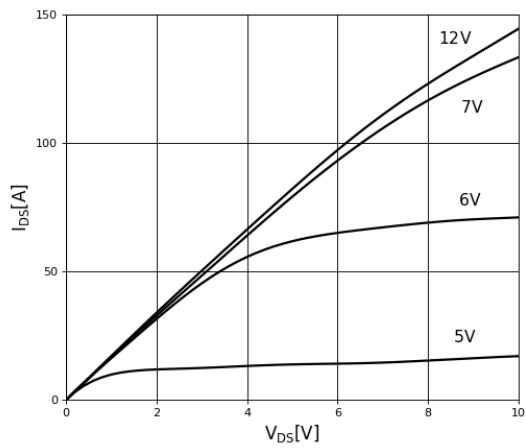


Figure 4. Typical Output Characteristics, $T_J = 150^{\circ}\text{C}$
Parameter: V_{GS}

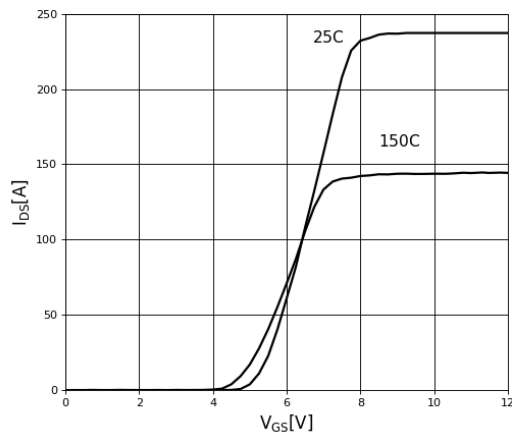


Figure 5. Typical Transfer Characteristics
 $V_{DS} = 10\text{V}$, parameter: T_J

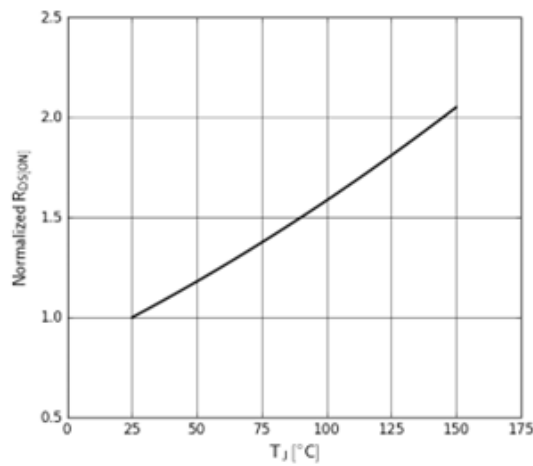


Figure 6. Normalized On-Resistance
 $I_D = 30\text{A}$, $V_{GS} = 12\text{V}$

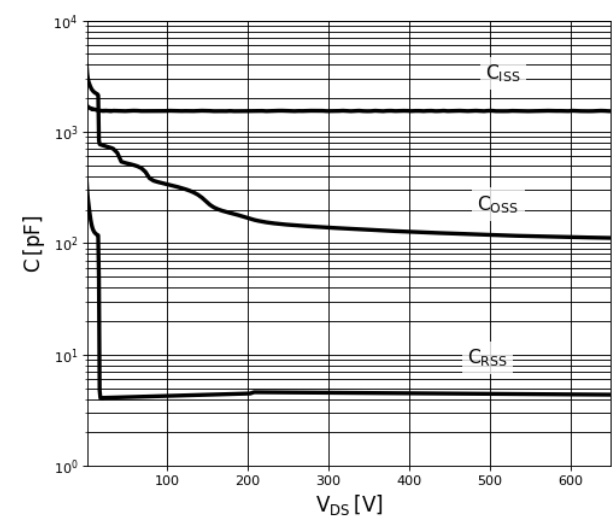


Figure 7. Typical Capacitance
 $V_{GS} = 0V, f = 1MHz$

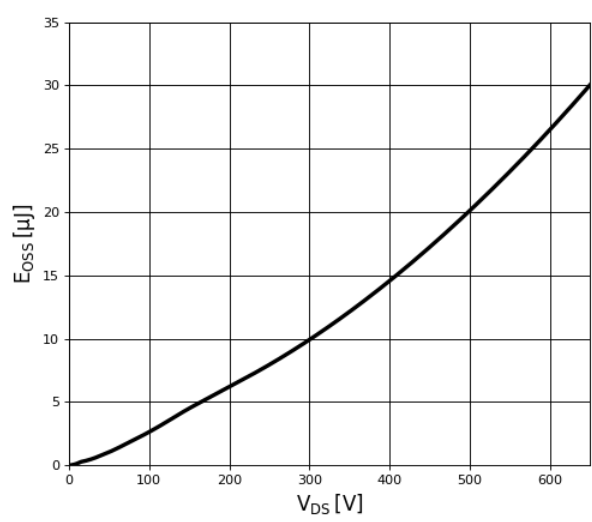


Figure 8. Typical C_{oss} Stored Energy

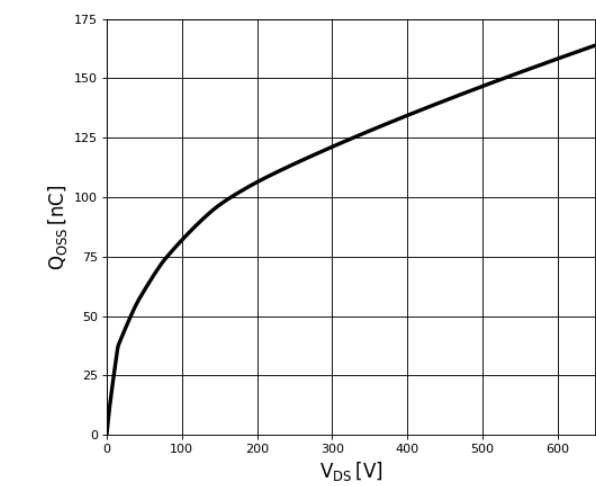


Figure 9. Typical Q_{oss}

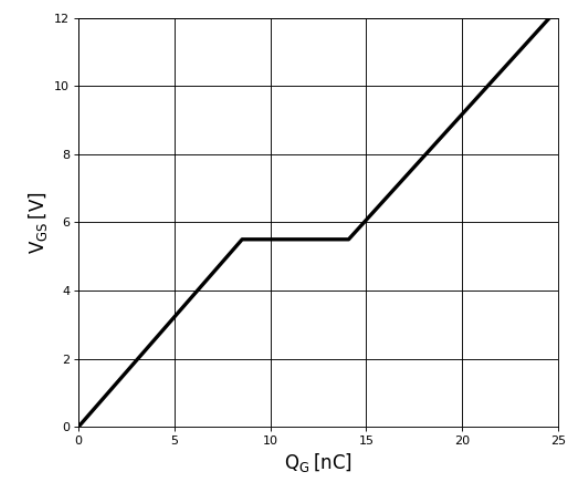


Figure 10. Typical Gate Charge
 $I_{DS} = 30A, V_{DS} = 400V$

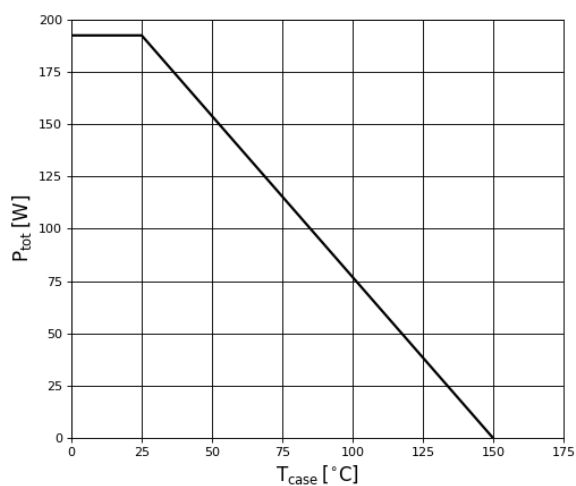


Figure 11. Power Dissipation

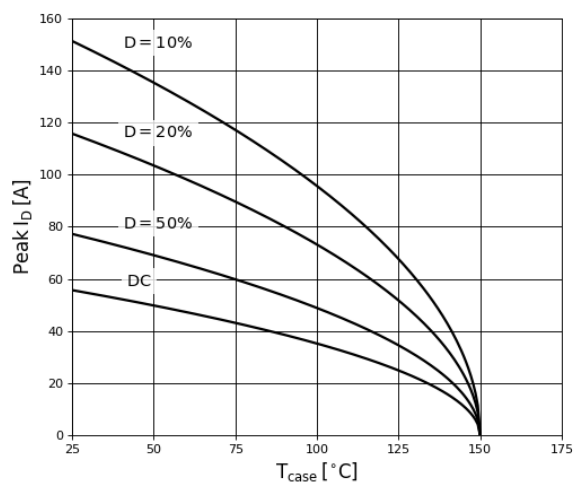


Figure 12. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 12V

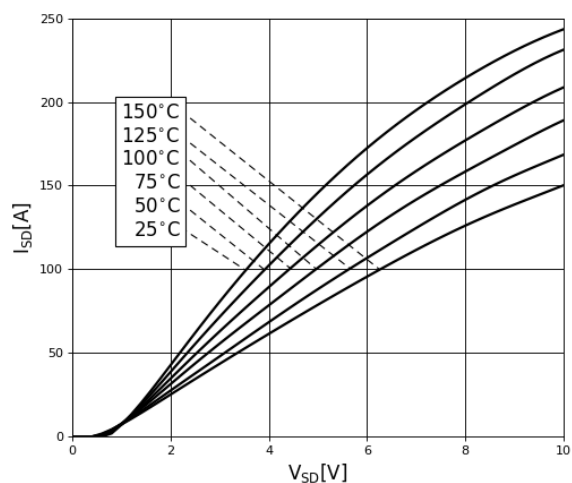


Figure 13. Forward Characteristics of Rev. Diode

I_S = f(V_{SD}), parameter: T_J

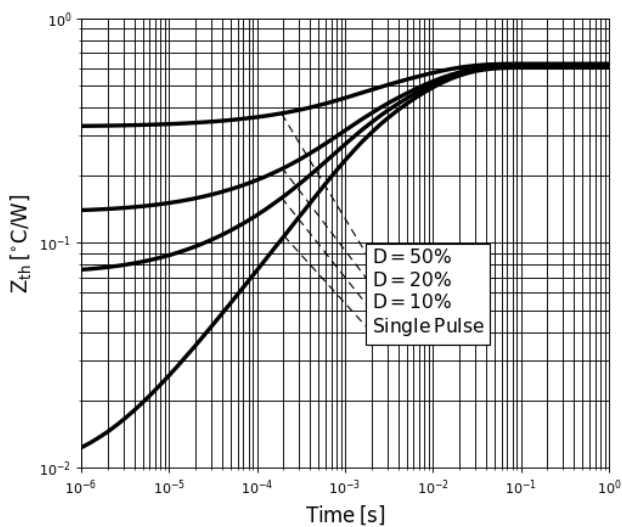


Figure 14. Transient Thermal Resistance

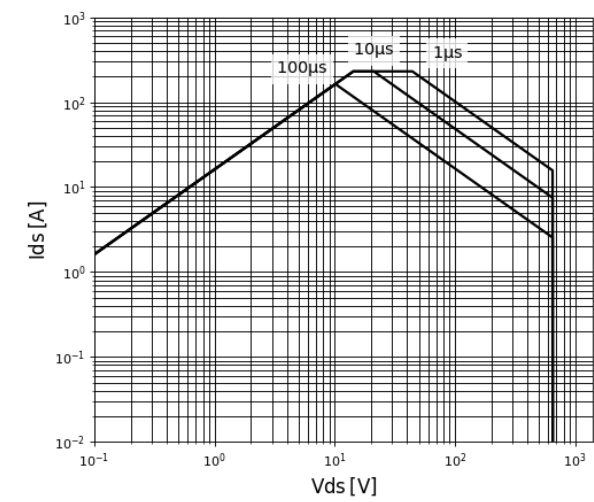


Figure 15. Safe Operating Area $T_c = 25^\circ\text{C}$

4. Test Circuits and Waveforms

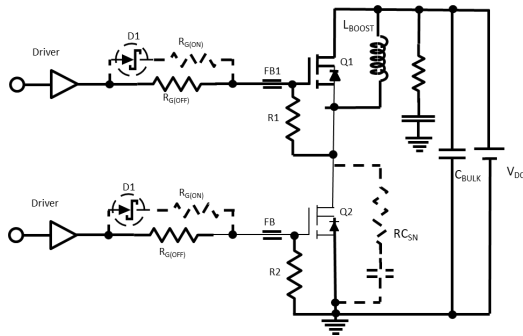


Figure 16. Switching Time Test Circuit

(For methods to ensure clean switching, see [Circuit Implementation](#))

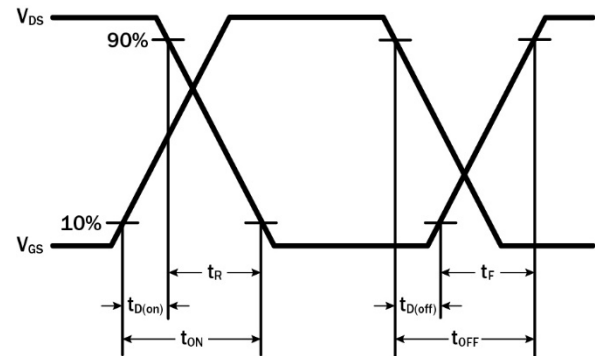


Figure 17. Switching Time Waveform

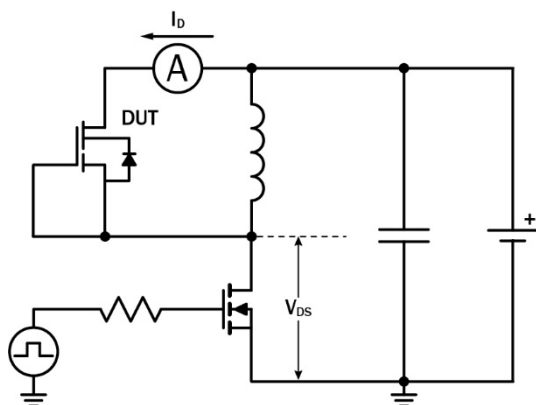


Figure 18. Diode Characteristics Test Circuit

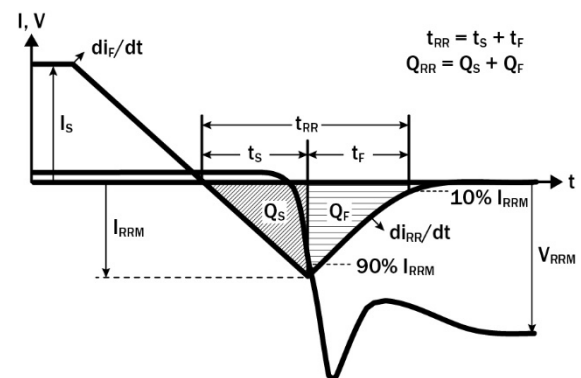


Figure 19. Diode Recovery Waveform

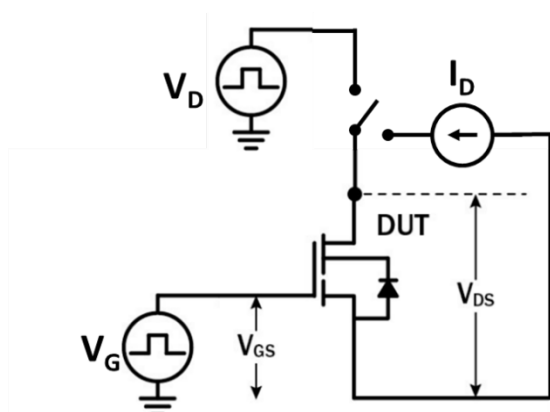


Figure 20. Dynamic $R_{DS(on)eff}$ Test Circuit

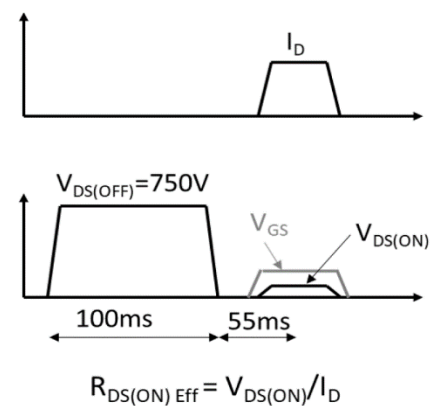


Figure 21. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



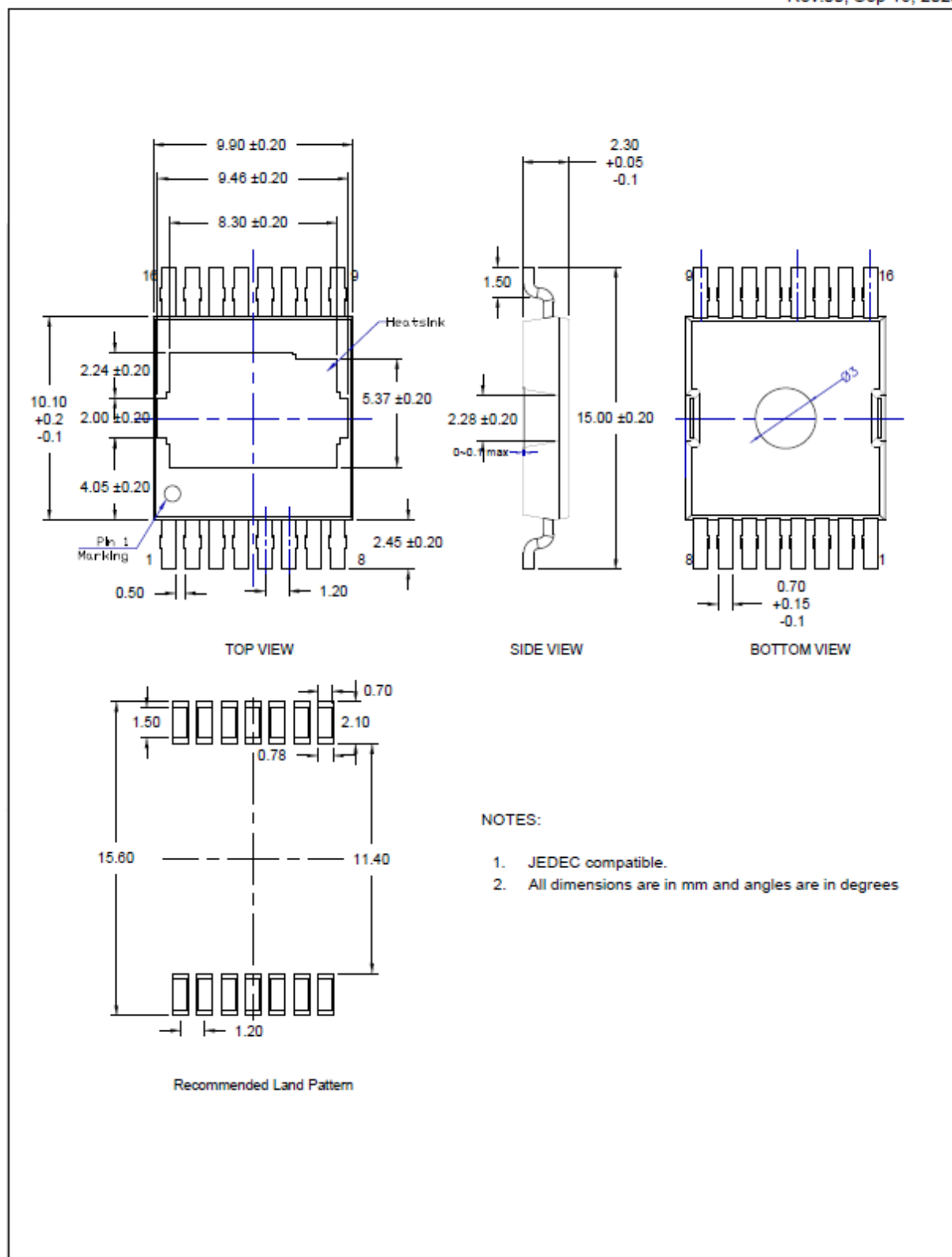
Package Outline Drawing

PSC-5184-01

TN0016AA

16-TOLT 10.1 x 9.9 x 2.3 mm Body, 1.2 mm Pitch (ePad Top Side: 8.3 x 5.37 mm)

Rev.00, Sep 16, 2025



© Renesas Electronics Corporation

6. Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high-frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The following table provides some practical rules to follow during the evaluation.

When Evaluating Renesas GaN Devices:	
DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop.	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout.
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB.	Use long traces in drive circuit, long lead length of the devices.
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points.	Use differential mode probe or probe ground clip with long wire.

7. Related Information

The complete technical library of GaN design tools can be found at [Renesas](#):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Specific resources include:

- [Printed Circuit Board Layout and Probing for GaN Power Switches](#)
- [Recommendations for Vapor Phase Reflow](#)
- [Recommended External Circuitry for GaN FETs](#)

8. Ordering Information

Part Number	Package Description
TP65H030G4PRS	TOLT

9. Revision History

Revision	Date	Description
1.02	Oct 23, 2025	Added ECAD Design Information .
1.01	Jul 10, 2025	Fixed typo for gate leakage unit to nA from μ A in section 2.4 .
1.00	Jun 25, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
TP65H030G4PRS	16	TOLT	TN0016AA/PSC-5184-01

A.2 Symbol Pin Information

A.2.1 16-TOLT

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	D	Passive	-
2	D	Passive	-
3	D	Passive	-
4	D	Passive	-
5	D	Passive	-
6	D	Passive	-
7	D	Passive	-
8	D	Passive	-
9	G	Passive	-
10	KS	Passive	-
11	S	Passive	-
12	S	Passive	-
13	S	Passive	-
14	S	Passive	-
15	S	Passive	-
16	S	Passive	-

A.3 Symbol Parameters

Orderable Part Number	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Max Power Dissipation	Gate Charge (Qg)	RoHS	Rds(on) Max	Drain-to-Source Voltage (Vdss)	Continuous Drain Current (Id)
TP65H030G4PRS	Industrial	SMD	-40 °C	150 °C	192 W	24.5 nC	Compliant	41 mΩ	650 V	55.7 A

A.4 Footprint Design Information

A.4.1 16-TOLT

IPC Footprint Type	Package Code/ POD number	Number of Pins
SOP	TN0016AA/PSC-5184-01	16

Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	14.80	Bottom View Side View
Maximum lead span (horizontal side)	Hmax	15.20	
Minimum body span (pin1 side)	Dmin	9.70	
Maximum body span (pin1 side)	Dmax	10.10	
Minimum body span	Emin	10.00	
Maximum body span	Emax	10.30	
Minimum Lead Width	Bmin	0.60	
Maximum Lead Width	Bmax	0.85	
Minimum Lead Length	Lmin	1.50	
Maximum Lead Length	Lmax	1.50	
Maximum Height	Amax	2.35	
Minimum Standoff Height	A1min	0.01	
Minimum Lead Thickness	cmin	0.50	
Maximum Lead Thickness	cmax	0.50	
Total number of pin positions (including absent pins)	PinCount	16	
Distance between the center of any two adjacent pins	Pitch	1.20	
Minimum thermal pad size (pin1 side)	D2min	8.10	
Maximum thermal pad size (pin1 side)	D2max	8.50	
Minimum thermal pad size	E2min	5.17	
Maximum thermal pad size	E2max	5.57	

Recommended Land Pattern			
Description	Dimension	Value (mm)	Diagram
Distance between left pad toe to right pad toe	Z	15.60	PCB Top View
Distance between left pad heel to right pad heel	G	11.40	
Row spacing. Distance between pad centers	C	13.50	
Pad Width	X	0.78	
Pad Length	Y	2.10	

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.