Features

- Fully specified rail to rail at V_{CC}= 2.5 V to 5.5 V
- Input common-mode voltage from -0.2 V to V_{CC}-1.5 V
- Low glitch CMOS-/TTL-compatible output stage
- 3.5 ns propagation delay
- Support 100pF capacitance loading
- 13.5mW at 3.3 V
- Shutdown pin
- Replacement for ADCMP601/MAX999
- −40°C to +125°C operation

Application

- High speed instrumentation
- Clock and data signal restoration
- Logic level shifting or translation
- Pulse spectroscopy
- High speed line receivers
- Threshold detection
- Peak and zero-crossing detectors
- High speed trigger circuitry
- Pulse-width modulators
- Current/voltage-controlled oscillators
- Automatic test equipment (ATE)

Description

The TP1981 is a very fast comparator. These comparators are exceptionally versatile and easy to use. Features include an input common mode range from -0.2 V to VCC-1.5 V, low noise, TTL-/CMOS-compatible output drivers, and shutdown inputs.

The device offers 3.5 ns propagation delay with 100 mV overdrive with4 mA typical quiescent current. The maximum detectable signal frequency exceeds 250MHz.

The TTL-/CMOS-compatible output stage is designed to drive up to 10 pF with full timing specs and to degrade in a graceful and linear fashion as additional capacitance is added. The comparator input stage offers robust protection against large input overdrive, and the output does not phase-reverse when the valid input signal range is exceeded.

The TP1981 is available in a 6-lead SC70 package.

Product family table

Table 1.

P/N	CH	Tpd	Icc	Vcc	Output stype	Hyst	Package
TP1981	1	3.5 ns	4.1 mA	2.5V – 5.5V	Push-pull	5 mV	SC70-6

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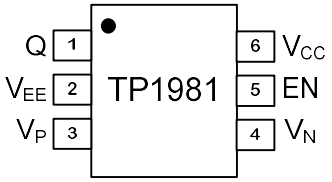
Revision History

Table 2.

Date	Revision	Notes
2017.03.21	Rev.A.0	Pre-release version
2017.05.21	Rev.A.1	Add test figure in Typical Performance Characteristics
2017.08.3	Rev.A.2	Update test data and timing definition

Pin Configuration and Functions



Pin Functions

Table 3.

Pin		I/O	Description
1	Q	O	The output of comparator
2	V_{EE}	I	The negative power supply
3	V_P	I	The positive input to comparator
4	V_N	I	The negative input of comparator
5	EN	I	Enable pin, Active high
6	V_{CC}	I	The positive power supply.

Order Information

Table 4.

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TP1981-CR	-40 to 125°C	6-Pin SC70	H81	3	Tape and Reel, 3000

Absolute Maximum Ratings*

Table 5.

Parameters		Value	Unit
Power Supply, V_{CC} to GND		6.0	V
V_{IN}	Input Voltage	GND - 0.5V to V_{CC} + 0.5V	
I_O	Output Current	50	mA
T_J	Maximum Junction Temperature	150	°C
T_A	Operating Temperature Range	–45 to 125	°C
T_{STG}	Storage Temperature Range	–65 to 150	°C
TL	Lead Temperature (Soldering 10 sec)	260	°C

*** Note:** (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

ESD, Electrostatic Discharge Protection

Table 6.

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	2	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	1	kV

Thermal Information

Table 7.

Package Type	θ_{JA}	Unit
TP1981-CR SC70 6-Lead	400	°C/W

Electrical Characteristics

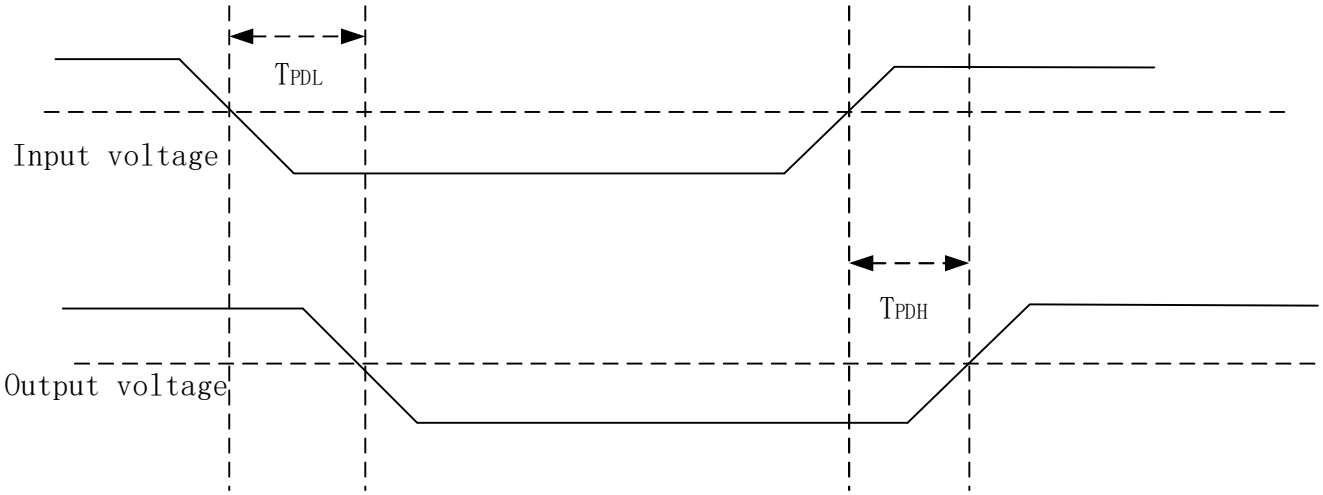
All test condition is V_{CC} = 3.3V, V_{CM}=1.65V, T_A = +25°C, R_L = 100Ω to V_{CM}, unless otherwise noted.

Table 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
V_P, V_N	Voltage Range	V_{CC} = 2.5 V to 5.5 V	−0.5		V_{CC}+ 0.2	V
	Common-Mode Range	V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC}-1.5	V
	Differential Voltage	V_{CC} = 2.5 V to 5.5 V			V_{CC}+ 0.5	V
V_{OS}	Offset Voltage		5	15	25	mV
C_P, C_N	Capacitance			1.5		pF
CMRR	Common-Mode Rejection Ratio			50		dB
		V_{CC}= 5.5 V		50		dB
	Hysteresis			5		mV
ENABLE PIN CHARACTERISTICS						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.6	V
I_{IN}	Input Current		-1		1	μA
	Sleep Time			70		Ns
	Wake-Up Time			300		Ns
DC OUTPUT CHARACTERISTICS						
V_{OH}	Output Voltage High Level	I_{OH} = –4 mA		3.25		V
V_{OL}	Output Voltage Low Level	I_{OL} = 4 mA		0.05		V
AC PERFORMANCE						
T_{RISE}	Rise Time	10% to 90% V_{CC}		0.6		ns
T_{FALL}	Fall Time	90% to 10% V_{CC}		0.6		ns
T_{PD}	Propagation Delay(T_{PDL}&T_{PDH})	$V_{OVERDRIVE}$ = 100mV		3.5		ns
PW_{MIN}	Minimum Pulse Width			2		ns
POWER SUPPLY						
V_{CC}	Supply Voltage Range		2.5		5.5	V
I_{CC}	Supply Current			4.1		mA
P_D	Power Dissipation			13.5		mW
I_{DIS}	Shut down mode current			300		μA

Timing descriptions

Symbol	Timing	Description
T_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
T_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
Trise	Output rise time	Amount of time required to transition from a low to a high output as measured at the 10% and 90% points.
Tfall	Output fall time	Amount of time required to transition from a high to a low output as measured at the 10% and 90% points
VOD	Voltage overdrive	Difference between the input voltages V A and V B



T_{PDL}&T_{PDH} system diagram

Typical Performance Characteristics

All test condition is V_{CC}= 3.3V, T_A = +25°C, R_L = 50Ω+ 10pF to GND, unless otherwise noted.

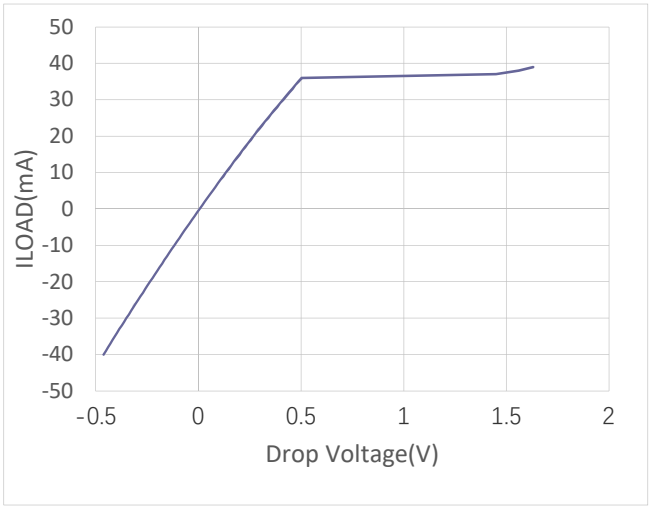


Figure 1. V_{OH}vs. Current Load

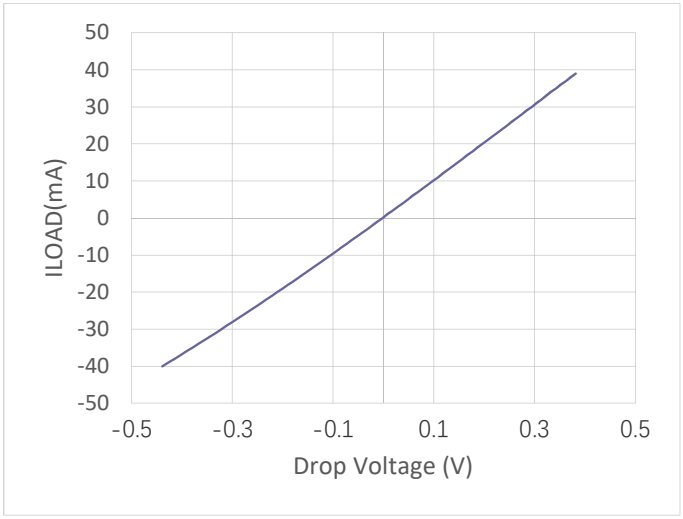


Figure 2. V_{OL} vs. Current Load

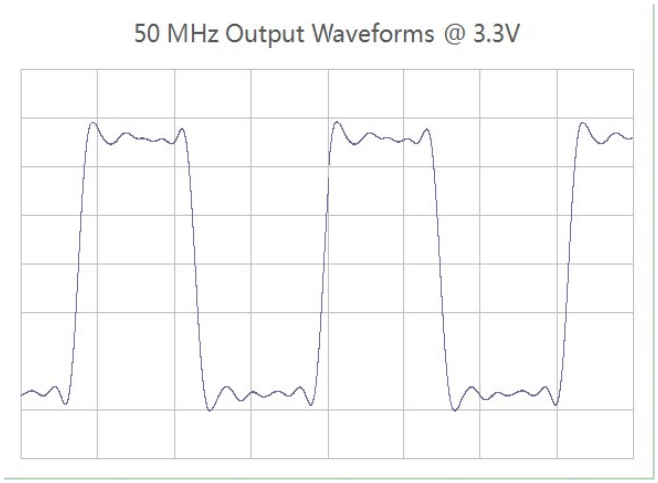


Figure 3. 50MHZ Output waveforms@3.3V

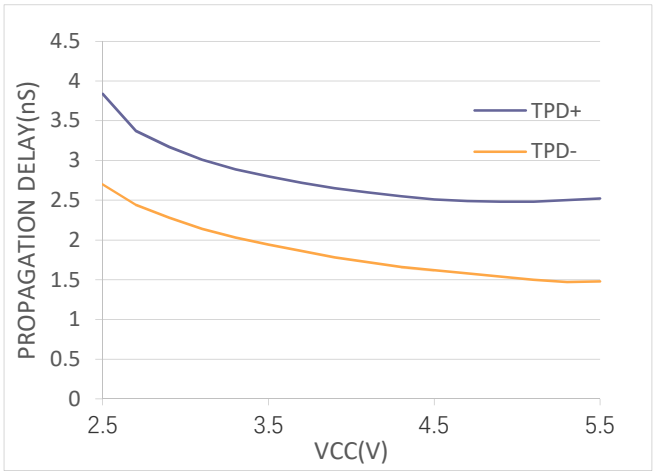


Figure 4. Propagation Delay vs. V_{CC}

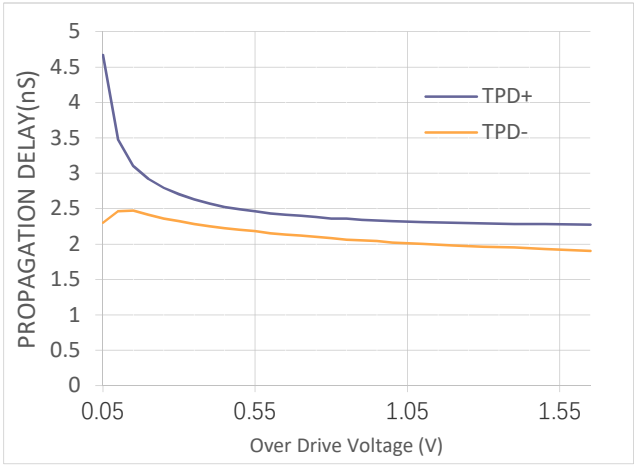


Figure 5. Propagation Delay vs. Overdrive Voltage

Package Outline Dimensions

SC70-6