



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	V _{GS(th)} (max)	Order Number / Package			
				TO-39	TO-92	SOW-20*	DICE
-20V	2.0Ω	-2.0A	-2.4V	TP0602N2	TP0602N3	—	TP0602ND
-40V	2.0Ω	-2.0A	-2.4V	TP0604N2	TP0604N3	TP0604WG	TP0604ND

*Same as SO-20 with 300 mil wide body.

Features

- ☐ Low threshold
- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Freedom from secondary breakdown
- ☐ Low input and output leakage

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

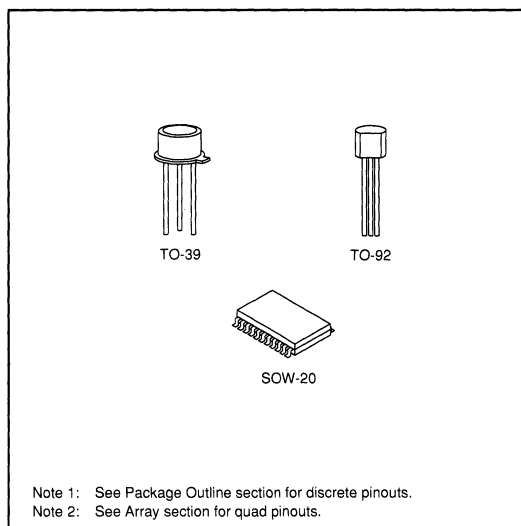
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switch
- ☐ General purpose line driver

Package Options

(Notes 1 and 2)



Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

TP06L

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JC} $^\circ\text{C/W}$	θ_{JA} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-39	-2.0A	-4.8A	6W	20	125	-2.0A	-4.8A
TO-92	-0.75A	-4.2A	1W	125	170	-0.75A	-4.2A
SOW-20	Refer to Arrays & Special Functions Section						

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

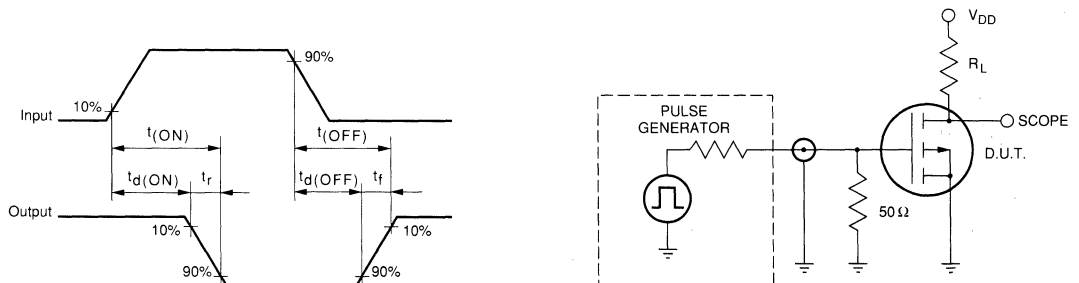
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP0604	-40			V	$V_{GS} = 0, I_D = -2.0\text{mA}$
		TP0602	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
I_{GSS}	Gate Body Leakage				-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-10	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
					-1	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.7		A	$V_{GS} = -5\text{V}, V_{DS} = -25\text{V}$
			-2.0	-3.3			$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	3.5	Ω	$V_{GS} = -5\text{V}, I_D = -250\text{mA}$
				1.5	2.0		$V_{GS} = -10\text{V}, I_D = -1.0\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	1.2	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -1.0\text{A}$
G_{FS}	Forward Transconductance		0.4	0.65		S	$V_{DS} = -25\text{V}, I_D = -1.0\text{A}$
C_{ISS}	Input Capacitance			85	150	pF	$V_{GS} = 0, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			55	85		
C_{RSS}	Reverse Transfer Capacitance			15	35		
$t_{d(ON)}$	Turn-ON Delay Time			5	10	ns	$V_{DD} = -25\text{V}$ $I_D = -1.0\text{A}$ $R_S = 50\Omega$
t_r	Rise Time			7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time			10	15		
t_f	Fall Time			6	10		
V_{SD}	Diode Forward Voltage Drop			-1.3	-2.0	V	$V_{GS} = 0, I_{SD} = -1.5\text{A}$
t_{rr}	Reverse Recovery Time			300		ns	$V_{GS} = 0, I_{SD} = -1.5\text{A}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

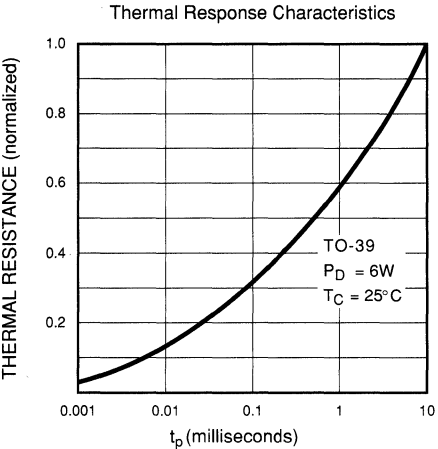
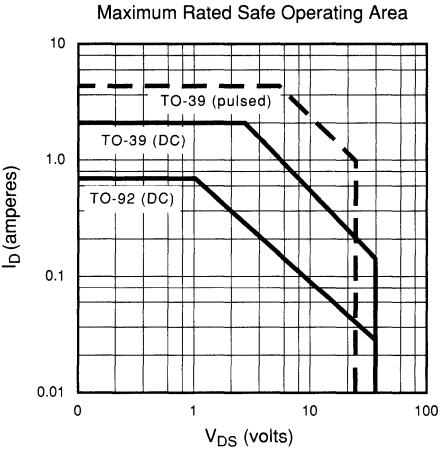
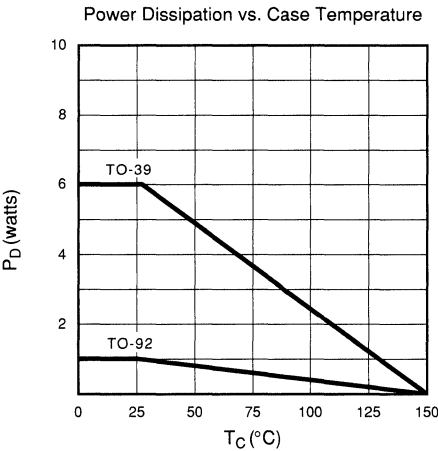
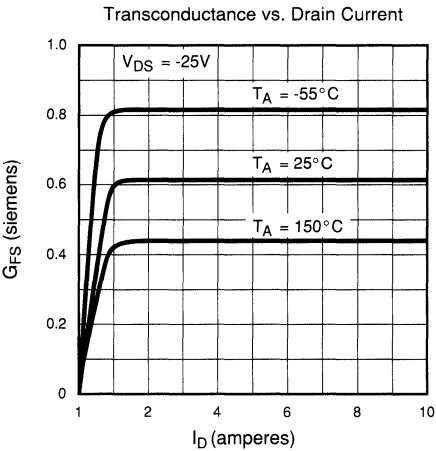
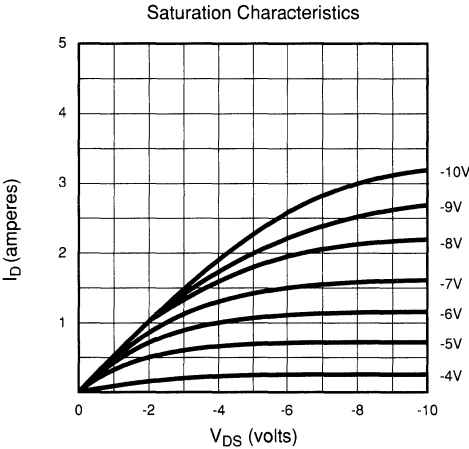
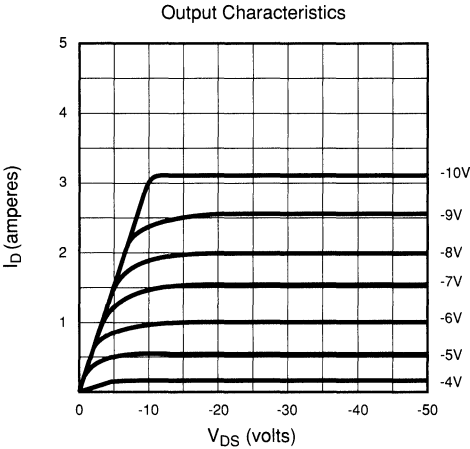
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

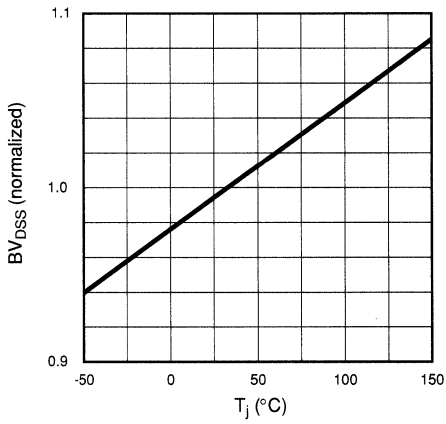


Typical Performance Curves

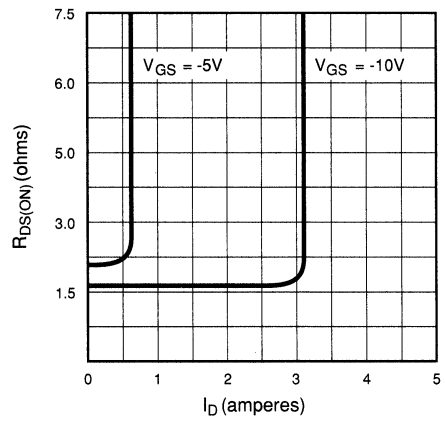
TP06L



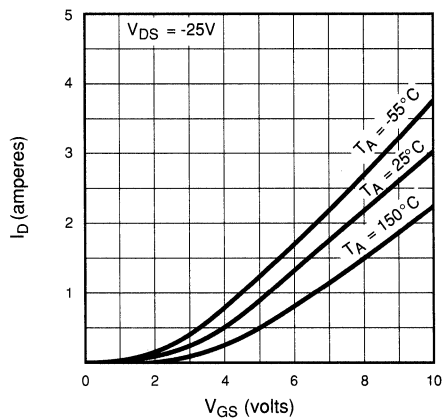
BV_{DSS} Variation with Temperature



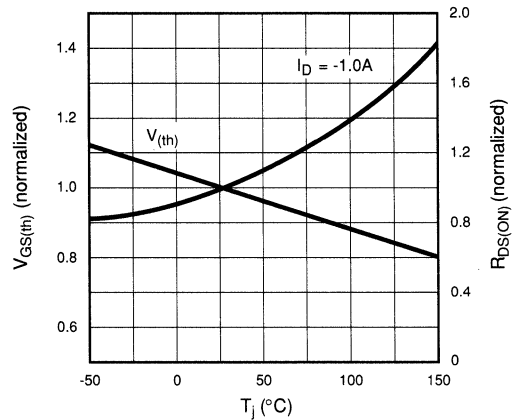
On-Resistance vs. Drain Current



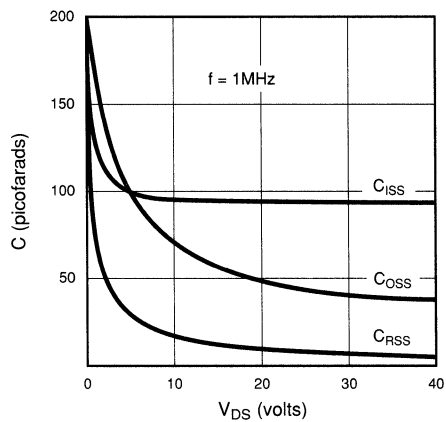
Transfer Characteristics



V_(th) and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

