# TOPT12-800C0

## TOPTriac

**21 September 2015** **Product data sheet**

## 1. General description

Planar passivated Temperature and Overload Protected Triac with high commutation performance in a SOT78 (TO-220AB) plastic package. This TOPTriac conveniently self protects by turning off in the event of excessive temperature. It is triggered negatively using continuous DC or current pulses.

## 2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- Hi-Com technology gives maximum immunity to false triggering
- High immunity to false turn-on by dV/dt
- High minimum $I_{GT}$ for guaranteed immunity to gate noise
- Over-temperature self protection function
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability

## 3. Applications

- Any circuit where protection against overload and/or over temperature is required
- Motor controls and starters – e.g. refrigeration compressors
- High power density motors – e.g. vacuum cleaners, window blinds, food processors
- Heating and cooking appliances
- Water boilers

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 100$ °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 12 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5 | | - | - | 95 | A |
| $T_j$ | junction temperature | conducting mode | | - | - | 125 | °C |
| | | self-protection mode | | - | - | 150 | °C |

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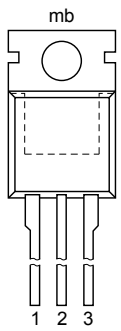
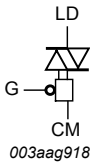
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; LD+ G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 35 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; LD- G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 35 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 35 | mA |
| $V_T$ | on-state voltage | $I_T$ = 15 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.3 | 1.6 | V |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 125 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | 500 | - | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $I_{T(RMS)}$ = 12 A; $dV_{com}/dt$ = 20 V/µs; (snubberless condition); gate open circuit | | 20 | - | - | A/ms |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | CM | common |   **TO-220AB (SOT78)** |   |
| 2 | LD | load | | |
| 3 | G | gate | | |
| mb | LD | mounting base; load | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TOPT12-800C0 | TO-220AB | plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB | SOT78 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| TOPT12-800C0 | TOPT12-800C0 |

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 100$ °C; Fig. 1; Fig. 2; Fig. 3 | | - | 12 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5 | | - | 95 | A |
| | | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms | | - | 104 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p = 10$ ms; sine-wave pulse | | - | 45 | A²s |
| $dI_T/dt$ | rate of rise of on-state current | $I_G = 70$ mA | | - | 100 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 2 | A |
| $P_{GM}$ | peak gate power | | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.5 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | conducting mode | | - | 125 | °C |
| | | self-protection mode | | - | 150 | °C |

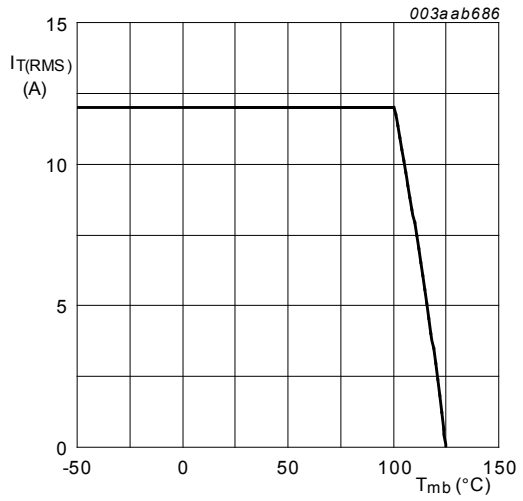
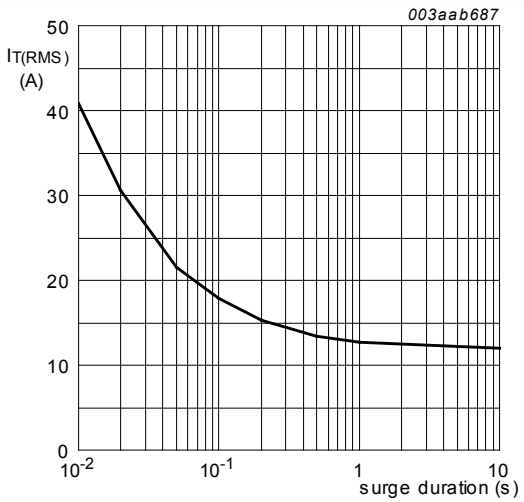
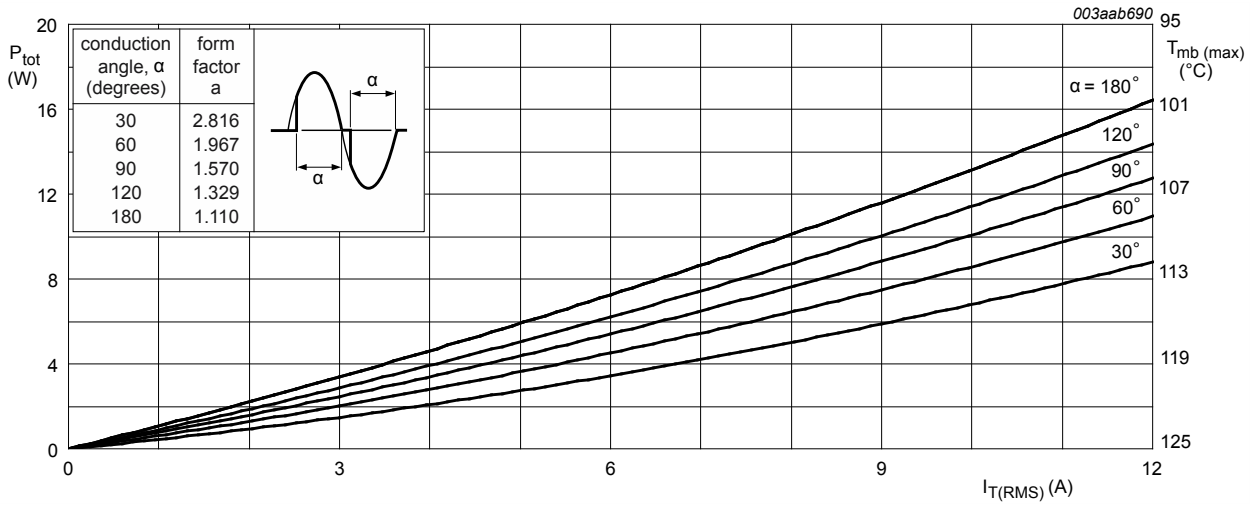



**Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values**




f = 50 Hz; $T_{mb}$ = 100 °C

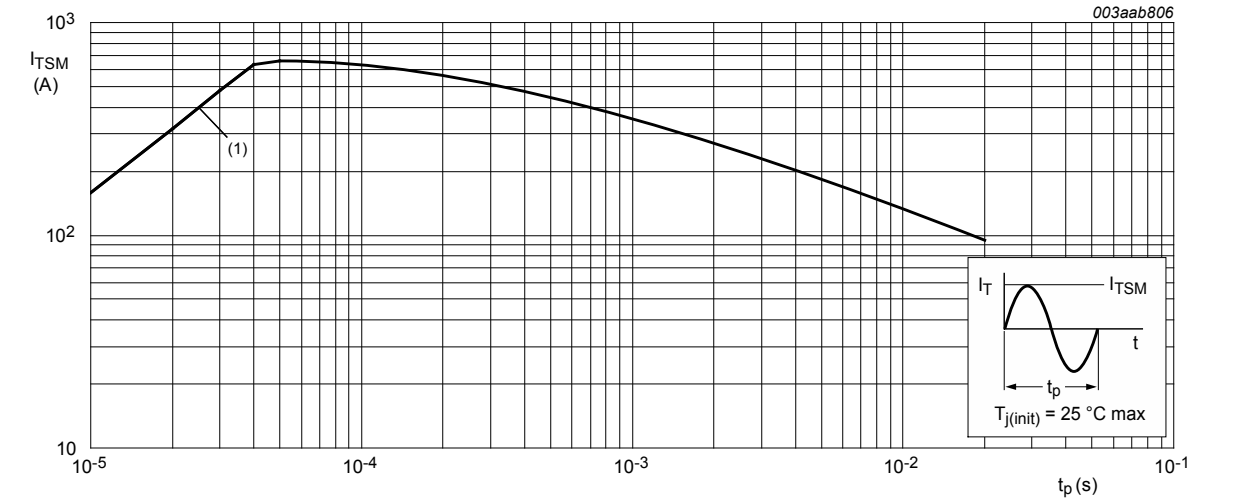
**Fig. 2. RMS on-state current as a function of surge duration; maximum values**




α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

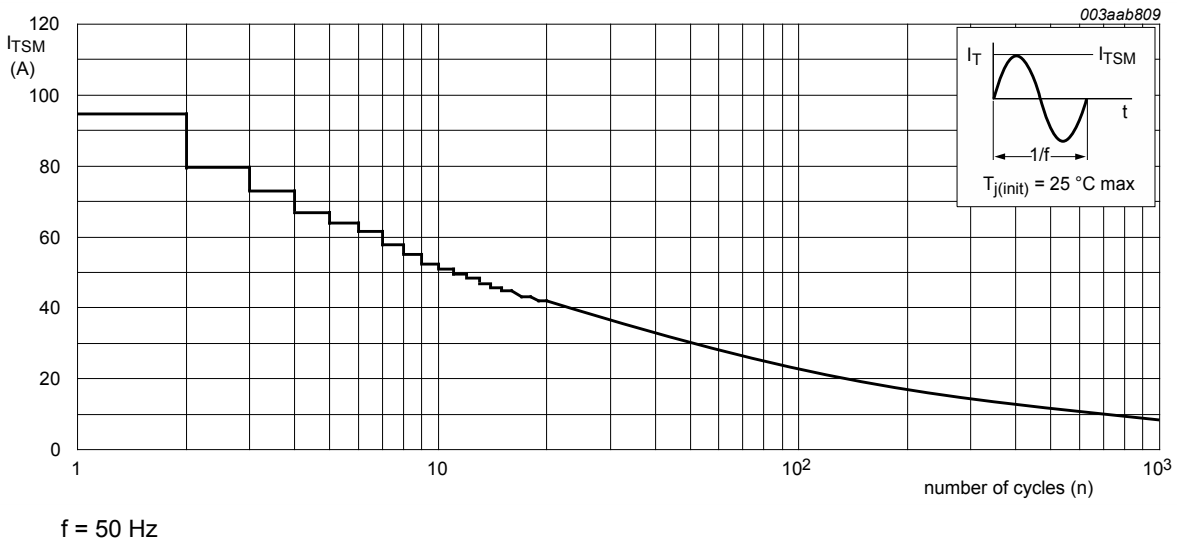
**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




$t_p \leq 20$ ms

(1) $dI_T/dt$ limit

**Fig. 4. Non-repetitive peak on-state current as a function of pulse duration; maximum values**




f = 50 Hz

**Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | full cycle; Fig. 6 | | - | - | 1.5 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air | | - | 60 | - | K/W |

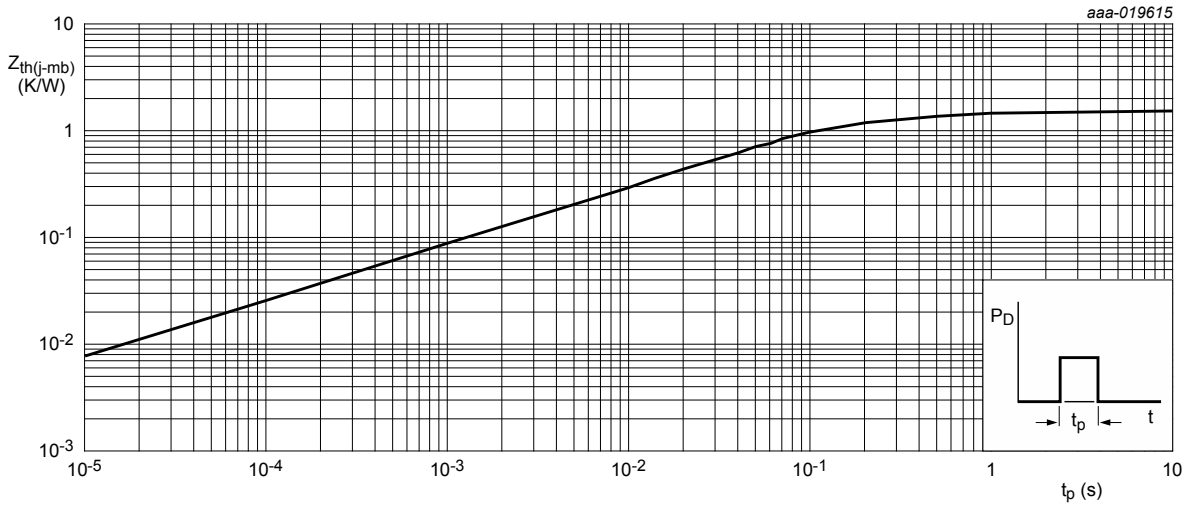
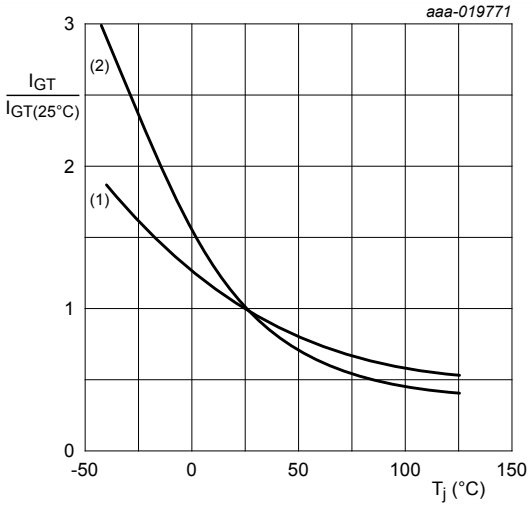



**Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 10. Characteristics

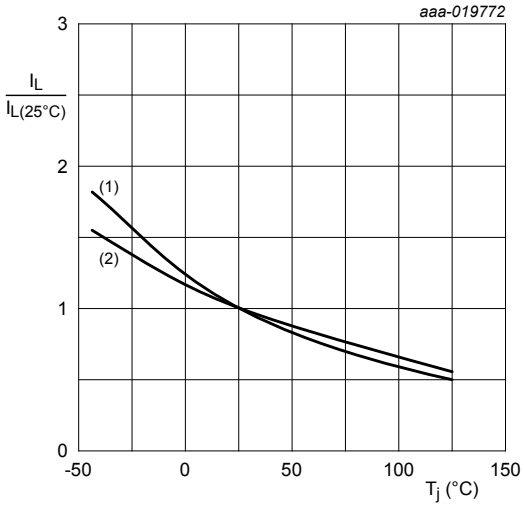
**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; LD+ G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 35 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; LD- G-; $T_j$ = 25 °C; Fig. 7 | | 5 | - | 35 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; LD+ G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 60 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; LD- G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 50 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 35 | mA |
| $V_T$ | on-state voltage | $I_T$ = 15 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 1.4 | 2.3 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11 | | 0.5 | - | - | V |
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 125 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit | | 500 | - | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $I_{T(RMS)}$ = 12 A; $dV_{com}/dt$ = 20 V/µs; (snubberless condition); gate open circuit | | 20 | - | - | A/ms |
| **Over-temperature protection characteristics** | | | | | | | |
| $T_{trip}$ | trip junction temperature | see application information | | 125 | - | 150 | °C |
| $V_{G(trip)}$ | trip gate voltage | $I_G$ = 2 mA; see application information | | 0.3 | - | - | V |
| | | $I_G$ = 50 mA; see application information | | - | - | 0.9 | V |
| **Operating requirement for pulsed gate triggering** | | | | | | | |
| $I_{G(bl)}$ | gate bleed current | $T_j$ = 25 °C; $V_G = V_{G(trip)}$; circuit-applied current requirement; see application information section | | 0.5 | - | - | mA |
| | | $T_j$ < 150 °C; $V_G = V_{GT}$; circuit-applied current requirement; see application information section | | - | - | 2 | mA |



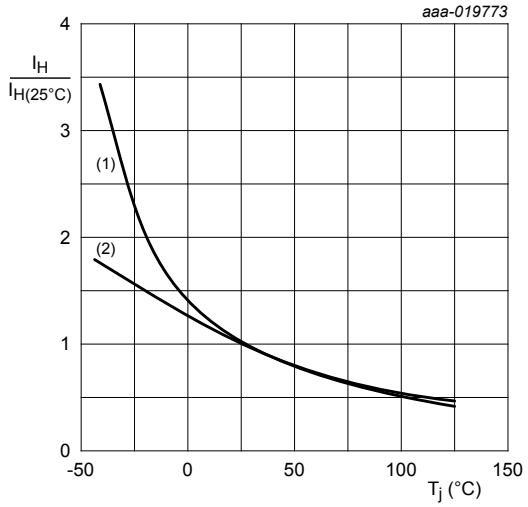

(1) LD+ G-
(2) LD- G-

**Fig. 7. Normalized gate trigger current as a function of junction temperature**



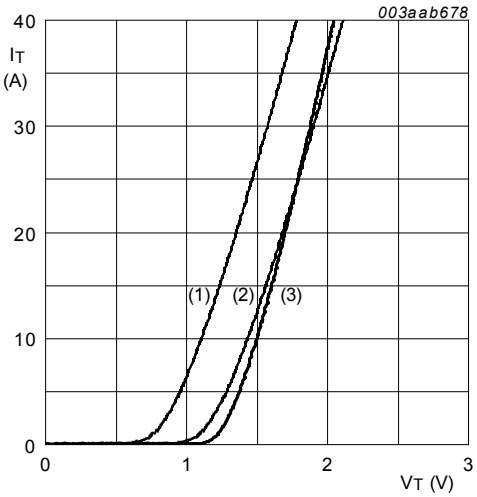

(1) LD+ G-
(2) LD- G-

**Fig. 8. Normalized latching current as a function of junction temperature**



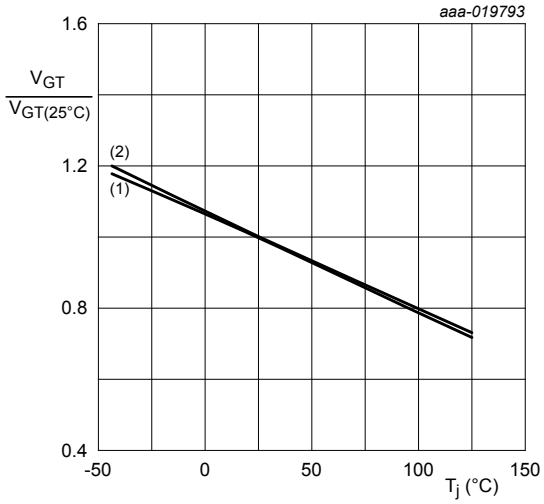

(1) LD+ G-
(2) LD- G-

**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.164 V; $R_s$ = 0.027 Ω
(1) $T_j$ = 125 °C; typical values
(2) $T_j$ = 125 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**




(1) LD+ G-

(2) LD- G-

**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**

# 11. Application information

TOPTriac is a three terminal device that will plug into existing triac circuits. There are some unique features that must be understood to gain its full benefits.

## 11.1 The Gate terminal is also a Feedback terminal

TOPTriac can be triggered like any normal triac. In this conventional mode, the Gate acts as an input. However, the Gate can also be an output, since it provides voltage signatures that indicate the status of TopTriac. The controlling microcontroller can analyse the feedback and act upon it, according to the needs of the application.

## 11.2 Normal triggering

TOPTriac is triggered with negative gate current and may be triggered from 5 V logic or higher voltage supply with suitable series gate resistor. $V_{GT}$ is higher than for standard triacs, so series gate resistors will be a little lower. For 35 mA $I_{GT}$ and 5 V trigger voltage, the current-limiting resistance will typically be 82 Ω instead of 100 Ω for standard triacs.

DC gate triggering is the simplest method that automatically achieves safe latch-off after the over-temperature trip protection has been activated.

Alternatively, pulse triggering may be applied to the gate in combination with a low level bleed current ($I_{G(bl)}$), to sustain the trip condition after the over-temperature trip protection has been activated.

## 11.3 Over-temperature protection

If an overload current or insufficient cooling causes the junction temperature to rise above $T_{trip}$, TOPTriac will disable its gate drive to prevent further conduction before it loses control or becomes damaged. When the over-temperature trip is activated, the Gate-to-Common voltage $V_{G\text{-}CM}$ reduces from the $V_{GT}$ to the $V_{G(trip)}$ level (please refer to the $V_{GT}$ and $V_{G(trip)}$ characteristics).

**Continuous DC gate drive** sustains continued safe latch-off even after TOPTriac temperature has dropped below $T_{trip}$. This allows a controlled reset by removing and reapplying gate drive after the fault condition has been removed.

**Pulsed gate drive**, which may be preferred for phase control or for efficiency reasons, is combined with a low level bleed current $I_{G(bl)}$ to sustain latch-off when the over-temperature trip is activated. (Please refer to the $I_{G(bl)}$ limiting values for the minimum and maximum allowable bleed current that may be applied during pulse triggering).

## 11.4 Resetting after over-temperature

As long as continuous gate current is applied after over-temperature trip, TOPTriac will remain deactivated even after the TOPTriac temperature has dropped below $T_{trip}$. This is the safest protection method that allows the removal of the fault condition before controlled reset is implemented.

The simplest reset is user-controlled, where TOPTriac will remain in the safe shutdown condition until gate drive or power is removed and reapplied.

Automatic reset will not require user intervention, but it may be ‘unintelligent/dumb’ open loop that does not involve a feedback stimulus, or ‘intelligent/smart’ closed loop that does respond to gate feedback.

**User-controlled reset**. The user removes and reapplies power to the application or presses a ‘reset’ button that momentarily removes the gate drive.

**Open loop automatic reset**. If there is a known or predictable overload conditon in the application that may cause an occasional overheat, a periodic discontinuity may be programmed into the gate drive (e.g. at the end of the program stage, once per hour, day or week, depending on the application) that allows automatic reset. For DC gate drive, removal of the gate drive achieves reset. For pulsed gate drive, $I_{G(bl)}$ must be removed and reapplied.

The previous two examples will work for applications that do not require immediate reaction to a fault conditon, hence gate feedback monitoring is not needed.

**Closed loop automatic reset**. Applications where an immediate reaction to an over-temperature trip is needed will require monitoring of TOPTriac status. This is possible by monitoring $V_{G\text{-}CM}$ while gate drive is being applied. During normal conduction, the higher level $V_{GT}$ will be apparent with a square wave at mains frequency superimposed upon it. (The square wave on the gate results from the load current.) During the over-temperature trip condition, the lower level $V_{G(trip)}$ will be apparent and there will be no AC ripple because no load current is flowing. The difference can be detected by the microcontroller, which can take the appropriate action that has been programmed according to the needs of the application.

The following four figures show oscilloscope current and voltage waveforms for the four principal operating modes of TOPTriac: DC triggering, normal conduction and over-temperature tripped; pulse triggering, normal conduction and over-temperature tripped. The pulse triggering waveforms show phase control at the peak of the mains sine wave at half power setting.

Channel 1 shows gate current (20mA/div).

Channel 2 shows load current (5A/div).

Channel 3 shows gate voltage $V_{G\text{-}CM}$ (1V/div).

Channel 4 shows load voltage $V_{LD\text{-}CM}$ (200V/div).

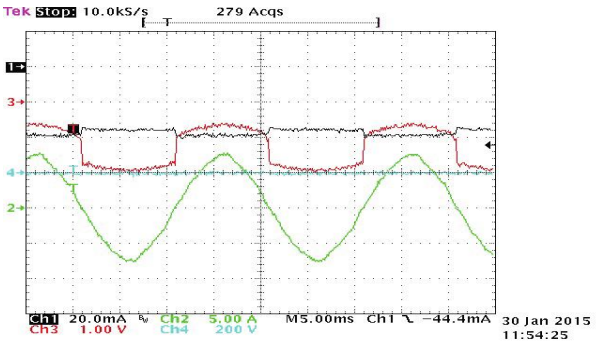



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**Fig. 12. DC triggering, normal conduction**

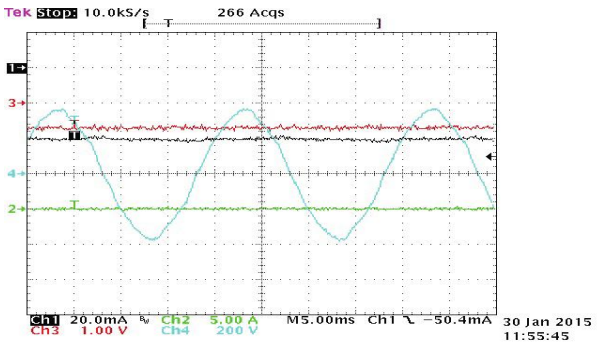


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**Fig. 13. DC triggering, over-temperature tripped**

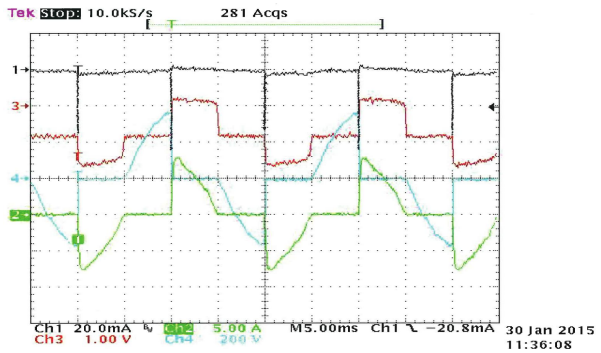


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**Fig. 14. Pulse triggering, normal conduction**

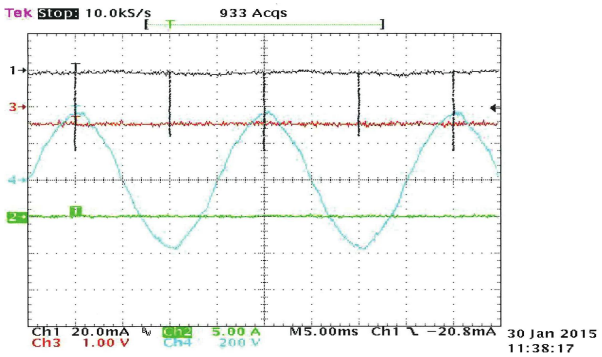


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**Fig. 15. Pulse triggering, over-temperature tripped**

## 11.5 Important characteristics

**$T_{trip}$** is the junction temperature at which TOPTriac will disable itself. It will be above 125 °C and below 150 °C .

**$V_{GT}$** is the gate voltage characteristic during normal triggering. It is higher than for normal triacs. $V_{GT}$ is used in the calculation of $R_G$ to set the gate trigger current.

**$V_{G(trip)}$** is the gate voltage characteristic when in the over-temperature trip condition. It is lower than $V_{GT}$. $V_{G(trip)}$ is used in the calculation of $R_{G(bl)}$ to set the gate bleed current $I_{G(bl)}$.

**$I_{G(bl)}$** is used during pulse triggering. It is the continuous DC bleed current that must flow out of the gate to achieve clean latch-off at the trip point and maintain this safe latch-off condition as TOPTriac cools down to ambient temperature.

The min $I_{G(bl)}$ value is the minimum bleed current to sustain latch-off after cooling.

The max $I_{G(bl)}$ value is the maximum bleed current that will not trigger TOPTriac up to maximum trip temperature.

## 11.6 How to calculate the bleed resistor $R_{G(bl)}$

When pulse triggering it is critical that the bleed current is set correctly.

If $I_{G(bl)}$ is too low (lower than 0.5 mA), TOPTriac may not be able to provide reliable over-temperature protection during continuous fault conditions. Normal trip may be achieved at $T_{trip}$, but self-reset may occur as it cools, leading to on-off cycling. This constitutes a loss of control and should be avoided.

If $I_{G(bl)}$ is too high (higher than 2 mA), TOPTriac may trigger uncontrollably at elevated temperature that is below the trip temperature (This is another form of loss of control that must not be allowed). However, it will still self-protect as intended above trip temperature.

The following examples show how to calculate the minimum and maximum $R_{G(bl)}$. The chosen value should be approximately mid-way between the two extremes.

**Example 1 (3.3 V logic supply)**

Maximum $I_{G(bl)}$ is 2 mA. During normal conduction when $I_{G(bl)}$ must not be high enough to cause false triggering, $V_{GT}$ applies and should be used in our calculations. Minimum $V_{GT}$ @ $T_{j(max)}$ is 0.5 V.

Therefore minimum RG(bl):

$R_{G(bl)}$ = (3.3 - 0.5) / 2 mA = 1.4 kOhm

Minimum $I_{G(bl)}$ is 0.5 mA. When tripped, $V_{G(trip)}$ applies and should be used in our calculations. $I_{G(bl)}$ must remain high enough to maintain the trip condition, even when $V_{G(trip)}$ is at a maximum. Maximum $V_{G(trip)}$ is 0.9 V.

Therefore maximum $R_{G(bl)}$:

$R_{G(bl)}$ = (3.3 - 0.9) / 0.5 mA = 4.8 kOhm

Suggested $R_{G(bl)}$ is 3 kΩ.

**Example 2 (5 V logic supply)**

Min $R_{G(bl)}$:

$R_{G(bl)}$ = (5 - 0.5) / 2 mA = 2.25 kOhm

Max $R_{G(bl)}$:

$R_{G(bl)}$ = (5 - 0.9) / 0.5 mA = 8.2 kOhm

Suggested $R_{G(bl)}$ is 5.1 kΩ.

**Example 3 (12 V auxiliary gate drive supply)**

Min $R_{G(bl)}$:

$R_{G(bl)}$ = (12 - 0.5) / 2 mA = 5.75 kOhm

Max $R_{G(bl)}$:

$R_{G(bl)}$ = (12 - 0.9) / 0.5 mA = 22.2 kOhm

Suggested $R_{G(bl)}$ is 15 kΩ.

## 11.7 Application schematics

The following schematics show possible implementations of TOPTriac. Gate trigger current is from a 5 V minimum logic supply. It is possible to trigger from a 3.3 V microcontroller by using a transistor level shifter to a higher voltage gate drive power supply, which may be 5 V minimum or the 12 V supply that may already be available for other loads such as lighting, indication and sounders.

For **DC triggering**, reset is achieved by removing the gate drive at any time and reapplying it after TOPTriac temperature has dropped below $T_{trip}$.

For **pulse triggering**, reset is achieved by removing and reapplying the gate bleed current $I_{G(bl)}$ after TOPTriac temperature has dropped below $T_{trip}$.

$I_{G(bl)}$ is set by $R_{G(bl)}$. It is best derived directly from the low voltage microcontroller supply (up to 5V max) and will most likely be direct drive from the microcontroller output.

In all of the following circuits, gate trigger and gate bleed current are applied by logic zero drive from the microcontroller.

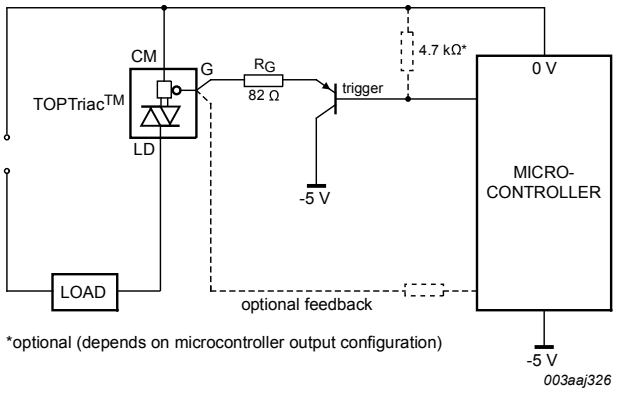



**Fig. 16. DC triggering from 5 V microcontroller**

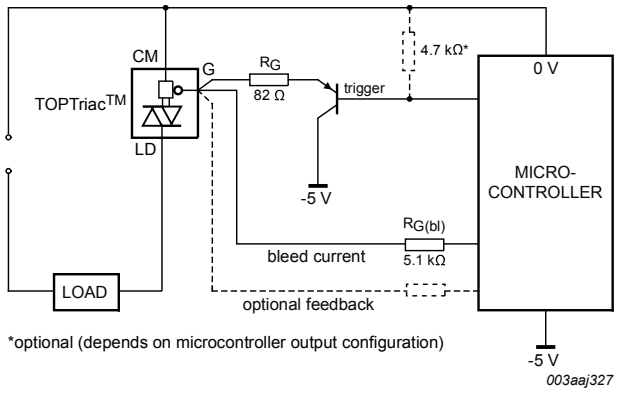



**Fig. 17. Pulse triggering from 5 V microcontroller**

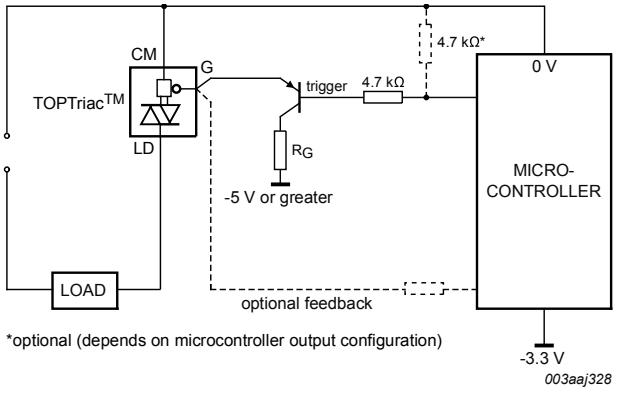



**Fig. 18. DC triggering from 3.3 V microcontroller**

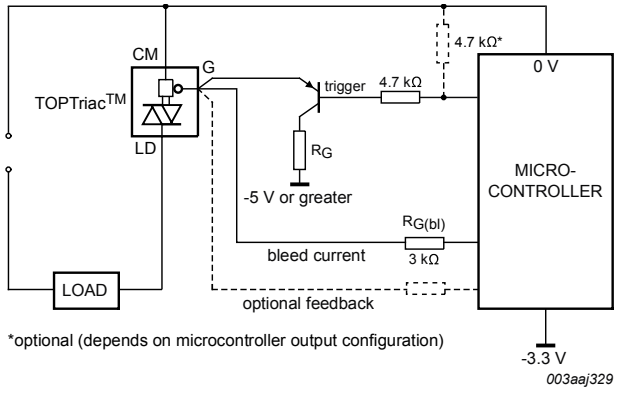
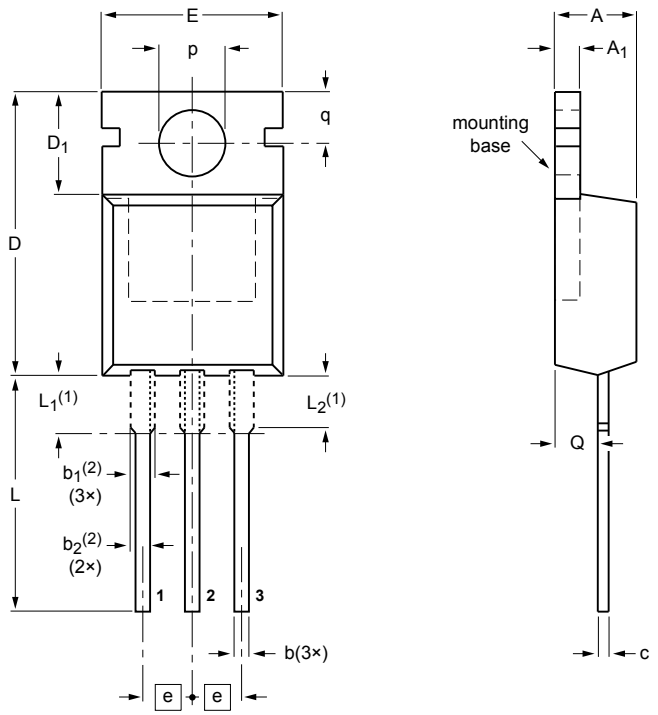



**Fig. 19. Pulse triggering from 3.3 V microcontroller**

# 12. Package outline

**Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB** **SOT78**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | $b_1$(2) | $b_2$(2) | c | D | $D_1$ | E | e | L | $L_1$(1) | $L_2$(1) max. | p | q | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7<br>4.1 | 1.40<br>1.25 | 0.9<br>0.6 | 1.6<br>1.0 | 1.3<br>1.0 | 0.7<br>0.4 | 16.0<br>15.2 | 6.6<br>5.9 | 10.3<br>9.7 | 2.54 | 15.0<br>12.8 | 3.30<br>2.79 | 3.0 | 3.8<br>3.5 | 3.0<br>2.7 | 2.6<br>2.2 |

**Notes**

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT78 | | 3-lead TO-220AB | SC-46 | | | ~~08-04-23~~<br>08-06-13 |

**Fig. 20. Package outline TO-220AB (SOT78)**

# 13. Legal information

## 13.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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[2] The term 'short data sheet' is explained in section "Definitions".
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