N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package		
				TO-39	TO-92	DICE
200V	10Ω	300mA	1.5V	TN0520N2	TN0520N3	TN0520ND
240V	10Ω	300mA	1.5V	TN0524N2	TN0524N3	TN0524ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Very low threshold voltage

Advanced DMOS Technology

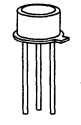
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Telecommunications: Outpulsing switch
  Muting switch
- ☐ Battery operated systems
- ☐ Solid state relays

Package Options (Notes 1 and 2)



TO-39

TO-92

Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-39	0.7A	1.5A	3.5W	35	125	0.7A	1.5A
TO-92	0.3A	1.0A	1.0W	125	170	0.3A	1.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

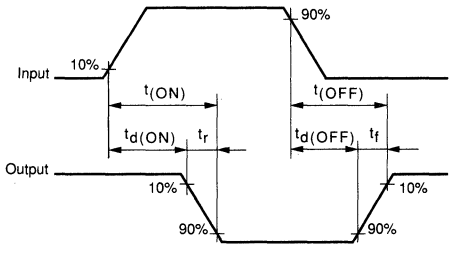
(Notes 1 and 2)

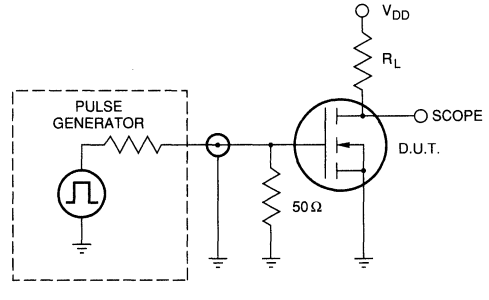
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0524	240			V	V_{GS}= 0, I_D =1mA
		TN0520	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.5	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.0	-4.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					500		V_{DS} = 0, V_{GS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		100	390		mA	V_{GS} = 3V, V_{DS} = 25V
			300	800			V_{GS} = 5V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			9	15	Ω	V_{GS} = 3V, I_D = 50mA
				7	10		V_{GS} = 5V, I_D = 100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.9	1.5	%/°C	V_{GS} = 5V, I_D = 0.2A
G_{FS}	Forward Transconductance		0.15	0.3		℧	V_{DS} = 25V, I_D = 0.2A
C_{ISS}	Input Capacitance			45	60	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			15	35		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	V_{DD} = 25V I_D = 0.2A R_S = 50Ω
t_r	Rise Time			3	5		
$t_{d(OFF)}$	Turn-OFF Delay Time			5	7		
t_f	Fall Time			3	5		
V_{SD}	Diode Forward Voltage Drop			1.1	2.5	V	V_{GS} = 0, I_{SD} = 100mA
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 100mA

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

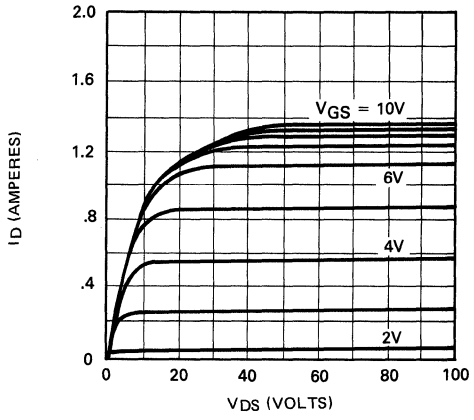
Switching Waveforms and Test Circuit



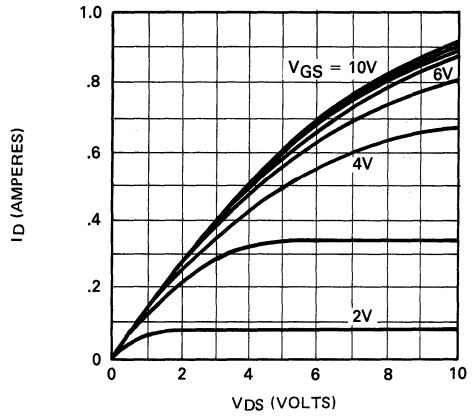


Typical Performance Curves

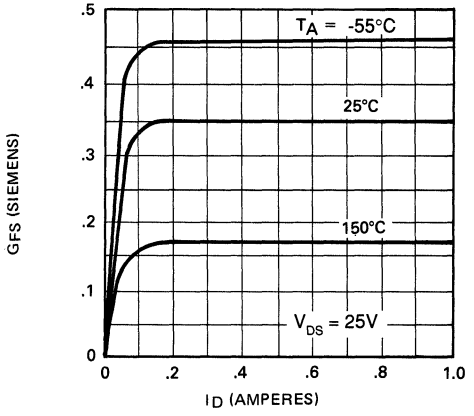
Output Characteristics



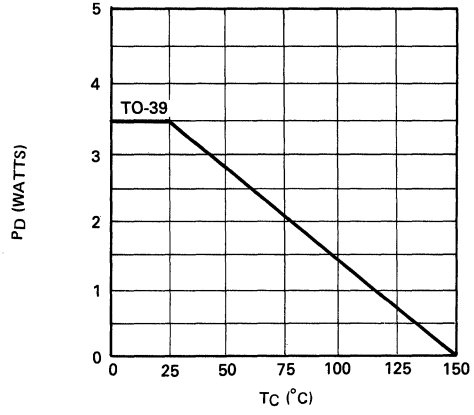
Saturation Characteristics



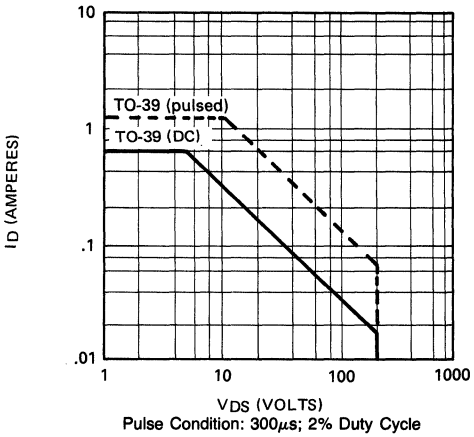
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

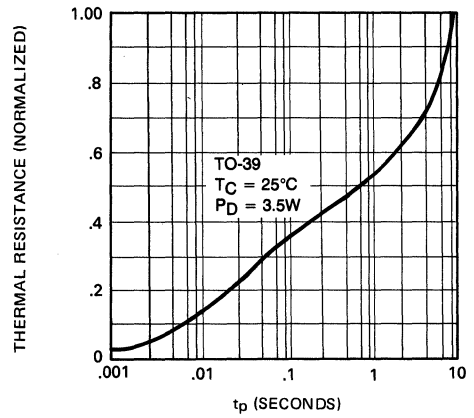


Maximum Rated Safe Operating Area



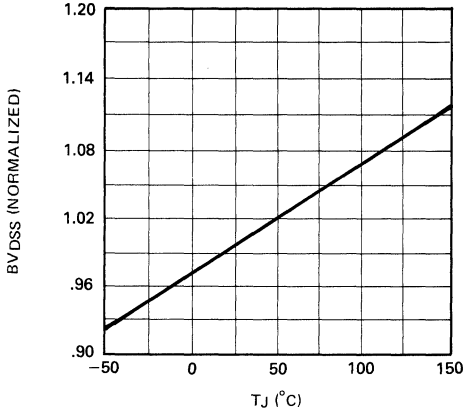
Pulse Condition: 300μs; 2% Duty Cycle

Thermal Response Characteristics

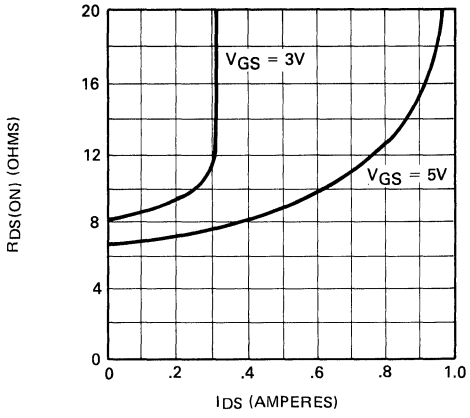


Typical Performance Curves

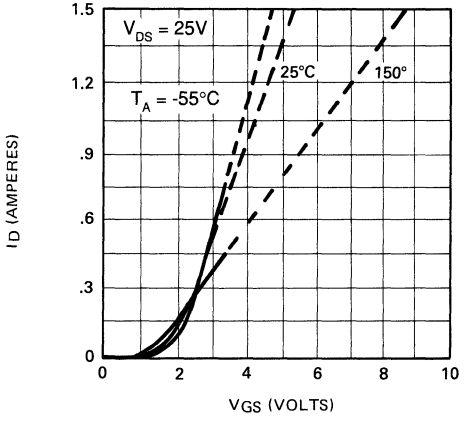
BVDSS Variation with Temperature



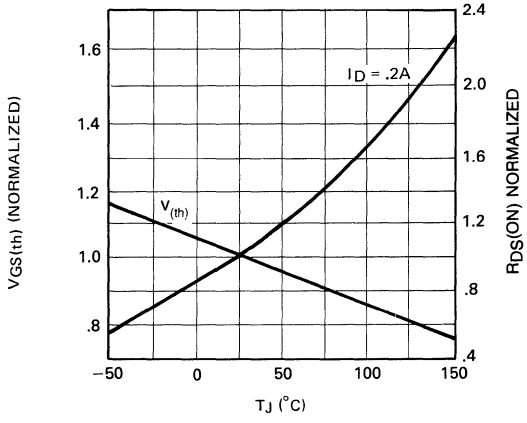
On-Resistance Vs. Drain Current



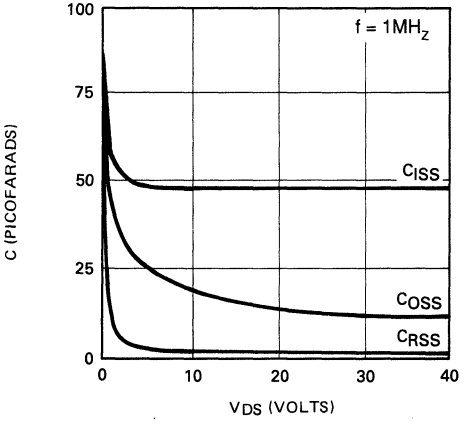
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics