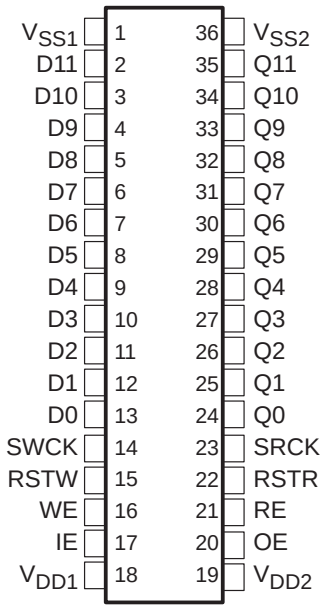
- **2949120 Bits of Memory**
- **Organization: 245760 Words × 12 Bits**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **Upwardly and Pin-to-Pin Compatible With TMS4C2970 and TMS4C2971**
- **2-Port Memory With FIFO Operation**
  - **Full-Word Continuous Read/Write**
  - **Asynchronous Read/Write**
- **Optional Random-Block Access Function (40 Words per Block) Enabled During Reset Operation, Two Modes for Write Access: D0- or IE-Controlled**
- **Fully Static (Refresh-Free and Infinite Length of Clocking Pauses)**
- **Write-Mask Function by Input Enable (IE)**
- **Cascade Connection Capability**
- **High-Speed Read/Write Operation**

	ACCESS TIME (MAX)	CYCLE TIME READ (MIN)	CYCLE TIME WRITE (MIN)
TMS4C2972-24	19 ns	24 ns	24 ns
TMS4C2972-26	21 ns	26 ns	26 ns
TMS4C2972-28	23 ns	28 ns	28 ns

- **16M-Bit CMOS DRAM Process Technology**
- **High-Reliability Plastic 36-Lead Surface-Mount Shrink Small-Outline Package (SSOP) (DT Suffix)**

DT PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
IE	Input Enable
WE	Write Enable
SWCK	Serial-Write Clock
RSTW	Reset Write
D0–D11	Data Inputs
OE	Output Enable
RE	Read Enable
SRCK	Serial-Read Clock
RSTR	Reset Read
Q0–Q11	Data Outputs
V_{DD1} – V_{DD2}	Power
V_{SS1} –V_{SS2}	Ground

description

The TMS4C2972 is a field memory (FMEM) that is upwardly and pin-to-pin compatible with the TMS4C2970 and TMS4C2971, except for the consequences of the block size change (40 instead of 80 words per block) on old data access mode enabling (see the section titled ‘‘old-/new-data access”).

The device is a two-port memory; data is written in through a 12-bit-wide write port and is read out through a 12-bit-wide read port. Both ports may be operated simultaneously and/or asynchronously. Dynamic storage cells are employed for main data memory to achieve high storage density, but the TMS4C2972 refreshes its cells automatically so that device operation appears fully static to the user. All internal pointers and registers are fully static so that read and write operations can be interrupted for indefinite periods of time without loss of data.

description (continued)

Maximum storage capacity is 245 760 words by 12 bits. Addressing is governed by write-address and read-address pointers, which can be easily controlled by the user. The TMS4C2972 can be addressed in a strictly sequential or FIFO manner, but it also offers an optional random-block access mode, which allows the user to direct either pointer to the beginning of any of the 6144 blocks that comprise the address space of the memory.

In sequential addressing mode, the TMS4C2972 functions like a FIFO register. The timing between write-reset and read-reset operations determines the delay or length of the FIFO. Data may be read out as many times as desired after it has been written into the storage array of the memory. Minimum delay between writing and reading is 160 write cycles; maximum delay is one full field plus one block or 245 800 words.

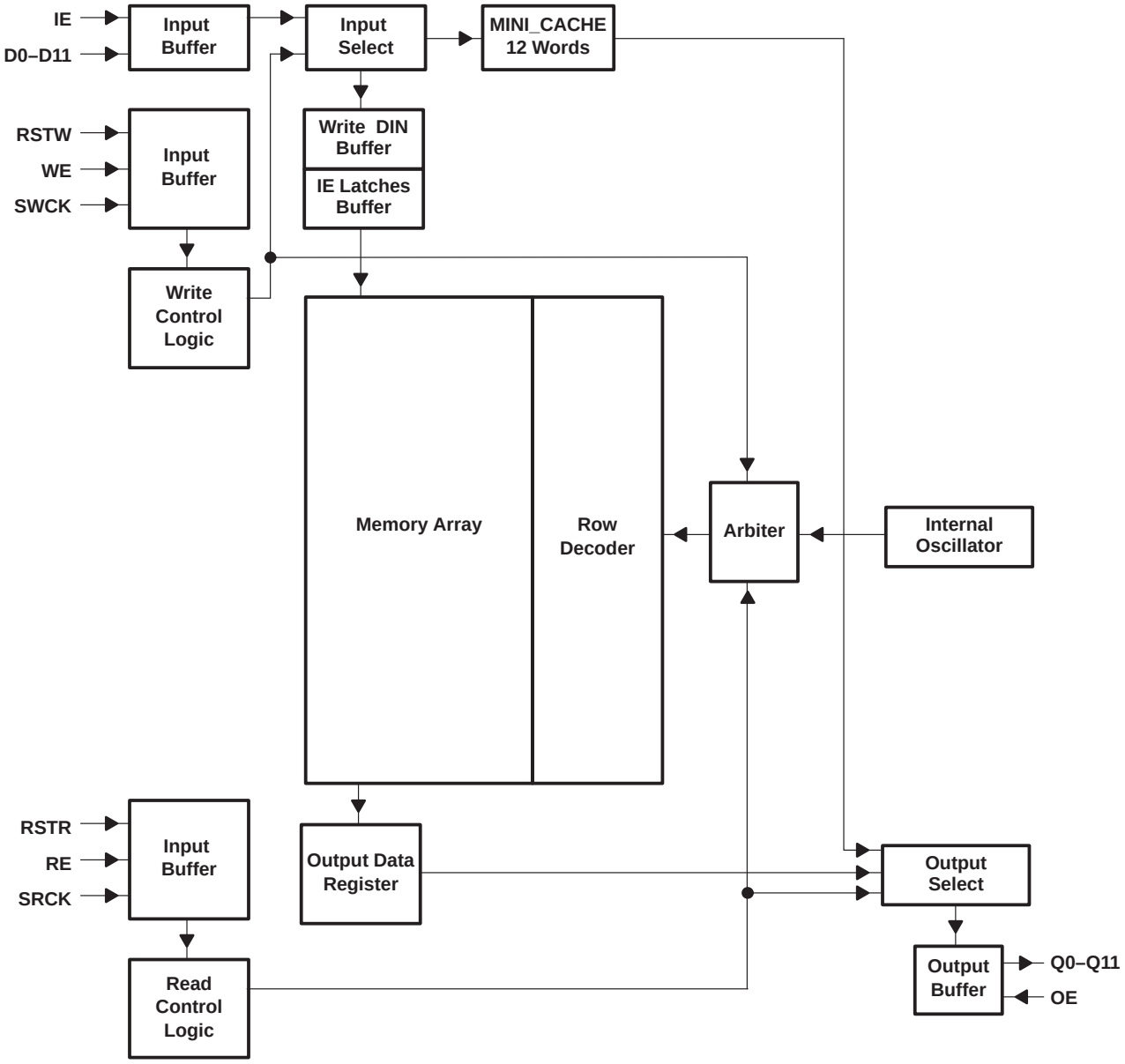
If the memory is used as a delay element only, there is no need to reset the read and write address pointers, because they wrap around after passing their maximum value. For details, see the section on wrap-around of pointers.

The TMS4C2972 employs state-of-the-art 16M-bit complementary metal-oxide semiconductor (CMOS) dynamic random-access memory (DRAM) technology for high performance, reliability, and low-power dissipation. The device is rated for operation in the 0°C to 70°C range and is available in a high-reliability 36-lead surface-mount shrink small-outline package (SSOP) (DT suffix).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
V_{SS1}	1	Ground
D11	2	Data Input
D10	3	Data Input
D09	4	Data Input
D08	5	Data Input
D07	6	Data Input
D06	7	Data Input
D05	8	Data Input
D04	9	Data Input
D03	10	Data Input
D02	11	Data Input
D01	12	Data Input
D0	13	Data Input
SWCK	14	Serial Write Clock
RSTW	15	Reset Write
WE	16	Write Enable
IE	17	Input Enable
V_{DD1}	18	+5-V Power
V_{DD2}	19	+5-V Power
OE	20	Output Enable
RE	21	Read Enable
RSTR	22	Reset Read
SRCK	23	Serial Read Clock
Q0	24	Data Output
Q1	25	Data Output
Q3	26	Data Output
Q4	27	Data Output
Q5	28	Data Output
Q6	29	Data Output
Q7	30	Data Output
Q8	31	Data Output
Q9	32	Data Output
Q10	33	Data Output
Q11	34	Data Output
Q12	35	Data Output
V_{SS2}	36	Ground

functional block diagram



operation

The TMS4C2972 device writes and reads through two separate 12-bit-wide data ports. Addressing is controlled by the write- and read-address pointers. Maximum storage capacity is 245760 words by 12 bits for a total of 2949120 bits. Before controlled data-write or data-read operations can begin, the write and read pointers must be set to 0 or set to the beginning of a valid address block as shown in Figure 1 and Figure 2.

operation (continued)

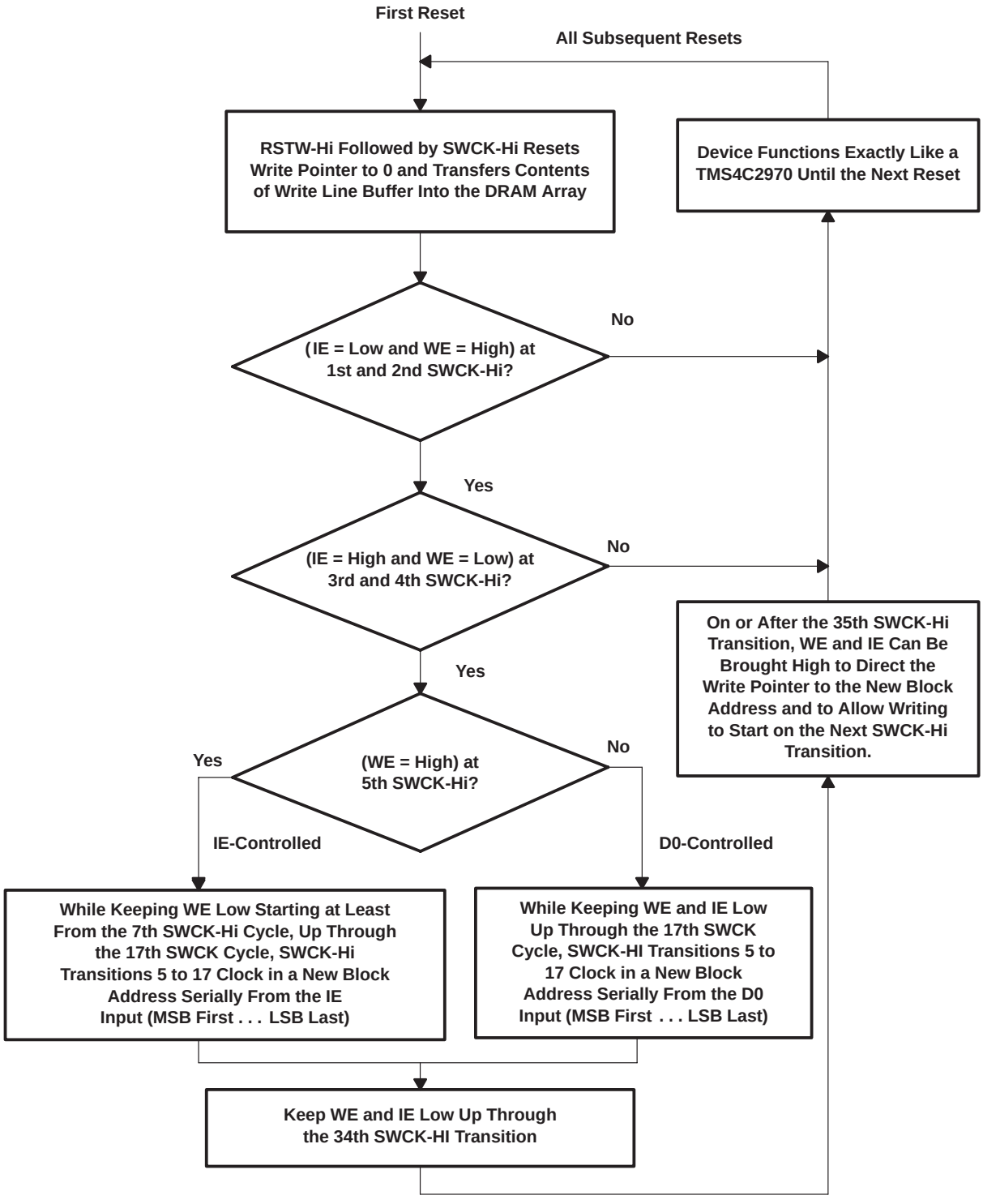


Figure 1. Write Flow Chart

operation (continued)

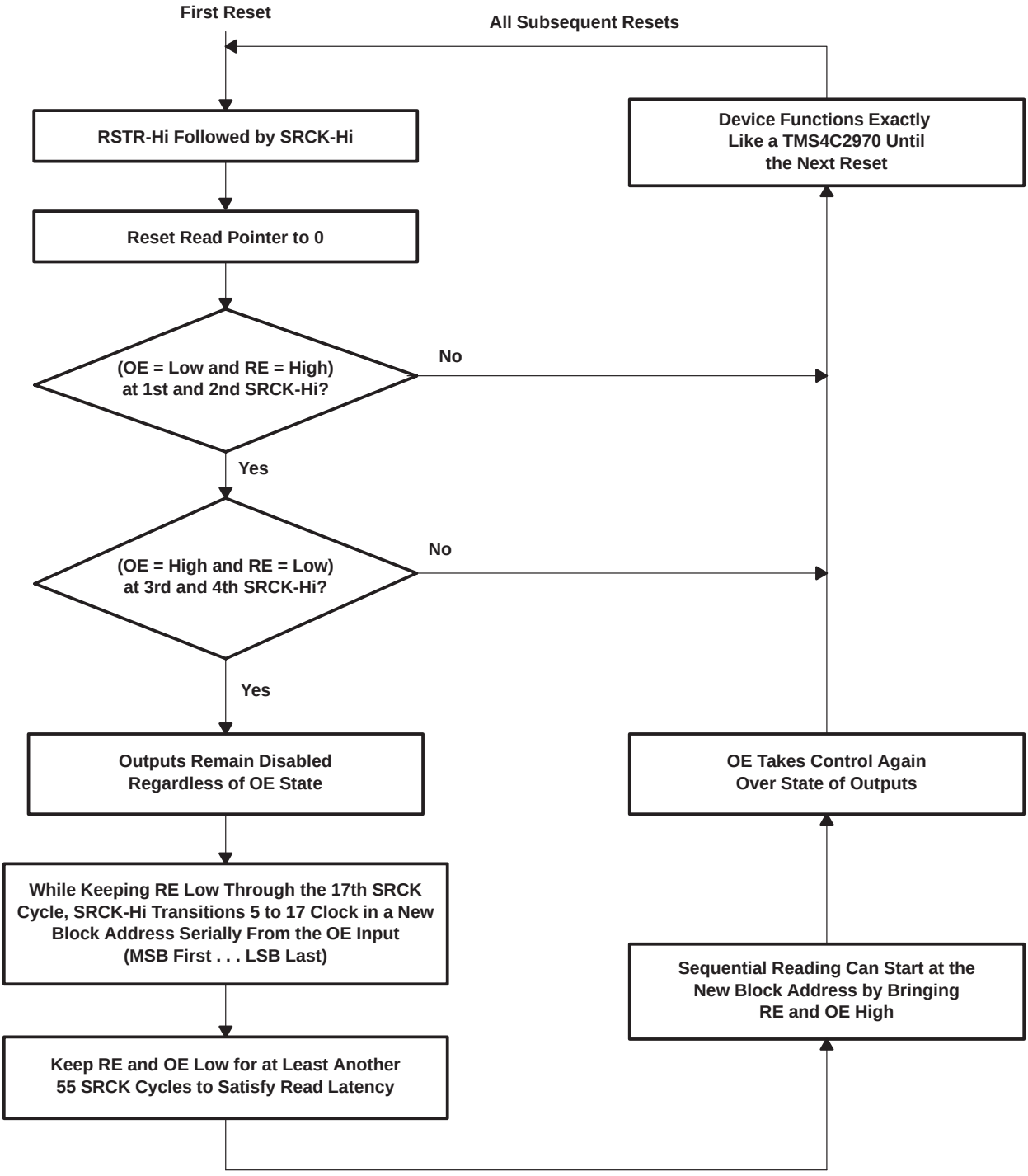


Figure 2. Read Flow Chart

write operation

Write operation is controlled by four signals: SWCK, RSTW, WE, and IE. Writing is accomplished by cycling SWCK and holding WE and IE high. Memory addressing is controlled by the write address pointer, which is usually reset to zero using the RSTW input, before a new video field is written in.

In most applications, addressing occurs sequentially, as in a FIFO memory. However, the write address pointer can be set to the beginning of each of the 6144 blocks of the memory by a special control sequence which must be initiated by RSTW. To minimize memory storage space, writing can be limited to the active portion of each video field by using the gating function of the WE input.

When data is written into the memory, it is first stored in temporary buffers before being transferred into the memory core in 40-word blocks. If further writing is disabled, using WE, after the end of a video field, between zero and 39 words may still remain stored in the temporary buffers, and cannot be read out using read operations of the memory. The user can transfer these last data words into the memory core by executing an RSTW operation. This RSTW operation then also resets the write address pointer to zero again, in preparation for writing in the next video field.

Each RSTW cycle must contain at least 56 active write cycles, that is, two successive positive RSTW transitions must be separated by at least 56 SWCK cycles while WE is high.

reset write (RSTW)

The first positive SWCK transition, after RSTW has gone high, resets the write address pointers to zero, provided WE is high. If WE is low, the pointers are reset to zero by the first positive SWCK transition after WE has gone high. Then, for both cases, data writing into address 0 occurs one positive SWCK transition later, as specified in the section “data inputs and write clock”. RSTW setup and hold times are referenced to the rising edge of SWCK. Before RSTW may be brought high again for a further reset operation, it must have been low for at least two active SWCK cycles (that is, cycles during which WE is high).

On the first four positive SWCK transitions, the memory operates exactly like a TMS4C2970, regarding its response to the control signals IE and WE. In addition, the data states of IE and WE are checked to determine whether the write pointer is to be set to the beginning of any one of its 6144 blocks or if the pointer is to be set to 0 (see Figure 1). In order to set the write pointer to an address other than 0, the following four conditions all have to be met:

1.	On first positive SWCK transition:	IE must be low	and	WE must be high.
2.	On second positive SWCK transition:	IE must be low	and	WE must be high.
3.	On third positive SWCK transition:	IE must be high	and	WE must be low.
4.	On fourth positive SWCK transition:	IE must be high	and	WE must be low.

If any one of these conditions is not met, the memory operates exactly like a TMS4C2970 until the next positive RSTW transition. After all four conditions have been met, the write pointer can be set to a new block address. This can be accomplished by two methods, according to the WE status on the fifth positive SWCK transition:

- If WE is low, the new block address is defined by clocking in the data states of the D0 pin during the next 13 positive SWCK transitions.
- If WE is high, the new address is defined by clocking in the data states of the IE pin during the next 13 positive SWCK transitions.

The most significant bit (MSB) of this address is clocked in on the fifth transition. The least significant bit (LSB) is clocked in on the 17th transition. Only block values between 0 and 6143 are recognized. Any value greater than 6143 results in an improper device operation or lockup. Recovery from this type of lockup requires a TMS4C2970-like reset operation to be performed.

reset write (RSTW) (continued)

To clock in a new block address, in case D0 is used, WE and IE must be kept low while this random block address is clocked in and for at least another 17 SWCK cycles (up through the 34th positive SWCK transition). Otherwise, if IE is used, WE only must be brought low starting from the 7th up through the 34th SWCK cycle. On the 35th SWCK cycle, WE and IE may be brought high again. Therefore, earliest possible writing may begin on the 36th SWCK cycle and proceed sequentially according to the states of control signals WE, IE, and SWCK, as described in detail in the following sections of the data sheet.

During the previously described sequence, only one positive RSTW transition is allowed. After RSTW has been kept high during the first positive SWCK transition, it can be maintained high or brought low as desired. But, once RSTW has gone low, it cannot be brought high again until the end of the entire 36 SWCK cycles sequence. Bringing RSTW high any earlier may cause improper operation of the device.

For regular device operations, RSTW cannot stay high for more than 1023 SWCK clock cycles while WE is high; if it does, the device enters a built-in test mode. After RSTW is brought low, it must remain low for at least two SWCK cycles before another reset write operation can take place.

wrap-around of pointers

It is not necessary to reset the read and write address pointers in case the memory is used as a delay element only. For this case (that is, if one or both of the pointers are allowed to increment past their maximum values of 245 771), the following device behavior must be taken into account:

After reaching the value of 245 771, the pointers will wrap around again to value 12. Pointer incrementing will then be as follows:

0 .... 11 $\rightarrow$ 12 ..... 245771 $\rightarrow$

$\rightarrow$ 12 ..... 245771 $\rightarrow$

$\rightarrow$ 12 ..... 245771 $\rightarrow$

While it is possible to reset one pointer only and let the other pointer wrap around, this is not recommended because the user would then have to keep track of the location of both write and read information. Such address tracking is difficult; therefore, it is recommended to either reset both pointers or to let both pointers wrap around.

If the user wishes to terminate wrap-around operation and change over to reset operation again, it is recommended to proceed as if the entire memory were filled with invalid data, and to write in new data before attempting the first read-out.

block address

When the block “0000” is addressed by random-block access mode, the pointer is forced to the value 12, that is, to the same value the pointer assumes after a wrap-around (see previous section). Consequently, the correspondence between block addresses and pointer values, is as follows:

Block address (hex)	Pointer value (decimal)
0000	12
0001	52
0002	92
....	....
....	....
17FF	245732

After a FIFO-mode reset-write operation (that is, reset the pointer to address 0), the first 52 words are written into an internal SRAM cache. On the other hand, if the pointer is set to 12 or block address 0000, the first 40 words are written into the DRAM core. Read access functions in the same manner.

block address (continued)

This means that the contents of block 0000 (that is, pointer values from 12 to 51) will be read out correctly only if read-access mode is the same as write-access mode. If writing occurs in FIFO mode and reading in random-access mode, or vice versa, block 0000 will not be read correctly.

If a mixing of modes is required between read and write, the recommendation is to write dummy information into the first 52 words, in order to avoid incorrect reading.

data inputs (D0–D11) and serial-write clock (SWCK)

Each rising edge of the SWCK latches the data present on inputs D0–D11 onto the chip, providing WE was high at the previous rising edge of SWCK. Data setup and hold times ($t_{su(D)}$, $t_{h(D)}$) are referenced to the rising edge of SWCK. Whether or not the data latched will be written into the memory depends on the state of the IE signal at the previous rising edge of SWCK.

write enable (WE)

WE is used to enable or disable incrementing of the internal write address pointer. When the WE input is at logic high, rising edges of the SWCK will increment the pointer. When the WE input is at logic low, the pointer will not be incremented. WE setup and hold times are referenced to the rising edge of SWCK.

As described in the previous section, WE also controls the latching of data on D0–D11 onto the chip.

input enable (IE)

IE is used to enable writing data from inputs D0–D11 into the memory, or to disable writing, thereby preserving the previous content of the memory. Each rising edge of the write clock SWCK samples the logic state of IE. Setup and hold times for IE are referenced to this rising edge.

When a logic-high level on IE is sampled by an SWCK rising edge, writing data into the memory at the following SWCK rising edge will be enabled. When a logic-low level on IE is sampled by an SWCK rising edge, writing into the memory at the following SWCK rising edge will be disabled.

Table 1. Write-Cycle State Table

SWCK RISING EDGE			
WE	IE	Write-address pointer	D0–D11
High	High	Address-pointer increment	Store data
High	Low		Not store
Low	Don't Care	Address-pointer stop	Not store

Table 1 does not apply at each rising edge of SWCK after WE has gone high. At those times, the actual state of IE is ignored, and instead, the memory behaves according to the state of IE at the first rising edge of SWCK after WE had gone low previously.

read operation

The read operation is controlled by four signals: SRCK, RSTR, RE, and OE. It is accomplished by cycling SRCK and holding RE and OE high after a read address pointer reset operation (RSTR). Each read operation, which begins with RSTR, must contain at least 56 active read cycles; that is, SRCK cycles while RE is high.

reset read (RSTR)

The first positive SRCK transition, after RSTR has gone high, resets the read address pointers to zero, provided RE is high. If RE is low, the pointers are reset to zero by the first positive SRCK transition after RE has gone high. RSTR setup and hold times are referenced to the rising edge of SRCK.

reset read (RSTR) (continued)

On the first four positive SRCK transitions after RSTR has gone high, the data states of OE and RE are checked to determine whether the read pointer is to be set to the beginning of any one of its 6144 blocks or if the pointer is to be set to 0 (see Figure 2). To set the read pointer to an address other than 0, the following four conditions all have to be met:

1.	On first positive SRCK transition:	OE must be low	and	RE must be high.
2.	On second positive SRCK transition:	OE must be low	and	RE must be high.
3.	On third positive SRCK transition:	OE must be high	and	RE must be low.
4.	On fourth positive SRCK transition:	OE must be high	and	RE must be low.

If any one of these conditions is not met, the memory operates exactly like a TMS4C2970 until the next positive RSTR transition.

On the first and second positive SRCK transitions, the memory operates exactly like a TMS4C2970, regarding its response to the control signals OE and RE. Once all the above conditions are met, the outputs will remain disabled regardless of the state of OE.

If all four check conditions above have been met, OE no longer controls the state of the outputs and it can be used to set the read pointer to a new block address. This is done by clocking in the data states of the OE pin during the next 13 positive SRCK transitions. The MSB of this address is clocked in on the 5th positive SRCK transition, the LSB on the 17th transition. Only block values between 0 and 6143 are recognized. The user must avoid clocking in a value above 6143 because this may result in improper device operation or lock-up. Recovery from this lock-up will require a TMS4C2970-like reset operation to be performed.

After a block address has been clocked in, RE and OE must be kept low for at least another 55 SRCK clock cycles to satisfy the read latency requirements of the memory. After that, sequential addressing may start at the beginning of the new block by bringing RE and OE high.

During the entire control sequence to change the read pointer, only one positive RSTR transition is allowed. After RSTR has been kept high during the first positive SRCK transition, it can be maintained high or brought low as desired. But once RSTR has gone low, it cannot be brought high again until the read latency is satisfied. Bringing RSTR high earlier may cause improper operation of the device.

RSTR can be kept high for many cycles, the essential actions detailed above are initiated by the first or the second SRCK cycle, if reset to zero is desired, or during the following 70 SRCK cycles. After RSTR is brought low, it must remain low for at least two active SRCK cycles (that is, while RE is high) , before another reset read operation can take place.

data outputs (Q0 – Q11) and serial-read clock (SRCK)

Data outputs are determined by the state of RE and OE at the rising edge of SRCK. If the outputs change state because the read pointer was advanced, they remain in the previous state for at least the output hold time interval $t_{h(OUT)}$ and assume the new valid state after the access time interval t_{AC}. See the timing diagrams for details.

The three-state output buffer provides direct TTL compatibility and no pull-up resistors are required. Data output has the same polarity as data input.

read enable (RE)

RE is used to enable or disable incrementing the internal read address pointer. When the RE input is at logic high, rising edges of the SRCK will increment the pointer. When the RE input is at logic low, the pointer will not be incremented. RE setup and hold times are referenced to the rising edge of SRCK.

output enable (OE)

OE is used to enable or disable output pins Q0 to Q11. A logic high on the OE input enables the output to Q0–Q11, and a logic low disables the output. The internal read address pointer is incremented by cycling SRCK regardless of OE logic level. The outputs will be clocked into the high-impedance (floating) state if OE is low at the rising edge of SRCK. The disable time ($t_{dis(CK)}$) applies. The outputs will be enabled if OE is high at the rising edge of SRCK. The enable time ($t_{en(CK)}$) applies. Note that OE setup and hold times are referenced to the rising edge of SRCK.

Table 2. Read-Cycle State Table

SRCK RISING EDGE			
RE	OE	Read-address pointer	Q0–Q11
High	High	Address pointer increment	Output data
High	Low		Hi-Z
Low	High	Address pointer stop	Output data
Low	Low		Hi-Z

power up and initialization

When the device is powered up, it is not assured to function properly until at least 100 µs after V_{DD} has stabilized to a value within the range of recommended operating conditions. This time is defined as $t_{POWER-OK}$. To properly initialize the device, the following operations must be performed after $t_{POWER-OK}$:

1. A minimum of 96 dummy read operations (SRCK cycles)
2. An RSTR operation
3. A minimum of 96 dummy write operations (SWCK cycles)
4. An RSTW operation

Dummy-read cycles/RSTR (operations 1 and 2) must be performed in sequence. Dummy-write cycles/RSTW (3 and 4) also must be performed in sequence; however, the dummy-read cycles/RSTR and dummy-write cycles/RSTW (that is, 1 and 2, 3 and 4) can occur simultaneously.

If the dummy-read and dummy-write operations start earlier than $t_{POWER-OK}$, an RSTR operation plus operations 1 and 2 listed above and an RSTW operation plus 3 and 4 must be performed after $t_{POWER-OK}$.

old-/new-data access

There must be a minimum delay of 160 SWCK cycles between writing into memory and reading out from memory. If reading of the first field starts, with an RSTR operation, before the start of writing the second field (that is, before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 39 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 40 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field (= old data) will still be read out.

In order to read out new data (that is, the second field written in), the delay between RSTW operation and RSTR operation must be at least 160 SWCK cycles. If the delay between RSTW and RSTR operations is more than 40 but less than 160 cycles, then the data read out will be undetermined, it may be old data or new data or a combination of old and new data. Such a timing should be avoided.

The above is still valid if write and/or read random-block access mode is used; the 160 SWCK cycles latency must be fulfilled by the user between any RSTW and RSTR related to the same block address.

cascade operation

The TMS4C2972 device allows the cascading of several memory devices to obtain a greater storage depth or a longer delay than that which can be obtained with using only one memory device. See the interconnection diagram for details. See Figure 3.

As the cascade-operation timing waveform indicates (see Figure 13), the beginning of the positive transition of SRCK/SWCK at the beginning of a clock cycle serves to initiate reading out, while writing in is initiated by the end of the rising edge of SWCK/SRCK at the end of a clock cycle.

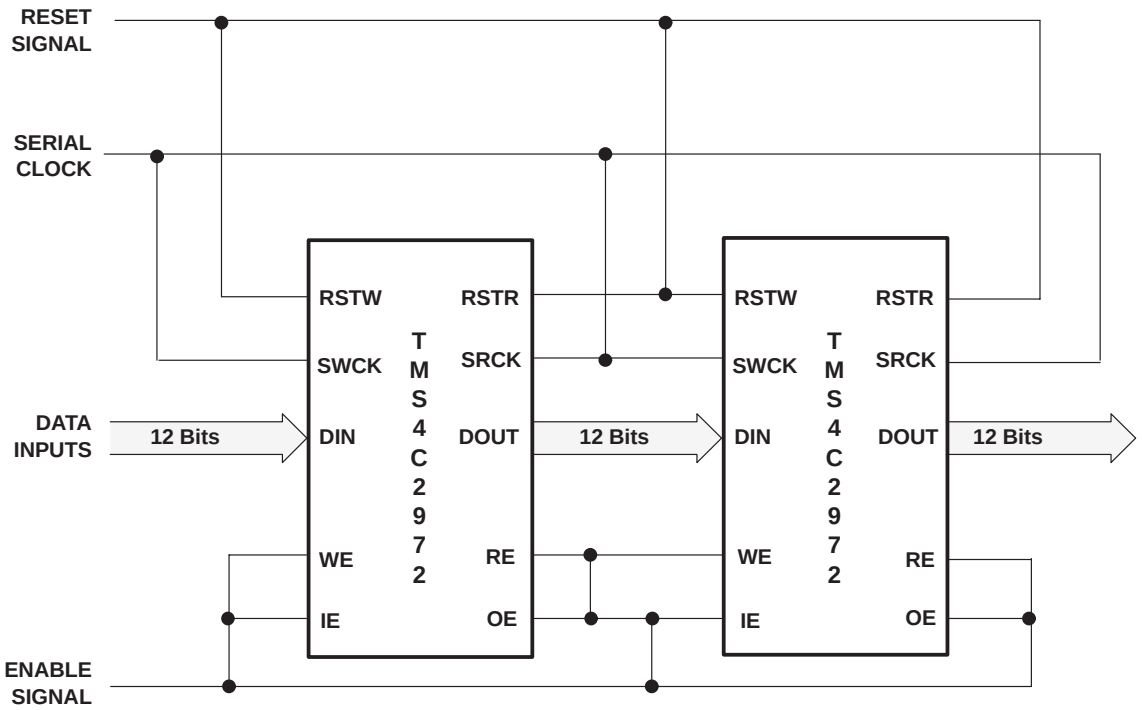


Figure 3. Cascade Operation – Signal Connections

test mode operations

The TMS4C2972 device has a special test mode function that is to be used by the factory only. End users of these devices must not use this function since doing so may cause the device to be stressed in an unpredictable manner. If WE, IE, and RSTW are maintained continuously at logic high at the same time, after 1024 SWCK cycles the device enters into the test mode. The device remains in the test mode as long as the WE clock is maintained at logic high. The TMS4C2972 device exits the test mode two SWCK cycles after the WE clock level is brought low again.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, (see Note 1) . . . . . 0 V to 7.0 V
Voltage range on any input pin, (see Note 1) . . . . . –1.0 V to 7.0 V
Voltage range on any nonInput pin, (see Note 1) . . . . . –1.0 V to 7.0 V
Voltage difference between V_{SS1} and V_{SS2} . . . . . – 0.7 V to 0.7 V
Short-circuit output current, I_{OS} . . . . . 50 mA
Power dissipation . . . . . 1.0 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		$V_{DD}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	– 1.0		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL}= –1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	’4C2972-24		’4C2972-26		’4C2972-28		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All others = 0 V to V_{DD}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 V to V_{DD}, V_{DD} = 5V, RE, OE low		± 10		± 10		± 10	µA
I_{DD1}	Average operating current	Minimum write/read cycle, Output open		50		50		50	mA
I_{DD2}	Average standby current	After one RSTW/RSTR cycle, WE, RE, OE low		15		15		15	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		MIN	MAX	UNIT
C_i	Input capacitance		7	pF
C_o	Output capacitance		10	pF

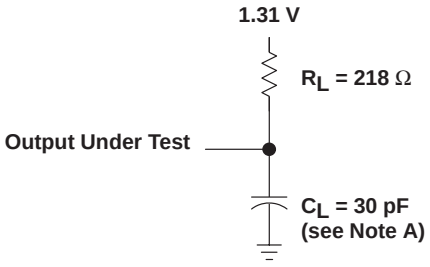
‡ V_{DD} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	'4C2972-24		'4C2972-26		'4C2972-28		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	See Note 3		19		21		23	ns
$t_{h(OUT)}$	Hold time, output after SRCK high	See Note 3	3		3		3		ns
$t_{dis(CK)}$	Disable time, output after SRCK high	See Note 4		12		12		12	ns
$t_{en(CK)}$	Enable time, output after SRCK high	See Note 3		17		19		21	ns

NOTES: 3. The load connected to each output is a 30 pF capacitor to ground, in parallel with a 218 Ω resistor to 1.31 V (see Figure 4).
4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output-voltage waveforms, sufficiently low-load resistors and capacitors must be used, and the RC time constants of the load have to be taken into account.

PARAMETER MEASUREMENT INFORMATION



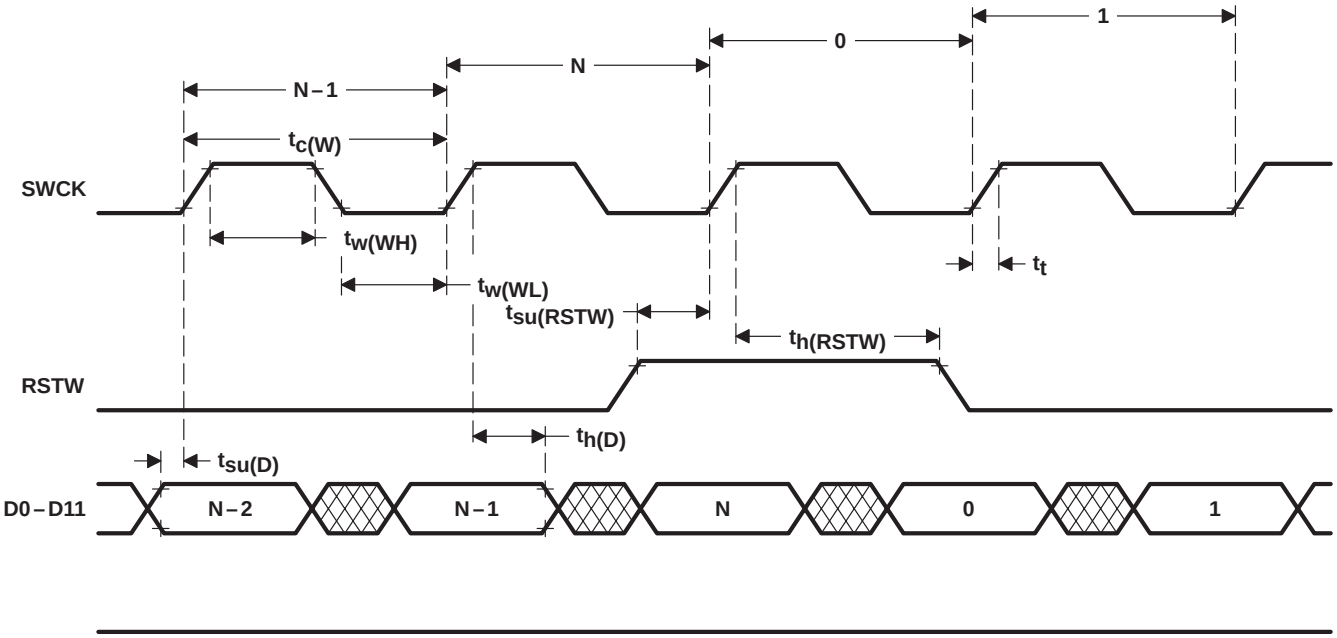
NOTE A: CL includes probe and fixture capacitance. (See Note 3.)

Figure 4. Output Load Circuit

timing requirements

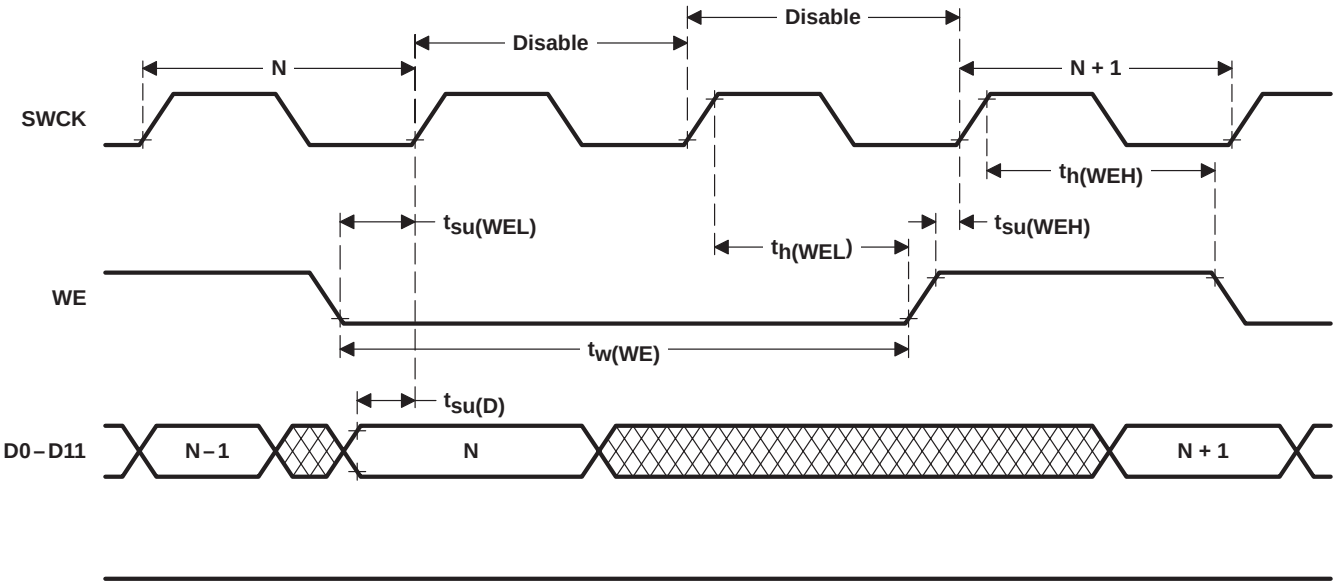
		’4C2972-24		’4C2972-26		’4C2972-28		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write	24		26		28		ns
$t_{c(R)}$	Cycle time, read	24		26		28		ns
$t_{h(D)}$	Hold time, data after SWCK high	3		3		3		ns
$t_{h(IEL)}$	Hold time, IE low after SWCK high	3		3		3		ns
$t_{h(IEH)}$	Hold time, IE high after SWCK high	3		3		3		ns
$t_{h(WEL)}$	Hold time, WE low after SWCK high	3		3		3		ns
$t_{h(WEH)}$	Hold time, WE high after SWCK high	3		3		3		ns
$t_{h(RSTW)}$	Hold time, RSTW after SWCK high	3		3		3		ns
$t_{h(OEL)}$	Hold time, OE low after SRCK high	3		3		3		ns
$t_{h(OEH)}$	Hold time, OE high after SRCK high	3		3		3		ns
$t_{h(REL)}$	Hold time, RE low after SRCK high	3		3		3		ns
$t_{h(REH)}$	Hold time, RE high after SRCK high	3		3		3		ns
$t_{h(RSTR)}$	Hold time, RSTR after SRCK high	3		3		3		ns
$t_{w(WH)}$	Pulse duration, SWCK high	6		7		8		ns
$t_{w(WL)}$	Pulse duration, SWCK low	6		7		8		ns
$t_{w(IE)}$	Pulse duration, IE low	7		8		9		ns
$t_{w(WE)}$	Pulse duration, WE low	7		8		9		ns
$t_{w(RH)}$	Pulse duration, SRCK high	6		7		8		ns
$t_{w(RL)}$	Pulse duration, SRCK low	6		7		8		ns
$t_{w(OE)}$	Pulse duration, OE low	7		8		9		ns
$t_{w(RE)}$	Pulse duration, RE low	7		8		9		ns
$t_{su(D)}$	Setup time, data before SWCK high	5		5		5		ns
$t_{su(IEL)}$	Setup time, IE low before SWCK high	5		5		5		ns
$t_{su(IEH)}$	Setup time, IE high before SWCK high	5		5		5		ns
$t_{su(WEL)}$	Setup time, WE low before SWCK high	5		5		5		ns
$t_{su(WEH)}$	Setup time, WE high before SWCK high	5		5		5		ns
$t_{su(RSTW)}$	Setup time, RSTW before SWCK high	5		5		5		ns
$t_{su(OEL)}$	Setup time, OE low before SRCK high	5		5		5		ns
$t_{su(OEH)}$	Setup time, OE high before SRCK high	5		5		5		ns
$t_{su(REL)}$	Setup time, RE low before SRCK high	5		5		5		ns
$t_{su(REH)}$	Setup time, RE high before SRCK high	5		5		5		ns
$t_{su(RSTR)}$	Setup time, RSTR before SRCK high	5		5		5		ns
t_t	Transition time	3	30	3	30	3	30	ns

write cycle timing



NOTE A: WE and IE signals remain at high level throughout entire cycle.

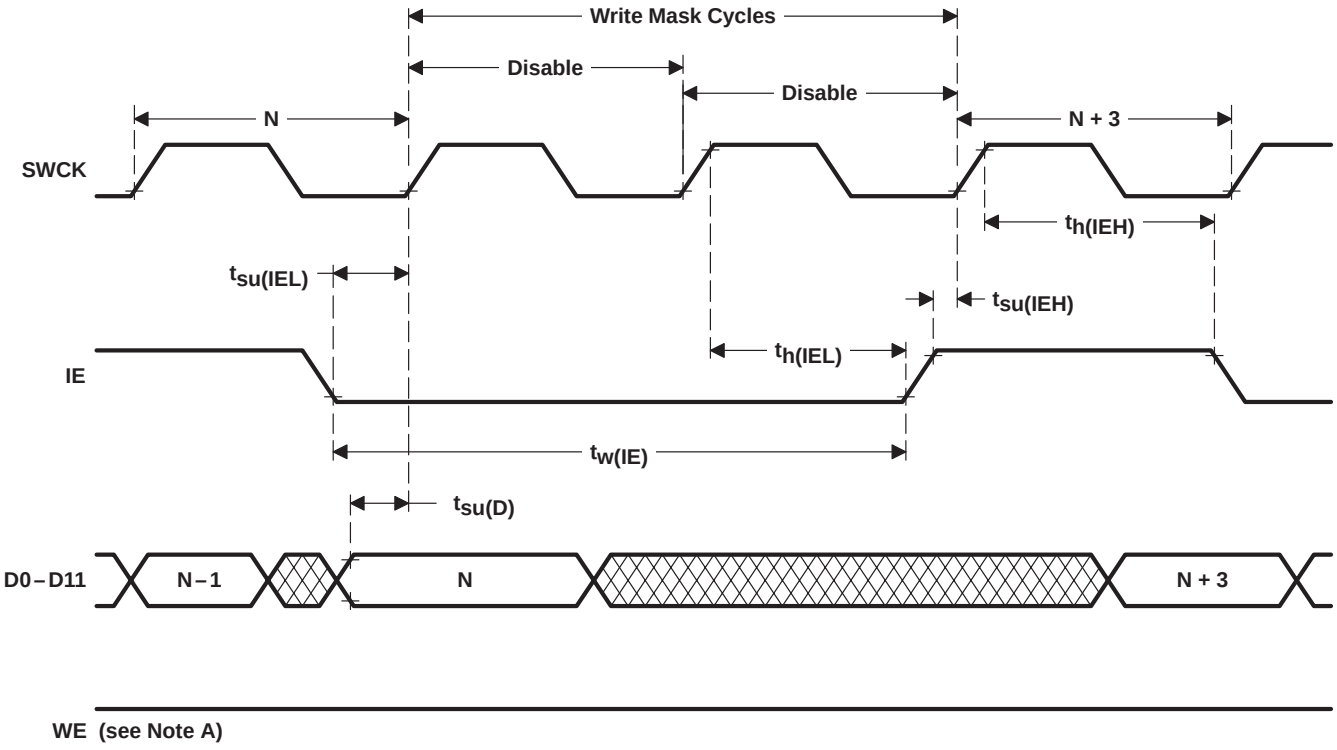
Figure 5. Write-Cycle Timing (Reset Write)



NOTE A: IE signal remains at high level throughout entire cycle.

Figure 6. Write-Cycle Timing (Write Enable)

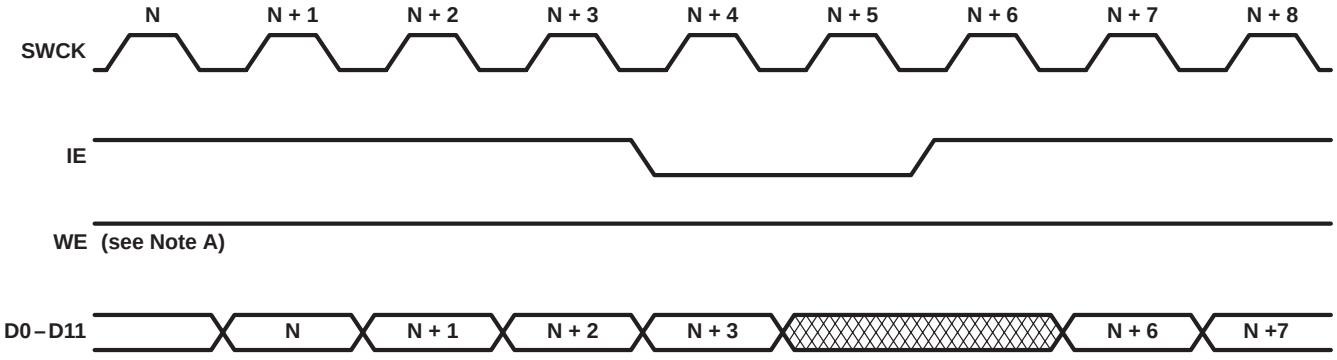
write cycle timing (continued)



NOTE A: WE signal remains at high level throughout entire cycle.

Figure 7. Write-Cycle Timing (Input Enable = Write-Mask Operation)

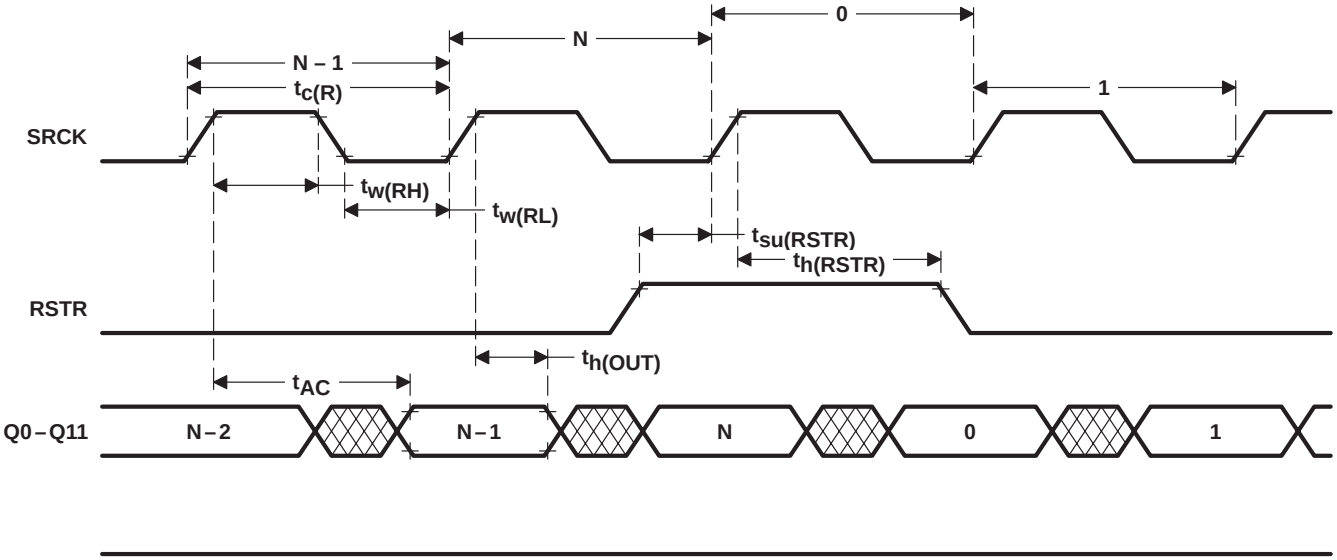
write mask operation



NOTE A: WE signal remains at high level throughout entire cycle.

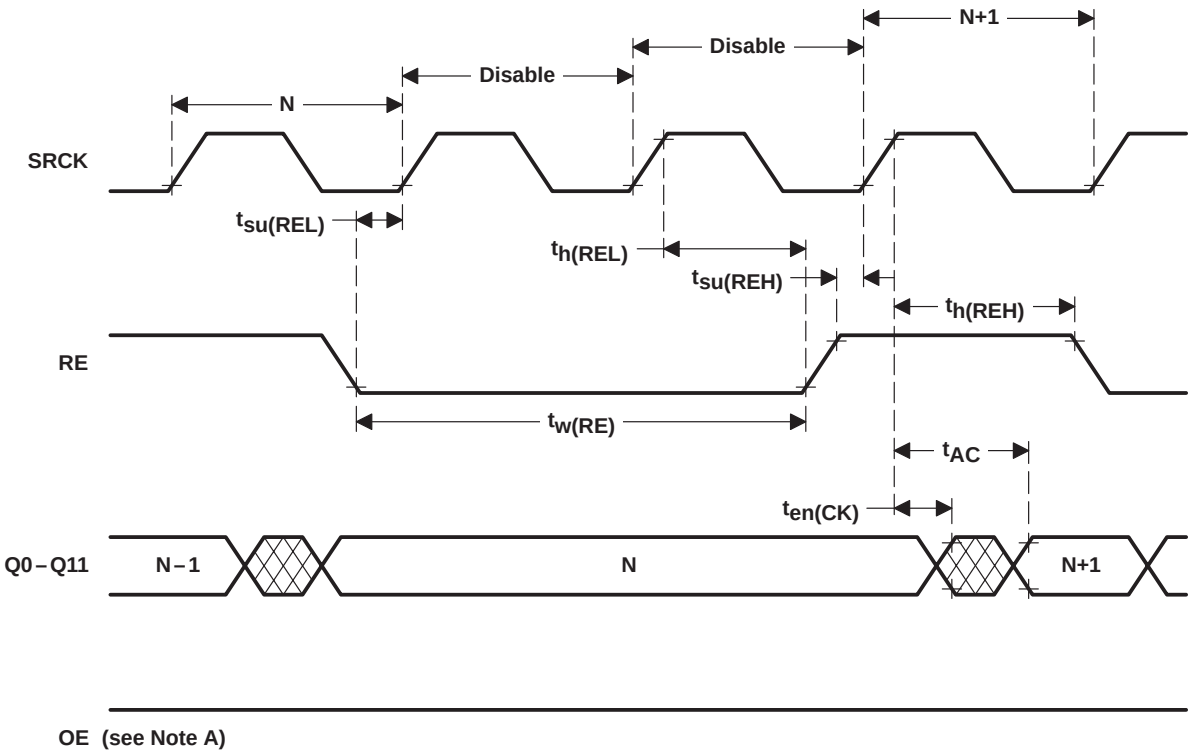
Figure 8. Write Mask Operation

read cycle timing



NOTE A: RE and OE signals remain at high level throughout entire cycle.

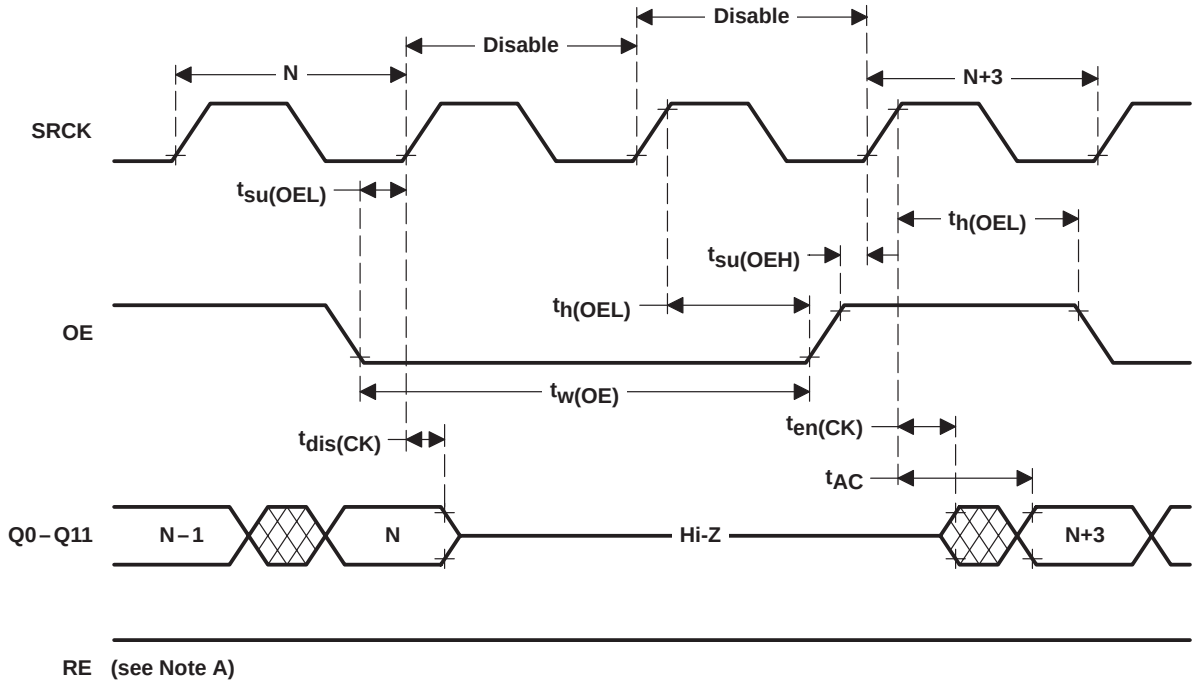
Figure 9. Read-Cycle Timing (Reset Read)



NOTE A: OE signal remains high level throughout entire cycle.

Figure 10. Read-Cycle Timing (Read Enable)

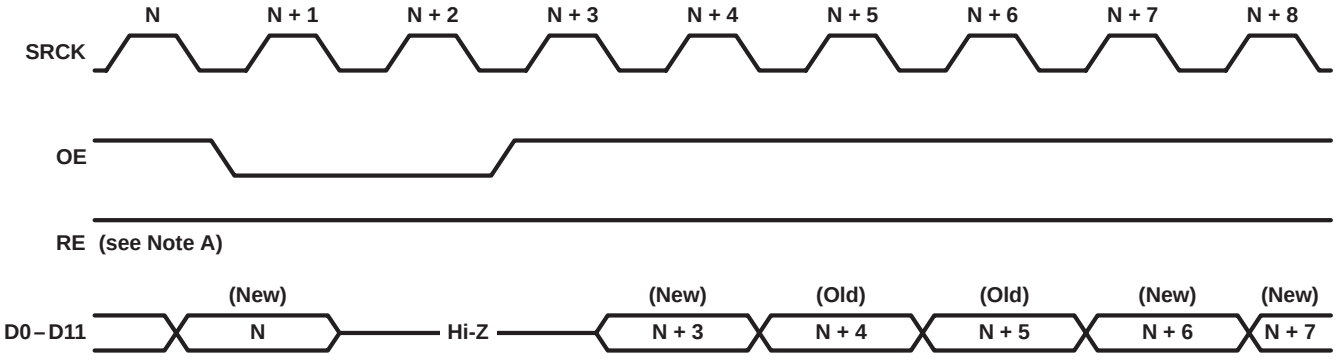
read cycle timing (continued)



NOTE A: RE signal remains high level throughout entire cycle.

Figure 11. Read-Cycle Timing (Output Enable)

read mask operation



NOTE A: RE signal remains high level throughout entire cycle.

Figure 12. Read Mask Operation

cascade operation

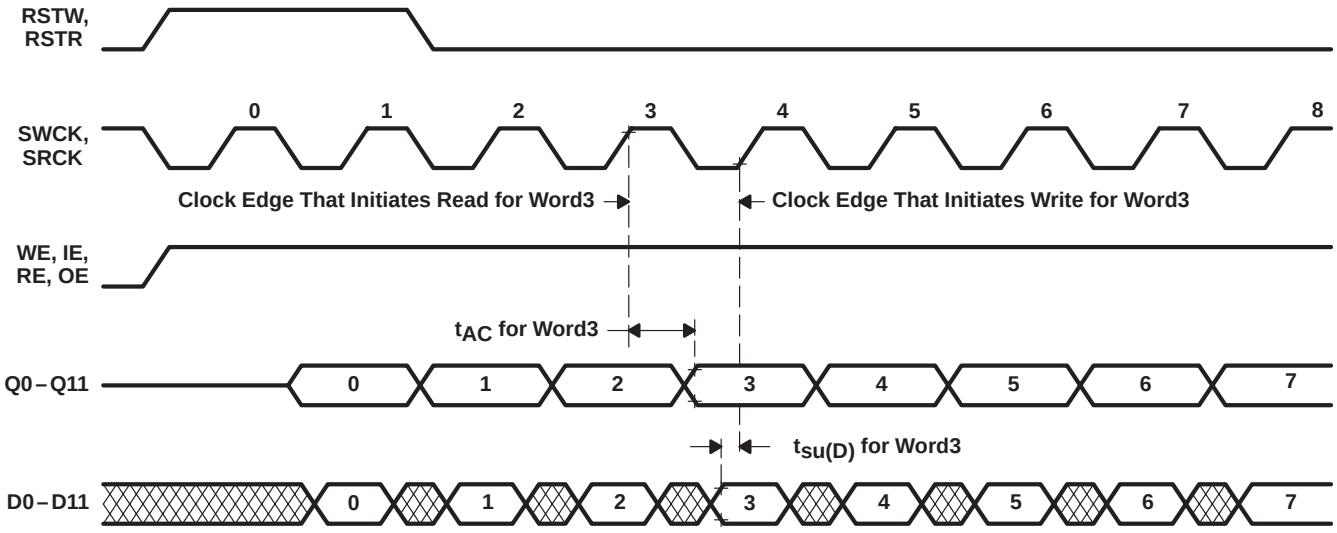


Figure 13. Cascade Operation – Timing Waveforms

data-access modes

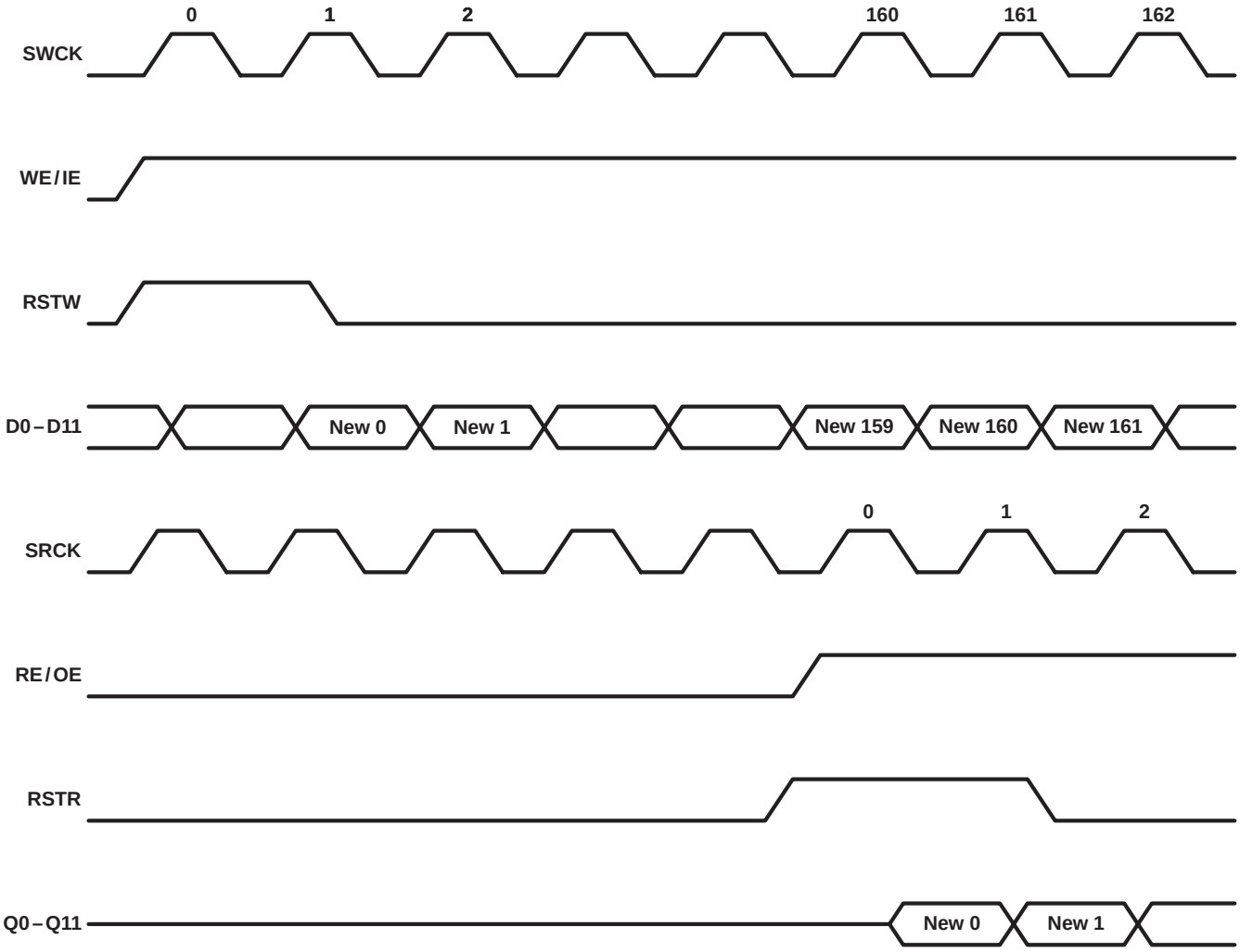


Figure 14. New Data-Access Mode

data-access modes (continued)

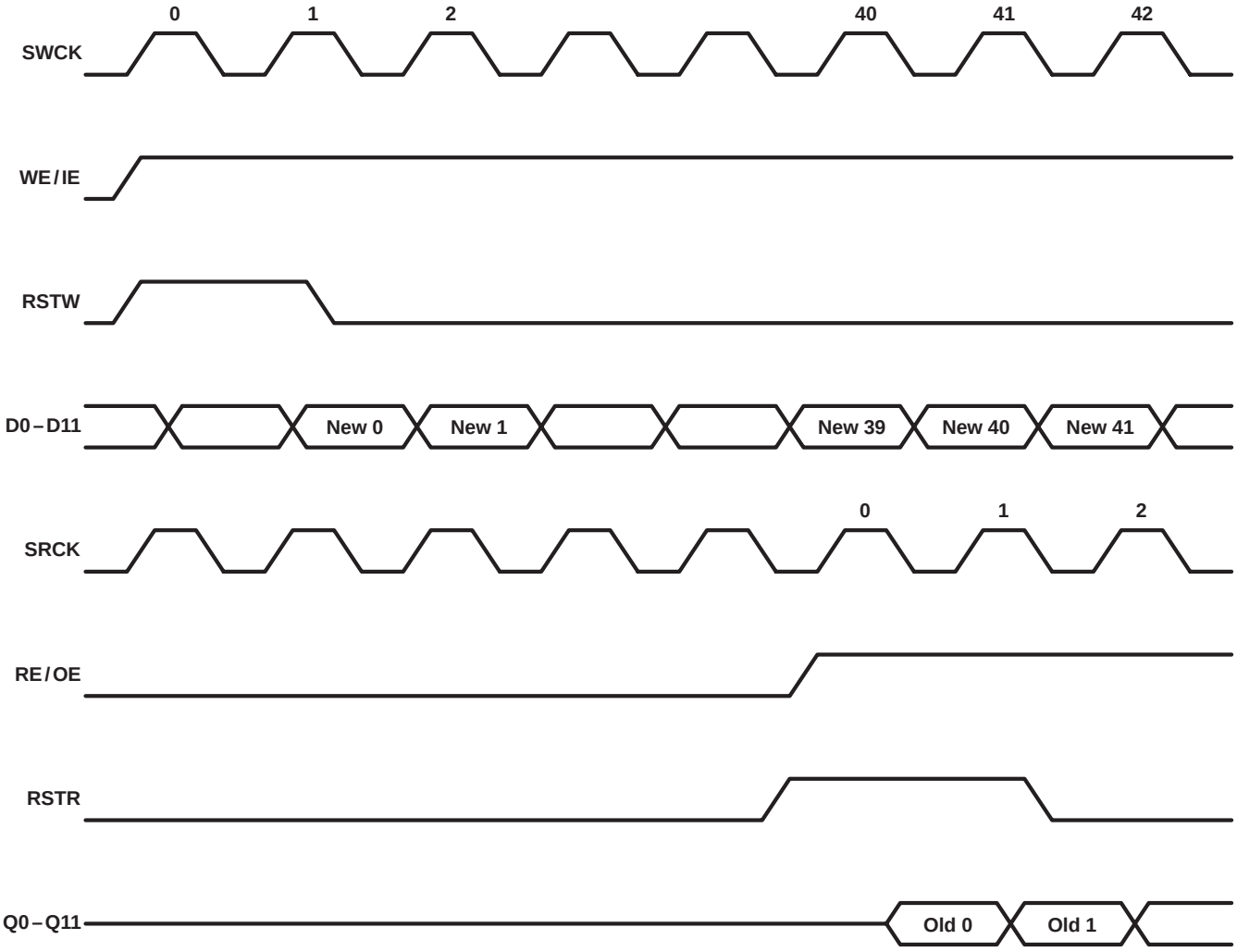


Figure 15. Old Data-Access Mode

entry sequences

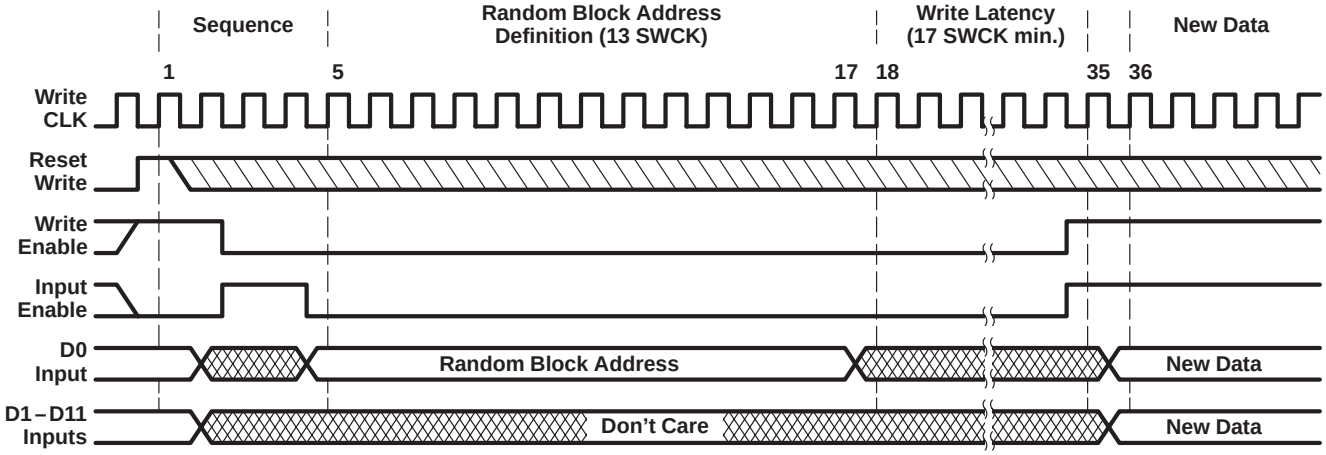


Figure 16. Entry Sequence for Write Random Block Access (D0-Controlled)

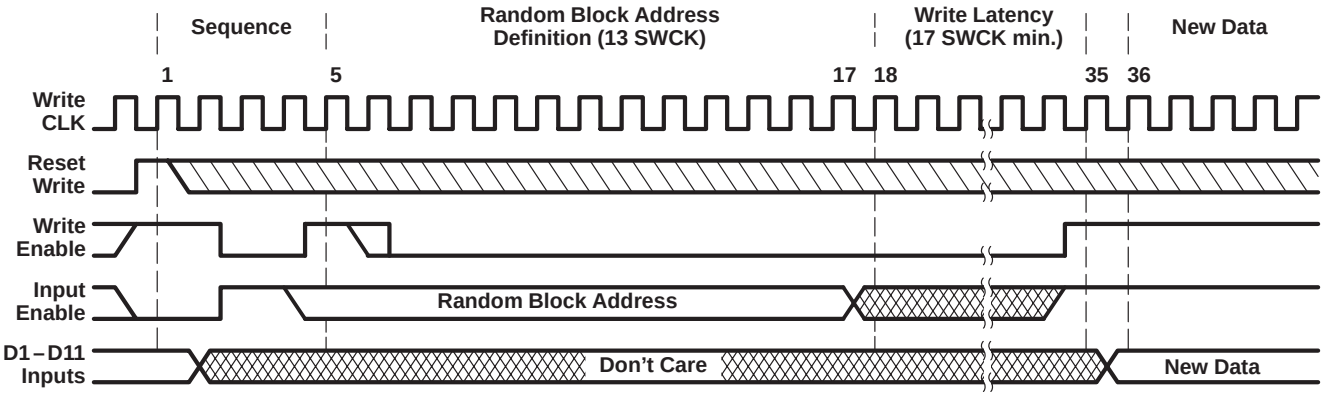


Figure 17. Entry Sequence for Write Random Block Access (IE-Controlled)

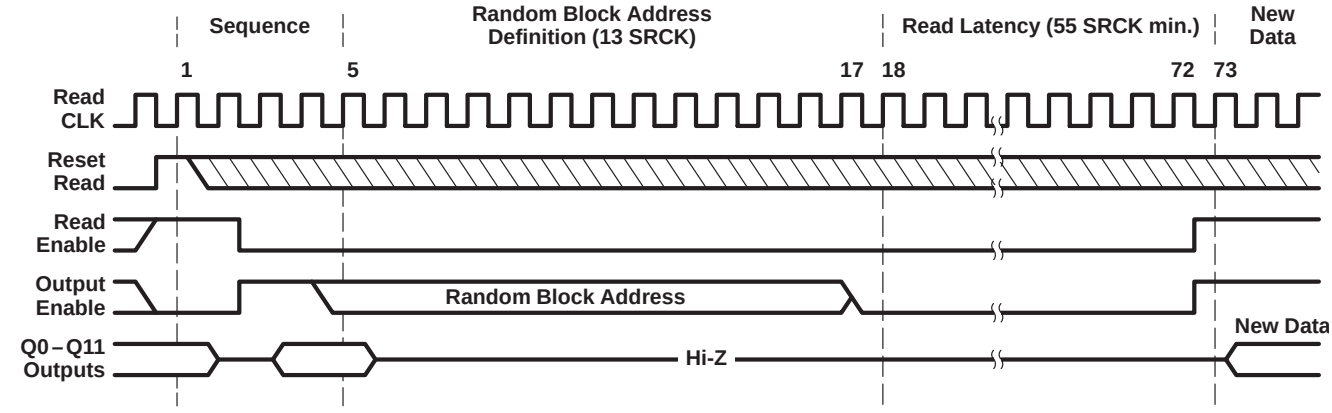
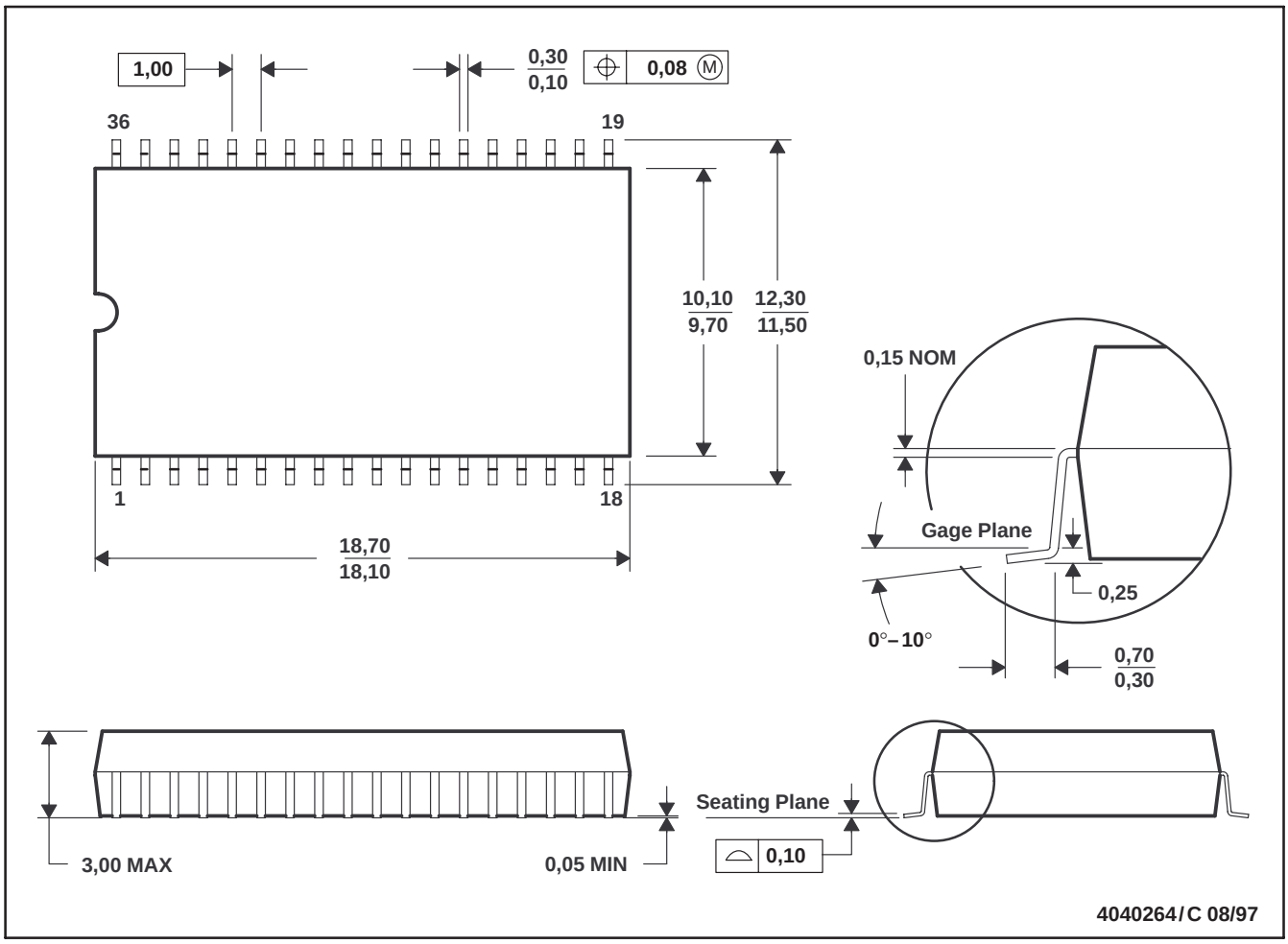


Figure 18. Entry Sequence for Read Random Block Access

MECHANICAL DATA

DT (R-PDSO-G36) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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