

- **Single Power Supply Supports 2.7-V and 3.6-V Read/Write Operation**
- **Organization**  
1048576 By 8 Bits  
524288 By 16 Bits
- **Array-Blocking Architecture**
  - One 16K-Byte/One 8K-Word Boot Sector
  - Two 8K-Byte/4K-Word Parameter Sectors
  - One 32K-Byte/16K-Word Sector
  - Fifteen 64K-Byte/32K-Word Sectors
  - Any Combination of Sectors Can Be Erased. Supports Full-Chip Erase
  - Any Combination of Sectors Can Be Marked as Read-Only
- **Boot-Code Sector Architecture**
  - T = Top Sector
  - B = Bottom Sector
- **Sector Protection**
  - Hardware Protection Method That Disables Any Combination of Sectors From Write or Erase Operations Using Standard Programming Equipment
- **Embedded Program/Erase Algorithms**
  - Automatically Pre-Programs and Erases Any Sector
  - Automatically Programs and Verifies the Program Data at Specified Address
- **JEDEC Standards**
  - Compatible With JEDEC Byte Pinouts
  - Compatible With JEDEC EEPROM Command Set
- **Fully Automated On-Chip Erase and Program Operations**
- **100 000 Program/Erase Cycles**
- **Low Power Dissipation**
  - 20-mA Typical Active Read for Byte Mode
  - 28-mA Typical Active Read for Word Mode
  - 30-mA Typical Program/Erase Current
  - Less Than 60-μA Standby Current
  - 5 μA in Deep Power-Down Mode
- **All Inputs/Outputs TTL-Compatible**
- **Erase Suspend/Resume**
  - Supports Reading Data From, or Programming Data to, a Sector Not Being Erased
- **Hardware-Reset Pin Initializes the Internal-State Machine to the Read Operation**
- **Package Options**
  - 44-Pin Plastic Small-Outline Package (PSOP) (DBJ Suffix)
  - 48-Pin Thin Small-Outline Package (TSOP) (DCD Suffix)
- **Detection Of Program/Erase Operation**
  - Data Polling and Toggle Bit Feature of Program/Erase Cycle Completion
  - Hardware Method for Detection of Program/Erase Cycle Completion Through Ready/Busy (RY/BY) Output Pin
- **High-Speed Data Access at 3.3-V**  
V<sub>CC</sub> ± 10% at Three Temperature Ranges
  - 90 ns      Commercial . . . 0°C to 70°C
  - 100 ns     Extended . . . –40°C to 85°C
  - 120 ns     Automotive . . . –40°C to 125°C

| PIN NOMENCLATURE    |                                    |
|---------------------|------------------------------------|
| A[0:18]             | Address Inputs                     |
| <u>BYTE</u>         | Byte/Word Enable                   |
| DQ[0:14]            | Data In/Data out                   |
| DQ15/A <sub>1</sub> | Data In/Out (Word-Wide mode)       |
| <u>CE</u>           | Low-Order Address (Byte-Wide mode) |
| <u>OE</u>           | Chip Enable                        |
| NC                  | Output Enable                      |
| <u>RESET</u>        | No Internal Connection             |
| RY/ <u>BY</u>       | Reset/Deep Power Down              |
| V <sub>CC</sub>     | Ready/Busy Output                  |
| V <sub>SS</sub>     | Power Supply                       |
| <u>WE</u>           | Ground                             |
|                     | Write Enable                       |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

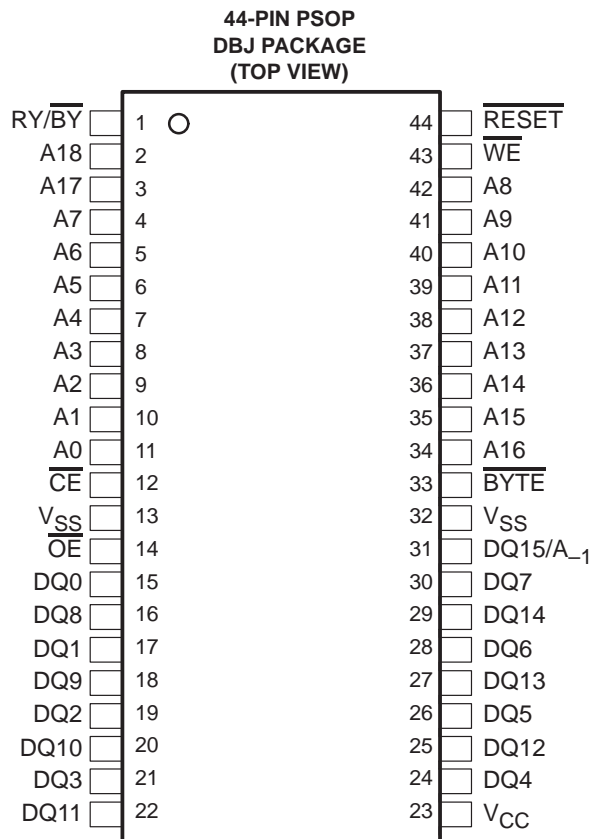


# TMS29LF800T, TMS29LF800B

## 1048576 BY 8-BIT/524288 BY 16-BIT

### FLASH MEMORIES

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997



#### description

The TMS29LF800T/B is a 1048576 by 8-bit/524288 by 16-bit (8388608-bit), 3-V single-supply, programmable read-only memory device that can be electrically erased and reprogrammed. This device is organized as 1024K by 8 bits or 512K by 16 bits, divided into 19 sectors:

- One 16K-byte/8K-word boot sector
- Two 8K-byte/4K-word sectors
- One 32K-byte/16K-word sector
- Fifteen 64K-byte/32K-word sectors

Any combination of sectors can be marked as read-only or erased. Full-chip erasure is also supported.

Sector data protection is afforded by methods that can disable any combination of sectors from write or read operations using standard programming equipment. An on-chip state machine provides an on-board algorithm that automatically pre-programs and erases any sector before it automatically programs and verifies program data at any specified address. The command set is compatible with that of the Joint Electronic Device Engineering Council (JEDEC) standards and is compatible with the JEDEC 8M-bit electrically erasable, programmable read-only memory (EEPROM) command set. A suspend/resume feature allows access to unaltered memory blocks during a section-erase operation. All outputs of this device are TTL-compatible. Additionally, an erase/suspend/resume feature supports reading data from, or programming data to, a sector that is not being erased.

48-PIN TSOP  
DCD PACKAGE  
(TOP VIEW)



PRODUCT PREVIEW

TMS29LF800T, TMS29LF800B  
 1048576 BY 8-BIT/524288 BY 16-BIT  
 FLASH MEMORIES

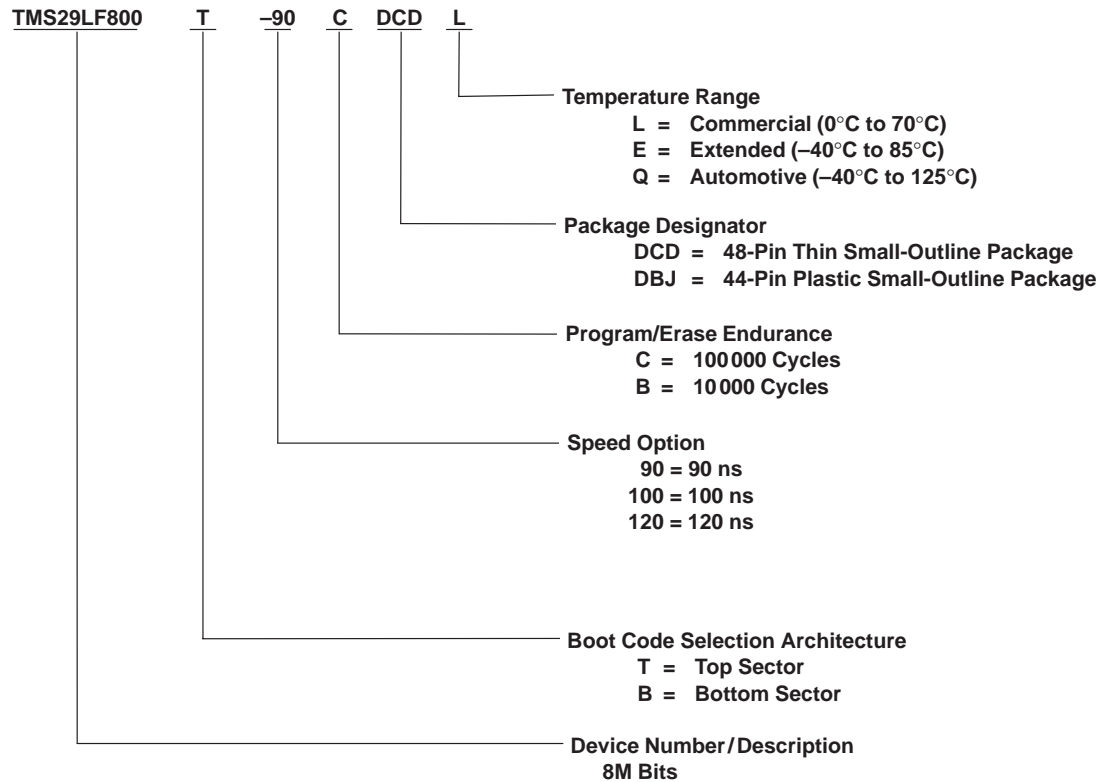
SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

description (continued)

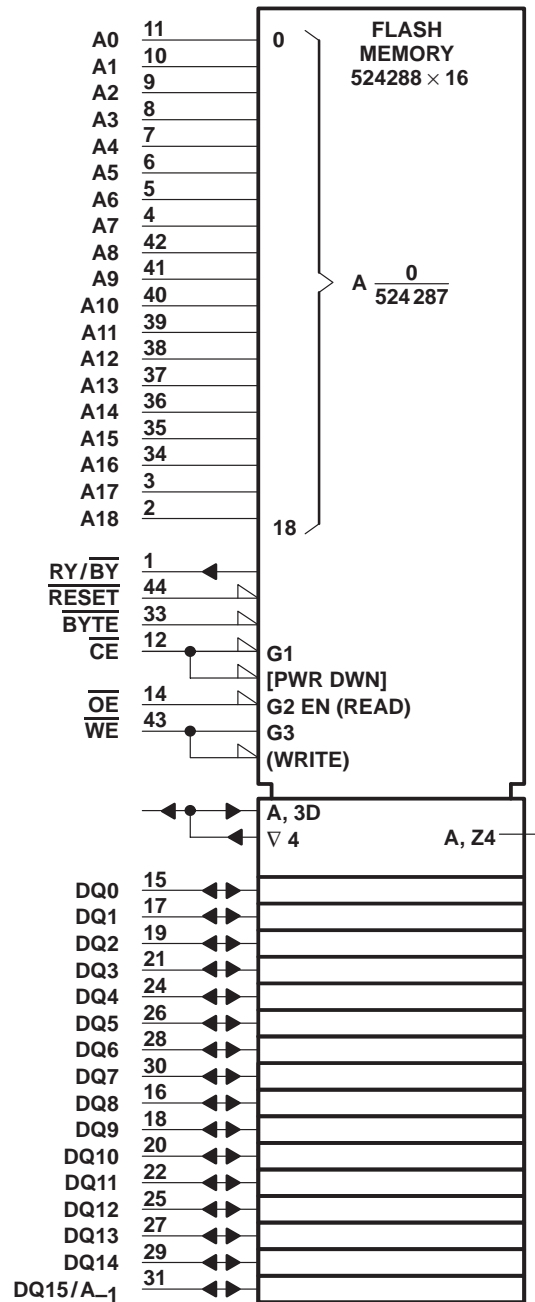
Device operations are selected by writing JEDEC-standard commands into the command register using standard microprocessor write timings. The command register acts as an input to an internal-state machine which interprets the commands, controls the erase and programming operations, outputs the status of the device, outputs the data stored in the device, and outputs the device algorithm-selection code. On initial power up, the device defaults to the read mode. A hardware-reset pin initializes the internal-state machine to the read operation.

The device has low power dissipation with a 20-mA active read for the byte mode, 28-mA active read for the word mode, 30-mA typical program/erase current mode, and less than 60-µA standby current with a 5-µA deep-power-down mode. These devices are offered with 90-, 100-, and 120-ns access times. Table 1 and Table 2 show the sector-address ranges. The TMS29LF800T/B is offered in a 48-pin thin small-outline package (TSOP ) (DCD suffix) and a 44-pin plastic small-outline package (PSOP) (DBJ suffix).

device symbol nomenclature



logic symbol for 44-pin package†

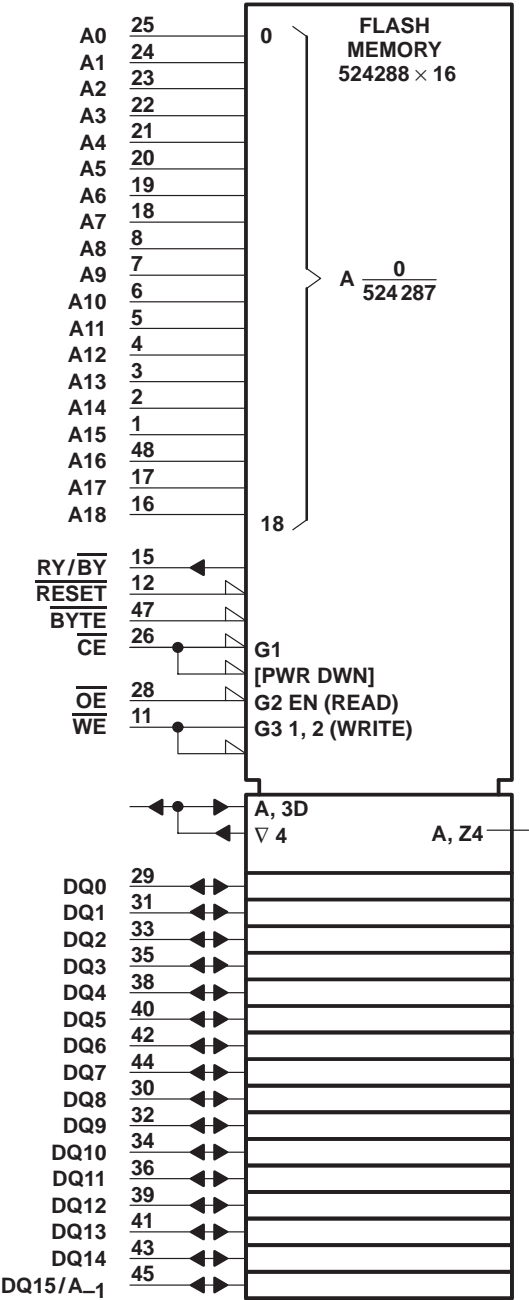


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DBJ package.

TMS29LF800T, TMS29LF800B  
 1048576 BY 8-BIT/524288 BY 16-BIT  
 FLASH MEMORIES

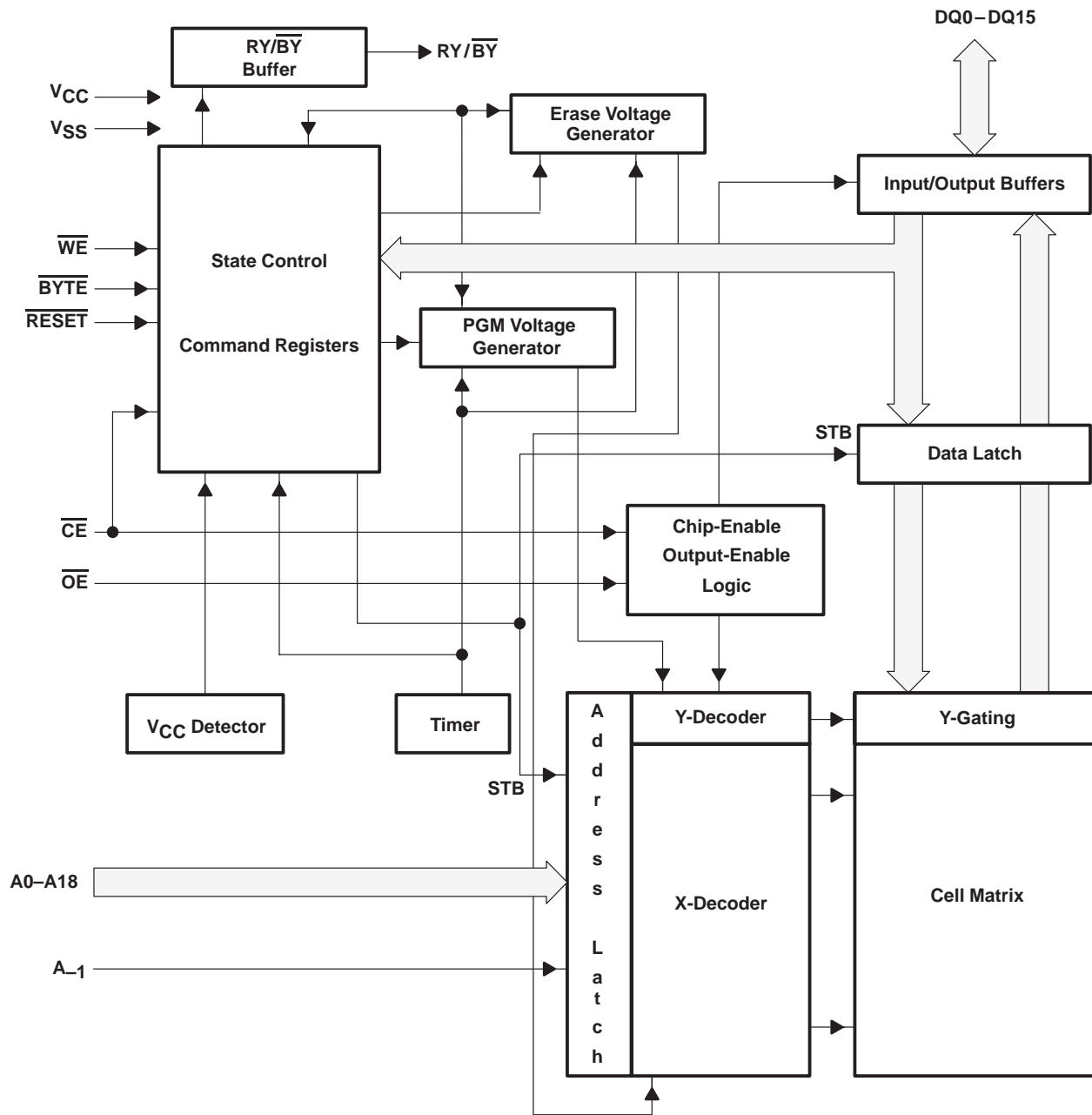
SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

logic symbol for 48-pin package†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the DCD package.

block diagram



PRODUCT PREVIEW

**TMS29LF800T, TMS29LF800B**  
**1048576 BY 8-BIT/524288 BY 16-BIT**  
**FLASH MEMORIES**

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

**operation**

See Table 1 and Table 2 for the sector-address ranges of the TMS29LF800T/B.

**Table 1. Top-Boot Sector-Address Ranges†**

|      | A18 | A17 | A16 | A15 | A14 | A13 | A12 | SECTOR SIZE | (x8) ADDRESS RANGE | (x16) ADDRESS RANGE |
|------|-----|-----|-----|-----|-----|-----|-----|-------------|--------------------|---------------------|
| SA18 | 1   | 1   | 1   | 1   | 1   | 1   | X   | 16K-Byte    | FC000H–FFFFFH      | 7E000H–7FFFFH       |
| SA17 | 1   | 1   | 1   | 1   | 1   | 0   | 1   | 8K-Byte     | FA000H–FBFFFFH     | 7D000H–7DFFFFH      |
| SA16 | 1   | 1   | 1   | 1   | 1   | 0   | 0   | 8K-Byte     | F8000H–F9FFFFH     | 7C000H–7CFFFFH      |
| SA15 | 1   | 1   | 1   | 1   | 0   | X   | X   | 32K-Byte    | F0000H–F7FFFFH     | 78000H–7BFFFFH      |
| SA14 | 1   | 1   | 1   | 0   | X   | X   | X   | 64K-Byte    | E0000H–EFFFFFH     | 70000H–77FFFFH      |
| SA13 | 1   | 1   | 0   | 1   | X   | X   | X   | 64K-Byte    | D0000H–DFFFFFH     | 68000H–6FFFFFH      |
| SA12 | 1   | 1   | 0   | 0   | X   | X   | X   | 64K-Byte    | C0000H–CFFFFFH     | 60000H–67FFFFH      |
| SA11 | 1   | 0   | 1   | 1   | X   | X   | X   | 64K-Byte    | B0000H–BFFFFFH     | 58000H–5FFFFFH      |
| SA10 | 1   | 0   | 1   | 0   | X   | X   | X   | 64K-Byte    | A0000H–AFFFFFH     | 50000H–57FFFFH      |
| SA9  | 1   | 0   | 0   | 1   | X   | X   | X   | 64K-Byte    | 90000H–9FFFFFH     | 48000H–4FFFFFH      |
| SA8  | 1   | 0   | 0   | 0   | X   | X   | X   | 64K-Byte    | 80000H–8FFFFFH     | 40000H–47FFFFH      |
| SA7  | 0   | 1   | 1   | 1   | X   | X   | X   | 64K-Byte    | 70000H–7FFFFFH     | 38000H–3FFFFFH      |
| SA6  | 0   | 1   | 1   | 0   | X   | X   | X   | 64K-Byte    | 60000H–6FFFFFH     | 30000H–37FFFFH      |
| SA5  | 0   | 1   | 0   | 1   | X   | X   | X   | 64K-Byte    | 50000H–5FFFFFH     | 28000H–2FFFFFH      |
| SA4  | 0   | 1   | 0   | 0   | X   | X   | X   | 64K-Byte    | 40000H–4FFFFFH     | 20000H–27FFFFH      |
| SA3  | 0   | 0   | 1   | 1   | X   | X   | X   | 64K-Byte    | 30000H–3FFFFFH     | 18000H–1FFFFFH      |
| SA2  | 0   | 0   | 1   | 0   | X   | X   | X   | 64K-Byte    | 20000H–2FFFFFH     | 10000H–17FFFFH      |
| SA1  | 0   | 0   | 0   | 1   | X   | X   | X   | 64K-Byte    | 10000H–1FFFFFH     | 08000H–0FFFFFH      |
| SA0  | 0   | 0   | 0   | 0   | X   | X   | X   | 64K-Byte    | 00000H–0FFFFFH     | 00000H–07FFFFH      |

† The address range is A<sub>1</sub>–A18 in byte mode.  
The address range is A0–A18 in word mode.



operation (continued)

Table 2. Bottom-Boot Sector-Address Ranges†

|      | A18 | A17 | A16 | A15 | A14 | A13 | A12 | SECTOR SIZE | (x8) ADDRESS RANGE | (x16) ADDRESS RANGE |
|------|-----|-----|-----|-----|-----|-----|-----|-------------|--------------------|---------------------|
| SA18 | 1   | 1   | 1   | 1   | X   | X   | X   | 64K-Byte    | F0000H–FFFFFH      | 78000H–7FFFFH       |
| SA17 | 1   | 1   | 1   | 0   | X   | X   | X   | 64K-Byte    | E0000H–EFFFFH      | 70000H–77FFFH       |
| SA16 | 1   | 1   | 0   | 1   | X   | X   | X   | 64K-Byte    | D0000H–DFFFFH      | 68000H–6FFFFH       |
| SA15 | 1   | 1   | 0   | 0   | X   | X   | X   | 64K-Byte    | C0000H–CFFFFH      | 60000H–67FFFH       |
| SA14 | 1   | 0   | 1   | 1   | X   | X   | X   | 64K-Byte    | B0000H–BFFFFH      | 58000H–5FFFFH       |
| SA13 | 1   | 0   | 1   | 0   | X   | X   | X   | 64K-Byte    | A0000H–AFFFFH      | 50000H–57FFFH       |
| SA12 | 1   | 0   | 0   | 1   | X   | X   | X   | 64K-Byte    | 90000H–9FFFFH      | 48000H–4FFFFH       |
| SA11 | 1   | 0   | 0   | 0   | X   | X   | X   | 64K-Byte    | 80000H–8FFFFH      | 40000H–47FFFH       |
| SA10 | 0   | 1   | 1   | 1   | X   | X   | X   | 64K-Byte    | 70000H–7FFFFH      | 38000H–3FFFFH       |
| SA9  | 0   | 1   | 1   | 0   | X   | X   | X   | 64K-Byte    | 60000H–6FFFFH      | 30000H–37FFFH       |
| SA8  | 0   | 1   | 0   | 1   | X   | X   | X   | 64K-Byte    | 50000H–5FFFFH      | 28000H–2FFFFH       |
| SA7  | 0   | 1   | 0   | 0   | X   | X   | X   | 64K-Byte    | 40000H–4FFFFH      | 20000H–27FFFH       |
| SA6  | 0   | 0   | 1   | 1   | X   | X   | X   | 64K-Byte    | 30000H–3FFFFH      | 18000H–1FFFFH       |
| SA5  | 0   | 0   | 1   | 0   | X   | X   | X   | 64K-Byte    | 20000H–2FFFFH      | 10000H–17FFFH       |
| SA4  | 0   | 0   | 0   | 1   | X   | X   | X   | 64K-Byte    | 10000H–1FFFFH      | 08000H–0FFFFH       |
| SA3  | 0   | 0   | 0   | 0   | 1   | X   | X   | 32K-Byte    | 08000H–0FFFFH      | 04000H–07FFFH       |
| SA2  | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 8K-Byte     | 06000H–07FFFH      | 03000H–03FFFH       |
| SA1  | 0   | 0   | 0   | 0   | 0   | 1   | 0   | 8K-Byte     | 04000H–05FFFH      | 02000H–02FFFH       |
| SA0  | 0   | 0   | 0   | 0   | 0   | 0   | X   | 16K-Byte    | 00000H–03FFFH      | 00000H–01FFFH       |

† The address range is A<sub>1</sub>–A18 in byte mode.  
The address range is A0–A18 in word mode.

PRODUCT PREVIEW

**TMS29LF800T, TMS29LF800B**  
**1048576 BY 8-BIT/524288 BY 16-BIT**  
**FLASH MEMORIES**

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

**operation (continued)**

See Table 3 and Table 4 for the operation modes of the TMS29LF800T/B.

**Table 3. Byte-Operation Mode ( $\overline{\text{BYTE}} = V_{\text{IL}}$ )**

| MODE                       | FUNCTIONS†             |                        |                        |                 |                 |                 |                 |                           | DQ0–DQ7   |
|----------------------------|------------------------|------------------------|------------------------|-----------------|-----------------|-----------------|-----------------|---------------------------|---|
|                            | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A0              | A1              | A6              | A9              | $\overline{\text{RESET}}$ |   |
| Algorithm-selection mode   | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Manufacturer-Equivalent Code 01h (TMS29LF800T/B – Byte) |
| 3-V power supply           | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IH}}$ | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Device-Equivalent Code DAh (TMS29LF800T – Byte)         |
|                            | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IH}}$ | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Device-Equivalent Code 5Bh (TMS29LF800B – Byte)         |
| Read                       | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | A0              | A1              | A6              | A9              | $V_{\text{IH}}$           | Data out  |
| Output disable             | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IH}}$        | X               | X               | X               | X               | $V_{\text{IH}}$           | Hi-Z  |
| Standby and write inhibit  | $V_{\text{IH}}$        | X                      | X                      | X               | X               | X               | X               | $V_{\text{IH}}$           | Hi-Z  |
| Write‡                     | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IL}}$        | A0              | A1              | A6              | A9              | $V_{\text{IH}}$           | Data in   |
| Temporary sector unprotect | X                      | X                      | X                      | X               | X               | X               | X               | $V_{\text{ID}}$           | X   |
| Verify sector protect      | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IL}}$ | $V_{\text{IH}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Data out  |
| Hardware reset             | X                      | X                      | X                      | X               | X               | X               | X               | $V_{\text{IL}}$           | Hi-Z  |

Legend:

$V_{\text{IL}}$  = Logic 0

$V_{\text{IH}}$  = Logic 1

$V_{\text{ID}}$  =  $12.0 \pm 0.5$  V

† X can be  $V_{\text{IL}}$  or  $V_{\text{IH}}$ .

‡ See Table 6 for valid address and data during write.

**Table 4. Word-Operation Mode ( $\overline{\text{BYTE}} = V_{\text{IH}}$ )**

| MODE                       | FUNCTIONS†             |                        |                        |                 |                 |                 |                 |                           | DQ0–DQ15  |
|----------------------------|------------------------|------------------------|------------------------|-----------------|-----------------|-----------------|-----------------|---------------------------|---|
|                            | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | A0              | A1              | A6              | A9              | $\overline{\text{RESET}}$ |   |
| Algorithm-selection mode   | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Manufacturer-Equivalent Code 01h (TMS29LF800T/B – Word) |
| 3-V power supply           | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IH}}$ | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Device-Equivalent Code 22DAh (TMS29LF800T – Word)       |
|                            | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IH}}$ | $V_{\text{IL}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Device-Equivalent Code 225Bh (TMS29LF800B – Word)       |
| Read                       | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | A0              | A1              | A6              | A9              | $V_{\text{IH}}$           | Data out  |
| Output disable             | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IH}}$        | X               | X               | X               | X               | $V_{\text{IH}}$           | Hi-Z  |
| Standby and write inhibit  | $V_{\text{IH}}$        | X                      | X                      | X               | X               | X               | X               | $V_{\text{IH}}$           | Hi-Z  |
| Write‡                     | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IL}}$        | A0              | A1              | A6              | A9              | $V_{\text{IH}}$           | Data in   |
| Temporary sector unprotect | X                      | X                      | X                      | X               | X               | X               | X               | $V_{\text{ID}}$           | X   |
| Verify sector protect      | $V_{\text{IL}}$        | $V_{\text{IL}}$        | $V_{\text{IH}}$        | $V_{\text{IL}}$ | $V_{\text{IH}}$ | $V_{\text{IL}}$ | $V_{\text{ID}}$ | $V_{\text{IH}}$           | Data out  |
| Hardware reset             | X                      | X                      | X                      | X               | X               | X               | X               | $V_{\text{IL}}$           | Hi-Z  |

Legend:

$V_{\text{IL}}$  = Logic 0

$V_{\text{IH}}$  = Logic 1

$V_{\text{ID}}$  =  $12.0 \pm 0.5$  V

† X can be  $V_{\text{IL}}$  or  $V_{\text{IH}}$ .

‡ See Table 6 for valid address and data during write.



## read mode

A logic-low signal applied to the  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  pins allows the output of the TMS29LF800T/B to be read. When two or more '29LF800T/B devices are connected in parallel, the output of any one device can be read without interference. The  $\overline{\text{CE}}$  pin is for power control and is used for device selection. The  $\overline{\text{OE}}$  pin is for output control, and is used to gate the data output onto the bus from the selected device.

The address-access time ( $t_{\text{AVQV}}$ ) is the delay from stable address to valid output data. The chip-enable ( $\overline{\text{CE}}$ ) access time ( $t_{\text{ELQV}}$ ) is the delay from  $\overline{\text{CE}}$  low and stable addresses to valid output data. The output-enable access time ( $t_{\text{GLQV}}$ ) is the delay from  $\overline{\text{OE}}$  low to valid output data when  $\overline{\text{CE}}$  equals logic low and addresses are stable for at least the duration of  $t_{\text{AVQV}} - t_{\text{GLQV}}$ .

## standby mode

$I_{\text{CC}}$  supply current is reduced by applying a logic-high level on  $\overline{\text{CE}}$  and  $\overline{\text{RESET}}$  to enter the standby mode. In the standby mode, the outputs are placed in the high-impedance state. Applying a CMOS logic-high level on  $\overline{\text{CE}}$  and  $\overline{\text{RESET}}$  reduces the current to 60  $\mu\text{A}$ . Applying a TTL logic-high level on  $\overline{\text{CE}}$  and  $\overline{\text{RESET}}$  reduces the current to 1 mA. If the '29LF800T/B is deselected during erasure or programming, the device continues to draw active current until the operation is complete.

## output disable

When  $\overline{\text{OE}}$  equals  $V_{\text{IH}}$  or  $\overline{\text{CE}}$  equals  $V_{\text{IH}}$ , output from the device is disabled and the output pins (DQ0–DQ15) are placed in the high-impedance state.

## automatic-sleep mode

The '29LF800T/B has a built-in feature called automatic-sleep mode to minimize device energy consumption which is independent of  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$ , and  $\overline{\text{OE}}$ , and is enabled when addresses remain stable for 300 ns. Typical sleep-mode current is 60  $\mu\text{A}$ . Sleep mode does not affect output data, which remains latched and available to the system.

## algorithm selection

The algorithm-selection mode provides access to a binary code that matches the device with its proper programming and erase command operations. This mode is activated when  $V_{\text{ID}}$  (11.5 V to 12.5 V) is placed on address pin A9. Address pins A1 and A6 must be logic low. Two bytes of code are accessed by toggling address pin A0 from  $V_{\text{IL}}$  to  $V_{\text{IH}}$ . Address pins other than A0, A1, and A6 can be at logic low or at logic high.

The algorithm-selection mode can also be read by using the command register, which is useful when  $V_{\text{ID}}$  is not available to be placed on address pin A9. Table 5 shows the binary algorithm-selection codes.

Table 5. Algorithm-Selection Codes (3-V Single Power Supply)<sup>†</sup>

|                              | CODE  | DQ15           | DQ14 | DQ13 | DQ12 | DQ11 | DQ10 | DQ9  | DQ8  | DQ7 | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |
|------------------------------|-------|----------------|------|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|
| Manufacturer-equivalent code | 01H   | 0              | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |
| TMS29LF800T-Byte             | DAH   | A <sub>1</sub> | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | 1   | 1   | 0   | 1   | 1   | 0   | 1   | 0   |
| TMS29LF800B-Byte             | 5BH   | A <sub>1</sub> | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | 0   | 1   | 0   | 1   | 1   | 0   | 1   | 1   |
| TMS29LF800T                  | 22DAH | 0              | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 1   | 1   | 0   | 1   | 1   | 0   | 1   | 0   |
| TMS29LF800B                  | 225BH | 0              | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 0   | 1   | 0   | 1   | 1   | 0   | 1   | 1   |
| Sector protection            | 01H   | 0              | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

<sup>†</sup> A1 =  $V_{\text{IL}}$ , A6 =  $V_{\text{IL}}$ ,  $\overline{\text{CE}}$  =  $V_{\text{IL}}$ ,  $\overline{\text{OE}}$  =  $V_{\text{IL}}$

# TMS29LF800T, TMS29LF800B

## 1048576 BY 8-BIT/524288 BY 16-BIT

### FLASH MEMORIES

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

---

#### erasure and programming

Erase and programming of the '29LF800 are accomplished by writing a sequence of commands using standard microprocessor write timing. The commands are written to a command register and input to the command-state machine (CSM). The CSM interprets the command entered and initiates program, erase, suspend, and resume operations as instructed. The CSM acts as the interface between the write-state machine (WSM) and external-chip operations. The WSM controls all voltage generation, pulse generation, preconditioning, and verification of memory contents. Program and block-/chip-erase functions are fully automatic. Once the end of a program or erase operation has been reached, the device resets internally to the read mode. If  $V_{CC}$  drops below the low-voltage-detect level ( $V_{LKO}$ ), any programming or erase operation is aborted and subsequent writes are ignored until the  $V_{CC}$  level is greater than  $V_{LKO}$ . The control pins must be logically correct to prevent unintentional command writes, programming, or erasing.

#### command definitions

Device operating modes are selected by writing specific address and data sequences into the command register. Table 6 defines the valid command sequences. Writing incorrect address and data values or writing them in the incorrect sequence causes the device to reset to the read mode. The command register does not occupy an addressable memory location. The register is used to store the command sequence along with the address and data needed by the memory array. Commands are written by setting  $\overline{CE} = V_{IL}$ ,  $\overline{OE} = V_{IH}$ , and bringing  $\overline{WE}$  from logic high to logic low. Addresses are latched on the falling edge of  $\overline{WE}$  and data is latched on the rising edge of  $\overline{WE}$ . Holding  $\overline{WE} = V_{IL}$  and toggling  $\overline{CE}$  is an alternative method. See the switching characteristics of the write/erase/program-operations section for specific timing information.

PRODUCT PREVIEW



**command definitions (continued)**

**Table 6. Command Definitions**

| COMMAND                     | BUS CYCLES | 1ST CYCLE<br>ADDR DATA | 2ND CYCLE<br>ADDR DATA                                | 3RD CYCLE<br>ADDR DATA | 4TH CYCLE<br>ADDR DATA | 5TH CYCLE<br>ADDR DATA | 6TH CYCLE<br>ADDR DATA |
|-----------------------------|------------|------------------------|---|------------------------|------------------------|------------------------|------------------------|
| Read/reset (word)           | 1          | xxxxH    xxF0H         |   |                        |                        |                        |                        |
| Read/reset (byte)           | 1          | xxx    F0H             |   |                        |                        |                        |                        |
| Read/reset (word)           | 3          | 555H    xxAAH          | 2AAH    xx55H   | 555H    xxF0H          | RA    RD               |                        |                        |
| Read/reset (byte)           | 3          | 2AAH    AAH            | 555H    55H   | 2AAH    F0H            | RA    RD               |                        |                        |
| Algorithm selection (word)  | 3          | 555H    xxAAH          | 2AAH    xx55H   | 555H    xx90H          | 01H                    | 22DAH<br>T             |                        |
|                             |            |                        |   |                        |                        | 225BH<br>B             |                        |
| Algorithm selection (byte)  | 3          | 2AAH    AAH            | 555H    55H   | 2AAH    90H            | 01H                    | DAH<br>T               |                        |
|                             |            |                        |   |                        |                        | 5BH<br>B               |                        |
| Program (word)              | 4          | 555H    xxAAH          | 2AAH    xx55H   | 555H    xxA0H          | PA    PD               |                        |                        |
| Program (byte)              | 4          | 2AAH    AAH            | 555H    55H   | 2AAH    A0H            | PA    PD               |                        |                        |
| Chip erase (word)           | 6          | 555H    xxAAH          | 2AAH    xx55H   | 555H    xx80H          | 555H    xxAAH          | 2AAH    xx55H          | 555H    xx10H          |
| Chip erase (byte)           | 6          | 2AAH    AAH            | 555H    55H   | 2AAH    80H            | 2AAH    AAH            | 555H    55H            | 2AAH    10H            |
| Sector erase (word)         | 6          | 555H    xxAAH          | 2AAH    xx55H   | 555H    xx80H          | 555H    xxAAH          | 2AAH    xx55H          | SA    xx30H            |
| Sector erase (byte)         | 6          | 2AAH    AAH            | 555H    55H   | 2AAH    80H            | 2AAH    AAH            | 555H    55H            | SA    30H              |
| Sector-erase suspend (word) | 1          | XXXXH    xxB0H         | Erase suspend valid during sector-erase operation     |                        |                        |                        |                        |
| Sector-erase suspend (byte) | 1          | XXX    B0H             | Erase suspend valid during sector-erase operation     |                        |                        |                        |                        |
| Sector-erase resume (word)  | 1          | XXXXH    xx30H         | Erase resume valid only after erase-suspend operation |                        |                        |                        |                        |
| Sector-erase resume (byte)  | 1          | XXX    30H             | Erase resume valid only after erase-suspend operation |                        |                        |                        |                        |

**LEGEND:**

- RA = Address of the location to be read
- PA = Address of the location to be programmed
- SA = Address of the sector to be erased  
Addresses A12—A18 select 1 to 19 sectors.
- RD = Data to be read at selected address location
- PD = Data to be programmed at selected address location

**read/reset command**

The read or reset mode is activated by writing either of the two read/reset command sequences into the command register. The device remains in this mode until another valid command sequence is input in the command register. Memory data is available in the read mode and can be read with standard microprocessor read-cycle timing.

### **read/reset command (continued)**

On power up, the device defaults to the read/reset mode. A read/reset command sequence is not required and memory data is available.

### **algorithm-selection command**

The algorithm-selection command allows access to a binary code that matches the device with the proper programming and erase command operations. After writing the three-bus-cycle command sequence, the first byte/word of the algorithm-selection code can be read from address XX00h. The second byte/word of the code can be read from address XX01h (see Table 6). This mode remains in effect until another valid command sequence is written to the device.

### **program command**

Programming is a four-bus-cycle command sequence. The first three bus cycles put the device into the program-setup state. The fourth bus cycle loads the address location and the data to be programmed into the device. The addresses are latched on the falling edge of  $\overline{WE}$  and the data is latched on the rising edge of  $\overline{WE}$  in the fourth bus cycle. The rising edge of  $\overline{WE}$  starts the program operation. The embedded programming function automatically provides needed voltage and timing to program and verify the cell margin. Any further commands written to the device during the program operation are ignored.

Programming can be performed at any address location in any sequence. When erased, all bits are in a logic-high state. Logic lows are programmed into the device and only an erase operation can change bits from logic lows to logic highs. Attempting to program a 1 into a bit that has been programmed previously to a 0 causes the internal-pulse counter to exceed the pulse-count limit, which sets the exceed-time-limit indicator (DQ5) to a logic-high state. The automatic-programming operation is complete when the data on DQ7 is equivalent to the data written to DQ5, at which time the device returns to the read mode and addresses are no longer latched. Figure 9 shows a flowchart of the typical device-programming operation.

### **chip-erase command**

Chip erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the chip-erase command. This command sequence is required to ensure that the memory contents are not erased accidentally. The rising edge of  $\overline{WE}$  starts the chip-erase operation. Any further commands written to the device during the chip-erase operation are ignored.

The embedded chip-erase function automatically provides voltage and timing needed to program and to verify all the memory cells prior to electrical erase. It then erases and verifies the cell margin automatically without programming the memory cells prior to erase.

Figure 12 shows a flowchart of the typical chip-erase operation.

### **sector-erase command**

Sector-erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode and then the sixth bus cycle loads the sector-erase command and the sector-address location to be erased. Any address location within the desired sector can be used. The addresses are latched on the falling edge of  $\overline{WE}$  and the sector-erase command (30h) is latched on the rising edge of  $\overline{WE}$  in the sixth bus cycle. After a delay of 80  $\mu$ s from the rising edge of  $\overline{WE}$ , the sector-erase operation begins on the selected sector(s).

Additional sectors can be selected to be erased concurrently during the sector-erase command sequence. For each additional sector to be selected for erase, another bus cycle is issued. The bus cycle loads the next sector-address location and the sector-erase command. The time between the end of the previous bus cycle and the start of the next bus cycle must be less than 100  $\mu$ s; otherwise, the new sector location is not loaded. A time delay of 100  $\mu$ s from the rising edge of the last  $\overline{WE}$  starts the sector-erase operation. If there is a falling edge of  $\overline{WE}$  within the 100  $\mu$ s time delay, the timer is reset.

### sector-erase command (continued)

One to nineteen sector-address locations can be loaded in any sequence. The state of the delay timer can be monitored using the sector-erase delay indicator (DQ3). If DQ3 is at logic low, the time delay has not expired. See the operation status section for a description.

Any command other than erase suspend (B0h) or sector erase (30h) written to the device during the sector-erase operation causes the device to exit the sector-erase mode and the contents of the sector(s) selected for erase are no longer valid. To complete the sector-erase operation, reissue the sector-erase command sequence.

The embedded sector-erase function automatically provides needed voltage and timing to program and to verify all of the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. Programming the memory cells prior to erase is not required.

See the operation status section for a full description. Figure 14 shows a flowchart of the typical sector-erase operation.

### erase-suspend command

The erase-suspend command (B0h) allows interruption of a sector-erase operation to read data from unaltered sectors of the device. Erase-suspend is a one-bus-cycle command. The addresses can be  $V_{IL}$  or  $V_{IH}$  and the erase-suspend command (B0h) is latched on the rising edge of  $\overline{WE}$ . Once the sector-erase operation is in progress, the erase-suspend command requests the internal write-state machine to halt operation at predetermined breakpoints. The erase-suspend command is valid only during the sector-erase operation and is invalid during programming and chip-erase operations. The sector-erase delay timer expires immediately if the erase-suspend command is issued while the delay is active.

After the erase-suspend command is issued, the device takes between 0.1  $\mu$ s and 15  $\mu$ s to suspend the operation. The toggle bit must be monitored to determine when the suspend has been executed. When the toggle bit stops toggling, data can be read from sectors that are not selected for erase. Reading from a sector selected for erase can result in invalid data. See the operation status section for a full description.

Once the sector-erase operation is suspended, reading from or programming to a sector that is not being erased can be performed. This command is applicable only during sector-erase operation. Any other command written during erase-suspend mode to the suspended sector is ignored.

### erase-resume command

The erase-resume command (30h) restarts a suspended sector-erase operation from the point where it was halted. Erase resume is a one-bus-cycle command. The addresses can be  $V_{IL}$  or  $V_{IH}$  and the erase-resume command (30h) is latched on the rising edge of  $\overline{WE}$ . When an erase-suspend/erase-resume command combination is written, the internal-pulse counter (exceed timing limit) is reset. The erase-resume command is valid only in the erase-suspend state. After the erase-resume command is executed, the device returns to the valid sector-erase state and further writes of the erase-resume command are ignored. After the device has resumed the sector-erase operation, another erase-suspend command can be issued to the device.

### operation status

The status of the device during an automatic-programming algorithm, chip-erase, or automatic-erase algorithm can be determined in three ways:

- DQ7: Data polling
- DQ6: Toggle bit
- $\overline{RY}/\overline{BY}$ : Ready/busy bit



# TMS29LF800T, TMS29LF800B

## 1048576 BY 8-BIT/524288 BY 16-BIT

### FLASH MEMORIES

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

#### status-bit definitions

During operation of the automatic embedded program and erase functions, the status of the device can be determined by reading the data state of designated outputs. The data-polling bit (DQ7) and toggle bit (DQ6) require multiple successive reads to observe a change in the state of the designated output. Table 7 defines the values of the status flags.

**Table 7. Operation Status Flags†**

|                               | DEVICE OPERATION‡           | DQ7                      | DQ6                               | DQ5    | DQ3 | DQ2    | RY/BY  |   |
|-------------------------------|-----------------------------|--------------------------|-----------------------------------|--------|-----|--------|--------|---|
| In progress                   | Programming                 | $\overline{\text{DQ7}}$  | T                                 | 0      | 0   | No Tog | 0      |   |
|                               | Program/erase in auto-erase |                          | 0                                 | T      | 0   | 1      | §      | 0 |
|                               | Erase-suspend mode          | Erase-sector address     | 1                                 | No Tog | 0   | 0      | T      | 1 |
|                               |                             | Non-erase sector address | D                                 | D      | D   | D      | D      | 1 |
|                               | Program in erase suspend    |                          | $\overline{\text{DQ7}}^{\dagger}$ | T      | 0   | 0      | 1§     | 0 |
| Exceeded time limits          | Programming                 | $\overline{\text{DQ7}}$  | T                                 | 1      | 0   | No Tog | 0      |   |
|                               | Program/erase in auto erase |                          | 0                                 | T      | 1   | 1      | #      | 0 |
|                               | Program in erase suspend    |                          | $\overline{\text{DQ7}}$           | T      | 1   | 0      | No Tog | 0 |
| Successful operation complete | Programming complete        | D                        | D                                 | D      | D   | D      | 1      |   |
|                               | Sector-/chip-erase complete |                          | 1                                 | 1      | 1   | 1      | 1      | 1 |

† T = toggle, D = data, No Tog = No toggle

‡ DQ4, DQ1, DQ0 are reserved for future use.

§ DQ2 can be toggled when the sector address applied is an erasing sector. DQ2 cannot be toggled when the sector address applied is a non-erasing sector. DQ2 is used to determine which sectors are erasing and which are not.

¶ Status flags apply when outputs are read from the address of a non-erase-suspend operation.

# If DQ5 is high (exceeded timing limits), successive reads from a problem sector causes DQ2 to toggle.

#### data-polling (DQ7)

The data-polling-status function outputs the complement of the data latched into the DQ7 data register while the write-state machine (WSM) is engaged in a program or erase operation. Data bit DQ7 toggling from complement to true indicates the end of an operation. Data-polling is available only during programming, chip-erase, sector-erase, and sector-erase-timing delay. Data-polling is valid after the rising edge of  $\overline{\text{WE}}$  in the last bus cycle of the command sequence loaded into the command register. Figure 16 shows a flowchart for data-polling.

During a program operation, reading DQ7 outputs the complement of the DQ7 data to be programmed at the selected address location. Upon completion, reading DQ7 outputs the true DQ7 data loaded into the program-data register. During erase operations, reading DQ7 outputs a logic low. Upon completion, reading DQ7 outputs a logic high. Also, data-polling must be performed at a sector address that is within a sector that is being erased; otherwise, the status is invalid. When using data-polling, the address should remain stable throughout the operation.

During a data-polling read, while  $\overline{\text{OE}}$  is logic low, data bit DQ7 can change asynchronously. Depending on the read timing, the system can read valid data on DQ7, while other DQ pins are still invalid. A subsequent read of the device is valid. See Figure 17 for the data-polling timing diagram.

#### toggle bit (DQ6)

The toggle-bit status function outputs data on DQ6, which toggles between logic high and logic low while the WSM is engaged in a program or erase operation. When DQ6 stops toggling after two consecutive reads to the same address, the operation is complete. The toggle bit is available only during programming, chip erase, sector erase, and sector-erase-timing delay. Toggle-bit data is valid after the rising edge of  $\overline{\text{WE}}$  in the last bus cycle of the command sequence loaded into the command register. Figure 18 shows a flowchart of the toggle-bit status-read algorithm. Depending on the read timing, DQ6 can stop toggling while other DQ pins are still invalid and a subsequent read of the device is valid. See Figure 19 for the toggle-bit timing diagram.





### exceed time limit (DQ5)

Program and erase operations use an internal-pulse counter to limit the number of pulses applied. If the pulse-count limit is exceeded, DQ5 is set to a logic-high data state. This indicates that the program or erase operation has failed. DQ7 does not change from complemented data to true data and DQ6 does not stop toggling when read. To continue operation, the device must be reset.

The exceed-time-limit condition occurs when attempting to program a logic-high state into a bit that has been programmed previously to a logic low. Only an erase operation can change bits from logic low to logic high. After reset, the device is functional and can be erased and reprogrammed.

### sector-load-timer (DQ3)

The sector-load-timer status bit, DQ3, is used to determine whether the time to load additional sector addresses has expired. After completion of a sector-erase command sequence, DQ3 remains at a logic low for 100  $\mu$ s. This indicates that another sector-erase command sequence can be issued. If DQ3 is at a logic high, it indicates that the delay has expired and attempts to issue additional sector-erase commands are ignored. See the sector-erase command section for a description.

The data-polling and toggle bit are valid during the 100- $\mu$ s time delay and can be used to determine if a valid sector-erase command has been issued. To ensure additional sector-erase commands have been accepted, the status of DQ3 should be read before and after each additional sector-erase command. If DQ3 is at a logic low on both reads, the additional sector-erase command was accepted.

### toggle bit 2 (DQ2)

The state of DQ2 determines whether the device is in algorithmic-erase mode or erase-suspend mode. DQ2 toggles if successive reads are issued to the erasing or erase-suspended sector, assuming in case of the latter that the device is in erase-suspend-read mode. DQ2 also toggles when DQ5 becomes a logic high due to the timer exceeding the time limit, and reads are issued to the failed sector. DQ2 does not toggle in any other sector due to DQ5 failure. When the device is in erase-suspend-program mode, successive reads from the non-erase-suspended sector causes a logic high on DQ2.

### ready/busy bit (RY/ $\overline{\text{BY}}$ )

The RY/ $\overline{\text{BY}}$  bit indicates when the device can accept new commands after performing algorithmic operations. If the RY/ $\overline{\text{BY}}$  (open-drain output) bit is low, the device is busy with either a program or erase operation and does not accept any other commands except for erase suspend. While it is in the erase-suspend mode, RY/ $\overline{\text{BY}}$  remains high. In program mode, the RY/ $\overline{\text{BY}}$  bit is valid (logic low) after the fourth  $\overline{\text{WE}}$  pulse. In erase mode, it is valid after the sixth  $\overline{\text{WE}}$  pulse. After a delay period,  $t_{\text{busy}}$ , the RY/ $\overline{\text{BY}}$  bit becomes valid. See Figure 28 for the timing waveform.

Since the RY/ $\overline{\text{BY}}$  bit is an open-drain output, several such bits can be combined in parallel with a pullup resistor to  $V_{\text{CC}}$ .

### hardware-reset bit ( $\overline{\text{RESET}}$ )

When the  $\overline{\text{RESET}}$  pin is driven to a logic low, it forces the device out of the currently active mode and into a reset state. It also avoids bus contention by placing the outputs into the high-impedance state for the duration of the  $\overline{\text{RESET}}$  pulse.

During a program or erase operation, if  $\overline{\text{RESET}}$  is asserted to logic low, the RY/ $\overline{\text{BY}}$  bit remains at logic low until the reset operation is complete. Since this can take from 1  $\mu$ s to 20  $\mu$ s, the RY/ $\overline{\text{BY}}$  bit can be used to sense reset completion or the user can allow a maximum of 20  $\mu$ s. If  $\overline{\text{RESET}}$  is asserted during read mode, then the reset operation is complete within 500 ns. See Figure 1 and Figure 2 for timing specifications.

The  $\overline{\text{RESET}}$  pin can also be used to drive the device into deep power-down (standby) mode by applying  $V_{\text{SS}} \pm 0.3$  V to it.  $I_{\text{CC4}}$  reads  $<1$   $\mu$ A typical, and 5  $\mu$ A maximum for CMOS inputs. Standby mode can be entered anytime, regardless of the condition of  $\overline{\text{CE}}$ .

TMS29LF800T, TMS29LF800B  
1048576 BY 8-BIT/524288 BY 16-BIT  
FLASH MEMORIES

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

hardware-reset bit ( $\overline{\text{RESET}}$ ) (continued)

Asserting  $\overline{\text{RESET}}$  during program or erase can leave erroneous data in the address locations. These locations need to be updated after the device resumes normal operations. A minimum of 50 ns must be allowed after  $\overline{\text{RESET}}$  goes high before a valid read can take place.

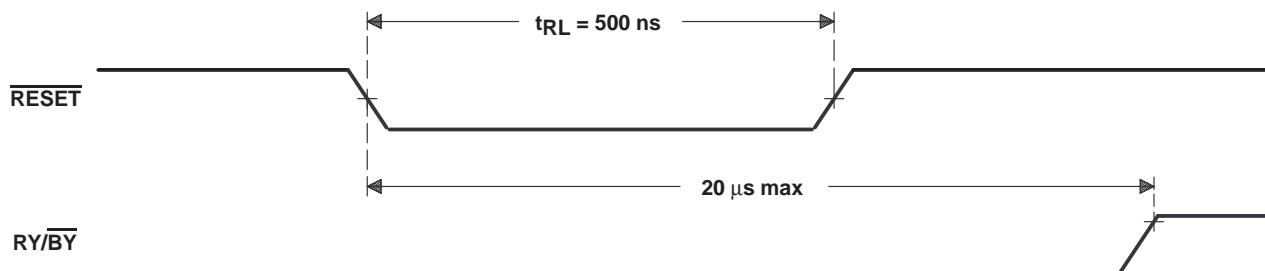


Figure 1. Device Reset During a Program or Erase Operation

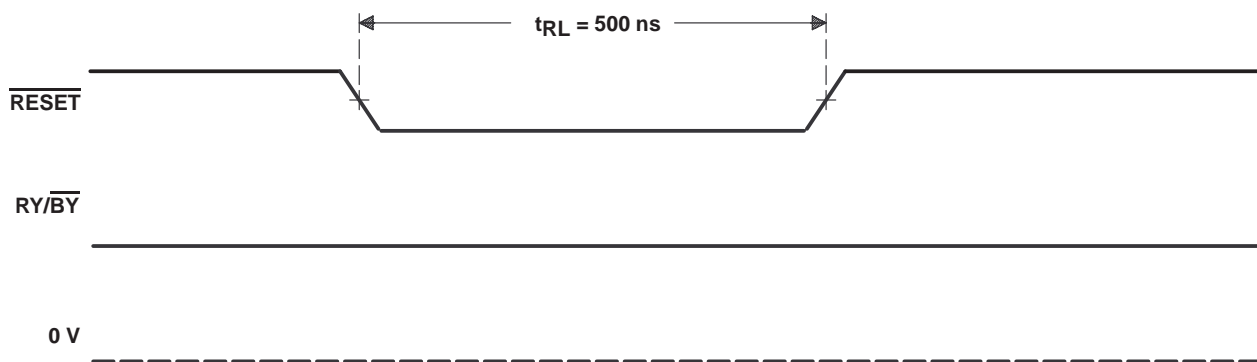


Figure 2. Device Reset During Read Mode

## word-/byte-mode configuration

The  $\overline{\text{BYTE}}$  pin is used to set the device configuration. If  $\overline{\text{BYTE}}$  is at a logic 1, the device is in word mode with all data outputs valid and the DQ15/A<sub>1</sub> output representing DQ15. Similarly, if  $\overline{\text{BYTE}}$  is at a logic 0, the device is in byte mode with only DQ0–DQ7 valid. The remaining outputs are in high-impedance mode and DQ15/A<sub>1</sub> is used as an input for the least significant bit (A<sub>1</sub>) address function. See Figure 3 and Figure 4 for timing specifications.

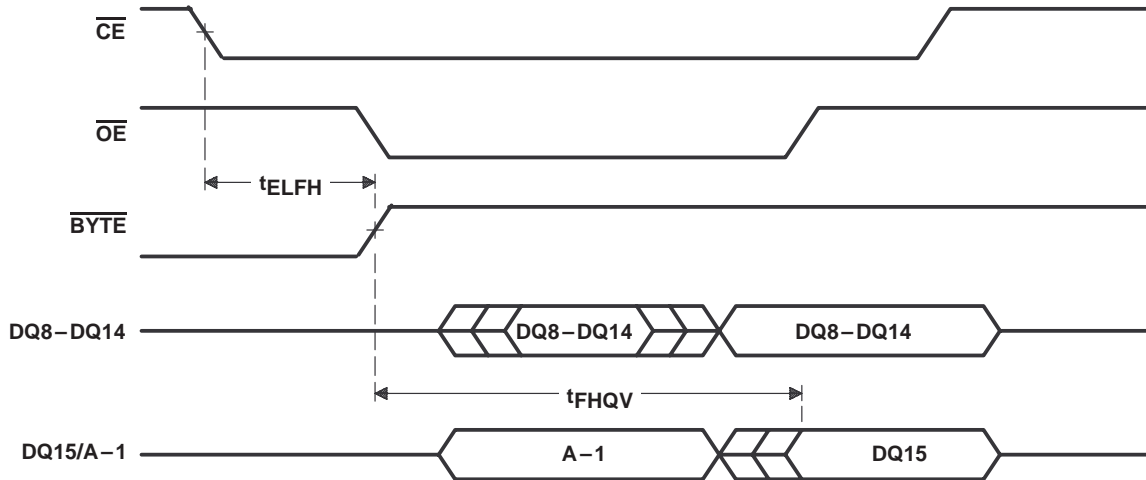


Figure 3. Word-Mode Configuration

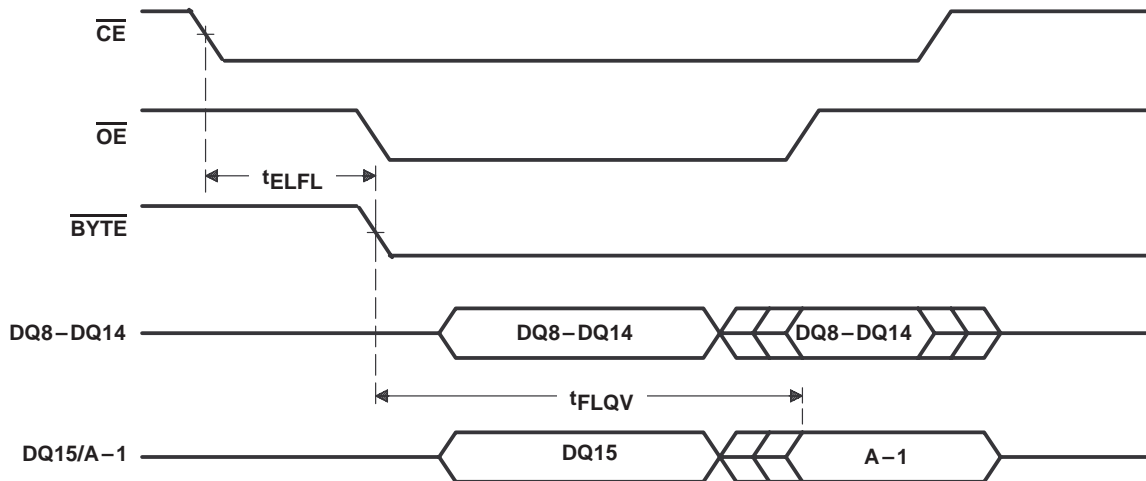


Figure 4. Byte-Mode Configuration

## temporary hardware-sector unprotect feature

This feature temporarily enables both programming and erase operations on any combination of one to nineteen sectors that were previously protected. The unprotect feature is enabled using high voltage  $V_{\text{ID}}$  (11.5 V to 12.5 V) on the RESET pin, using standard command sequences.

Normally, the device is delivered with all sectors unprotected.

## sector-protect programming

The sector-protect programming mode is activated when A6, A0, and  $\overline{\text{CE}}$  are at  $V_{\text{IL}}$ , and address pin A9 and control pin  $\overline{\text{OE}}$  are forced to  $V_{\text{ID}}$ . Address pin A1 is set to  $V_{\text{IH}}$ . The sector-select address pins A12–A18 are used to select the sector to be protected. Address pins A0–A11 and I/O pins must be stable and can be either  $V_{\text{IL}}$  or  $V_{\text{IH}}$ . Once the addresses are stable,  $\overline{\text{WE}}$  is pulsed low for 100  $\mu\text{s}$ , causing programming to begin on the falling edge of  $\overline{\text{WE}}$  and to terminate on the rising edge of  $\overline{\text{WE}}$ . Figure 20 is a flowchart of the sector-protect algorithm and Figure 21 shows a timing diagram of the sector-protect operation.

Commands to program or erase a protected sector do not change the data contained in the sector. Attempts to program and erase a protected sector cause the data-polling bit (DQ7), and the toggle bit (DQ6) to operate from 2  $\mu\text{s}$  to 100  $\mu\text{s}$  and then return to valid data.

## sector-protect verify

Verification of sector-protection programming is accomplished when  $\overline{\text{WE}} = V_{\text{IH}}$ ,  $\overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ , and address pin A9 =  $V_{\text{ID}}$ , and then address pins A0 and A6 are set to  $V_{\text{IL}}$  and A1 is set to  $V_{\text{IH}}$ . Sector-address pins A12–A18 select the sector that is to be verified. The other addresses can be  $V_{\text{IH}}$  or  $V_{\text{IL}}$ . If the selected sector is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h.

Sector-protect verify can also be read using the algorithm-selection command. After issuing the three-bus-cycle command sequence, the sector-protection status can be read on DQ0. Set address pins A0 =  $V_{\text{IL}}$ , A1 =  $V_{\text{IH}}$ , and A6 =  $V_{\text{IL}}$ , and then sector address pins A12–A18 select the sector to be verified. The remaining addresses are set to  $V_{\text{IL}}$ . If the sector selected is protected, DQ0 outputs a logic-high state. If the sector selected is not protected, DQ0 outputs a logic-low state. This mode remains in effect until another valid command sequence is written to the device. Figure 20 is a flowchart of the sector-protect algorithm and Figure 21 shows a timing diagram of the sector-protect operation.

## sector unprotect

Prior to sector unprotect, all sectors must be protected using the sector-protect programming mode. Sector unprotect is activated when address pin A9 and control pin  $\overline{\text{OE}}$  are forced to  $V_{\text{ID}}$ . Address pins A1 and A6 are set to  $V_{\text{IH}}$  while  $\overline{\text{CE}}$  and A0 are set to  $V_{\text{IL}}$ . The sector-select address pins A12–A18 can be  $V_{\text{IL}}$  or  $V_{\text{IH}}$ . All sectors are unprotected in parallel and once the inputs are stable,  $\overline{\text{WE}}$  is pulsed low for 10 ms, causing the unprotect operation to begin on the falling edge of  $\overline{\text{WE}}$  and to terminate on the rising edge of  $\overline{\text{WE}}$ . Figure 22 is a flowchart of the sector-unprotect algorithm and Figure 23 shows a timing diagram of the sector-unprotect operation.

## sector-unprotect verify

Verification of sector unprotect is accomplished when  $\overline{\text{WE}} = V_{\text{IH}}$ ,  $\overline{\text{OE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ , and A9 =  $V_{\text{ID}}$ , and then select the sector to be verified. Address pins A1 and A6 are set to  $V_{\text{IH}}$ , and A0 is set to  $V_{\text{IL}}$ . The other addresses can be  $V_{\text{IH}}$  or  $V_{\text{IL}}$ . If the sector selected is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h. Sector unprotect can also be read using the algorithm-selection command.

## low $V_{\text{CC}}$ write lockout

During power-up and power-down operations, write cycles are locked out for  $V_{\text{CC}}$  less than  $V_{\text{LKO}}$ . If  $V_{\text{CC}} < V_{\text{LKO}}$ , the command input is disabled and the device is reset to the read mode. On power up, if  $\overline{\text{CE}} = V_{\text{IL}}$ ,  $\overline{\text{WE}} = V_{\text{IL}}$ , and  $\overline{\text{OE}} = V_{\text{IH}}$ , the device does not accept commands on the rising edge of  $\overline{\text{WE}}$ . The device automatically powers up in the read mode.

## glitching

Pulses of less than 5 ns (typical) on  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$ , or  $\overline{\text{CE}}$  do not issue a write cycle.

## power supply considerations

Each device should have a 0.1- $\mu\text{F}$  ceramic capacitor connected between  $V_{\text{CC}}$  and  $V_{\text{SS}}$  to suppress circuit noise. Printed circuit traces to  $V_{\text{CC}}$  should be appropriate to handle the current demand and minimize inductance.

**absolute maximum ratings over ambient temperature range (unless otherwise noted)†**

|   |                          |
|---|--------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1)   | –0.6 V to 7 V            |
| Input voltage range: All inputs except A9, $\overline{CE}$ , $\overline{OE}$ (see Note 2) | –0.6 V to $V_{CC} + 1$ V |
| A9, $\overline{CE}$ , $\overline{OE}$   | –0.6 V to 13.5 V         |
| Output voltage range (see Note 3)   | –0.6 V to $V_{CC} + 1$ V |
| Ambient temperature range during read/erase/program, $T_A$                                |                          |
| (L)   | 0°C to 70°C              |
| (E)   | –40°C to 85°C            |
| (Q)   | –40°C to 125°C           |
| Storage temperature range, $T_{stg}$  | –65°C to 150°C           |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to  $V_{SS}$ .  
2. The voltage on any input pin can undershoot to –2 V for periods less than 20 ns (see Figure 6).  
3. The voltage on any input or output pin can overshoot to 7 V for periods less than 20 ns (see Figure 7).

**recommended operating conditions**

|           |  | MIN       | MAX          | UNIT         |
|-----------|--|-----------|--------------|--------------|
| $V_{CC}$  | Supply voltage                                       | 2.7       | 3.6          | V            |
| $V_{IH}$  | High-level dc input voltage                          | TTL       | 2            | $V_{CC}+0.5$ |
|           |  | CMOS      | $V_{CC}-0.5$ | $V_{CC}+0.5$ |
| $V_{IL}$  | Low-level dc input voltage                           | TTL       | –0.5         | 0.8          |
|           |  | CMOS      | –0.5         | 0.8          |
| $V_{ID}$  | Algorithm selection and sector-protect input voltage | 11.5      | 12.5         | V            |
| $V_{LKO}$ | Low $V_{CC}$ lock-out voltage                        | 2.3       | 2.5          | V            |
| $T_A$     | Ambient temperature                                  | L version | 0            | 70           |
|           |  | E version | –40          | 85           |
|           |  | Q version | –40          | 125          |

**PRODUCT PREVIEW**

**TMS29LF800T, TMS29LF800B**  
**1048576 BY 8-BIT/524288 BY 16-BIT**  
**FLASH MEMORIES**

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

**electrical characteristics over recommended ranges of supply voltage and ambient temperature**

| PARAMETER        |   |   | TEST CONDITIONS   | MIN                  | MAX | UNIT |
|------------------|---|---|---|----------------------|-----|------|
| V <sub>OH</sub>  | High-level output voltage                             | TTL-input level   | V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OH</sub> = −2.0 mA                      | 0.85*V <sub>CC</sub> |     | V    |
|                  |   | CMOS-input level  | V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OH</sub> = − 100 μA                     | V <sub>CC</sub> −0.4 |     |      |
| V <sub>OL</sub>  | Low-level output voltage                              | V <sub>CC</sub> = V <sub>CC</sub> MIN, I <sub>OL</sub> = 5.8 mA                               |   | 0.45                 |     | V    |
| I <sub>I</sub>   | Input current (leakage)                               | V <sub>CC</sub> = V <sub>CC</sub> MAX, V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>   |   | ±1                   |     | μA   |
| I <sub>O</sub>   | Output current (leakage)                              | V <sub>O</sub> =V <sub>SS</sub> to V <sub>CC</sub> , $\overline{\text{CE}}$ = V <sub>IH</sub> |   | ±1                   |     | μA   |
| I <sub>ID</sub>  | High-voltage current (standby)                        | A9 or $\overline{\text{CE}}$ or $\overline{\text{OE}}$ = V <sub>ID</sub> MAX                  |   | 35                   |     | μA   |
| I <sub>CC1</sub> | V <sub>CC</sub> supply current (standby)              | TTL-input level   | $\overline{\text{CE}}$ = V <sub>IH</sub> , V <sub>CC</sub> = V <sub>CC</sub> MAX      | 1                    |     | mA   |
|                  |   | CMOS-input level  | $\overline{\text{CE}}$ = V <sub>CC</sub> ± 0.2, V <sub>CC</sub> = V <sub>CC</sub> MAX | 60                   |     |      |
| I <sub>CC2</sub> | V <sub>CC</sub> supply current (see Notes 4 and 5)    | Byte  | $\overline{\text{CE}}$ = V <sub>IL</sub> , $\overline{\text{OE}}$ = V <sub>IH</sub>   | 30                   |     | mA   |
|                  |   | Word  |   | 35                   |     |      |
| I <sub>CC3</sub> | V <sub>CC</sub> supply current (see Note 6)           | $\overline{\text{CE}}$ = V <sub>IL</sub> , $\overline{\text{OE}}$ = V <sub>IH</sub>           |   | 60                   |     | mA   |
| I <sub>CC4</sub> | V <sub>CC</sub> supply current (standby during reset) | V <sub>CC</sub> = V <sub>CC</sub> MAX, RESET = V <sub>SS</sub> ± 0.3 V                        |   | 5                    |     | μA   |
| I <sub>CC5</sub> | Automatic sleep mode (see Notes 5 and 7)              | V <sub>IH</sub> = V <sub>CC</sub> ± 0.3 V, V <sub>IL</sub> = V <sub>SS</sub> ± 0.3 V          |   | 60                   |     | μA   |

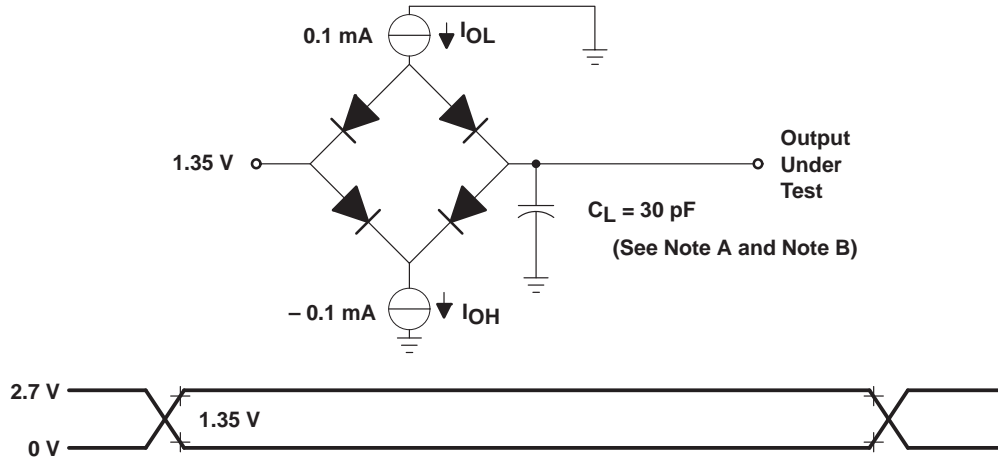
NOTES: 4. I<sub>CC</sub> current in the read mode, switching at 6 MHz  
5. I<sub>OUT</sub> = 0 mA  
6. I<sub>CC</sub> current while erase or program operation is in progress  
7. Automatic sleep mode is entered when addresses remain stable for 300 ns.

**capacitance over recommended ranges of supply voltage and ambient temperature**

| PARAMETER       |  | TEST CONDITIONS                 | MIN | MAX | UNIT |
|-----------------|--|---------------------------------|-----|-----|------|
| C <sub>i1</sub> | Input capacitance (All inputs except A9, $\overline{\text{CE}}$ , $\overline{\text{OE}}$ ) | V <sub>I</sub> = 0 V, f = 1 MHz | 7.5 |     | pF   |
| C <sub>i2</sub> | Input capacitance (A9, $\overline{\text{CE}}$ , $\overline{\text{OE}}$ )                   | V <sub>I</sub> = 0 V, f = 1 MHz | 9   |     | pF   |
| C <sub>O</sub>  | Output capacitance   | V <sub>O</sub> = 0 V, f = 1 MHz | 12  |     | pF   |



## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and fixture capacitance.  
B. The ac testing inputs are driven at 2.7 V for logic high and 0 V for logic low. Timing measurements are made at 1.35 V for logic high and 1.35 V for logic low on both inputs and outputs. Each device should have a 0.1- $\mu$ F ceramic capacitor connected between  $V_{CC}$  and  $V_{SS}$  as closely as possible to the device pins.

Figure 5. AC Test Output Load Circuit

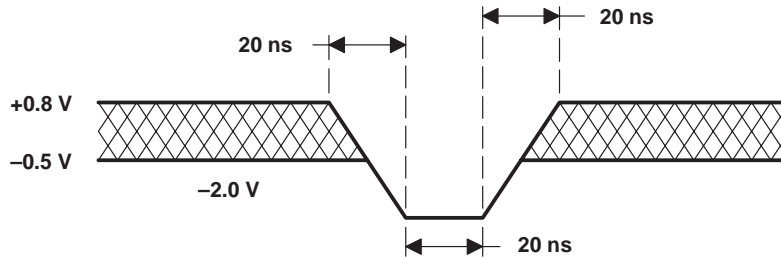


Figure 6. Maximum Negative Overshoot Waveform

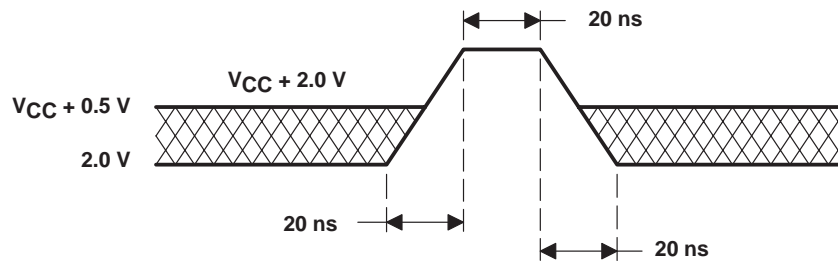


Figure 7. Maximum Positive Overshoot Waveform

TMS29LF800T, TMS29LF800B  
1048576 BY 8-BIT/524288 BY 16-BIT  
FLASH MEMORIES

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

PARAMETER MEASUREMENT INFORMATION

switching characteristics over recommended ranges of supply voltage and ambient temperature,  
read-only operation

| PARAMETER   | ALTERNATE SYMBOL  | '29LF800-90 |     | '29LF800-100 |     | '29LF800-120 |     | UNIT |
|---|-------------------|-------------|-----|--------------|-----|--------------|-----|------|
|   |                   | MIN         | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>c</sub> (R) Cycle time, read   | t <sub>AVAV</sub> | 90          |     | 100          |     | 120          |     | ns   |
| t <sub>a</sub> (A) Access time, address   | t <sub>AVQV</sub> | 90          |     | 100          |     | 120          |     | ns   |
| t <sub>a</sub> (E) Access time, $\overline{\text{CE}}$  | t <sub>ELQV</sub> | 90          |     | 100          |     | 120          |     | ns   |
| t <sub>a</sub> (G) Access time, $\overline{\text{OE}}$  | t <sub>GLQV</sub> | 40          |     | 50           |     | 55           |     | ns   |
| t <sub>dis</sub> (E) Disable time, $\overline{\text{CE}}$ to high impedance                               | t <sub>EHQZ</sub> | 30          |     | 30           |     | 40           |     | ns   |
| t <sub>dis</sub> (G) Disable time, $\overline{\text{OE}}$ to high impedance                               | t <sub>GHQZ</sub> | 30          |     | 30           |     | 40           |     | ns   |
| t <sub>en</sub> (E) Enable time, $\overline{\text{CE}}$ to low impedance                                  | t <sub>ELQX</sub> | 0           |     | 0            |     | 0            |     | ns   |
| t <sub>en</sub> (G) Enable time, $\overline{\text{OE}}$ to low impedance                                  | t <sub>GLQX</sub> | 0           |     | 0            |     | 0            |     | ns   |
| t <sub>h</sub> (D) Hold time, output from address $\overline{\text{CE}}$ or $\overline{\text{OE}}$ change | t <sub>AXQX</sub> | 0           |     | 0            |     | 0            |     | ns   |
| t <sub>READY</sub>  |                   |             |     | 20           |     | 20           |     | μs   |



**switching characteristics over recommended ranges of supply voltage and ambient temperature, controlled by  $\overline{WE}$** 

| PARAMETER    |   | ALTERNATE<br>SYMBOL | '29LF800-90 |     |     | '29LF800-100 |     |     | '29LF800-120 |     |     | UNIT    |
|--------------|---|---------------------|-------------|-----|-----|--------------|-----|-----|--------------|-----|-----|---------|
|              |   |                     | MIN         | TYP | MAX | MIN          | TYP | MAX | MIN          | TYP | MAX |         |
| $t_{c(W)}$   | Cycle time, write   | $t_{AVAV}$          | 90          |     |     | 100          |     |     | 120          |     |     | ns      |
| $t_{su(A)}$  | Setup time, address   | $t_{AVWL}$          | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{h(A)}$   | Hold time, address  | $t_{WLAX}$          | 50          |     |     | 50           |     |     | 65           |     |     | ns      |
| $t_{su(D)}$  | Setup time, data  | $t_{DVWH}$          | 50          |     |     | 50           |     |     | 65           |     |     | ns      |
| $t_{h(D)}$   | Hold time, data valid after $\overline{WE}$ high                            | $t_{WHDX}$          | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{su(E)}$  | Setup time, $\overline{CE}$   | $t_{ELWL}$          | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{h(E)}$   | Hold time, $\overline{CE}$  | $t_{WHEH}$          | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{w(WL)}$  | Pulse duration, $\overline{WE}$ low   | $t_{WLWH1}$         | 50          |     |     | 50           |     |     | 65           |     |     | ns      |
| $t_{w(WH)}$  | Pulse duration, $\overline{WE}$ high  | $t_{WHWL}$          | 30          |     |     | 30           |     |     | 35           |     |     | ns      |
| $t_{rec(R)}$ | Recovery time, read before write  | $t_{GHWL}$          | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
|              | Hold time, $\overline{OE}$ read   | $t_{WHGL1}$         | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
|              | Hold time, $\overline{OE}$ toggle, data                                     | $t_{WHGL2}$         | 10          |     |     | 10           |     |     | 10           |     |     | ns      |
|              | Setup time, $V_{CC}$  | $t_{VCEL}$          | 50          |     |     | 50           |     |     | 50           |     |     | $\mu s$ |
|              | Transition time, $V_{ID}$ (see Notes 8 and 9)                               | $t_{HVT}$           | 4           |     |     | 4            |     |     | 4            |     |     | $\mu s$ |
|              | Pulse duration, $\overline{WE}$ low (see Note 8)                            | $t_{WLWH2}$         | 100         |     |     | 100          |     |     | 100          |     |     | $\mu s$ |
|              | Pulse duration, $\overline{WE}$ low (see Note 9)                            | $t_{WLWH3}$         | 10          |     |     | 10           |     |     | 10           |     |     | ms      |
|              | Setup time, $\overline{CE}$ $V_{ID}$ to $\overline{WE}$ (see Note 9)        | $t_{EHVWL}$         | 4           |     |     | 4            |     |     | 4            |     |     | $\mu s$ |
|              | Setup time, $\overline{CE}$ $V_{ID}$ to $\overline{WE}$ (see Notes 8 and 9) | $t_{GHVWL}$         | 4           |     |     | 4            |     |     | 4            |     |     | $\mu s$ |
| $t_{c(W)PR}$ | Cycle time, programming operation   | $t_{WHWH1}$         | 8           |     |     | 8            |     |     | 8            |     |     | $\mu s$ |
|              |   |                     | 14          |     |     | 14           |     |     | 14           |     |     | $\mu s$ |
|              | Write recovery time from $RY/\overline{BY}$                                 | $t_{RB}$            | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
|              | $\overline{RESET}$ low time   | $t_{RL}$            | 500         |     |     | 500          |     |     | 500          |     |     | ns      |
|              | $\overline{RESET}$ high time before read                                    | $t_{RH}$            | 50          |     |     | 50           |     |     | 50           |     |     | ns      |
|              | $\overline{RESET}$ to power-down time                                       | $t_{RPD}$           | 20          |     |     | 20           |     |     | 20           |     |     | $\mu s$ |
|              | $\overline{RESET}$ to $\overline{CE}/\overline{WE}$ low                     | $t_{VLHT}$          | 4           |     |     | 4            |     |     | 4            |     |     | $\mu s$ |
|              | Program/erase valid to $RY/\overline{BY}$ delay                             | $t_{BUSY}$          | 90          |     |     | 90           |     |     | 90           |     |     | ns      |
|              | $\overline{CE}$ to $\overline{BYTE}$ switching low or high                  | $t_{ELFL}/t_{ELFH}$ | 5           |     |     | 5            |     |     | 5            |     |     | ns      |
|              | $\overline{BYTE}$ switching low to output 3-state                           | $t_{FLQZ}$          | 30          |     |     | 40           |     |     | 40           |     |     | ns      |
|              | $\overline{BYTE}$ switching high to output active                           | $t_{FHQV}$          | 30          |     |     | 40           |     |     | 40           |     |     | ns      |
| $t_{c(W)ER}$ | Cycle time, sector-erase operation  | $t_{WHWH2}$         | 1           |     |     | 1            |     |     | 1            |     |     | s       |
|              | Cycle time, chip-erase operation  | $t_{WHWH3}$         | 6           | 50  |     | 6            | 50  |     | 6            | 50  |     | s       |

NOTES: 8. Sector-protect timing  
9. Sector-unprotect timing

TMS29LF800T, TMS29LF800B

1048576 BY 8-BIT/524288 BY 16-BIT

FLASH MEMORIES

SMUS828B - SEPTEMBER 1996 - REVISED OCTOBER 1997

## PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and ambient temperature, controlled by  $\overline{CE}$ 

| PARAMETER   |   | ALTERNATE SYMBOL | '29LF800-90 |     |     | '29LF800-100 |     |     | '29LF800-120 |     |     | UNIT    |
|---|---|------------------|-------------|-----|-----|--------------|-----|-----|--------------|-----|-----|---------|
|   |   |                  | MIN         | TYP | MAX | MIN          | TYP | MAX | MIN          | TYP | MAX |         |
| $t_{c(W)}$  | Cycle time, write                       | $t_{AVAV}$       | 90          |     |     | 100          |     |     | 120          |     |     | ns      |
| $t_{su(A)}$                                       | Setup time, address                     | $t_{AVEL}$       | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{h(A)}$  | Hold time, address                      | $t_{ELAX}$       | 50          |     |     | 50           |     |     | 65           |     |     | ns      |
| $t_{su(D)}$                                       | Setup time, data                        | $t_{DVEH}$       | 50          |     |     | 50           |     |     | 65           |     |     | ns      |
| $t_{h(D)}$  | Hold time, data                         | $t_{EHDX}$       | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{su(W)}$                                       | Setup time, $\overline{WE}$             | $t_{WLEL}$       | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{h(W)}$  | Hold time, $\overline{WE}$              | $t_{EHWH}$       | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{w(EL)}$                                       | Pulse duration, $\overline{CE}$ low     | $t_{ELEH1}$      | 50          |     |     | 50           |     |     | 65           |     |     | ns      |
| $t_{w(EH)}$                                       | Pulse duration, $\overline{CE}$ high    | $t_{EHEL}$       | 30          |     |     | 30           |     |     | 35           |     |     | ns      |
| $t_{rec(R)}$                                      | Recovery time, read before write        | $t_{GHLEL}$      | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
|   | Setup time, $\overline{OE}$             | $t_{GLEL}$       | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
| $t_{h(C)}$  | Hold time, $\overline{OE}$ read         | $t_{EHGL1}$      | 0           |     |     | 0            |     |     | 0            |     |     | ns      |
|   | Hold time, $\overline{OE}$ toggle, data | $t_{EHGL2}$      | 10          |     |     | 10           |     |     | 10           |     |     | ns      |
| Programming operation                             |   | Byte             | 8           |     |     | 8            |     |     | 8            |     |     | $\mu s$ |
|   |   | Word             | 14          |     |     | 14           |     |     | 14           |     |     | $\mu s$ |
| Cycle time, sector-erase operation                |   | $t_{EHEH2}$      | 1           |     |     | 1            |     |     | 1            |     |     | s       |
| Cycle time, chip-erase operation                  |   | $t_{EHEH3}$      | 6 50        |     |     | 6 50         |     |     | 6 50         |     |     | s       |
| $\overline{BYTE}$ switching low to output 3-state |   | $t_{FLQZ}$       | 30          |     |     | 40           |     |     | 40           |     |     | ns      |

## erase and program performance†

| PARAMETER             | TEST CONDITIONS                           | MIN     | TYP       | MAX   | UNIT   |
|-----------------------|---|---------|-----------|-------|--------|
| Sector-erase time     | Excludes 00H programming prior to erasure |         | 1‡        | 15§   | s      |
| Program time          | Excludes system-level overhead            | 9       | 9         | 3600§ | µs     |
| Chip-programming time | Excludes system-level overhead            |         | 6‡        | 50§   | s      |
| Erase/program cycles  |   | 100 000 | 1 000 000 |       | cycles |

† The internal algorithms allow for 2.5-ms/byte program time. DQ5 = 1 only after a byte takes the theoretical maximum time to program. A minimal number of bytes can require significantly more programming pulses than the typical byte. The majority of the bytes program within one or two pulses. This is demonstrated by the typical and maximum programming time listed above.

‡ 25°C, 3-V  $V_{CC}$ , 100 000 cycles, typical pattern

§ Under worst-case conditions: 90°C, 2.7-V  $V_{CC}$ , 100 000 cycles

## latchup characteristics (see Note 10)

| PARAMETER  | MIN   | MAX          | UNIT |
|--|-------|--------------|------|
| Input voltage with respect to $V_{SS}$ on all pins except I/O pins (including A9 and $\overline{OE}$ ) | – 1   | 13           | V    |
| Input voltage with respect to $V_{SS}$ on all I/O pins   | – 1   | $V_{CC} + 1$ | V    |
| Current  | – 100 | 100          | mA   |

NOTE 10: Includes all pins except  $V_{CC}$  test conditions:  $V_{CC} = 3$  V, one pin at a time

## pin capacitance, all packages (see Note 11)

| PARAMETER                         | TEST CONDITIONS | TYP | MAX | UNIT |
|-----------------------------------|-----------------|-----|-----|------|
| $C_{IN}$ Input capacitance        | $V_{IN} = 0$    | 6   | 7.5 | pF   |
| $C_{OUT}$ Output capacitance      | $V_{OUT} = 0$   | 8.5 | 12  | pF   |
| $C_{IN2}$ Control pin capacitance | $V_{IN} = 0$    | 8   | 10  | pF   |

NOTE 11: Test conditions:  $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz

## data retention

| PARAMETER                           | TEST CONDITIONS | MIN | MAX | UNIT  |
|-------------------------------------|-----------------|-----|-----|-------|
| Minimum pattern data retention time | 150°C           | 10  |     | Years |
|                                     | 125°C           | 20  |     |       |

## read operation

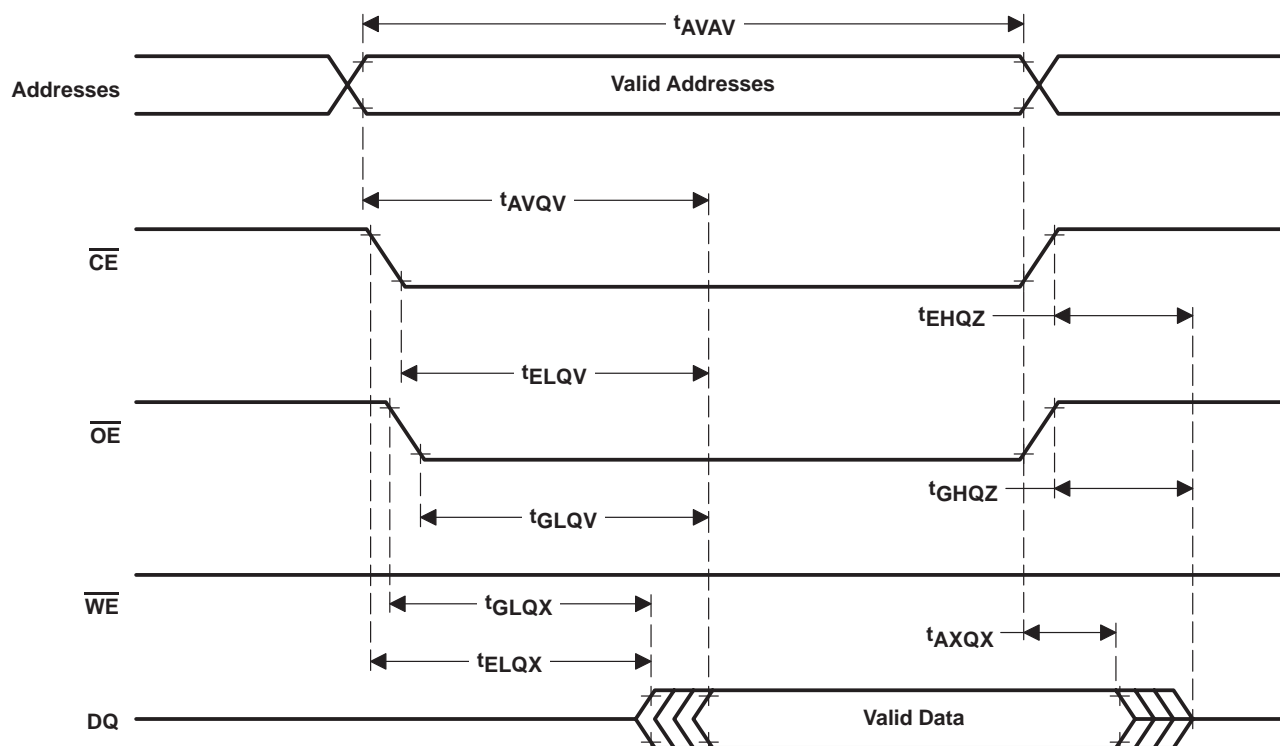


Figure 8. AC Waveform for Read Operation

write operation

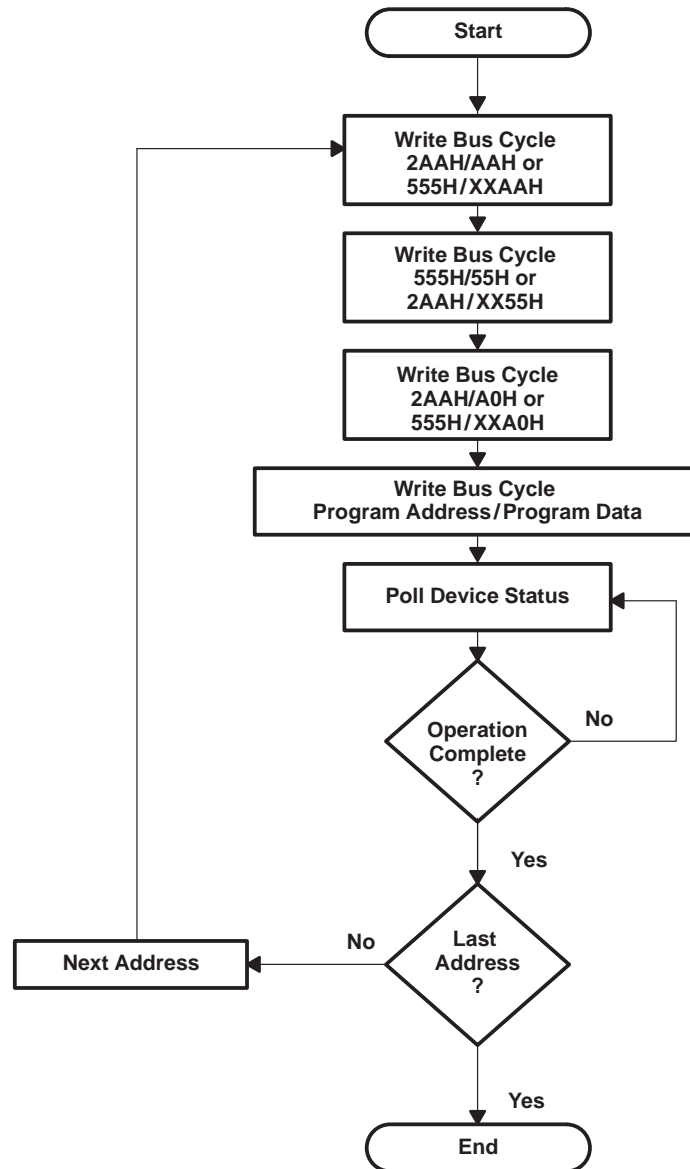


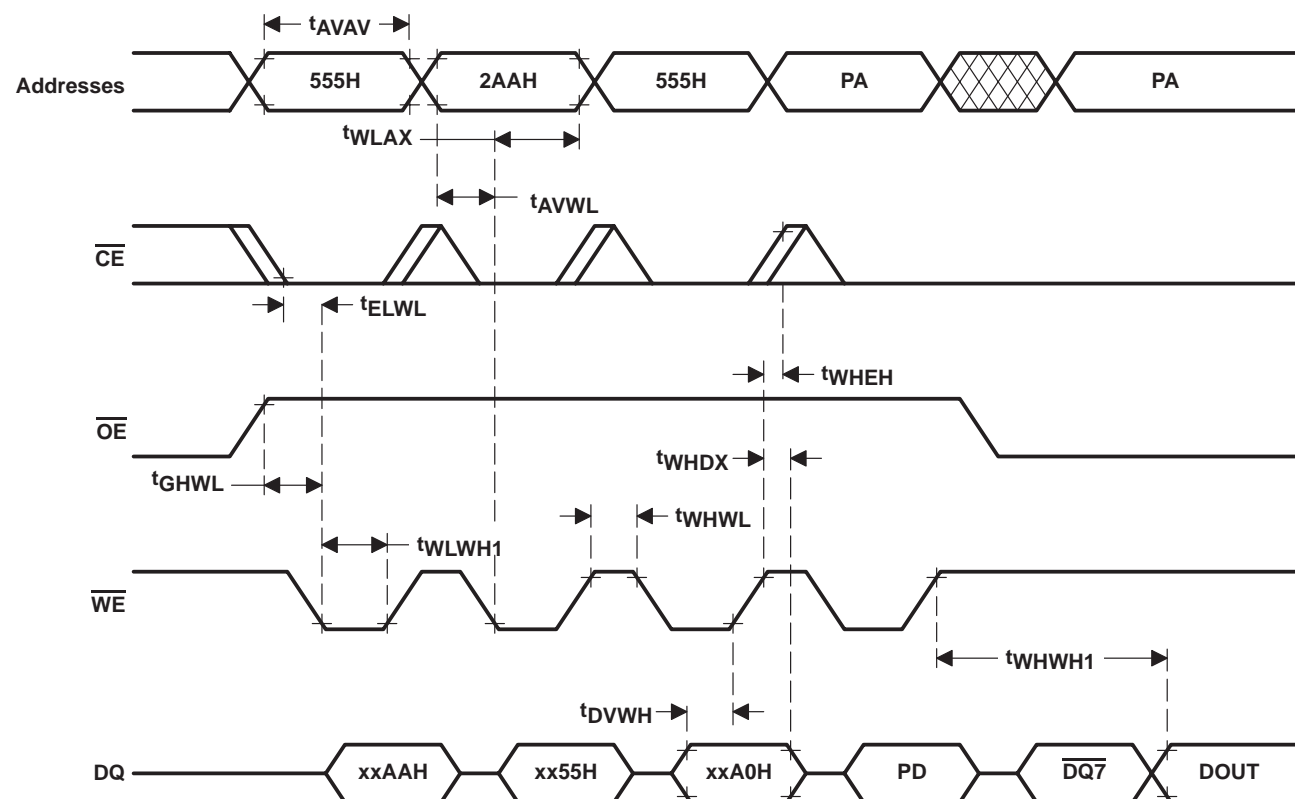
Figure 9. Program Algorithm

PRODUCT PREVIEW

TMS29LF800T, TMS29LF800B  
1048576 BY 8-BIT/524288 BY 16-BIT  
FLASH MEMORIES

SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

write operation (continued)



- NOTES: A. PA = Address to be programmed  
B. PD = Data to be programmed  
C.  $\overline{DQ7}$  = Complement of data written to DQ7  
D. Timing diagram shown is for word-mode operation

Figure 10. AC Waveform for Program Operation

write operation (continued)

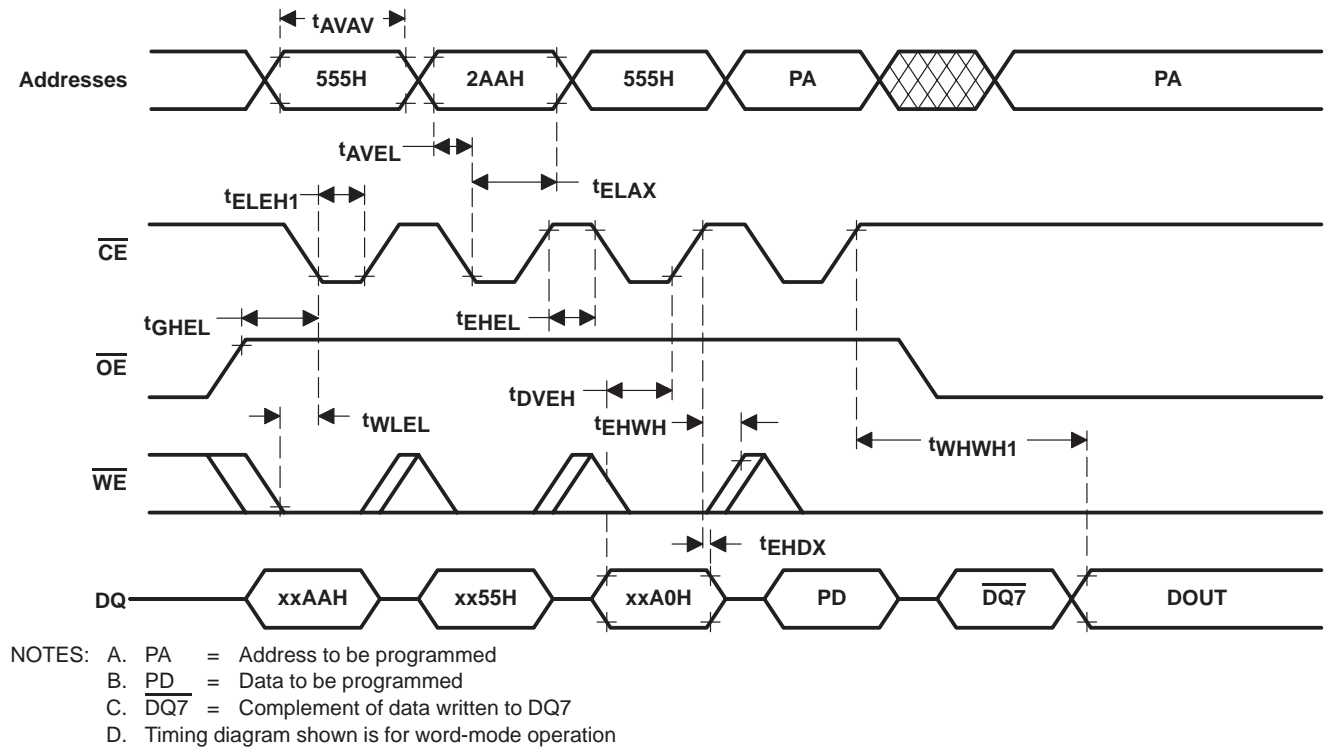


Figure 11. Alternate  $\overline{\text{CE}}$ -Controlled Write Operation

PRODUCT PREVIEW

## chip-erase operation

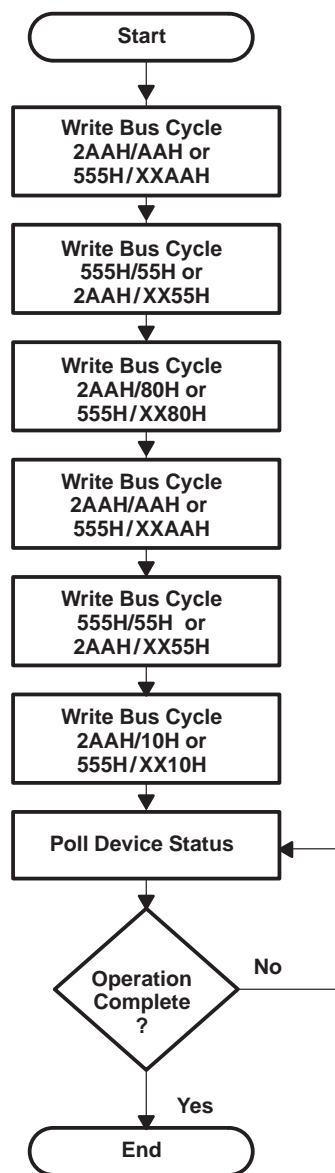
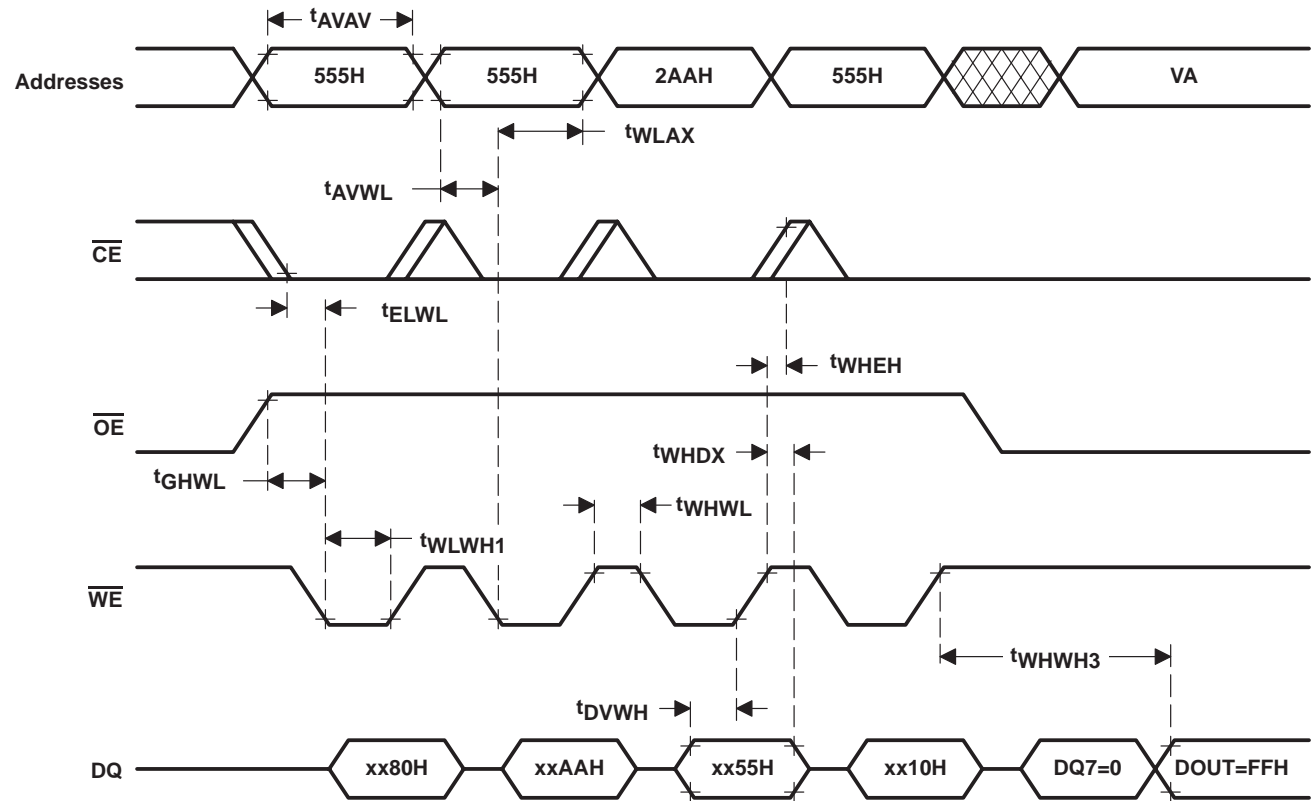


Figure 12. Chip-Erase Algorithm



# chip-erase operation (continued)



- NOTES: A. VA = any valid address  
B. Figure details the last four bus cycles in a six-bus-cycle operation.  
C. Timing diagram shown is for word-mode operation

Figure 13. AC Waveform for Chip-Erase Operation

## sector-erase operation

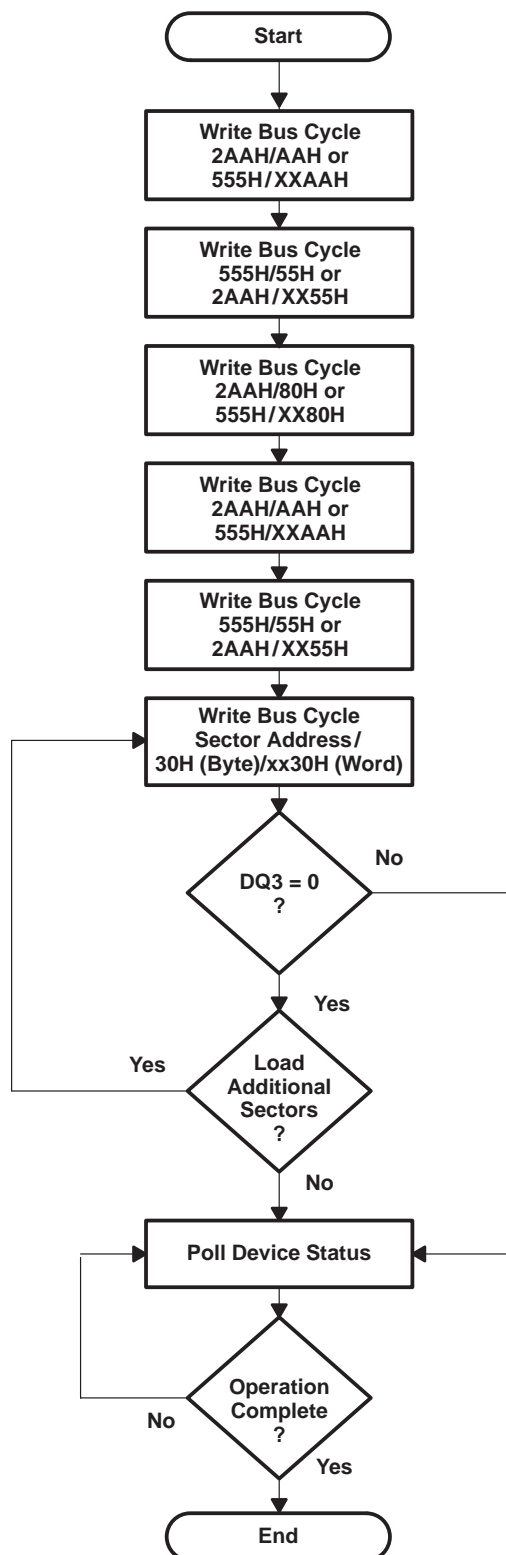
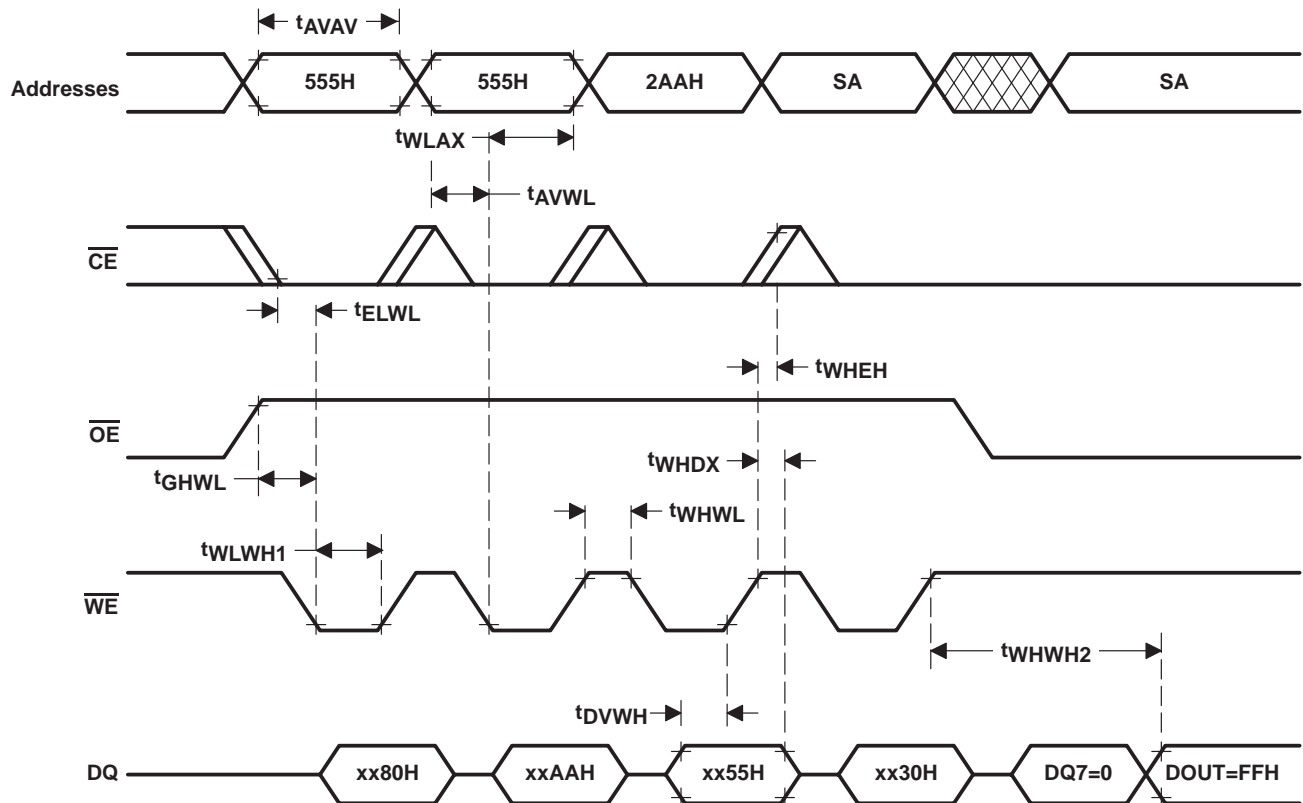


Figure 14. Sector-Erase Algorithm

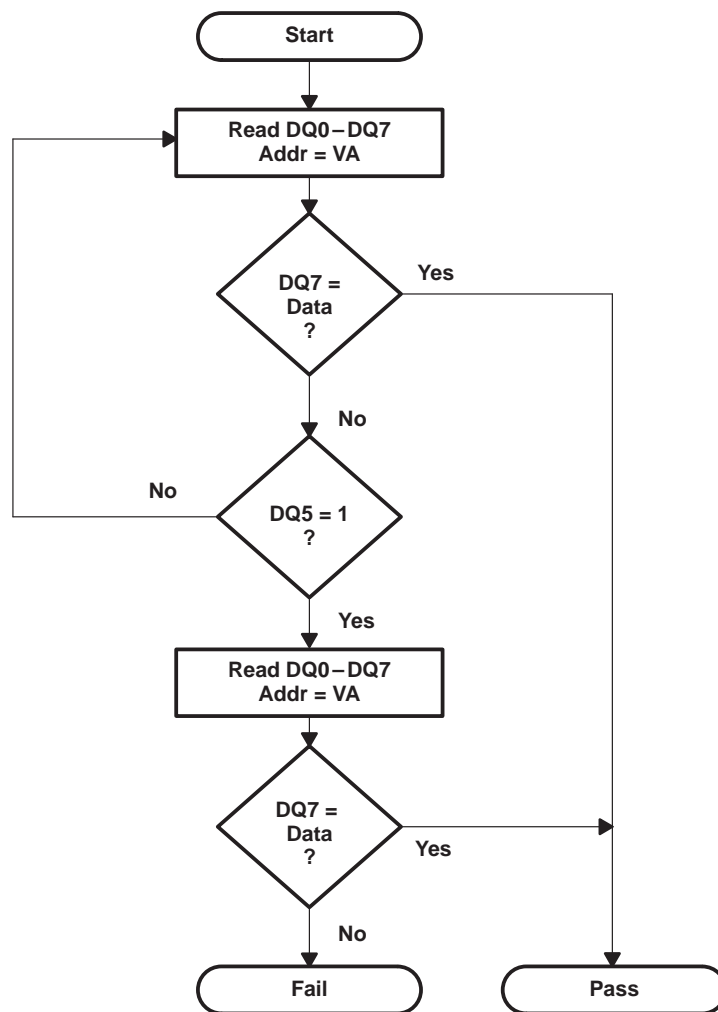
# sector-erase operation (continued)



- NOTES: A. SA = Sector address to be erased  
B. Figure details the last four bus cycles in a six-bus-cycle operation.  
C. Timing diagram shown is for word-mode operation

Figure 15. AC Waveform for Sector-Erase Operation

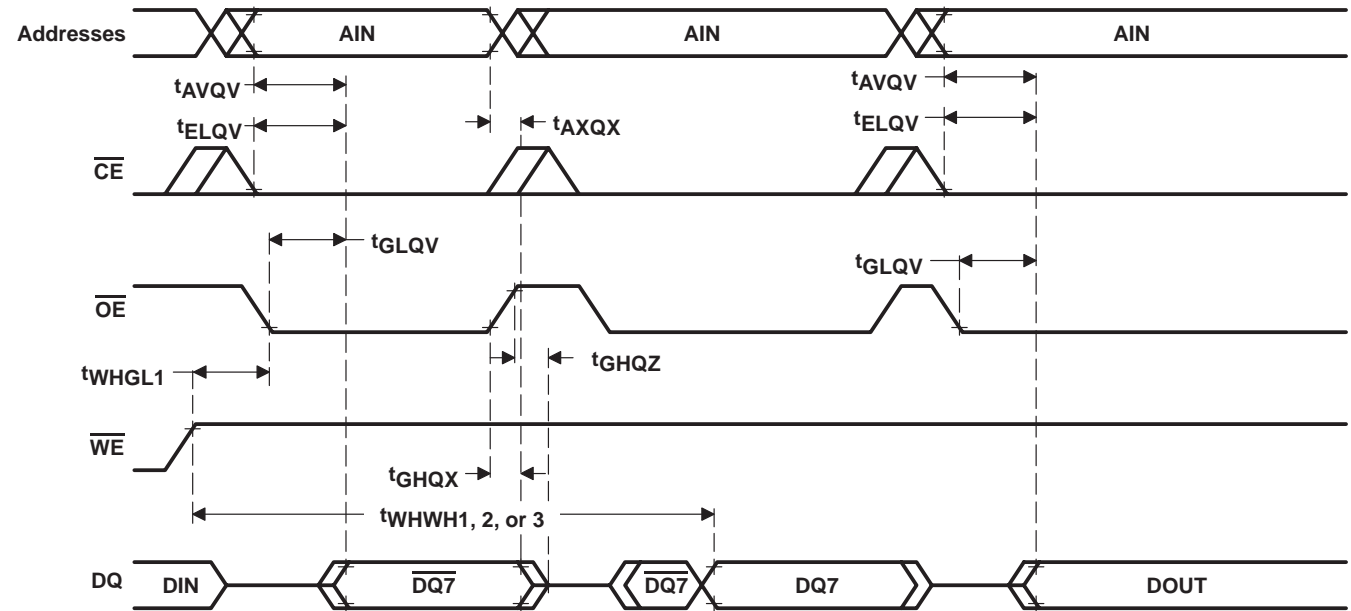
## data-polling operation



- NOTES: A. Polling status bits DQ7 and DQ5 may change asynchronously.  
Read DQ7 after DQ5 changes states.
- B. VA = Program address for byte-programming  
= Selected sector address for sector erase  
= Any valid address for chip erase

**Figure 16. Data-Polling Algorithm**

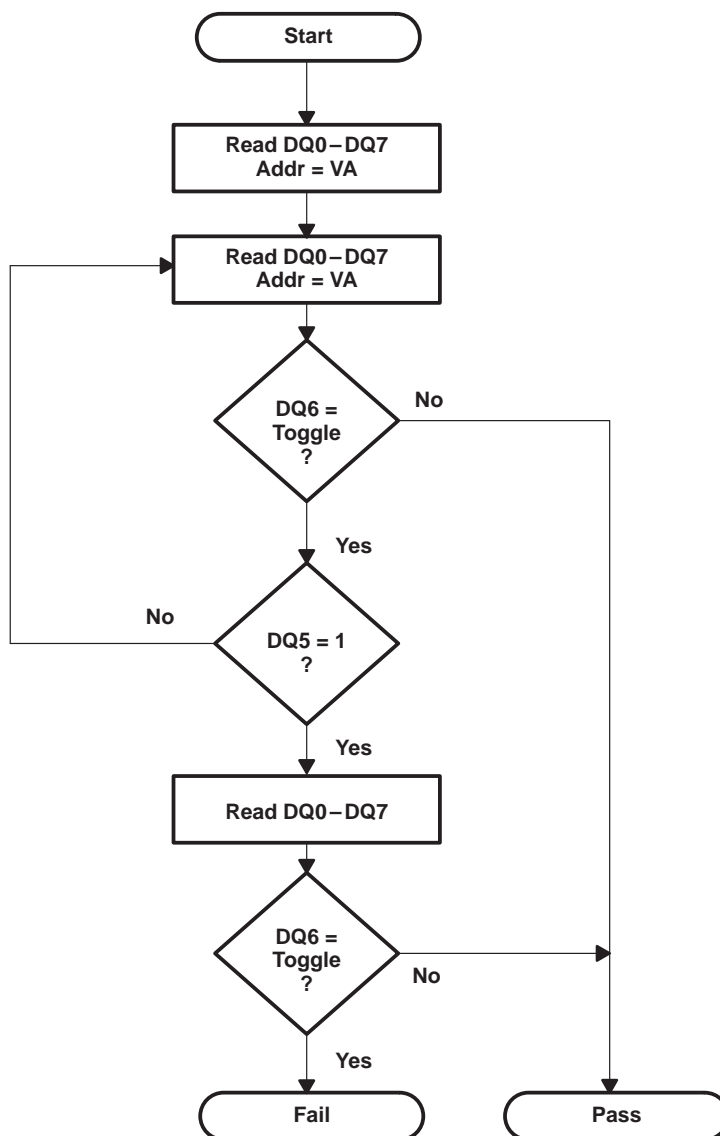
data-polling operation (continued)



- NOTES: A.  $\overline{\text{DIN}}$  = Last command data written to the device  
 B.  $\overline{\text{DQ7}}$  = Complement of data written to DQ7  
 C.  $\text{DOUT}$  = Valid data output  
 D.  $\text{AIN}$  = Valid address for byte-program, sector-erase, or chip-erase operation

Figure 17. AC Waveform for Data-Polling Operation

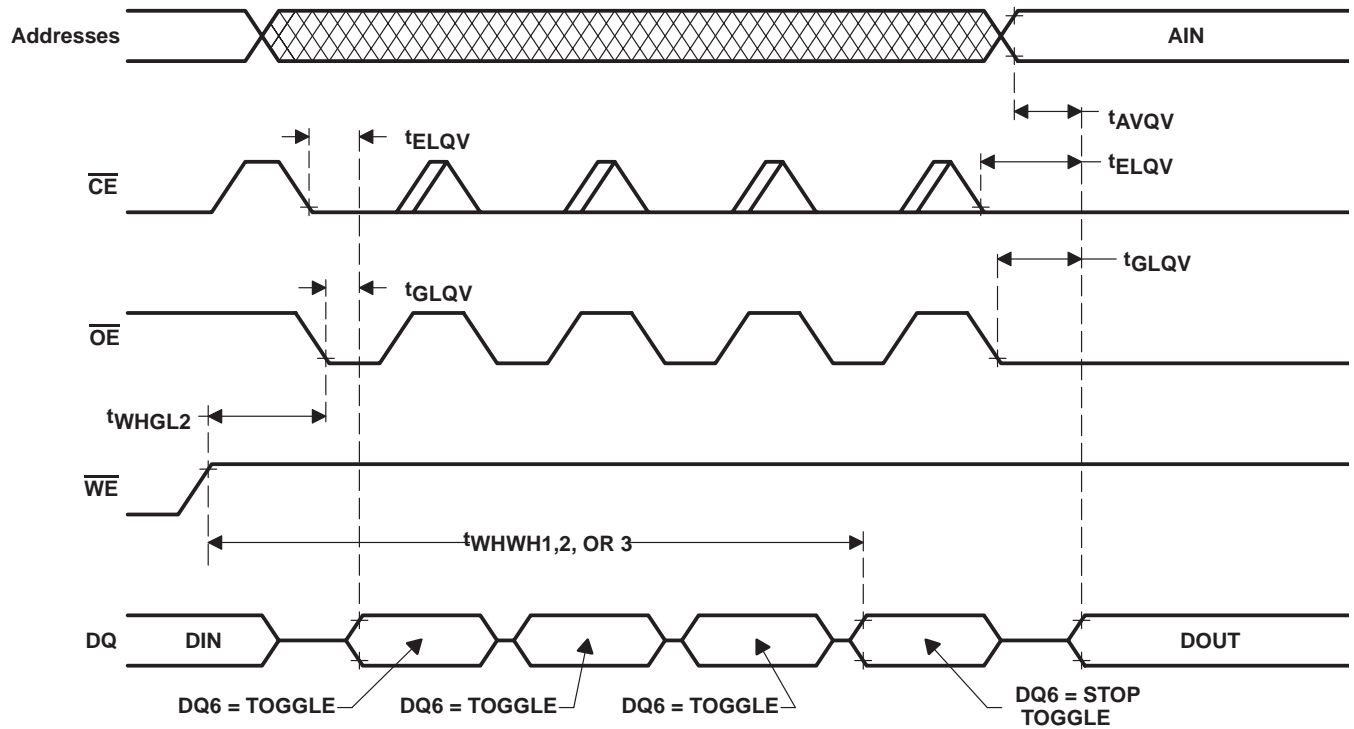
## toggle-bit operation



NOTE A: Polling status bits DQ6 and DQ5 can change asynchronously. Read DQ6 after DQ5 changes states.

Figure 18. Toggle-Bit Status-Read Algorithm

## toggle-bit operation (continued)



- NOTES: A. DIN = Last command data written to the device  
B. DQ6 = Toggle bit output  
C. DOUT = Valid data output  
D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation

Figure 19. AC Waveforms for Toggle-Bit Operation

## sector-protect operation

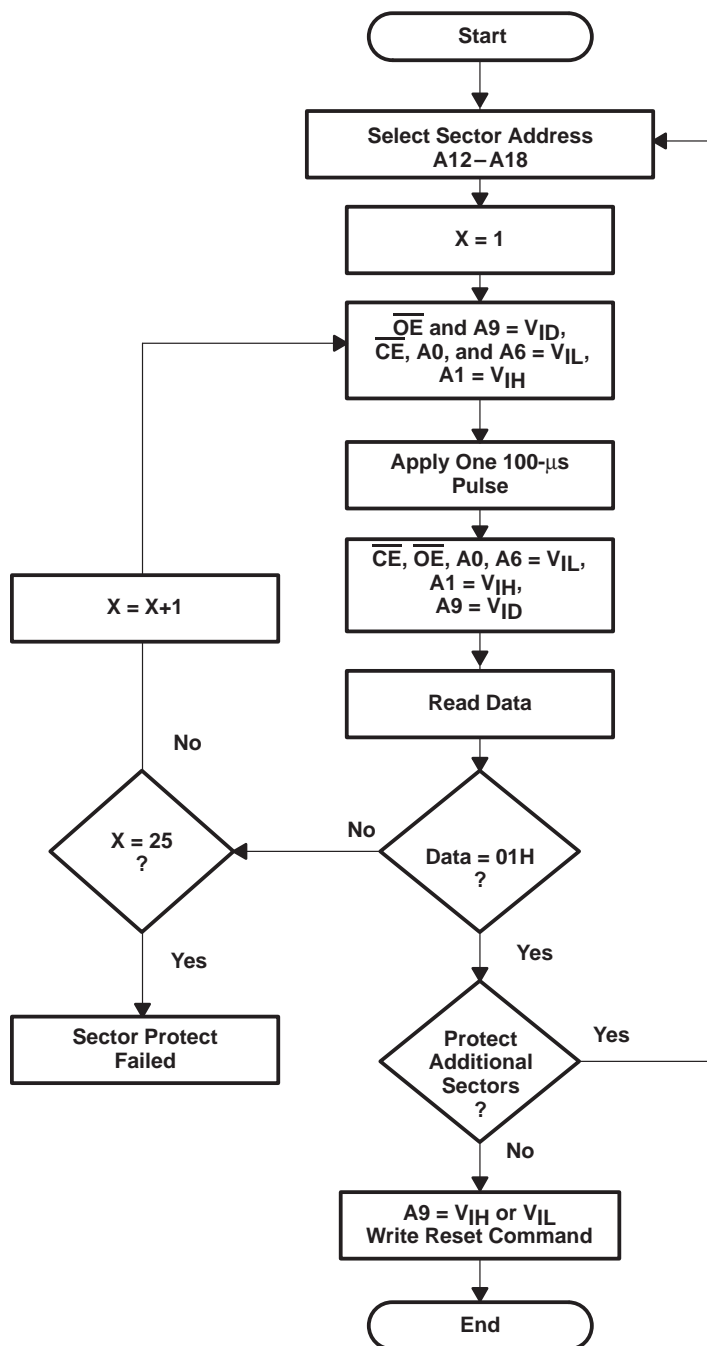
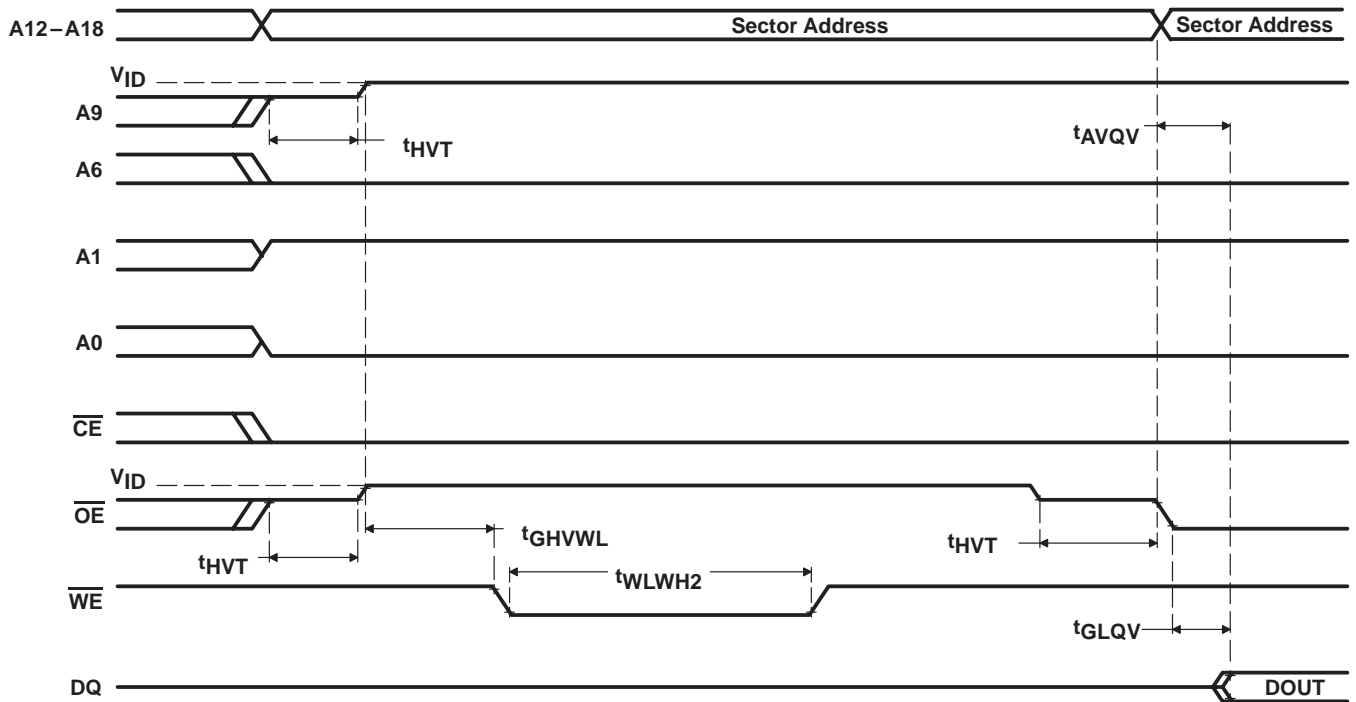


Figure 20. Sector-Protect Algorithm



sector-protect operation (continued)



NOTE A: DOUT = 00H if selected sector is not protected,  
 01H if the sector is protected

Figure 21. AC Waveform for Sector-Protect Operation

PRODUCT PREVIEW

## sector-unprotect operation

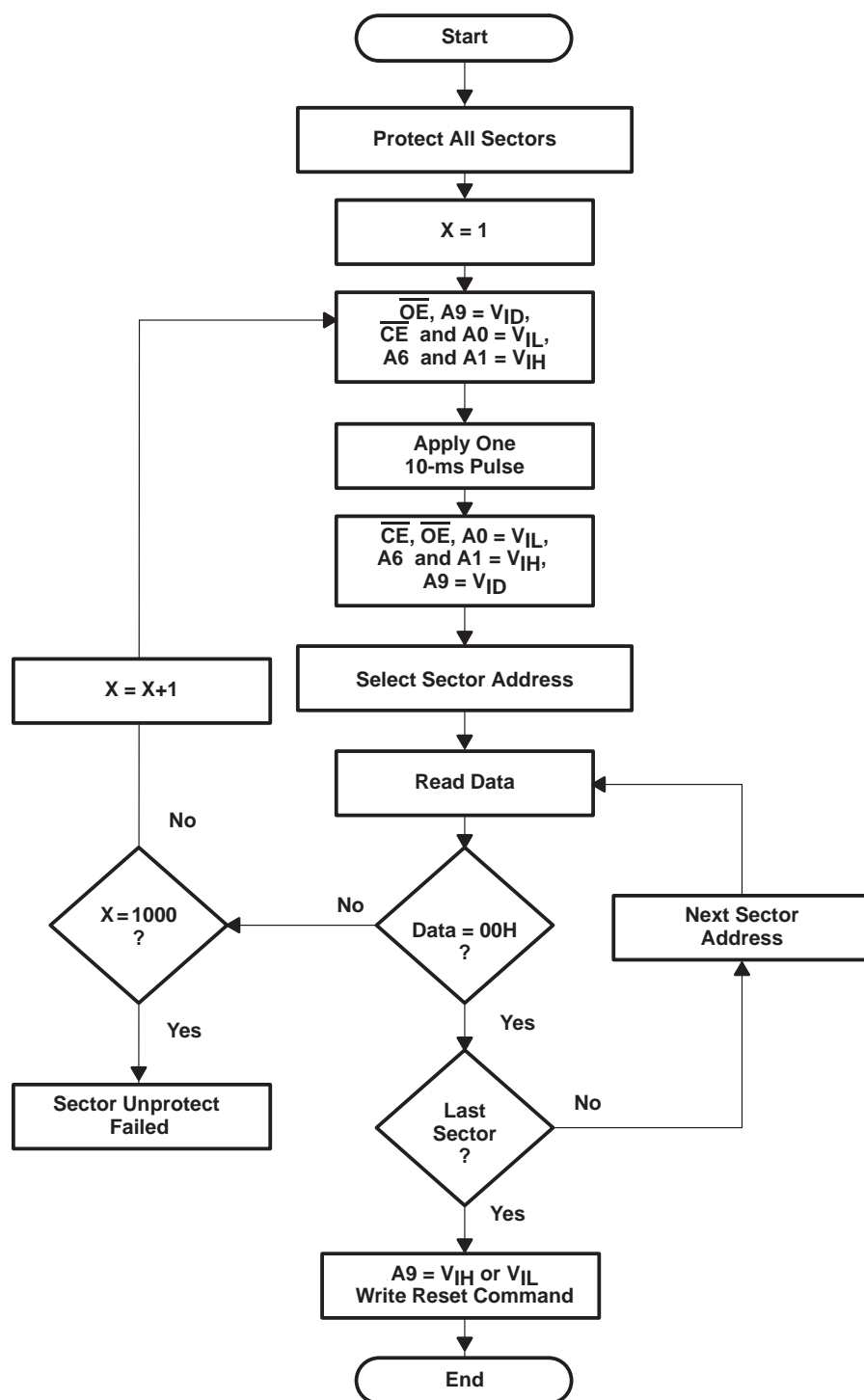
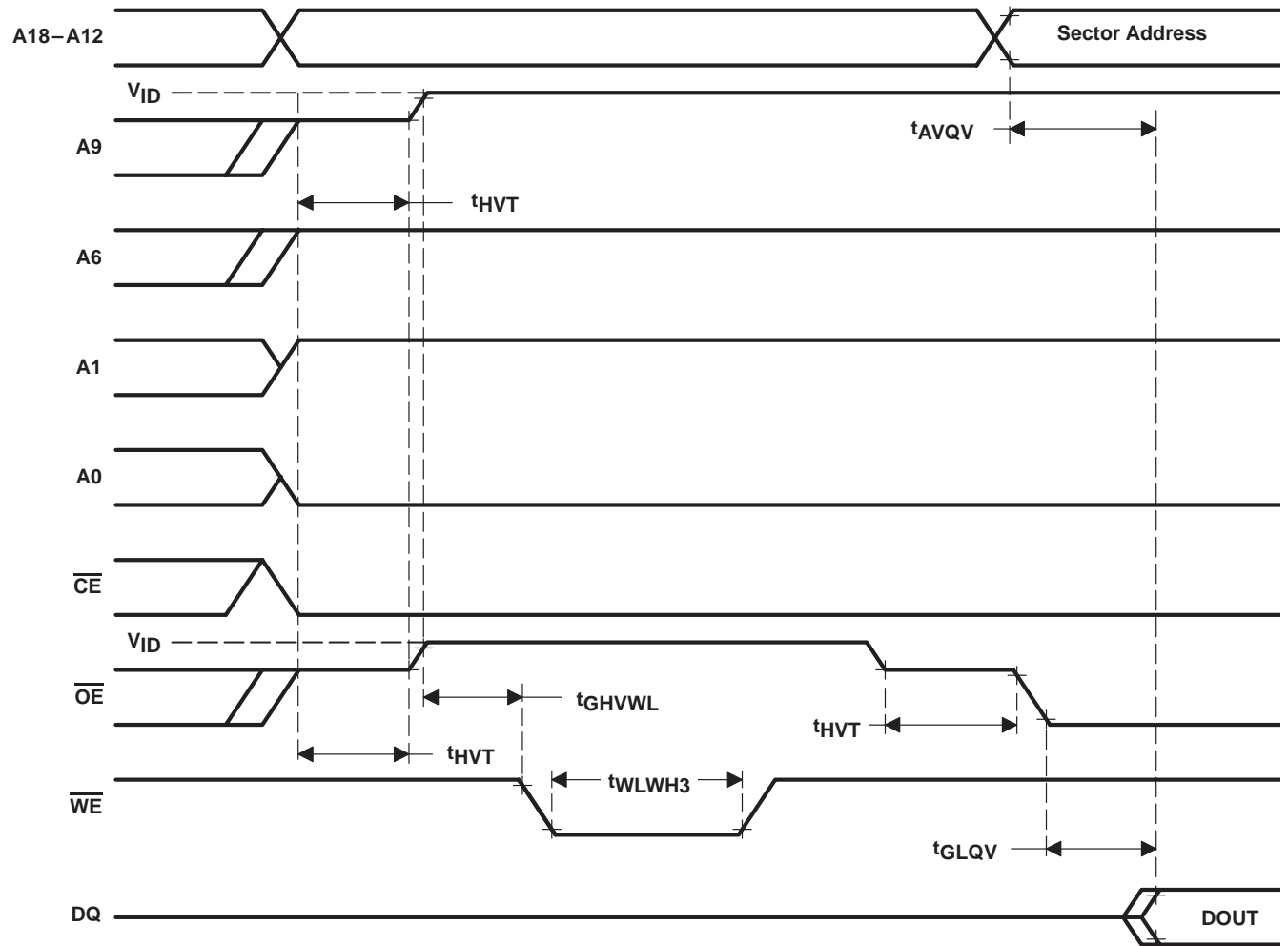


Figure 22. Sector-Unprotect Algorithm

sector-unprotect operation (continued)

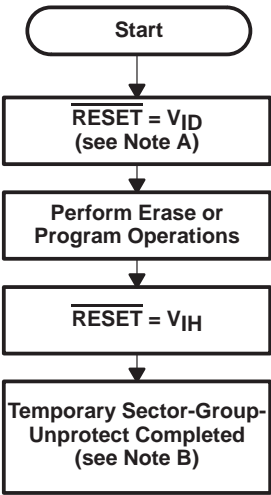


NOTE A: DOUT = 00H if selected sector is not protected,  
01H if the sector is protected

Figure 23. AC Waveform for Sector-Unprotect Operation

PRODUCT PREVIEW

temporary sector-unprotect operation



NOTES: A. All protected sectors unprotected  
 B. All previously protected sectors are protected once again

Figure 24. Temporary Sector-Unprotect Algorithm

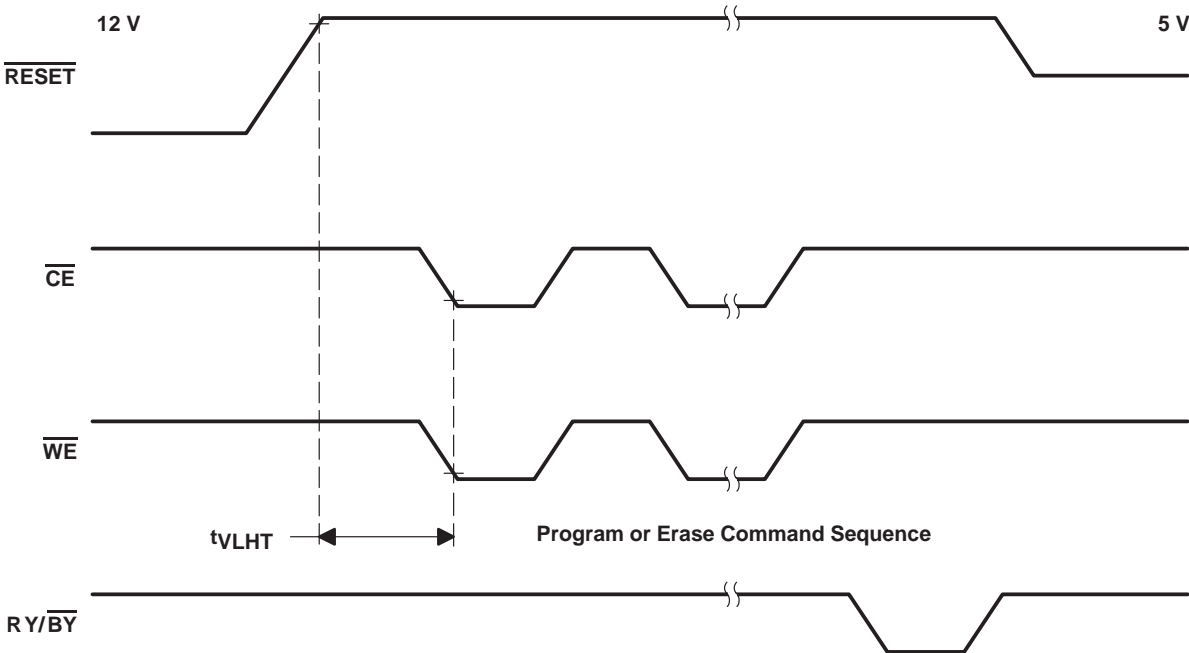


Figure 25. Temporary Sector-Unprotect Timing Diagram

## PARAMETER MEASUREMENT INFORMATION

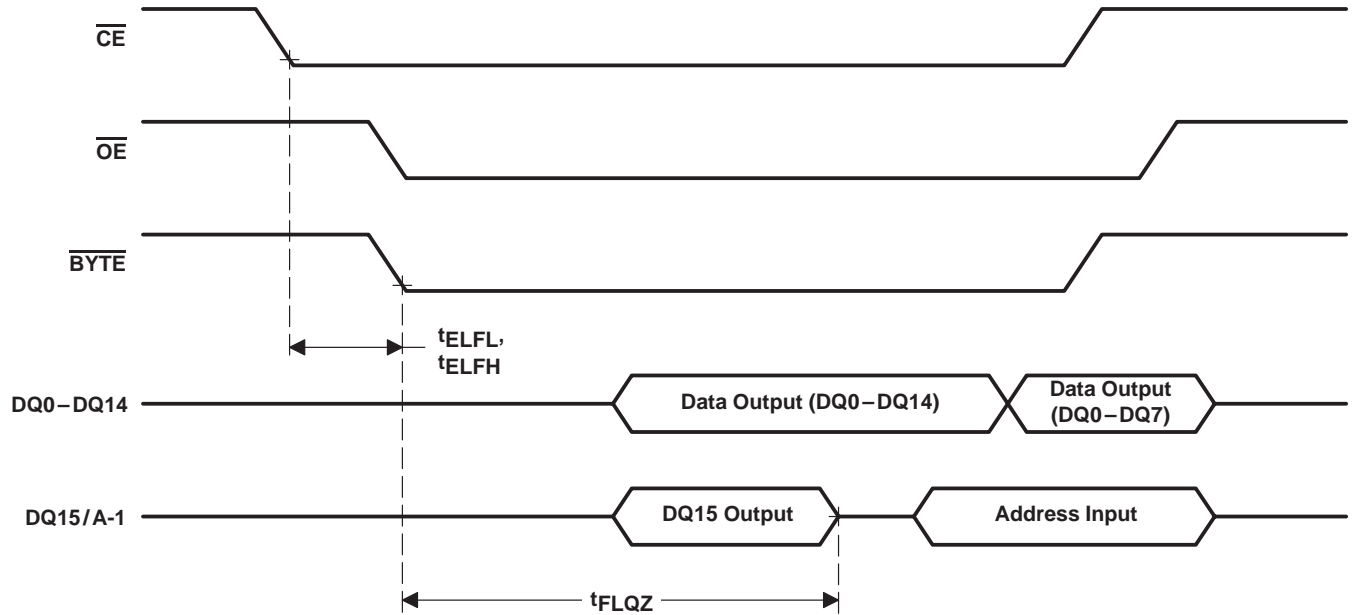


Figure 26.  $\overline{BYTE}$  Timing Diagram for Read Operation

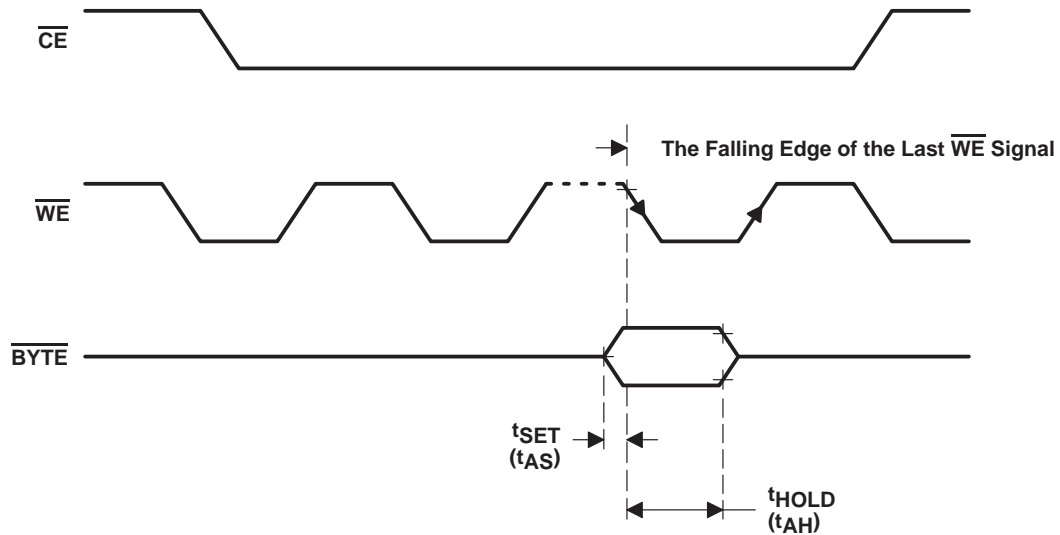


Figure 27.  $\overline{BYTE}$  Timing Diagram for Write Operation

PRODUCT PREVIEW

# PARAMETER MEASUREMENT INFORMATION

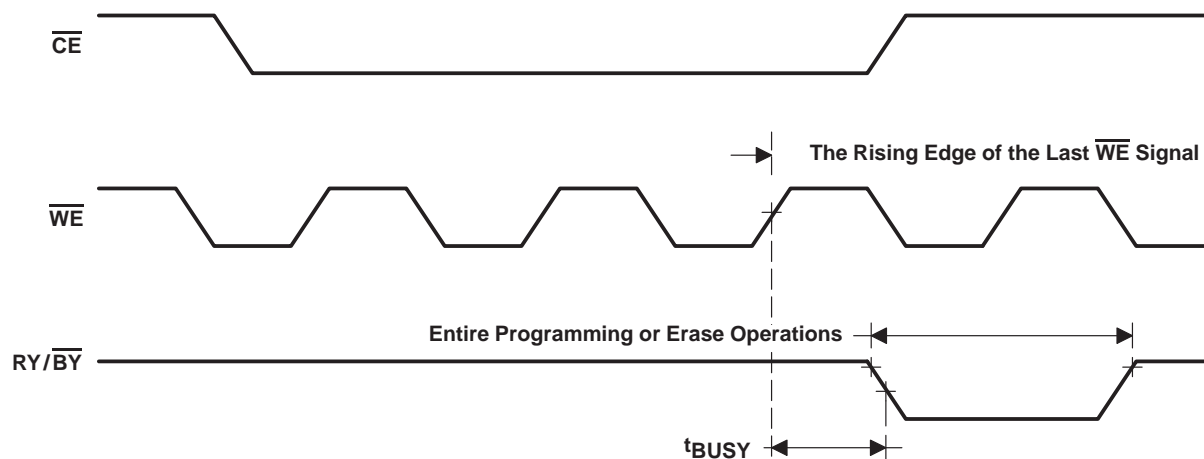
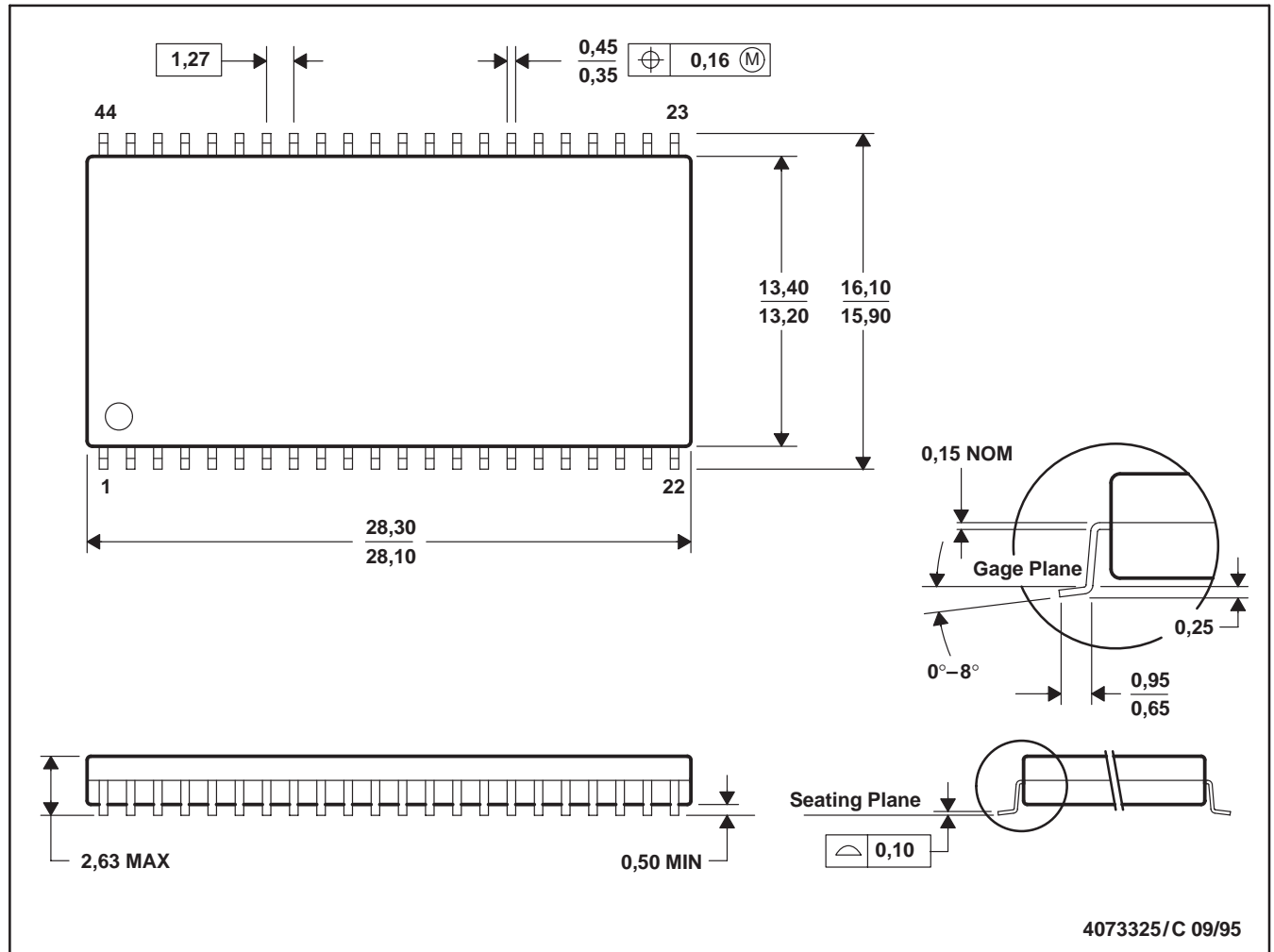


Figure 28.  $\overline{RY}/\overline{BY}$  Timing Diagram During Program/Erase Operations

## MECHANICAL DATA

DBJ (R-PDSO-G44)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion.

PRODUCT PREVIEW

TMS29LF800T, TMS29LF800B  
1048576 BY 8-BIT/524288 BY 16-BIT  
FLASH MEMORIES

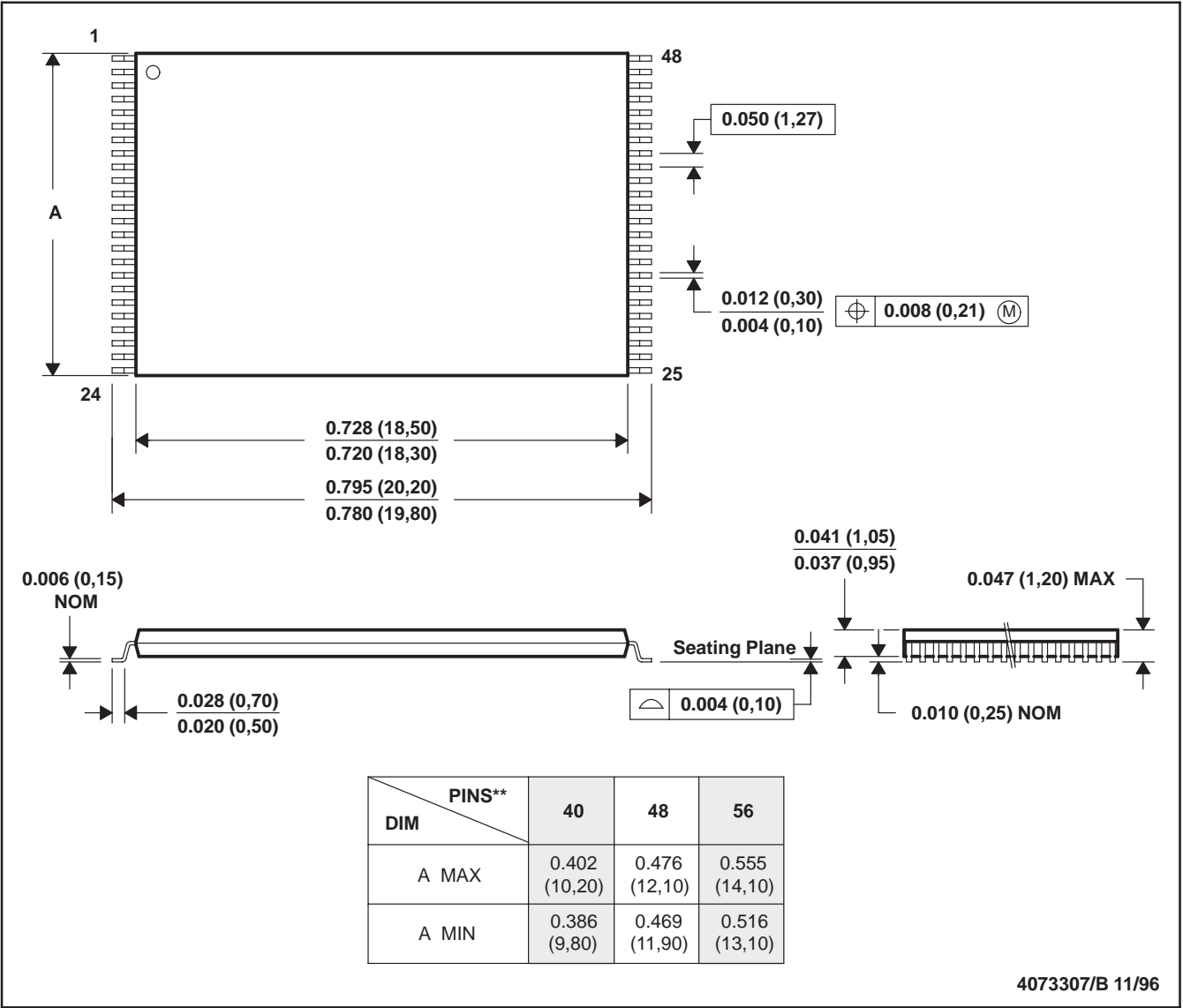
SMJS828B – SEPTEMBER 1996 – REVISED OCTOBER 1997

MECHANICAL DATA

DCD (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.