TMPZ84C61AP-6
TLCS-Z80 CGC : Z80 CLOCK GENERATOR/CONTROLLER

1. GENERAL DESCRIPTION AND FEATURES

The TMPZ84C61A is a clock generator/controller (CGC) for the TLCS-Z80 Family (Microprocessor (MPU) and its peripheral LSIs) fabricated with Toshiba's CMOS Silicon Gate Technology. The TMPZ84C61A is provided with two input terminals which are capable of selecting one of the following 3 modes when the TLCS-Z80 MPU executes the HALT instruction.

(1) RUN Mode

The clock (CLK) output operation of the TMPZ84C61A is continued. The TLCS-Z80 MPU is in the HALT state at this time and continues to execute the NOP instruction.

(2) IDLE Mode

The clock (CLK) output by the TMPZ84C61A is stopped. However, only the internal oscillator continues to run.

(3) STOP Mode

The operation of the TMZ84C61A is completely stopped.

In the STOP mode, the operation of the microcomputer system is completely stopped. Therefore, it becomes possible to keep the system at low power consumption.

When "0" is inputted to the $\overline{DIV}$ terminal, the signal obtained by dividing input frequency from the external oscillator is transmitted from the CLK terminal, and when "1" is inputted, the signal of the same frequency, as that of the external oscillator is transmitted from the CLK terminal.

The TMPZ84C61A is enclosed in 16 pin standard DIP.

The principal functions and features of the TMPZ84C61A are as follows.

(1) Upper compatible with TMPZ84C60P

(2) Low power consumption

3mA Typ.	(@5V, 6MHz operation)	
500μA Typ.	(@5V 6MHz)	(IDLE Mode)
10μA MAX.	(@5V stationary)	(STOP Mode)

(3) Single 5V power supply (5V ± 10%)

(4) Extended operating temperature (−40°C to 85°C)

(5) The following 3 modes are selectable :

- RUN Mode
- IDLE Mode
- STOP Mode

(6) Clock output frequency division

(7) With the $\overline{\text{RESOUT}}$ terminal signal, stable reset pulse can be provided to the MPU and its peripheral LSIs.

Compatibility with TMPZ84C60

TMPZ84C61A is used in the same mode as TMPZ84C60 under the following conditions.

(1) Leave the $\overline{\text{RESOUT}}$ terminal open, and connect the $\overline{\text{RESET}}$ terminal of the MPU with that of TMPZ84C61A.

(2) Input "1" to the $\overline{\text{DIV}}$ terminal.

2. PIN CONNECTIONS AND PIN FUNCTIONS

The pin connections and I/O pin names and brief functions of the TMPZ84C61A are shown below.

2.1 PIN CONNECTIONS

The pin connections of the TMPZ84C61A are as shown in Figure 2.1.

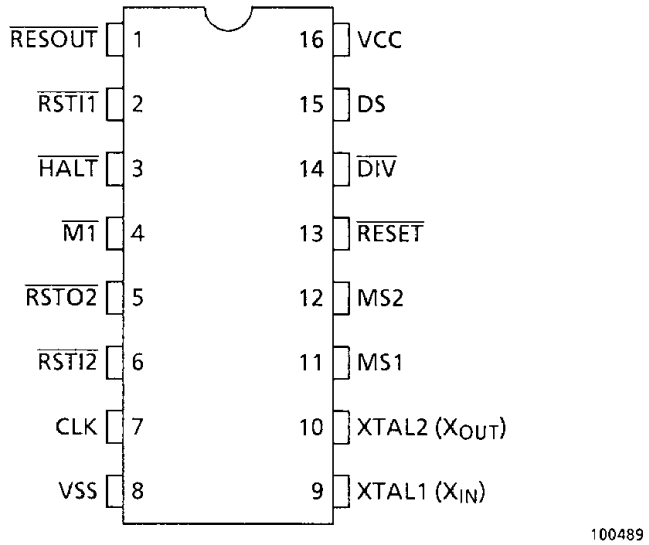

Figure 2.1 Pin Connections

2.2 PIN NAMES AND FUNCTIONS

I/O pin names and functions of the TMPZ84C61A are as shown in Table 2.1.

Table 2.1 Pin Names and Functions

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{RSTI1}$	1	Input	Restart signal from clock (CLK) stop state (Level trigger input)
$\overline{HALT}$	1	Input	Halt signal ($\overline{HALT}$) input
$\overline{M1}$	1	Input	Machine cycle 1 ($\overline{M1}$) signal input
$\overline{RSTO2}$	1	Output	Restart signal $\overline{RSTI2}$ output
$\overline{RSTI2}$	1	Input	Restart signal from clock (CLK) stop state (Edge trigger input)
CLK	1	Output	Single-phase clock output. When the HALT instruction in STOP or IDLE Mode is executed, The TMPZ84C61A holds clock output at "0" level.
DS	1	Input	Counter output stage selecting input. Input to set up a warming-up time at time of restart ftom the clock stop state in stop mode.
$\overline{RESET}$	1	Input	Reset signal input. Restart signal from clock (CLK) stop state (Level trigger input)
$\overline{RESOUT}$	1	Output	Reset signal output. Restart signal output to MPU and peripherals.
$\overline{DIV}$	1	Input	Determinds division or non-division of oscillation frequency. Division mode is selected by the input of "0".
MS1, MS2	2	Input	Mode selection input. One of 3 modes (RUN, IDLE,STOP) is selected according to the state of these 2 pins
XTAL1 (X_{IN}), XTAL2 (X_{OUT})	2	Input Output	Crystal oscillator connecting terminal
VCC	1	Power supply	+5V
VSS	1	Power supply	0V

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3. DESCRIPTION OF OPERATION

The system configuration, functions and basic operation of the TMPZ84C61A Clock Generator are described here.

3.1 BLOCK DIAGRAM

The block diagram of the internal configuration is shown in Figure 3.1.

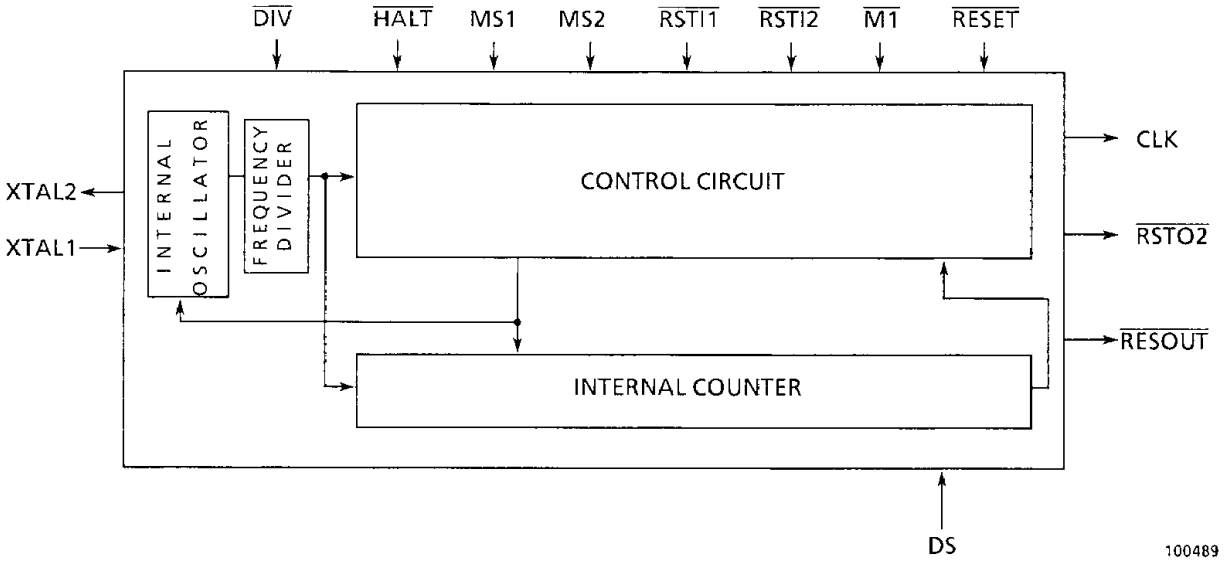

Figure 3.1 Block Diagram

3.2 SYSTEM CONFIGURATION

The internal configuration of TMPZ84C61A is as shown in Figure 3.1.

The waveform that is inputted by the external oscillator is converted into the square-wave for clock by the internal oscillator, Clock is controlled by the control circuit and the counter, and outputted to the outside.

In this section, the following principal components and functions which must be known in using the TMPZ84C61A will be described.

(1) Generation of clock

(2) Operation mode

(3) Warming-up time at restart

3.2.1 Generation of clock

TMPZ84C61A internally supports an oscillation circuit to facilitate the clock output. A desired clock is generated from the CLK terminal by simply connecting the oscillator with the external terminals (XTAL1 and XTAL2). The input of "1" to the $\overline{DIV}$ terminal allows the output of the same frequency as that of the oscillator. By entering "0" to the $\overline{DIV}$ terminal, TMPZ84C61A generates the clock signal with a 1/2 the input frequency. The $\overline{DIV}$ terminal must be kept "Low" for a frequency level of more than 6MHz.

Figure 3.2 shows a typical connection of the oscillator.

(1) A quartz crystal should conform to the follwing characteristics or MR12000-C20 of TokyoDempa (oscillation frequency : 12MHz) :

Output clock frequency (f) : 6MHz

MR12000-C20 quarts crystal oscillator $C_S < 4pF$ $R_S < 25\Omega$

$Cin = Cout = 33pF$

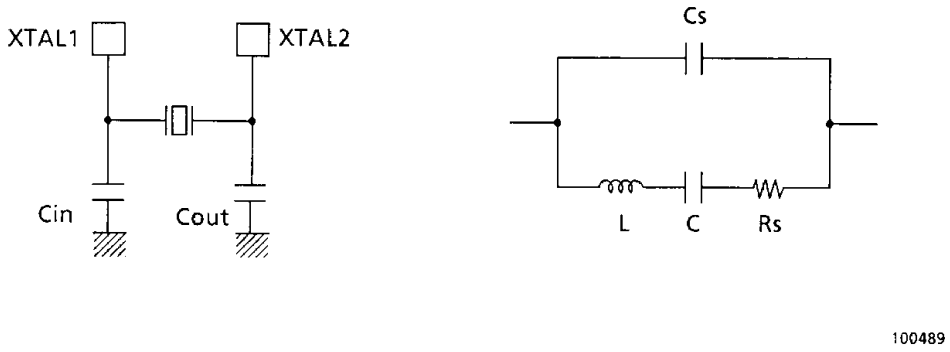

Figure 3.2 Examples of Oscillator Connection

3.2.2 Operation modes

There are 3 kinds of operations modes ; RUN mode, IDLE mode,and STOP mode available for the TMPZ84C61A. One of these modes can be selected by the mode select input (MS1, MS2). These operation modes are effective when the TLCS-Z80 MPU is executing the HALT instruction. When fetching the HALT instruction, MPU outputs "0" to the $\overline{HALT}$ terminal to indicate that MPU enters into the HALT state. After executing the HALT instruction, the TMPZ84C61A performs the operation in one of these mode by this signal.

The operations of these modes in the HALT state are shown in Table 3.1.

Table 3.1 TMPZ84C61A Operation Modes

MS1	MS2	Operation Mode	Content of Operation at Halt State
1	1	RUN Mode	Continues to supply clock to the outside.
0	* Note)	IDLE Mode	The internal oscillator only operates and supply of clock to the outside is stopped. Clock output (CLK) is held at "0" level.
1	0	STOP Mode	The internal operations are all stopped. Clock output (CLK) is held at "0" level.

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Note : MS2 can be used for any modes.

Clock is continuously supplied in any mode except the HALT state. MPU is restarted from the clock stop state in IDLE mode and STOP mode by inputting one of $\overline{\text{RSTI1}}$, $\overline{\text{RSTI2}}$ or $\overline{\text{RESET}}$ signal.

MPU is released from the HALT state by the input of $\overline{\text{RESET}}$ signal or acceptance of maskable ($\overline{\text{INT}}$ signal) or non-maskable ($\overline{\text{NMI}}$ signal) interrupt request. Therefore, these signals are normally connected to MPU as follows :

- Connect the $\overline{\text{RESET}}$ signal of the system with TMPZ84C61A.
- Connect the $\overline{\text{RESET}}$ signals of the MPU and peripherals with the $\overline{\text{RESOUT}}$ signal.
- $\overline{\text{INT}}$ signal (maskable interrupt input) and $\overline{\text{RSTI1}}$ signal (restart input) are commonly used.
- $\overline{\text{RETO2}}$ signal (output of restart input signal $\overline{\text{RSTI2}}$) is connected to $\overline{\text{NMI}}$ signal (non-maskable interrupt input).

3.2.3 Warming-up time at restart (STOP mode)

When released from the HALT state by acceptance of interrupt request, MPU will execute the interrupt routine. Therefore, to restart the clock by $\overline{\text{RSTI1}}$ or $\overline{\text{RSTI2}}$ restart signal in STOP mode it is necessary to supply clock to the outside after the oscillation is sufficiently stabilized. The TMPZ84C61A provides a sufficient warming-up time enough to reach stabilized frequency by operating the internal counter. The warming-up is completed and clock output is started at the rising edge of the internal counter output which is divided oscillation frequency. There is the DS input terminal provided for setting this warming-up time, and a time of 2^{17} (DS=0) or 2^{14} (DS=1) division of the externally connected oscillator is provided.

The block diagram of the internal counter unit is shown in Figure 3.3 and the relationship between the logic of the DS terminal and warming-up time is shown in Table 3.2.

Further, in case of the restart by $\overline{\text{RESET}}$ signal, the internal counter does not operate for a quick operation at time of power ON.

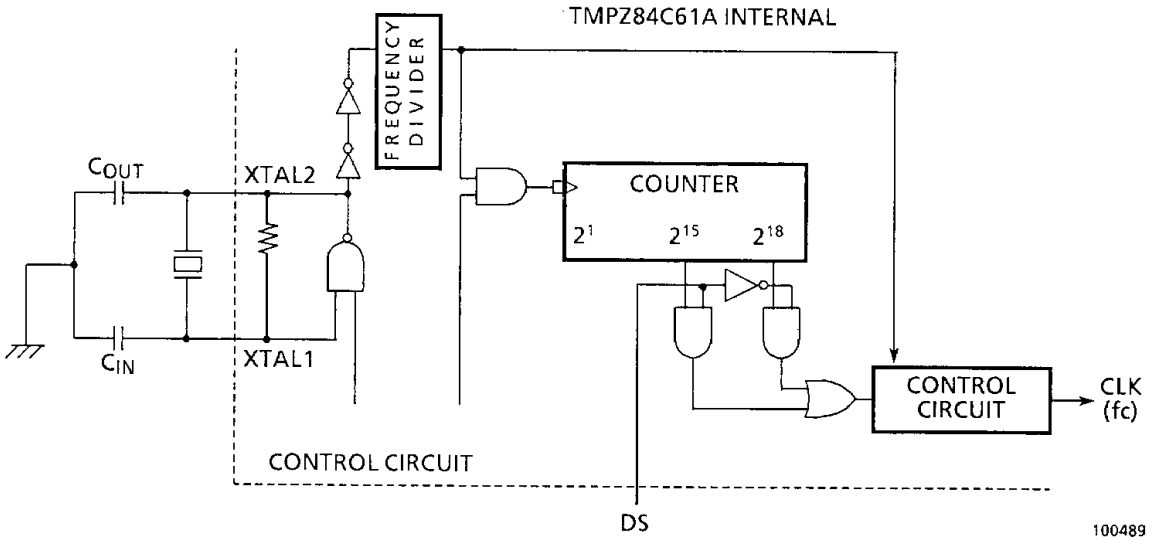

Figure 3.3 Block Diagram of Internal Counter

Table 3.2 Warming-up Time

DS	Counter Output	fc = 6MHz	Unit
0	2^{18}	21.9	ms
1	2^{15}	2.7	

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3.3 STATUS CHANGE FLOWCHART AND BASIC TIMING

In this section, the status change and basic timing when the TMPZ84C61A is operating are explained.

3.3.1 Status change flowchart

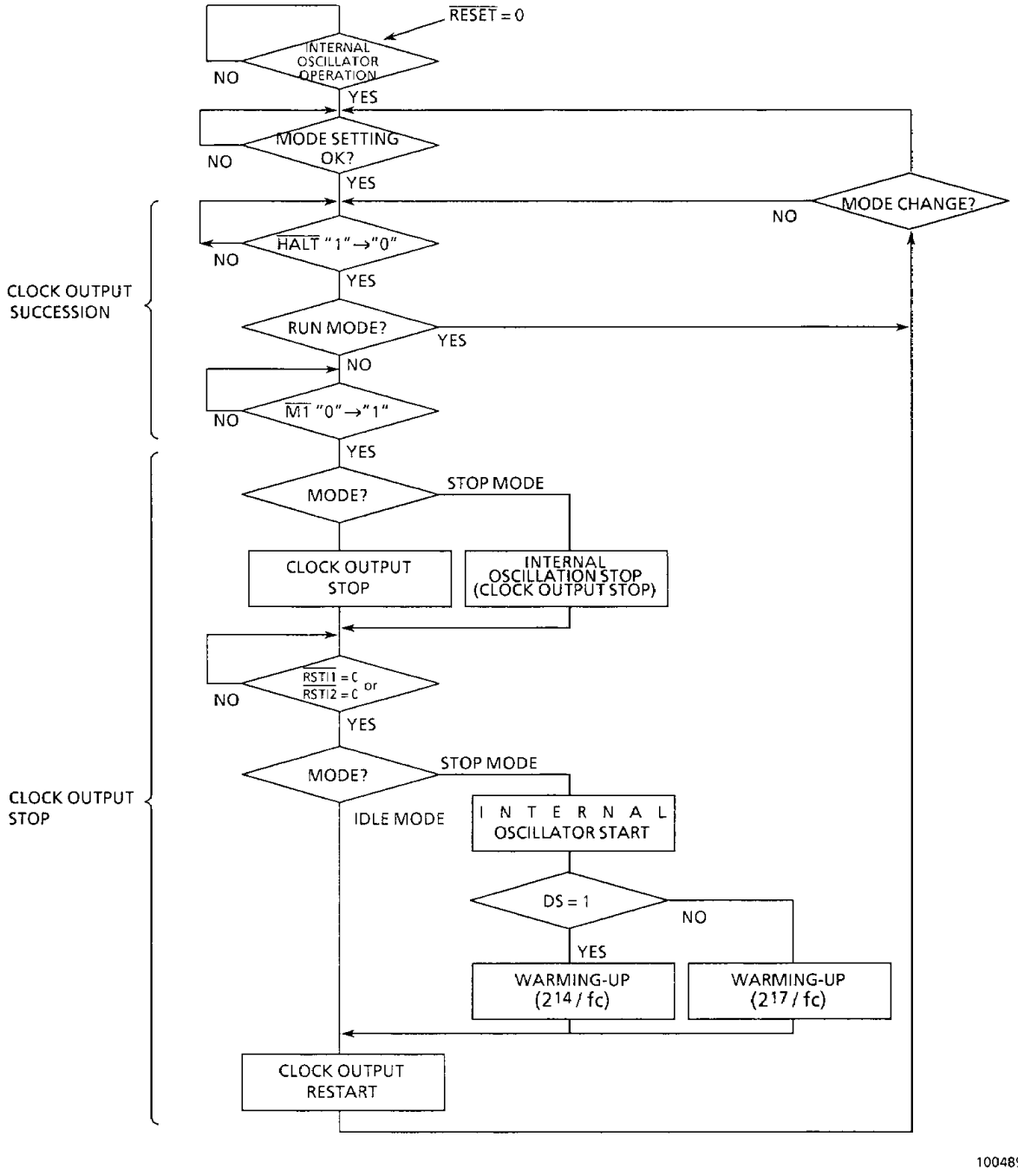

Figure 3.4 Status Change Flowchart

3.3.2 Basic timing

(1) Operation when HALT instruction is executed

The basic timing of each mode when the TLCS-Z80 MPU executes the HALT intruction is explained. Synchronously with the fall of T4 state of the HALT instruction opcode fetch cycle (M1), MPU makes the $\overline{HALT}$ signal to "0" level. By this signal,the TMPZ84C61A detects that MPU is going to enter into the HALT state.

(a) RUN mode (MS = 1, MS2 = 1)

The basic timing of RUN mode is shown in Figure 3.5.
In the RUN mode, clock is continuously supplied to the outside even when MPU is in the HALT state. This mode is used on a system requiring the memory address refresh.

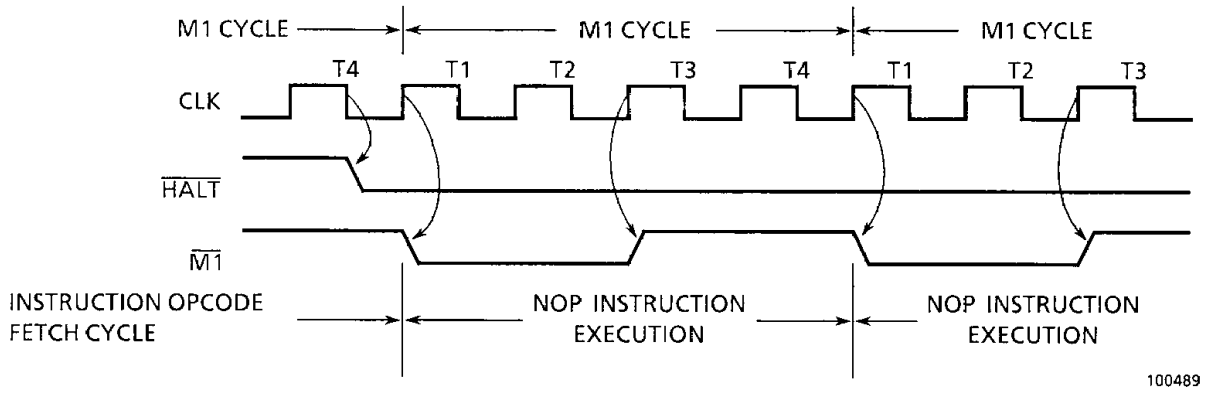

Figure 3.5 RUN Mode Timing

(b) IDLE mode (MS1 = 0) and STOP mode (MS1 = 1, MS2 = 0)

The basic timing in the IDLE and STOP modes is shown in Figure 3.6.
In these modes, clock output is stopped at the "0" level during T4 state by the $\overline{HALT}$ signal and $\overline{M1}$ signal following the HALT instruction.
However, in case of the STOP mode the internal oscillator of the TMPZ84C61A is also stopped.

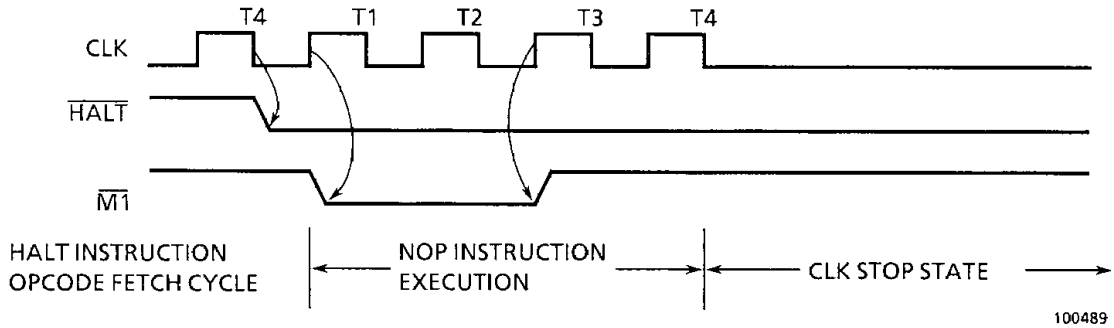

Figure 3.6 IDLE/STOP Mode Timing

(2) Restart from clock stop

The clock is restarted from the stopped state in the IDLE or STOP mode when "0" is inputted to any one of the following signals :

- $\overline{\text{RSTI1}}$ (level trigger input)
- $\overline{\text{RSTI2}}$ (edge trigger input)
- $\overline{\text{RESET}}$ (level trigger input)

(a) Restart in IDLE mode

The restart sequence from the clock output stop state in the IDLE mode is shown in Figure 3.7. In the restart in the IDLE mode, the clock output is restarted in a relatively short delay time as the internal oscillator is in operation even when the clock output is kept stopped.

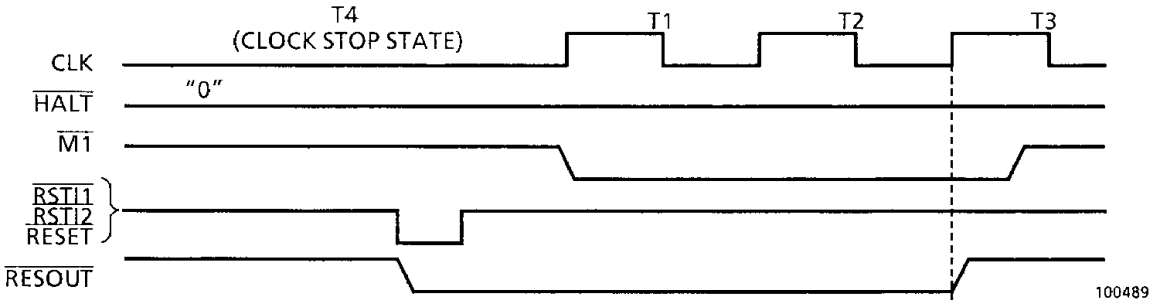

Figure 3.7 Restart Sequence Timing from Clock Stop State (IDLE mode)

(b) Restart in STOP mode

The restart sequence from the clock output stopped state in the STOP mode is shown in Figure 3.8. In restarting the clock output by inputting "0" into $\overline{\text{RSTI1}}$ or $\overline{\text{RSTI2}}$ signal, a warming-up time is automatically provided by the internal counter.

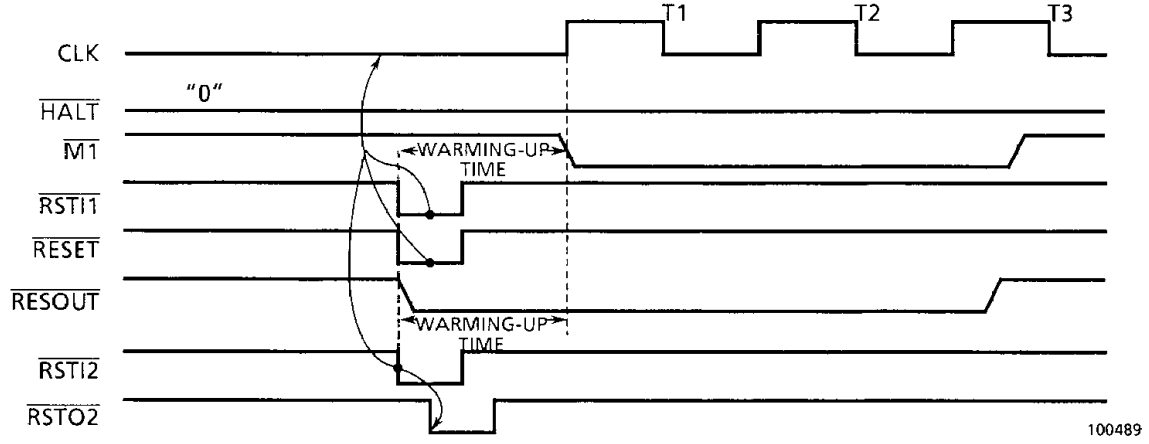

Figure 3.8 Restart Sequence Timing from Clock Stop State (STOP mode)

3.4 METHOD OF USE

Connection of the TMPZ84C61A with MPU when executing the HALT instruction is explained here.

3.4.1 $\overline{\text{RESET}}$ Signal

Figure 3.9 shows the examples of restart timing in the STOP mode when the TLCS-Z80 MPU and TMPZ84C61A use $\overline{\text{RESET}}$ signal commonly.

To reset the TLCS-Z80 MPU, $\overline{\text{RESET}}$ signal must be kept at "0" level for at least 3 clocks. Further, when $\overline{\text{RESET}}$ signal becomes "1" level, MPU is released from the HALT state after the dummy cycle for at least 2T states and executes an instruction starting from address 0000H.

In restarting the clock output in the STOP mode by $\overline{\text{RESET}}$ signal, the internal counter for determining the warming-up time does not operate.

Note that MPU may not be restarted properly due to unstable clock output immediately after the internal oscillator is restarted. Therefore, $\overline{\text{RESET}}$ signal should be kept at "0" level for a sufficient period of time enough to firmly reset MPU by taking stability of crystal oscillation at time of power ON.

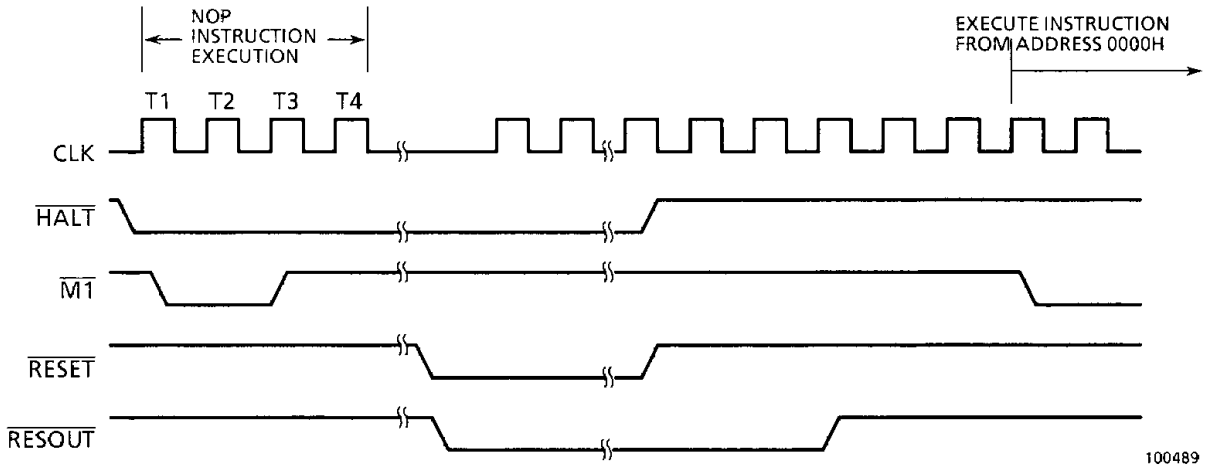

Figure 3.9 Example of Clock Restart Timing by $\overline{\text{RESET}}$ Signal

3.4.2 HALT release by interrupt signal

When the TMPZ84C61A is in the IDLE or STOP mode, the clock output is restarted by $\overline{\text{RSTI1}}$ or $\overline{\text{RSTI2}}$ signal input and MPU starts to run according to that clock input. However, after the clock output, MPU is still in the HALT state and executes the NOP instruction. To release MPU from the HALT state, it is necessary to input the interrupt signal ($\overline{\text{INT}}$ or $\overline{\text{NMI}}$). MPU samples the interrupt signal at the falling edge of the last clock of each instruction (NOP instruction for the HALT state).

(1) When non-maskable interrupt ($\overline{NMI}$) is used:

The non-maskable interrupt is the edge trigger input, and there is flip-flop (F/F) in MPU. The state of this internal NMI F/F is sampled at the falling edge of the last clock of an instruction. Therefore, if a short low active ("0") pulse has been input before the interrupt signal sampling timing, this interrupt request is accepted.

$\overline{RSTI2}$ input of the TMPZ84C61A is output to $\overline{RSTO2}$ through the internal circuit. It is therefore recommended that the restart signal is generated to the $\overline{RSTI2}$ input terminal and $\overline{RSTO2}$ signal is output into the $\overline{NMI}$ terminal of MPU.

(2) When maskable interrupt ($\overline{INT}$) is used :

For maskable interrupt, the interrupt enable flip-flop (IFF) must be set to "1" before "0" of $\overline{INT}$ input signal is recognized. In the connection of MPU and TMPZ84C61A, this interrupt signal $\overline{INT}$ is jointly used with the restart signal $\overline{RSTI1}$ of the TMPZ84C61A. Shown in Figure 3.10 are examples of the timing when $\overline{RSTO2}$ output signal of the TMPZ84C61A is input to $\overline{NMI}$ of MPU and $\overline{RSTI1}$ signal of the TMPZ84C61A is jointly used with $\overline{INT}$ signal of MPU.

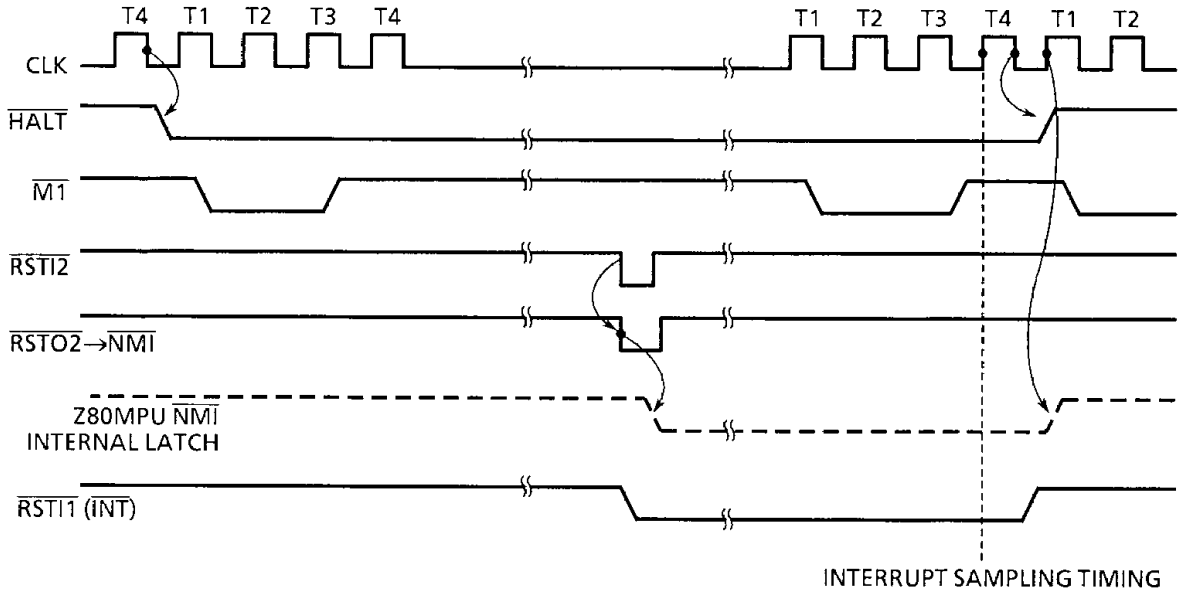

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Figure 3.10 Example of Clock Restart Timing by $\overline{RSTI1}$ or $\overline{RSTI2}$ Signals

3.4.3 Example of connection

A connecting example of the TMPZ84C61A and MPU is shown in Figure 3.11.1. This figure shows an example when $\overline{RSTO2}$ output signal of the TMPZ84C61A is input into $\overline{NMI}$ of MPU by jointly using $\overline{RESET}$ signal with MPU and $\overline{RSTI1}$ signal of the TMPZ84C61A and $\overline{INT}$ signal of MPU are jointly used.

Also refer to Figure 3.11.2 for the example of connecting the $\overline{RESOUT}$ signal of TMPZ84C61A with the $\overline{RESET}$ signal of the MPU.

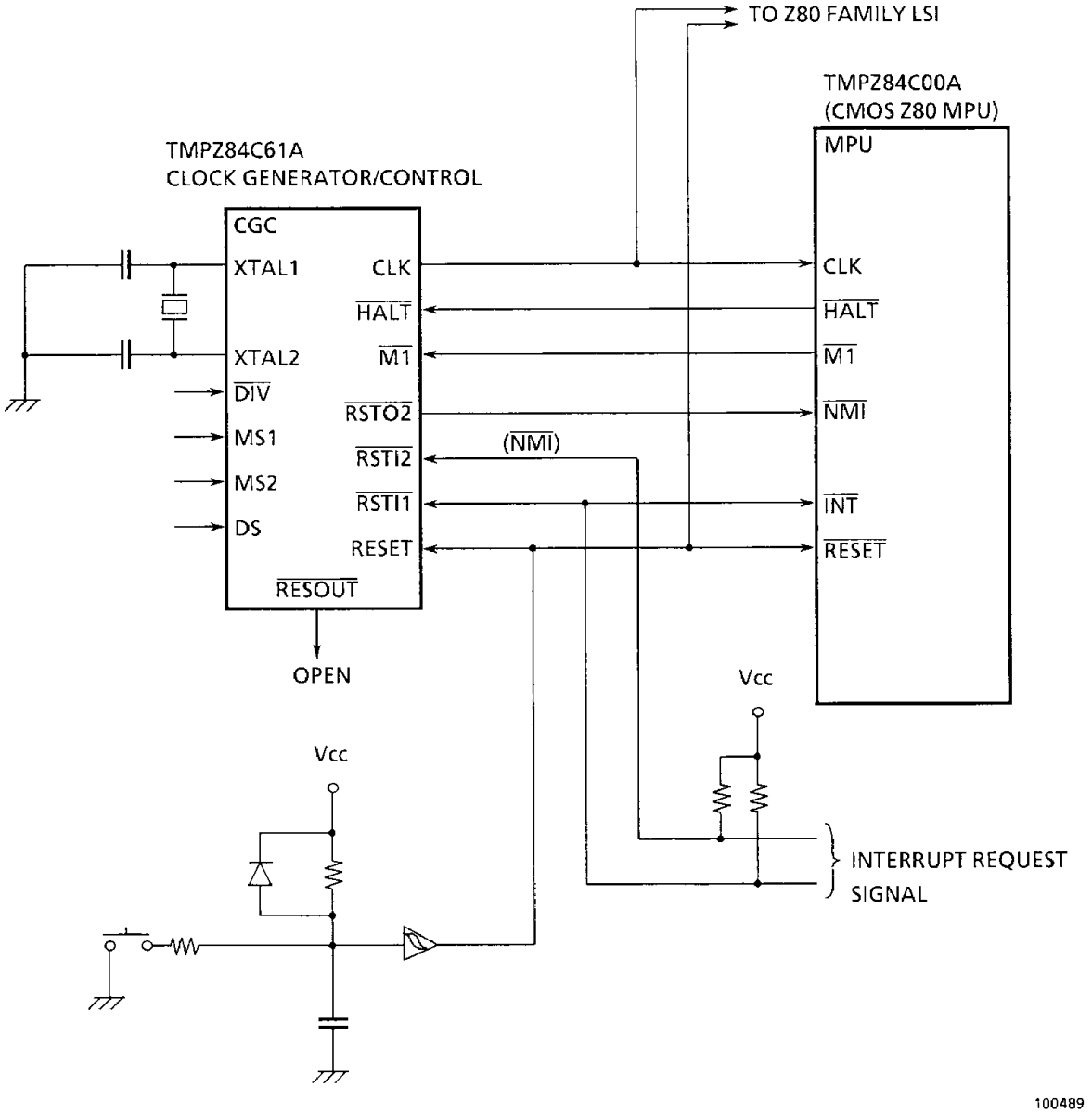

Figure 3.11.1 Connecting Example of the TMPZ84C61A and TLCS-Z80 MPU without using $\overline{\text{RESOUT}}$

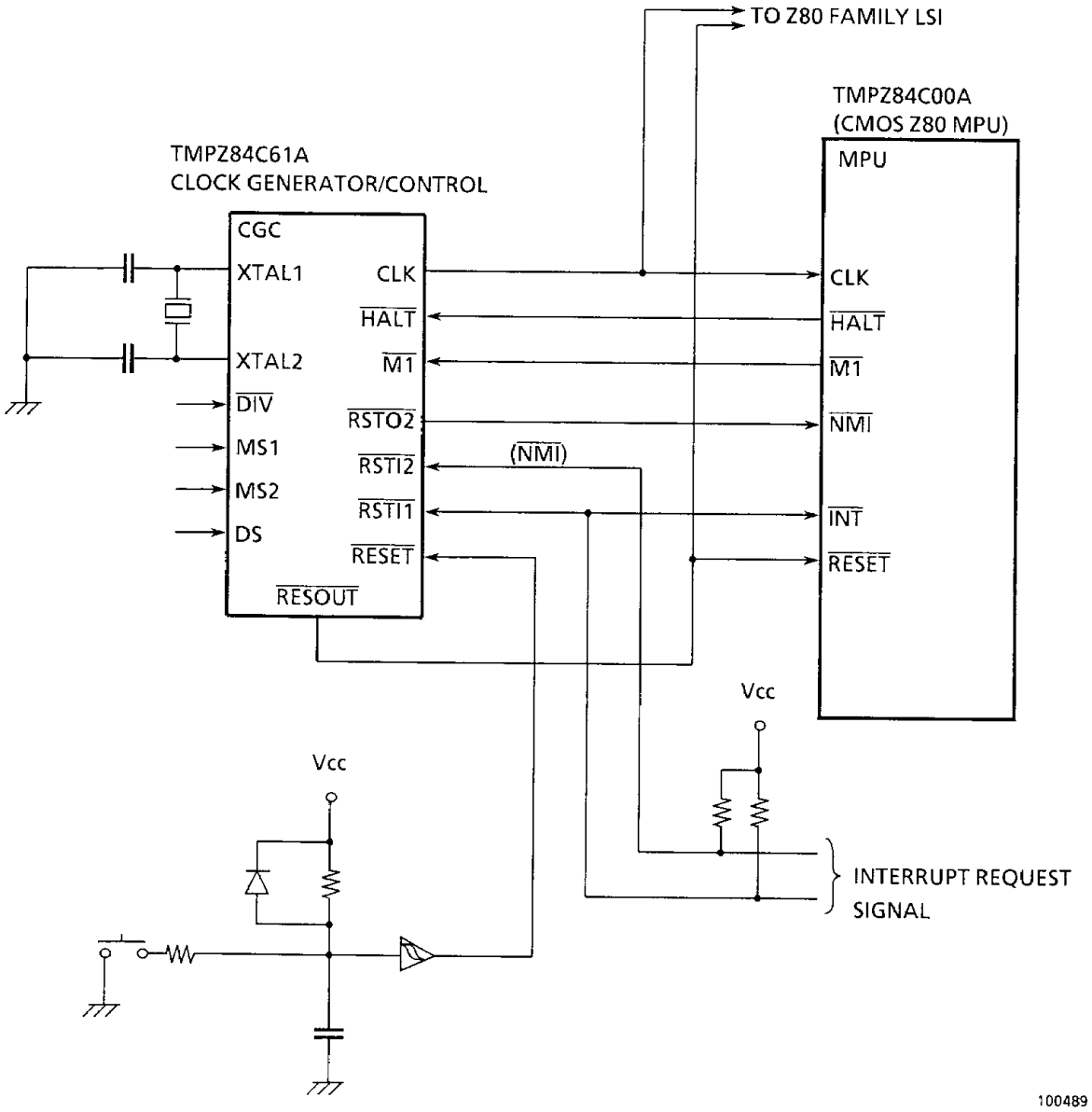

Figure 3.11.2 Conncting Example of the TMPZ84C61A and TLCS-Z80 MPU using $\overline{\text{RESOUT}}$

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	− 0.5 to + 7	V
V_{IN}	Input Voltage	− 0.5 to Vcc + 0.5	V
P_D	Power Dissipation (TA = 85°C)	250	mW
T_{SOLDER}	Soldering Temperature (10sec)	260	°C
T_{stg}	Storage Temperature	− 65 to 150	°C
T_{opr}	Operating Temperature	− 40 to 85	°C

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4.2 DC ELECTRICAL CHARACTERISTICS

TOPR = −40°C to 85°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	ITEM	TEST CONDITIOIN	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage (Except XTAL 1,2)		− 0.5	−	0.8	V
V_{IH}	Input High Voltage (Except XTAL 1,2)		2.2	−	V_{CC}	V
V_{OLC}	Output Low Vlotage (CLK)	I_{OL} = 2.0mA	−	−	0.4	V
V_{OL}	Output Low Vlotage (Except CLK)	I_{OL} = 2.0mA	−	−	0.4	V
V_{OHC}	Output High Vlotage (CLK)	I_{OH} = − 250μA	V_{CC} − 0.6	−	−	V
V_{OH1}	Output High Vlotage (Except CLK)	I_{OH} = − 1.6mA	2.4	−	−	V
V_{OH2}	Output High Vlotage (Except CLK)	I_{OH} = − 250μA	V_{CC} − 0.8	−	−	V
I_{IL}	Input Leak Current	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	−	−	± 1	μA

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DIV = "0" (6MHz) (Oscillation frequency: 12MHz)

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ICC1	Supply Current (Operation) (RUN Mode)	V_{CC} = 5V, fXTAL = 12MHz $V_{IHC} = V_{IH} = V_{CC} - 0.2V$, $V_{ILC} = V_{IL} = 0.2V$	—	3	5	mA
ICC2	Supply Current (STOP Mode)	V_{CC} = 5V, $V_{IHC} = V_{IH} = V_{CC} - 0.2V$, $V_{ILC} = V_{IL} = 0.2V$	—	0.3	10	μA
ICC3	Supply Current (IDLE Mode)	V_{CC} = 5V, fXTAL = 12MHz $V_{IHC} = V_{IH} = V_{CC} - 0.2V$, $V_{ILC} = V_{IL} = 0.2V$	—	0.5	1	mA

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4.3 AC ELECTRICAL CHARACTERISTICS

TOPR = −40°C to 85°C, VCC = 5V ± 10%, VSS = 0V, $\overline{DIV}$ = "1", $\overline{DIV}$ = "0"

NO.	SYMBOL	ITEM		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	TcC	CLK Frequency		CL = 100pF	165	–	–	ns
2	TwCh	High CLK width			70	–	–	ns
3	TwCl	Low Clk width			70	–	–	ns
4	TrC	CLK rising time			–	–	12	ns
5	TfC	CLK falling time			–	–	12	ns
6	TsHALT (M1r)	$\overline{HALT}$ set-up time			10	–	–	ns
7	TwRSTI1	Low $\overline{RSTI1}$ width			70	–	–	ns
8	TwRSTI2	Low $\overline{RSTI2}$ width			160	–	–	ns
9	TdRSTO2 ($\overline{RSTI2}$f)	$\overline{RSTO2}$ delay time			–	–	60	ns
10	TwRSTO2	Low $\overline{RSTO2}$ width			70	–	–	ns
11	TwRESET	Low $\overline{RESET}$ width			70	–	–	ns
12	TRST1S	CLK restart time by $\overline{RSTI1}$ (STOP Mode)	DS = 0		–	$(2^{17} + 2.5)\ T_{CC}$	–	ns
			DS = 0		–	$(2^{14} + 2.5)\ T_{CC}$	–	ns
13	TRST2S	CLK restart time by $\overline{RSTI2}$ (STOP Mode)	DS = 0		–	$(2^{17} + 2.5)\ T_{CC}$	–	ns
			DS = 0		–	$(2^{14} + 2.5)\ T_{CC}$	–	ns
14	TRST1I	CLK restart time by $\overline{RSTI1}$ (IDLE mode)			2.5 TcC			ns
15	TRST2I	CLK restart time by $\overline{RSTI2}$ (IDLE mode)			2.5 TcC			ns
16	TRESETI	CLK restart time by $\overline{RESET}$ (IDLE mode)			1 TcC			ns

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Note :Test conditions

1) Input high voltage VIH = 2.4V, Input low voltage VIL = 0.4V
2) Testing point
   a VOH = 2.2V, VOL = 0.8V (except CLK output)
   b CLK Output : VOH = VCC − 0.6V, VOL = 0.4V

4.4 CAPACITANCE

$TA = 25°C$

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{CLOCK}	Clock Input Capacitance (XTAL2)	f = 1MHz All terminals except that to be measured should be earthed.	–	–	15	pF
C_{IN}	Input Capacitance		–	–	5	pF
C_{OUT}	Output Capacitance		–	–	6	pF

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4.5 TIMING DIAGRAM

Figure 4.1 to 4.4 show the basic timings of respective operation. Numbers shown in the figures correspond with those in the AC Electrical Characteristics Table in 4.3.

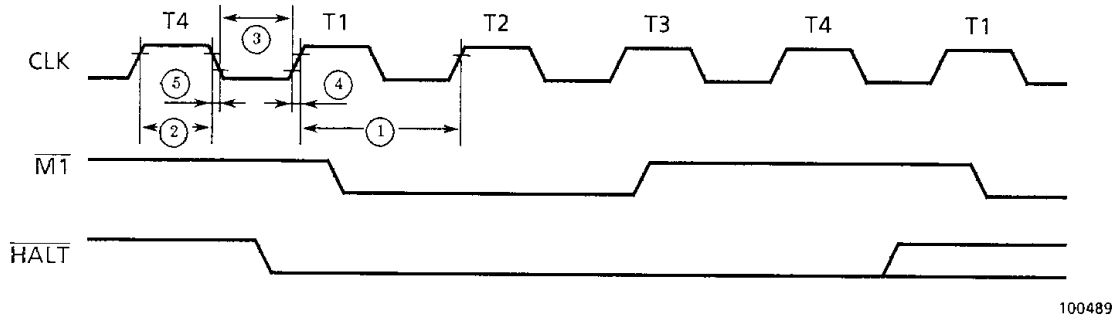


Figure 4.1 Clock Timing

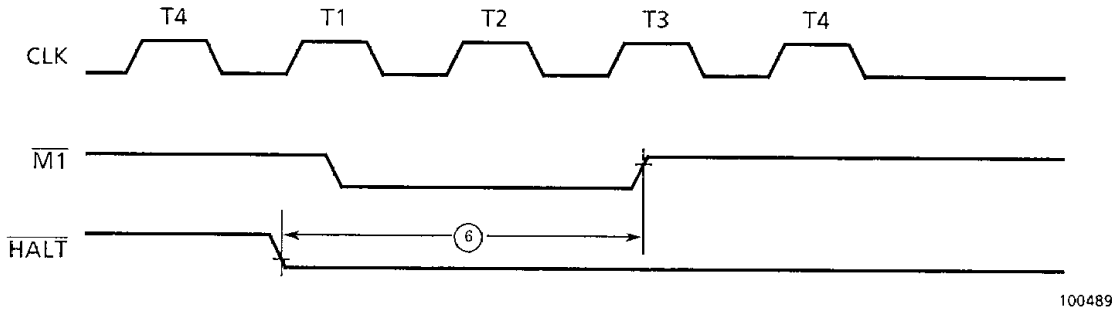


Figure 4.2 Clock Stop Timing (IDLE/STOP Mode)

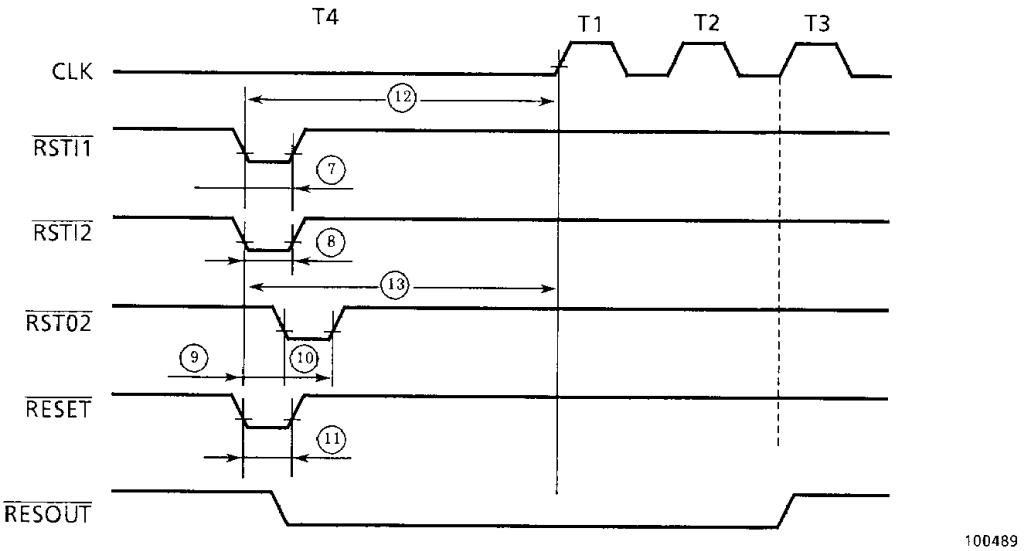


Figure 4.3 Clock Restart Timing (STOP Mode)

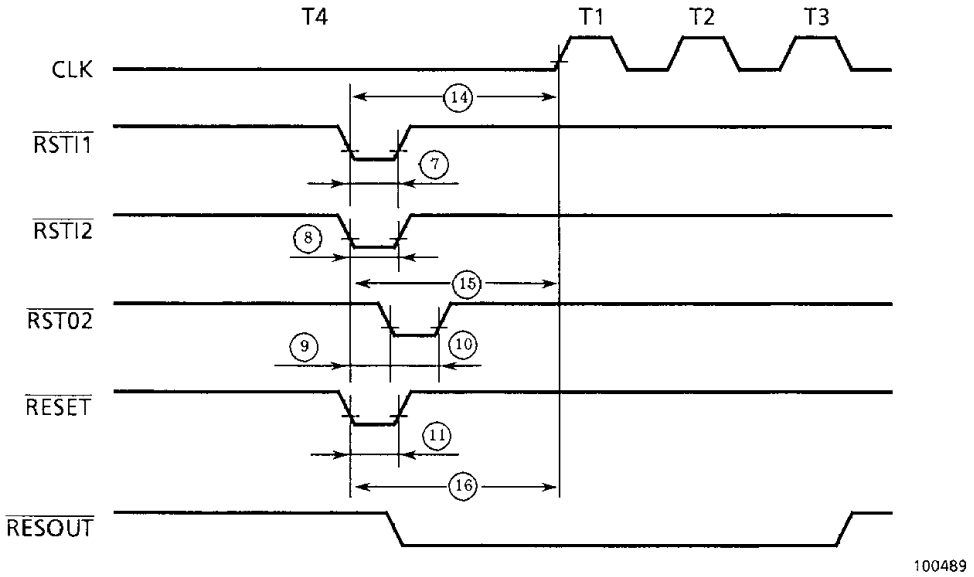
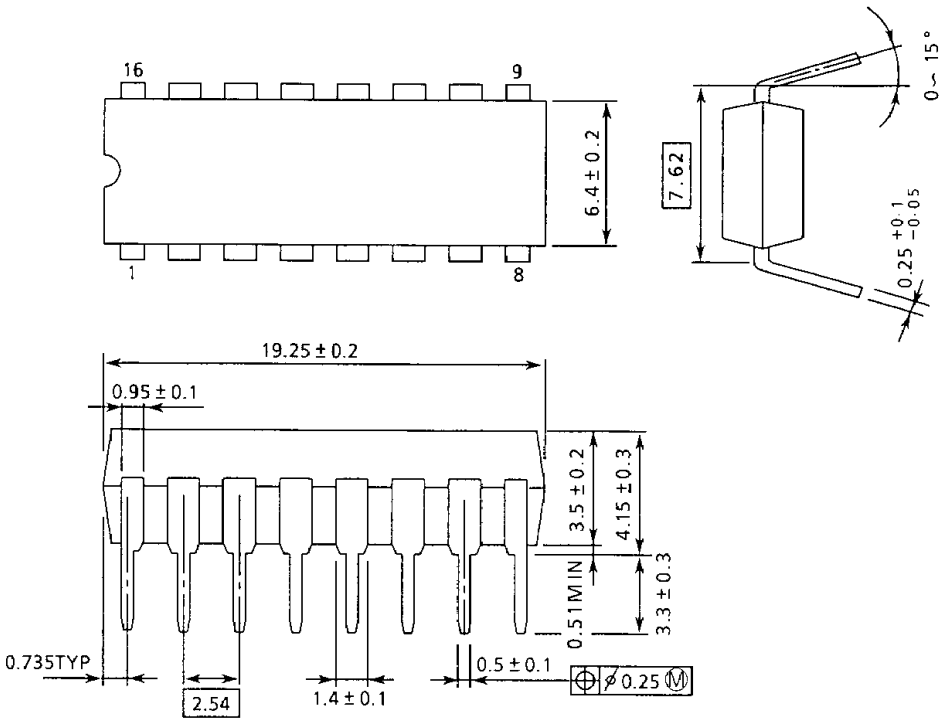


Figure 4.4 Clock Restart Timing (IDLE Mode)

5. OUTLINE DRAWING

DIP16-P-300A

Unit : mm



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Note :

1. This dimension is measured at the center of bending point of leads.
2. Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.16 leads.

6. PRECAUTIONS

When the TMPZ84C61A is used, care should be taken to the following points.

(1) In using $\overline{\text{RESET}}$ signal commonly with MPU, hold $\overline{\text{RESET}}$ signal at "0" for a sufficient period of time enough to positively reset MPU. Especially, in case of the restart in the STOP mode using $\overline{\text{RESET}}$ signal, be careful as output of the internal oscillator is not stable.

(2) MPU is not released from the HALT state simply when the clock input is resumed. To release MPU, it is necessary to reset MPU or accept an interrupt request.

(3) Since $\overline{\text{RSTI2}}$ signal of the TMPZ84C61A and $\overline{\text{NMI}}$ signal of MPU are both trailing edge trigger inputs. if both signals are jointly used, $\overline{\text{RSTI2}}$ signal only may be detected and $\overline{\text{NMI}}$ signal may not be detected in some cares. This trouble can be solved by using $\overline{\text{RSTO2}}$ signal, which is the output signal of $\overline{\text{RSTI2}}$ input signal, as the input signal to $\overline{\text{NMI}}$ in order to a sufficient pulse for the detection.