TMPZ84C01F, TMPZ84C02AF-6
TLCS-Z80MPU : 8-BIT MICROPROCESSOR
CMOS Z80 8-BIT MICROPROCESSOR

1. OUTLINE AND FEATURES

The TMPZ84C01F/02AF-6 is an 8-bit microprocessor (hereinafter referred to as MPU) with a built-in clock generator/controller, which provides low power operation and high performance.

Built into the TMPZ84C01F/02AF-6 are a control function and clock generator for the standby function in addition to paired 6 general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits. TMPZ84C02AF-6 can insure duty 50% clock output easily with Internal Oscillation Divider.

The TMPZ84C01F/02AF-6 is fabricated using Toshiba's CMOS Silicon Gate Technology and molded in a 44-pin mini-flat package.

The principal functions and features of the TMPZ84C01F/02AF-6 are as follows.

(1) Instruction Set compatible with the Zilog's Z80 MPU.

(2) Low power consumption

Table 1.1 Operation modes and Supply Current (Vcc = 5v.TYPICAL)

Product name	Operating frequency	RUN MODE	IDLE1 MODE	IDLE2 MODE	STOP MODE
TMPZ84C01F	fosc = 4MHz fCLK = 4MHz	15mA	1mA	3mA	0.5μA
TMPZ84C02AF-6	fosc = 12MHz fCLK = 6MHz	20mA	1.5mA	4.5mA	0.5μA

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(3) DC to 6MHz operation (at 5V ± 10%)

(4) Single 5V power supply (at 5V ± 10%)

(5) Operating temperature (−40°C to 85°C)

(6) On-chip clock generator

(7) In the HALT state, the following 4 modes are selectable:

- Run mode
- IDLE 1 mode
- IDLE 2 mode
- STOP mode

In the following explanation for the same content, IDLE1 Mode and IDLE2 Mode are referred to as IDLE1/2.

(8) Powerful set of 158 instructions available

(9) Powerful interrupt function

(a) Non-maskable interrupt terminal ($\overline{NMI}$)

(b) Maskable interrupt terminal ($\overline{INT}$)

The following 3 modes are selectable ;

- 8080 compatible interrupt mode (interrupt by Non-Z80 family peripharal LSI) (Mode 0)
- Restart interrupt (Mode 1)
- Daisy chain structure interrupt using Z80 family peripheral LSI (Mode 2)

(10) An auxiliary register provided to each of general purpose registers.

(11) Two index registers

(12) 10 addressing modes

(13) Built-in refresh circuit for dynamic memory.

(14) Molded in 44-pin mini flat package

(15) Built-in clock divider for insuring duty 50% easily (TMPZ84C/02AF-6)

(16) Low voltage oparation Vcc = 2.7V~5.5V (TMPZ84C01F)

Further, in the following text and explanations for charts and tables, hexadecimal numbers are directly used without giving an identification to explanation of address, etc. to the extent not to cause confusions.

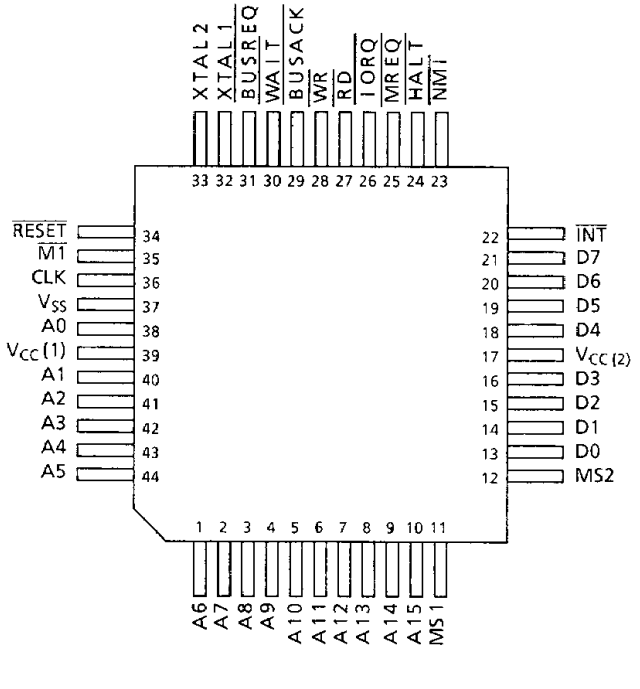
Note : Z80 is a trademark of Zilog Inc., U.S.A.

2. PIN CONNECTIONS AND PIN FUNCTIONS

The pin connections and I/O pin names and brief functions of the TMPZ84C01/02A are shown below.

2.1 PIN CONNECTIONS

The pin connections of the TMPZ84C01/02A are as shown in Figure 2.1.



Note : Connect Pin 39 and Pin 17 externally.

Figure 2.1 Pin Connections (Top View)

2.2 PIN NAMES AND FUNCTIONS

I/O pin names and functions are as shown in Table 2.1.

Table 2.1 Pin Names and Functions (1/3)

Pin Name	Number of Pin	Input/Output 3-state	Function
A0~A15	16	Output 3-state	16-bit address bus. Specify addresses of memories and I/O to be accessed. During the refresh period, addresses for refreshing are output.
MS1, MS2	2	Input	Mode selection input. One of 4 modes (RUN, IDLE1/2, STOP) is selected according to the state of these 2 pins.

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Table 2.1 Pin Names and Functions (2/3)

Pin Name	Number of Pin	Input/Output 3-state	Function
D0-D7	8	I/O 3-state	8-bit bidirectional data bus.
$\overline{INT}$	1	Input	Maskable interrupt request signal. Interrupt is generated by peripheral LSI. This signal is accepted if the interrupt enable flip-flop (IFF) is set at "1". $\overline{INT}$ is normally used on Wired-OR. In this case, a pull-up resistor is externally connected.
$\overline{NMI}$	1	Input	Non-maskable interrupt request signal. This interrupt request has the higher priority than the maskable interrupt request and does not rely upon the state of the interrupt enable flip-flop (IFF).
$\overline{HALT}$	1	Output	Halt signal. MPU execute HALT instruction and when the halt state is resulted. "0" is output.
$\overline{MREQ}$	1	Output 3-state	Memory request signal. When an effective address for memory access is on the address bus, "0" is output.
$\overline{IORQ}$	1	Output 3-state	I/O request signal. When addresses for I/O are on the lower 8 bits (A0-A7) of the address bus in the I/O operation, "0" is output. In addition, $\overline{IORQ}$ signal is output together with $\overline{M1}$ signal at time of interrupt acknowledge cycle to inform peripheral LSI of the state that the interrupt response vector may be put on the data bus.
$\overline{RD}$	1	Output 3-state	Read signal "0" signal is output for a period when MPU can receive data from a memory or peripheral LSI. It is possible to put data from a specified peripheral LSI or memory on the MPU data bus after gating by this signal.
$\overline{WR}$	1	Output 3-state	Write signal. This signal is output when data to be stored in a specified memory or peripheral LSI is on the MPU data bus.
$\overline{BUSACK}$	1	Output	Bus acknowledge signal. In response to $\overline{BUSREQ}$ signal, this signal informs a peripheral LSI of the fact that the address bus, data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$ signals have been placed in the high impedance state.
$\overline{WAIT}$	1	Input	Wait signal. $\overline{WAIT}$ signal is a signal to inform MPU of specified memory or peripheral LSI which is not ready for data transfer. As long as $\overline{WAIT}$ signal as at "0" level, MPU is continuously kept int the wait state.

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Table 2.1 Pin Names and Functions (3/3)

Pin Name	Number of Pin	Input/Output 3-state	Function
$\overline{BUSREQ}$	1	Input	Bus request signal. $\overline{BUSREQ}$ signal is a signal requesting placement of the address bus , data bus, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$ signals in the high impedance state. $\overline{BUSREQ}$ signal is normally used on wired-OR. In this case, a pull-up resistor is externally connected.
$\overline{RESET}$	1	Input	Reset signal. $\overline{RESET}$ signal is used for initialization MPU and must be kept in active state ("0") for a period of at least 3 clocks.
$\overline{MI}$	1	Output	Signal showing machine cycle 1. "0" is output together with $\overline{MREQ}$ signal in the operation code fetch cycle. This signal is output for every opcode fetch when 2byte opcode is executed. In the maskable interrupt acknowledge cycle, this signal is output together with $\overline{IORQ}$ signal.
XTAL 1 (XIN) XTAL 2 (XOUT)	2	Input output	Crystal oscillator connecting terminal. For 01F, connects an oscillator having the oscillation frequency as high as the system clock (CLK) frequency. For 02AF/02AF-6, connects an oscillator having the oscillation frequency 2 times as high as the system clock (CLK) frequency.
CLK	1	Output	Single-phase clock output. When the HALT instruction in STOP Mode is executed, MPU stops its operation and holds clock output at "0" level.
Vcc (1), (2)	2	Power supply	+5 Connent 39 pin and 17 pin externally.
Vss	1	Power supply	0V

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3. FUNCTIONAL DESCRIPTION

The system configuration, functions and basic operation of the TMPZ84C01F/02AF-6 are described here.

3.1 BLOCK DIAGRAM

The block diagram of the interval configuration is shown in Figure 3.1.

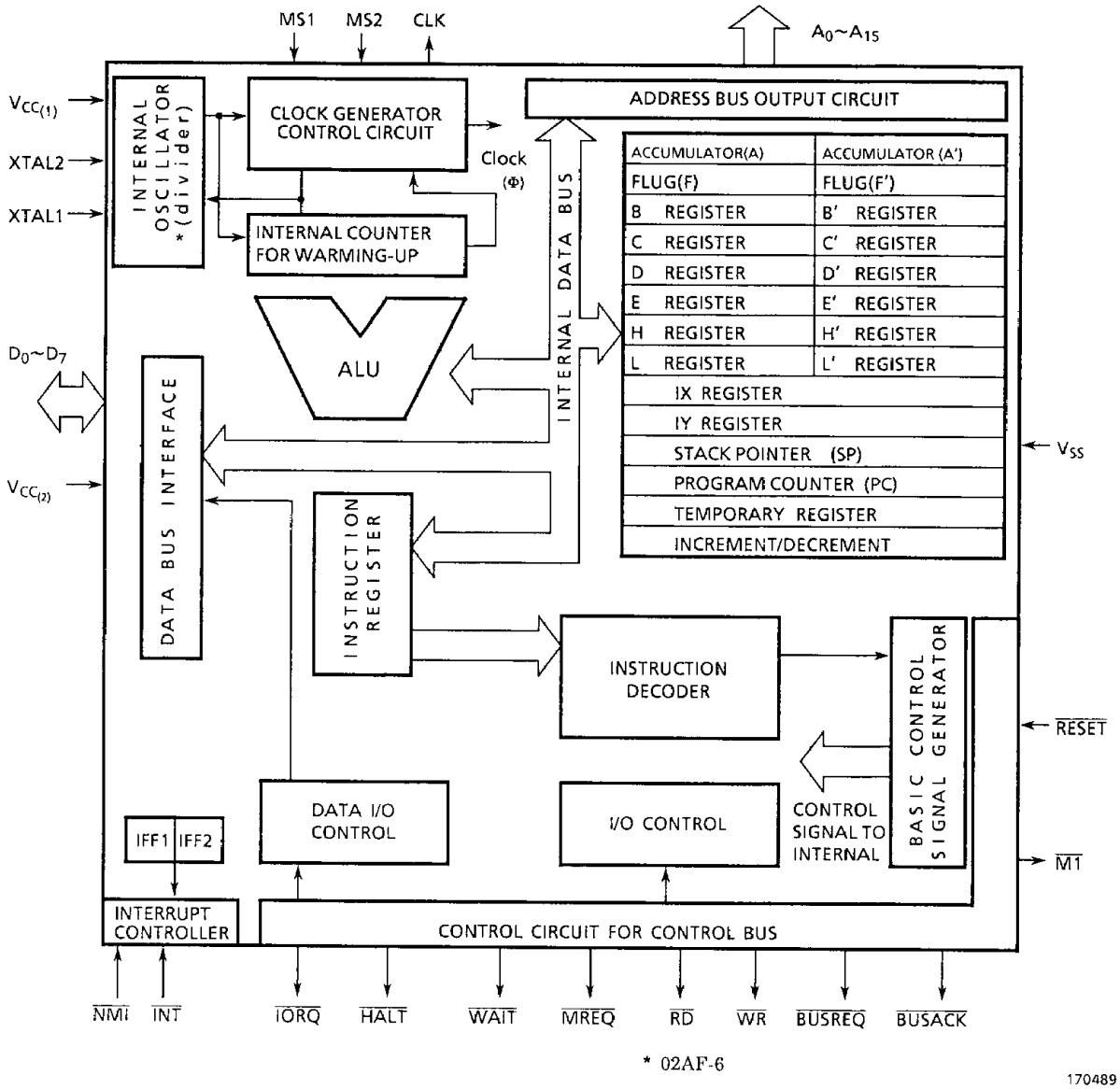

Figure 3.1 Block Diagram

3.2 SYSTEM CONFIGURATION

The TMPZ84C01F/02AF-6 has a built-in system clock generator for CMOS Z80 in addition to the standard functions of the TMPZ84C00A CMOS Z80 MPU.

The explanation is provided here with emphases placed on the halt function relative to the clock generator, which is an additional function. The internal register group, reset and interrupt function are identical to those of the TMP84C00A. For details please refer to the data sheet for the TMPZ84C00A.

In this section, the following principal components and functions will be described,

(1) Generation of clock

(2) Operation mode

(3) Warming-up time at time of restart

3.2.1 Generating the system clock

The TMPZ84C01F/02AF-6 has a built-in oscillation circuit and required clock can be easily generated by connecting an oscillator to the external terminals (XTAL1, XTAL2). For the TMPZ84C01F, Clock in the same frequency as input oscillation frequency is generated. As the TMPZ84C02AF-6 has a built-in divider, Clock in the half frequency as input oscillation frequency is generated.

Examples of oscillator connection are shown in Figure 3.2.

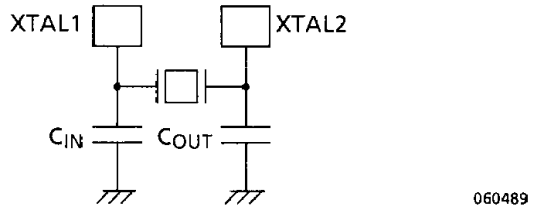

Figure 3.2 Example of Oscillator Connection

Table 3.1 External connecting capacitance

Oscillation Frequency	CIN	COUT	Application Product
4MHz	22PF	33PF	TMPZ84C01F
8MHz	22PF	33PF	TMPZ84C02AF-6
12MHz	33PF	33PF	TMPZ84C02AF-6

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In case of using Crystal oscillator, please use products with the following characteristics or use the following maker's products.

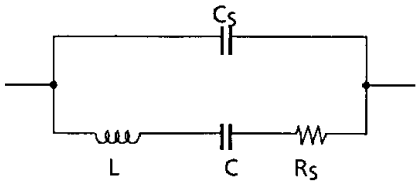

Figure 3.2 Crystal oscillator equivalent circuit

Table 3.2 Crystal oscillator necessary characteristics

Oscillation Frequency	CS	Rs	Application Product
4MHz	under4PF	under50Ω	TMPZ84C01F
8MHz	under4PF	under30Ω	TMPZ84C02AF-6
12MHz	under4PF	under25Ω	TMPZ84C02AF-6

Table 3.3 Crystal oscillator of recommendation

Oscillation Frequency	Product name	Maker
4MHz	MR4000-C20	Tokyo Denpa Inc.
8MHz	MR8000-C20	
12MHz	MR12000-C20	

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3.2.2 Operation modes

There are 4 kinds of operations modes available for the TMPZ84C01F/02AF-6 in connection with generation of clock ; RUN Mode, IDLE1/2 Modes and STOP Mode. One of these modes is selected by the mode select inputs (MS1, MS2).

The operation mode is effective when the halt instruction is executed and when the halt instruction is not executed, clock is supplied continuously. Restart of MPU from the stopped state under IDLE1/2 Mode or STOP Mode is effected by inputting either $\overline{\text{RESET}}$ signal or interrupt signal ($\overline{\text{INT}}$ or $\overline{\text{NMI}}$).

Operations of these modes in the halt state are shown in Table 3.4.

Table 3.4 Clock Generating Operation Modes

Operation Mode	MS1	MS2	Description at HALT State
RUN Mode	1	1	MPU continues the operation and supplies clock to the outside continuously.
IDLE1 Mode	0	0	The internal oscillator's operation only is continued and clock (CLK) output as well as internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
IDLE2 Mode	0	1	The internal oscillator's operation and clock (CLK) output are continued but the internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.
STOP Mode	1	0	All operations of the internal oscillator, clock (CLK) output, and internal operation are stopped at "0" level of T4 state in the halt instruction operation code fetch cycle.

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3.2.3 Warming-up time at time of restart (STOP Mode)

When MPU is released from the halt state by accepting an interrupt request,MPU, then, will execute an interrupt service routine. Therefore, when an interrupt request is accepted, MPU starts generation of internal system clock and clock output after a warming-up time by the internal counter ($2^{14}+2.5$) TcC (TcC ; Clock Cycle) to obtain a stabilized oscillation for MPU operation.

Further, in case of the restart by $\overline{\text{RESET}}$ signal, the internal counter does not operate for a quick operation at time of power ON.

3.3 STATUS CHANGE FLOWCHART AND BASIC TIMING

In this section, the status change and basic timing when the TMPZ84C01F/02AF-6 is operating are explained.

3.3.1 Status change flowchart

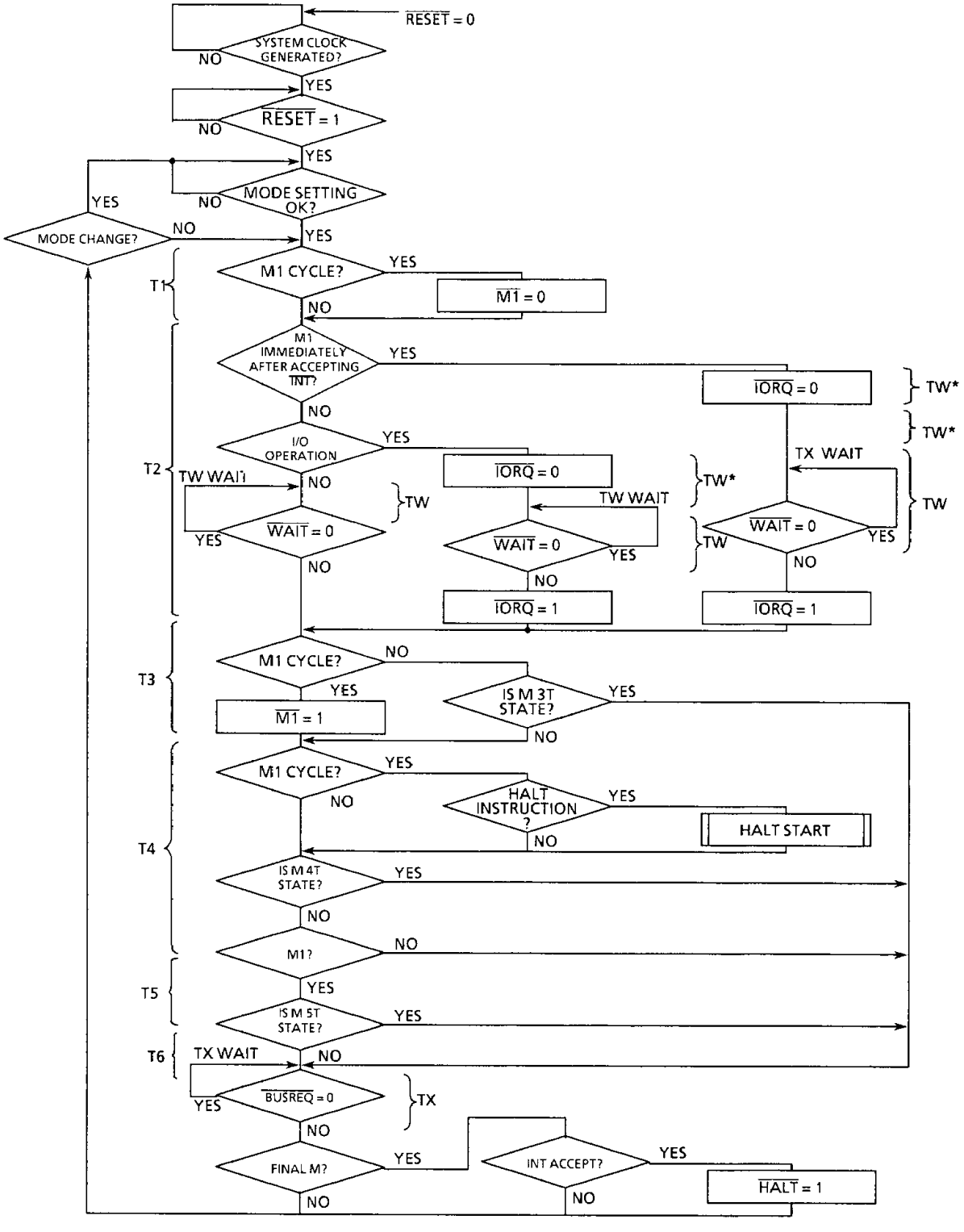

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Figure 3.4 (a) Status Change Flowchart

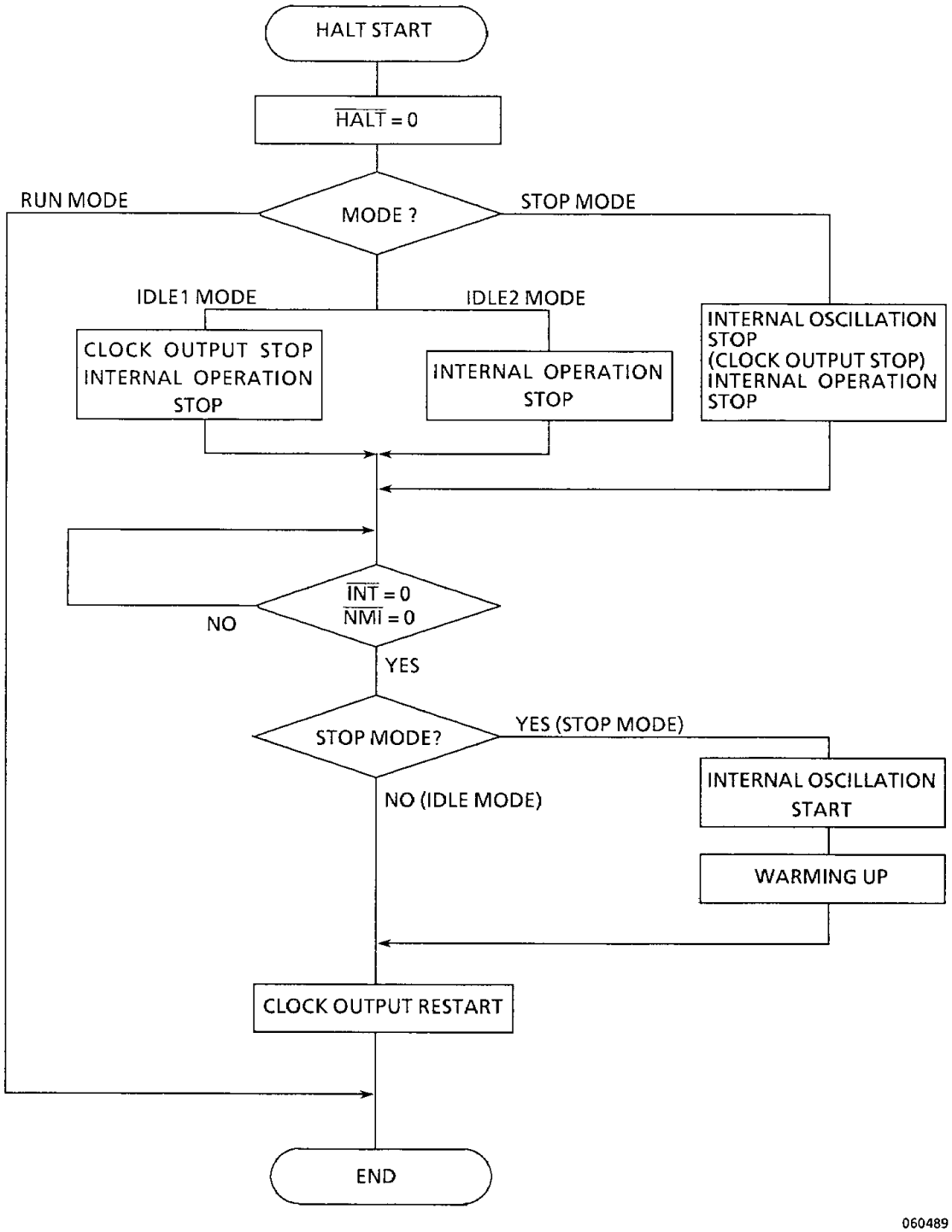

Figure 3.4 (b) Status Change Flowchart

3.3.2 Basic timing

The basic timing is explained here with emphases placed on the halt function relative to the clock generator. Except $\overline{RFSH}$ signal output, the following items are identical to those for the TMPZ84C00A. Refer to the data sheet for the TMPZ84C00A.

- Operation code fetch cycle
- Memory read/write operation
- Input/output operation
- Bus request/acknowledge operation
- Maskable interrupt request accepting operation
- Non-maskable interrupt request accepting operation
- Reset operation

Note that the TMPZ84C01F/02AF-6 dose not have the refresh terminal $\overline{RFSH}$ but refresh address is output on the address bus in the operation code fetch cycle ($\overline{M1}$) as in the TMPZ84C00A since the on-chip refresh control circuit is available.

(1) Operation when HALT instruction is execution

When MPU fetches a halt instruction in the operation code fetch cycle, $\overline{HALT}$ signal goes active (low level) in synchronous with falling edge of T4 state for the peripheral LSI and MPU stops the operation. The system clock generating operation after this differs depending upon the operation mode (RUN Mode, IDLE1/2 Mode or STOP Mode). If the internal system clock is running, MPU continues to execute NOP instruction even in the halt state.

(a) RUN Mode (MS1 = 1, MS2 = 1)

Shown in Figure 3.6 is the basic timing when the halt instruction is executed in RUN Mode.

In RUN Mode, system clock (ø) in MPU and clock output (CLK) to the outside of MPU are not stopped even after the halt instruction is executed. Therefore, until the halt state is released by the interrupt signal ($\overline{MNI}$ OR $\overline{INT}$) or $\overline{RESET}$ signal, MPU continues to execute NOP instruction.

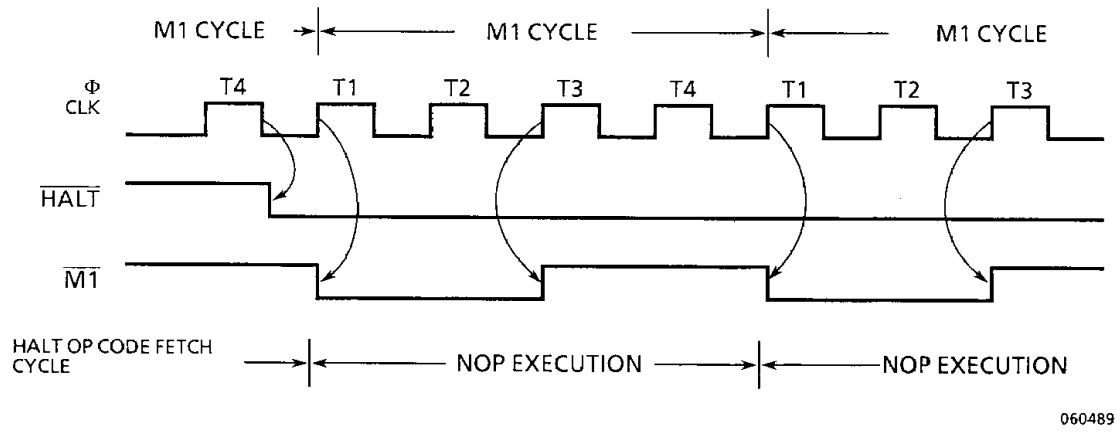

Figure 3.6 Timing of RUN Mode (at Halt Instruction Execution)

(b) IDLE1 Mode (ML1 = 0, MS2 = 0)

Shown in Figure 3.7 is the basic timing when the halt instruction is executed in IDLE1 Mode.

In IDLE1 Mode, system clock (ø) in MPU and clock output (CLK) to the outside of MPU are stopped and MPU stops its operation after the halt instruction is executed.

However, the internal oscillator continues to operate.

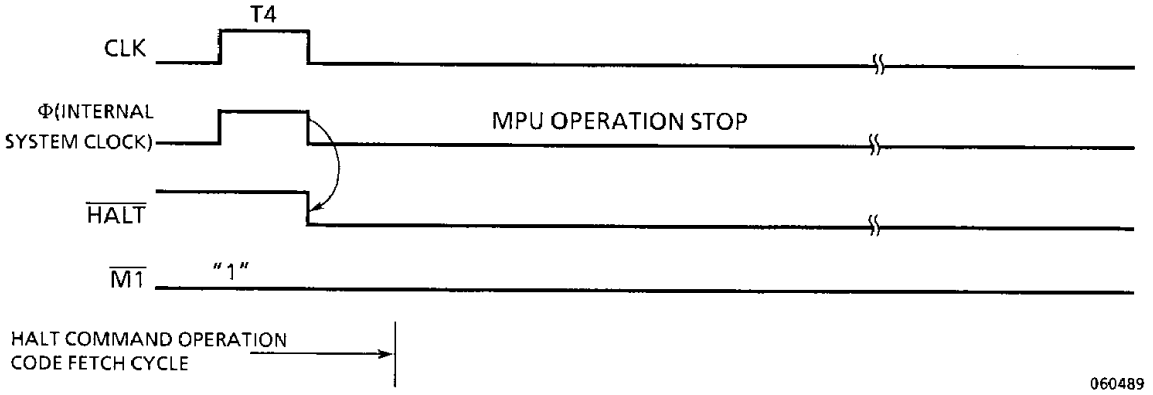

Figure 3.7 IDLE1 Mode Timing (at Halt Instruction Execution)

(c) IDLE2 Mode (MS1 = 0, MS2 = 1)

Shown in Figure 3.8 is the basic timing when the halt instruction is executed in IDLE2 Mode.

In IDLE2 Mode, system clock (ø) in MPU is stopped and MPU stops its operation after the halt instruction is executed.

However,the internal oscillator and clock output (CLK) to the outside of MPU continues to operate.

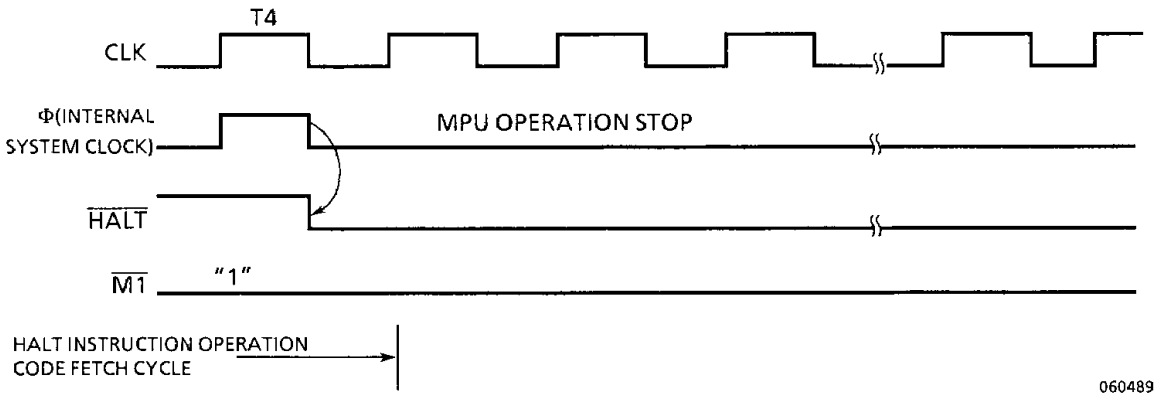

Figure 3.8 IDLE2 Mode timing (at Halt Instruction Execution)

(d) STOP Mode (MS1 = 1,MS2 = 0)

Shown in Figure 3.9 is the basic timing when the halt instruction is executed in STOP Mode.

In STOP Mode, internal operation and internal oscillator are stopped after the halt instruction is executed. Therefore, system clock (ø) in MPU and clock output (CLK) to the outside of MPU are stopped.

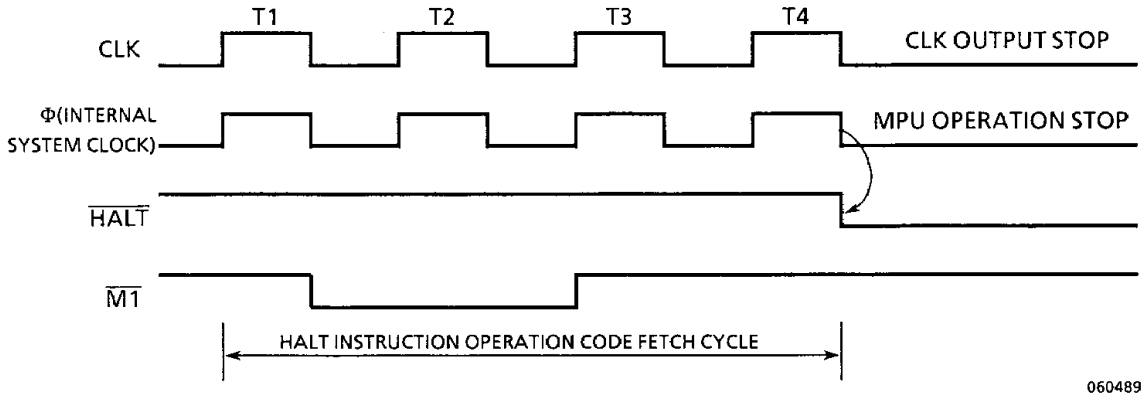

Figure 3.9 STOP Mode Timing (at Halt Instruction Execution)

(2) Release from halt state

The halt state of MPU is released when "0" is input to $\overline{\text{RESET}}$ signal and MPU is reset or an interrupt request is accepted. An interrupt request signal is sampled at the leading edge of the last clock cycle (T4 state) of NOP instruction. In case of the maskable interrupt, interrupt will be accepted by an active $\overline{\text{INT}}$ signal ("0" level). In case of the non-maskable interrupt, if the internal $\overline{\text{NMI}}$ F/F which is set at the leading edge of $\overline{\text{MNI}}$ signal is set to "1", the interrupt is accepted.

However, in case of the maskable interrupt, the interrupt enable flip-flop must have been set to "1". The accepted interrupt process is started from next cycle.

Further, when the internal system clock is stopped (IDLE1/2 Mode, STOP Mode), it is necessary first to restart the internal system clock. The internal system clock is restarted when $\overline{\text{RESET}}$ or interrupt signal ($\overline{\text{NMI}}$ or $\overline{\text{INT}}$) is input.

(a) RUN Mode (MS1, MS2 = 1)

The halt release operation by acceptance of interrupt request in RUN Mode is shown in Figure 3.10.

In RUN Mode the internal system clock is not stopped and therefore, if the interruption signal is recognized at the rise of T4 state of the continued NOP instruction, MPU will executes the interrupt process from next cycle.

The halt release operation by resetting MPU in RUN Mode is shown in Figure 3.11. After reset, MPU will execute an instruction starting from address 0000H. However, in order to reset MPU it is necessary to keep $\overline{\text{RESET}}$ signal at "0" for at least 3 clocks. In addition, if $\overline{\text{RESET}}$ signal becomes "1", after the dummy cycle for at least 2T states, MPU executes an instruction from address 0000H.

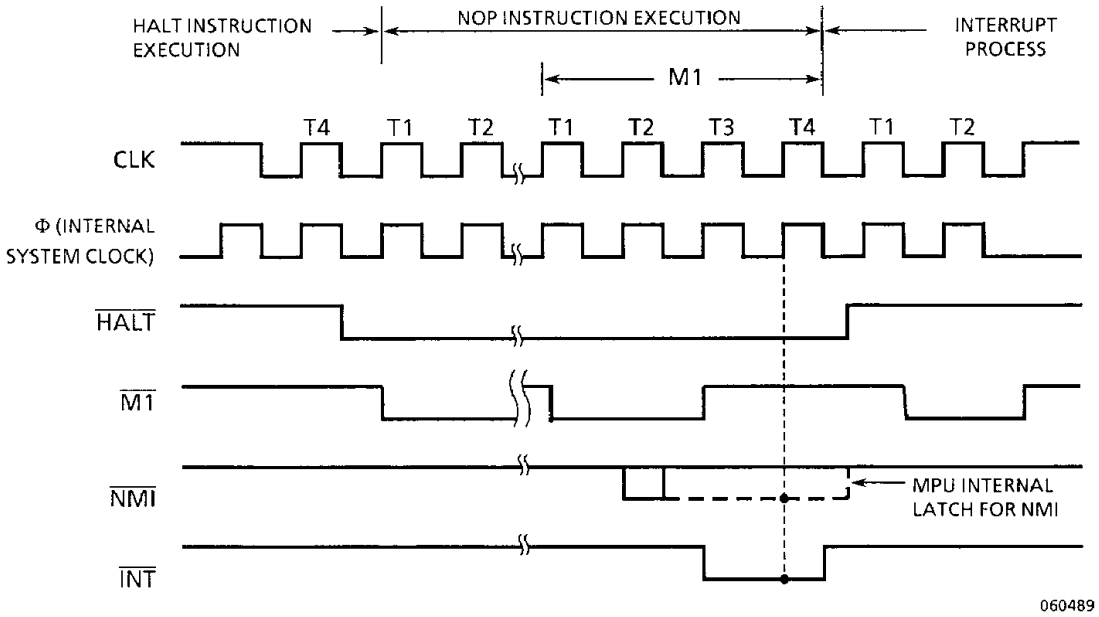

Figure 3.10 Halt Release Operation Timing by Interrupt Request Signal in RUN Mode

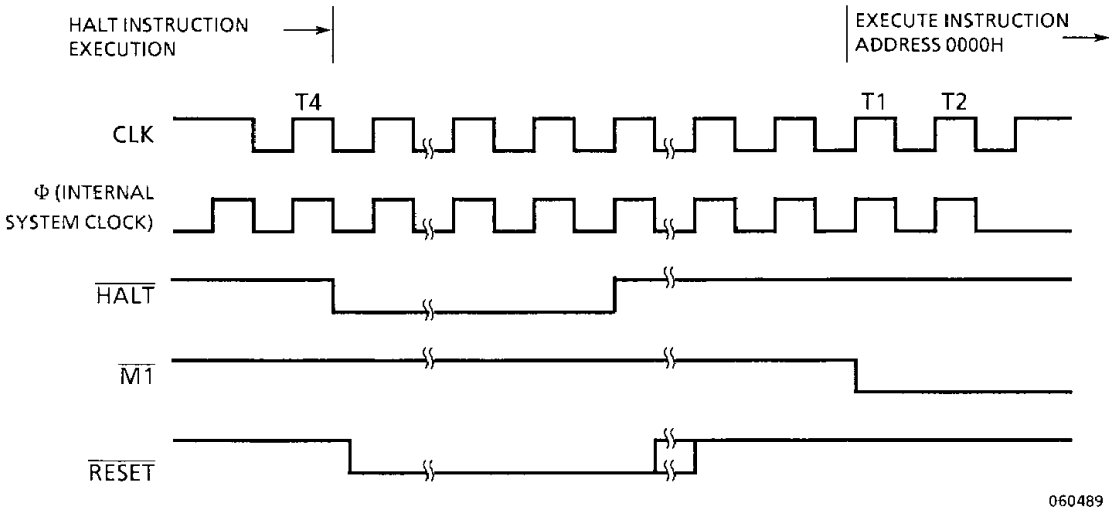

Figure 3.11 Halt Release Operation Timing by Reset in RUN Mode

(b) IDLE1 Mode (MS1 = 0, MS2 = 0), IDLE2 Mode (MS1 = 0, MS2 = 1)

The halt release operation by interrupt signal in IDLE1 Mode is shown in Figure 3.12 (a) and in IDLE2 Mode in Figure 3.12 (b).

When receiving $\overline{\text{NMI}}$ or $\overline{\text{INT}}$ signal, MPU starts the internal system clock operation . In IDLE1 Mode, MPU starts clock output to the outside at the same time. The operation stop of MPU in IDLE1/2 Mode is taken place at "0" level during T4 state in the halt instruction operation code fetch cycle. Therefore, after restarted by the interruption signal, MPU executes one NOP instruction and samples an interrupt signal at the rise of T4 state during the execution of this NOP instruction, and executes the interrupt process from next cycle.

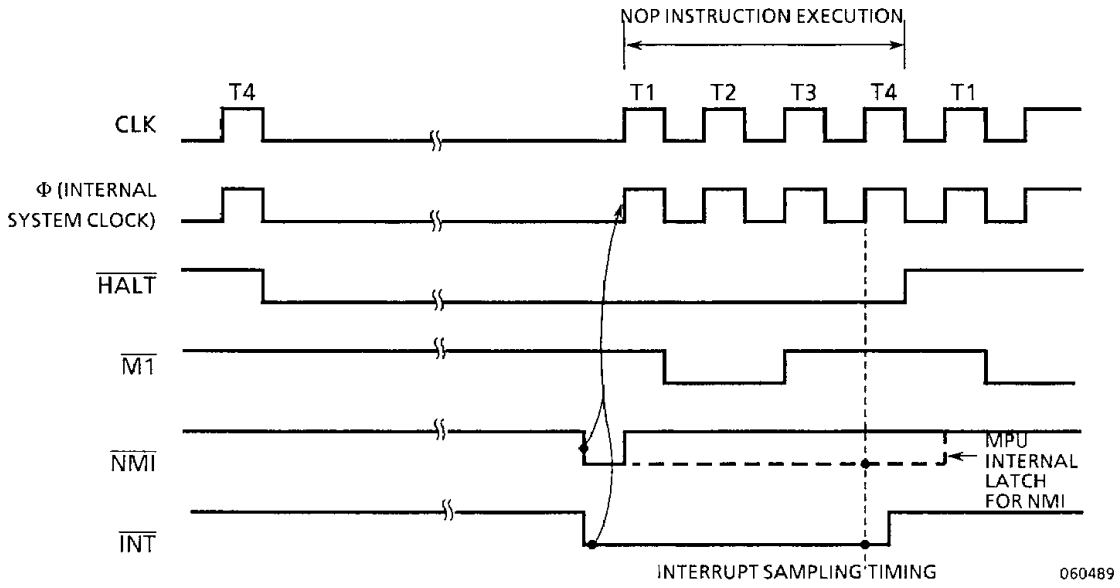

Fig 3.12 (a) IDLE1 Mode

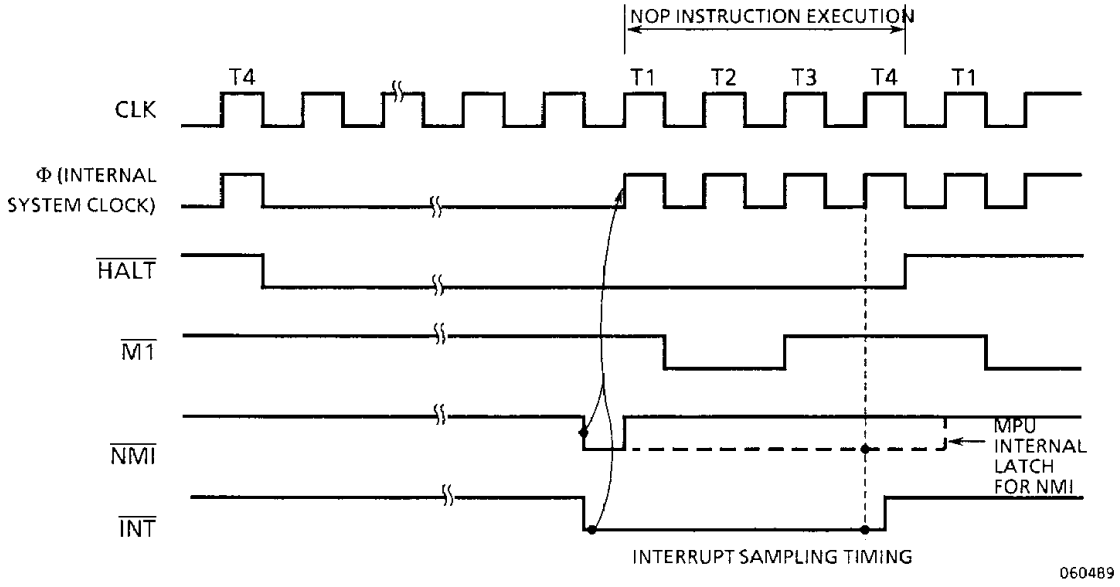

Fig 3.12(b) IDLE2 Mode

Fig.3.12Halt Release Operation Timing by Interrupt Request Signal in IDLE1/2 Mode

If no interrupt signal is accepted during the execution of the first NOP instruction after the internal system clock is restarted, MPU is not released from the halt state and is placed in IDLE1/2 Mode again at "0" level during T4 state of the NOP instruction, stopping the internal system clock. If $\overline{INT}$ signal is not at "0" level at the rise of T4 state, no interrupt request is accepted.

The halt release operation by resetting MPU in IDLE1 Mode is shown in Figure 3.13 (a) and that in IDLE2 Mode in Figure 3.13 (b).

When $\overline{\text{RESET}}$ signal at "0" level is input into MPU, the internal system clock is restarted and MPU will execute an instruction stored in address 0000H.

At time of $\overline{\text{RESET}}$ signal input, it is necessary to take the same care as that in resetting MPU in RUN Mode.

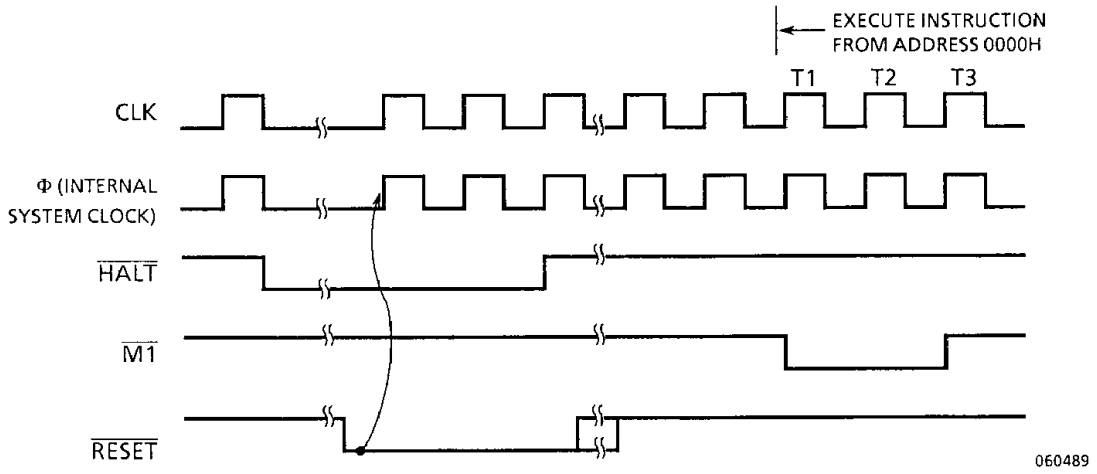

Figure 3.13 (a) IDLE1 Mode

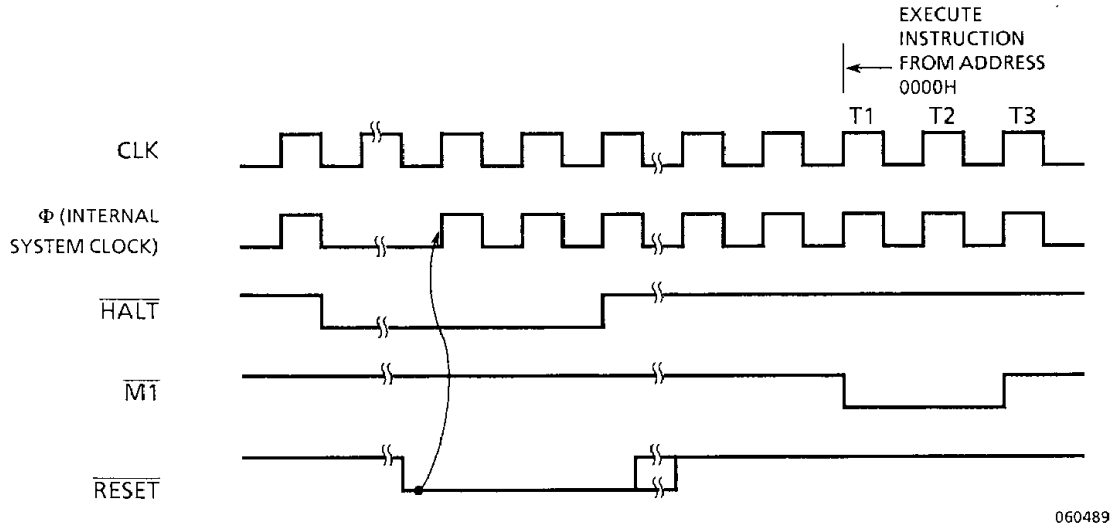

Figure 3.13 (b) IDLE2 Mode

(c) STOP Mode (MS1 = 1, MS2 = 0)

The halt release operation by interrupt signal in STOP Mode is shown in Figure 3.14.

When MPU received an interrupt signal, the internal oscillator is restarted. In order to obtain stabillized oscillation, the internal system clock and clock output to the outside are started after a warming-up time of $(2^{14}+2.5)$ TcC (TcC : Clock Cycle) by the internal counter passed.

MPU executes one NOP instruction after the internal system clock is restarted and at the same time, sampling an interrupt signal at the rise of T4 state during the execution of this NOP instruction. If the interrupt signal is accepted, MPU executes the interrupt process operation from next cycle.

At time of interrupt signal input, it is necessary to take the same care as that in the interrupt signal input in IDLE1/2 Mode. The halt release operation by MPU resetting in STOP Mode is shown in Figure 3.15.

When $\overline{\text{RESET}}$ signal at "0" level is input into MPU, the internal oscillator is restarted. However, since it performs a quick operation at time of power ON, the internal counter does not operate. Therefore, the operation may not be carried out properly due to unstable clock immediately after the internal oscillator is restarted. To restart the clock by $\overline{\text{RESET}}$ signal in STOP Mode, it is necessary to hold $\overline{\text{RESET}}$ signal at "0" level for sufficient time. When $\overline{\text{RESET}}$ signal becomes "1", after the dummy cycle for at least 2T states, MPU starts to execute an execution from address 0000H.

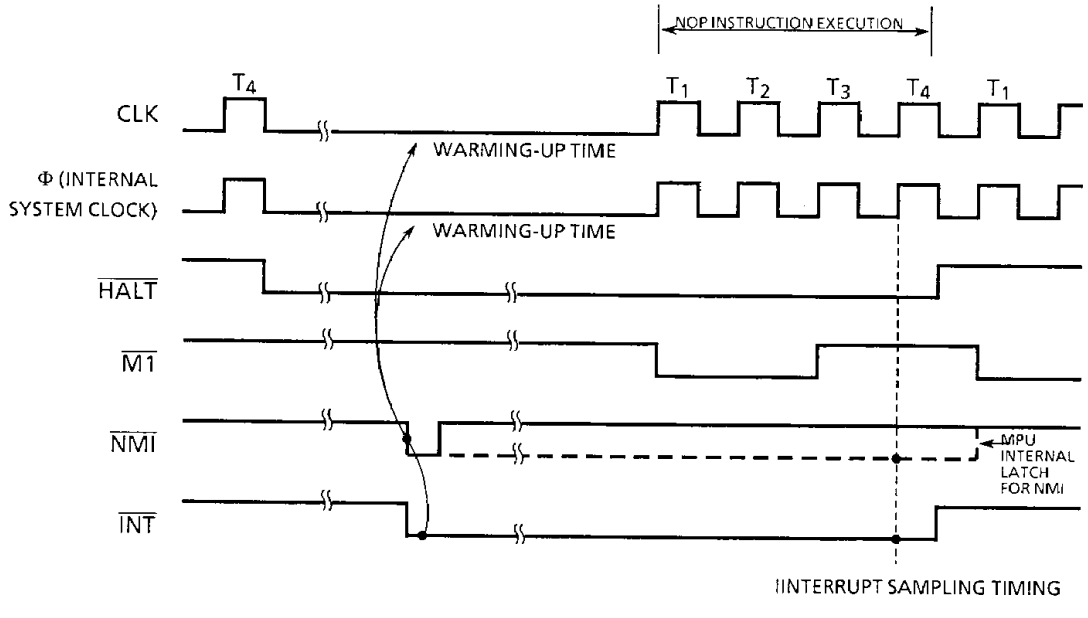

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Figure 3.14 Halt Release Operation Timing by Interrupt Request Signal in STOP Mode

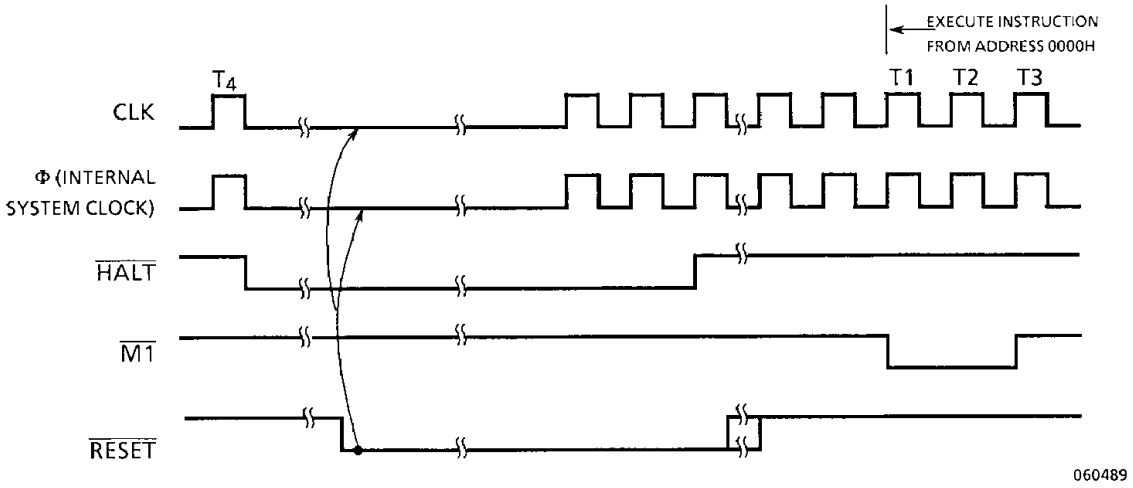

Figure 3.15 Halt Release Operation Timing by Reset in STOP Mode

3.4 INSTRUCTION SET

Instruction set of the TMPZ84C01F/02AF-6 are the same as those for the TMPZ84C00A. For details refer to the data sheet for the TMPZ84C00A.

3.5 METHOD OF USE

A connecting example of the TMPZ84C01F/02AF-6 with the TLCS-Z80 family peripheral LSI's is shown in Figure 3.16. For the explanation and precautions for connection, refer to Section 3.5 Method of use of the data sheet for the TMPZ84C00A.

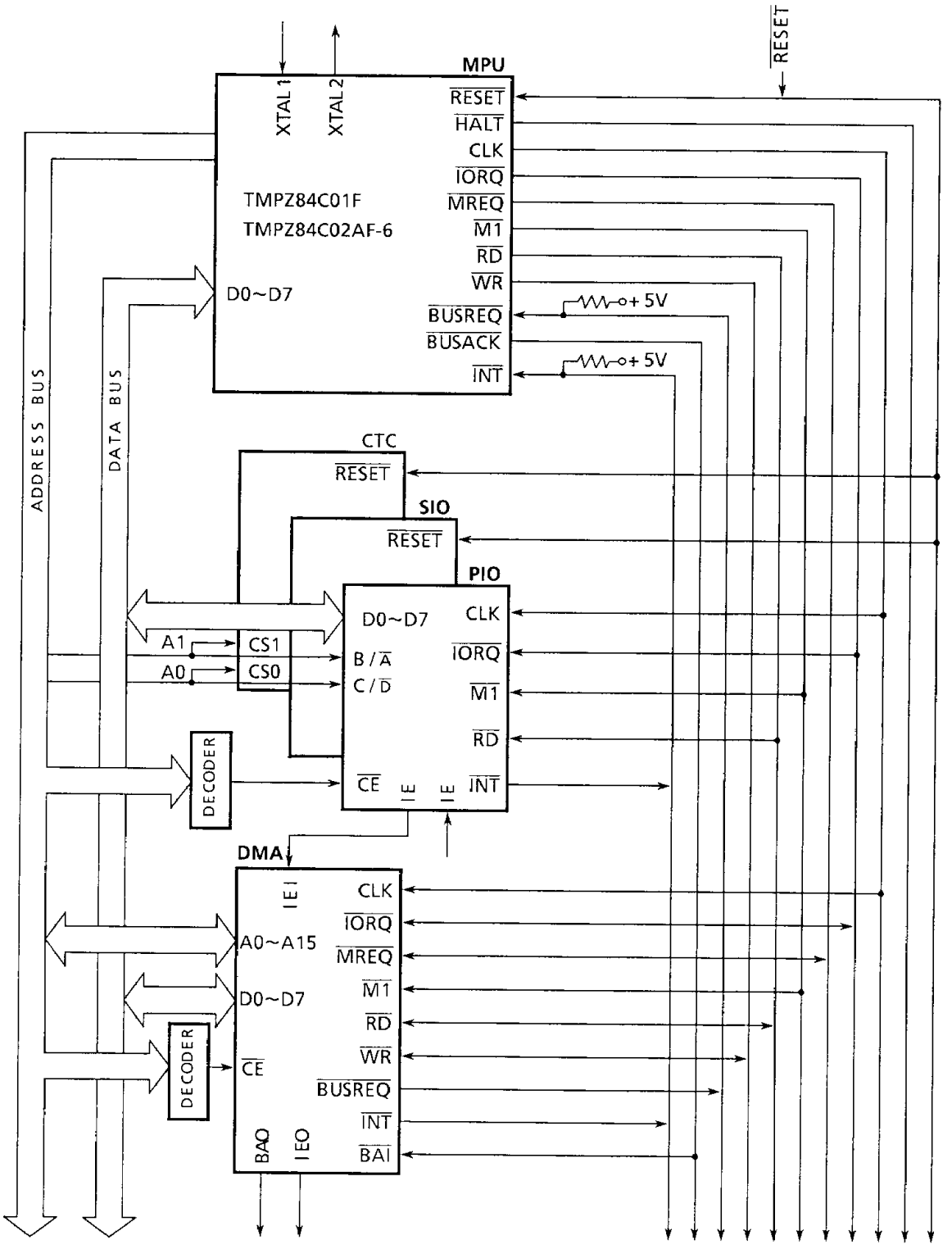

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Figure 3.16 Example Connection with Z80 family peripheral LSI

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
VCC	Supply Voltage	− 0.5 to + 7	V
VIN	Input Voltabe	− 0.5 to V_{CC} + 0.5	V
PD	Power Dissipation (TA = 85°C)	250	mW
TSOLDER	Soldering Temperature (10sec)	260	°C
TSTG	Storage Temperature	− 65 to 150	°C
TOPR	Operating Temperature	− 40 to 85	°C

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4.2 DC ELECTRICAL CHARACTERISTICS

4.2.1 DC Chracteristics

$T_A = 10°C$ to $+60°C$ (TMPZ84C01F @ Low voltage operation)

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage		2.7	—	5.5	V
VIHC	Input High Voltage (XTAL1)		VCC-0.2	—	VCC + 0.3	V
VIH	Input High Voltage (Except XTAL1)		VCC-0.2	—	VCC + 0.3	V
VILC	Input Low Voltage (XTAL1)		-0.3	—	0.2	V
VIL	Input Low Voltage (Except XTAL1)		-0.5	—	0.2	V

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4.2.2 DC Chracteristics (I)

VCC = 2.7V to 5.5V, T_A = -40°C to +85°C (TMPZ84C01F @ Low voltage operation)

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
ILI	Input Leak Current	VSS ≦ VIN ≦ VCC	—	—	± 10	μA
ILO	3 State Output Current in Floating	VSS ≦ VIN ≦ VCC	—	—	± 10	μA
IOH	Output High Current (Except XTAL2)	VOH = VCC-0.2V	0.1	—	—	mA
IOL	Output Low Current (Except XTAL2)	VOL = 0.2V	0.4	—	—	mA
ICC1	Supply Current (@Run Mode)	VCC = 3V, f = 1MHz VIH = Vcc, VIL = 0V	—	2.5	5.0	mA
ICC2	Supply Current (@Stop Mode)	VCC = 3V, VIH = Vcc, VIL = 0V	—	0.5	10	μA
ICC3	Supply Current (@IDLE1 Mode)	VCC = 3V, f = 1MHz VIH = Vcc, VIL = 0V	—	0.5	1.0	mA
ICC4	Supply Current (@IDLE2 Mode)	VCC = 3V, f = 1MHz VIH = Vcc, VIL = 0V	—	1.0	2.0	mA

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4.2.3 DC Chracteristics (II)

$T_A = -40°C$ to $85°C$, $VCC = 5V \pm 10\%$, $VSS = 0V$

SYMBOL	ITEM	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
VOLC	Low Level Clock Output Voltabe	IOL = 2.0mA		—	—	0.4	V
VOHC	High Level Clock Output Voltage	IOH = −2.0mA		V_{CC} − 0.6	—	—	V
VIL	Input Low Voltage			−0.5	—	0.8	V
VIH	Input High Voltage			2.2	—	VCC	V
VIHR	Input High Voltage ($\overline{RESET}$)			V_{CC} − 0.6	—	VCC	V
VILR	Input Low Voltage ($\overline{RESET}$)			−0.5	—	0.45	V
VOL	Output Low Voltage (Except Clock)	IOL = 2.0mA		—	—	0.4	V
VOH1	Output High Voltage (I) (Except Clock)	IOH = −1.6mA		2.4	—	—	V
VOH2	Output High Voltage (II) (Except Clock)	IOH = −250uA		VCC − 0.8	—	—	V
ILI	Input Leak Current	VSS ≦ VIN ≦ VCC		—	—	± 10	μA
ILO	3 State Output Current in Floating	VSS + 0.4 ≦ VOUT ≦ VCC		—	—	± 10	μA
ICC1	Supply Current (@ RUN Mode)	VCC = 5V, fCLK = (NOTE1) VIHC = VIH = VCC − 0.2, VILC = VIL = 0.2V	01F	—	15	20	mA
			02AF -6	—	20	24	

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SYMBOL	ITEM	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
ICC2	Supply Current (@ STOP Mode)	VCC = 5V, fCLK = (Note2) VIHC = VIH = VCC – 0.2V VILC = VIL = 0.2V		—	0.5	10	μA
ICC3	Supply Current (@ IDLE1 Mode)	VCC = 5V, fCLK = (Note1) VIHC = VIH = VCC – 0.2V VILC = VIL = 0.2V	01F	—	1.0	2.0	mA
			02AF-6	—	1.5	3.0	
ICC4	Supply Current (@ IDLE2 Mode)	VCC = 5V, fCLK = (Note1) VIHC = VIH = VCC – 0.2V VILC = VIL = 0.2V	01F	—	3.0	6.0	mA
			02AF-6	—	4.5	7.5	

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Note 1 : $fCLK = 1/T_{CC}$ (MIN)
Note 2 : At T4 "LOW" state of the halt instruction fetch cycle.

4.3 AC ELECTRICAL CHARACTERISTICS

TOPR = −40℃ to 85℃, VCC = 5V ± 10%, VSS = 0V

(1/4)

No.	SYMBOL	ITEM	01F (V_{CC} = 2.7V~5.5V fCLK = 1MHz)		01F (fCLK = 4MHz)		02AF-6 (fCLK = 6MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
1	TcC	Clock frequency	1000	DC	250	DC	165	DC	ns
2	TwCh	High clock pulse width	400	DC	110	DC	65	DC	ns
3	TwCl	Low clock pulse width	400	DC	110	DC	65	DC	ns
4	TfC	Clock falling time	—	200	—	30	—	20	ns
5	TrC	Clock rising time	—	200	—	30	—	20	ns
6	TdCr (A)	Effective address output delay from clock rise	—	400	—	110	—	90	ns
7	TdA (MREQf)	Address output definite time prior to $\overline{MREQ}$	200	—	65	—	35	—	ns
8	TdCf (MREQf)	Delay from clock fall to $\overline{MREQ}$ = "L"	—	300	—	85	—	70	ns
9	TdCr (MREQr)	Delay from clock rise to $\overline{MREQ}$ = "H"	—	300	—	85	—	70	ns
10	TwMREQh	$\overline{MREQ}$ high level pulse width	400	—	110	—	65	—	ns
11	TwMREQl	$\overline{MREQ}$ low level pulse width	800	—	220	—	135	—	ns
12	TdCf (MREQr)	Delay from clock fall to $\overline{MREQ}$ = "H"	—	300	—	85	—	70	ns
13	TdCf (RDf)	Delay from clock fall to $\overline{RD}$ = "L"	—	350	—	95	—	80	ns
14	TdCr (RDr)	Delay from clock rise to $\overline{RD}$ = "H"	—	300	—	85	—	70	ns
15	TsD (Cr)	Data set-up time for clock rise	180	—	35	—	30	—	ns
16	ThD (RDr)	Data hold time for $\overline{RD}$ rise	0	—	0	—	0	—	ns
17	TsWAIT (Cf)	$\overline{WAIT}$ signal set-up time for clock fall	350	—	70	—	60	—	ns
18 *	ThWAIT (Cf)	$\overline{WAIT}$ hold time after clock fall	10	—	10	—	10	—	ns
19	TdCr (M1f)	Delay from clock rise to $\overline{M1}$ = "L"	—	400	—	100	—	80	ns

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No.	SYMBOL	ITEM	01F (V_{CC} = 2.7V~5.5V fCLK = 1MHz)		01F (fCLK = 4MHz)		02AF-6 (fCLK = 6MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
20	TdC r(M1r)	Delay from clock rise to $\overline{M1}$ = "H"	—	400	—	100	—	80	ns
21	TdCf (RDr)	Delay from clock fall to $\overline{RD}$ = "H"	—	300	—	85	—	70	ns
22	TdCr (RDf)	Delay from clock rise to $\overline{RD}$ = "L"	—	300	—	85	—	70	ns
23	TsD (Cf)	Data set-up time for clock fall (at time of M2, M3, M4, M5 cycle)	250	—	50	—	40	—	ns
24	TdA (IORQf)	Address definite time prior to $\overline{IORQ}$ fall	550	—	180	—	110	—	ns
25	TdCr (IORQf)	Delay from clock rise to $\overline{IORQ}$ = "H"	—	300	—	75	—	65	ns
26	TdCf (IORQr)	Delay from clock fall to $\overline{IORQ}$ = "H"	—	300	—	85	—	70	ns
27	TdD (WRf)	Data definit time prior to $\overline{WR}$ fall	200	—	80	—	25	—	ns
28	TdCf (WRf)	Delay from clock fall to $\overline{WR}$ = "L"	—	300	—	80	—	70	ns
29	TwWR	$\overline{WR}$ pulse width	750	—	220	—	135	—	ns
30	TdCf (WRr)	Delay from clock fall to $\overline{WR}$ = "H"	—	300	—	80	—	70	ns
31	TdD (WRf)	Data definit time prior to $\overline{WR}$ fall	10	—	−10	—	−55	—	ns
32	TdCr (WRf)	Delay from clock rise to $\overline{WR}$ = "L"	—	250	—	65	—	60	ns
33	TdWRr (D)	Output data holding after $\overline{WR}$ = "H"	200	—	60	—	30	—	ns
34	TdCf (HALT)	Delay from clock fall to HALT = "L" or"H"	—	1000	—	300	—	260	ns
35	TwNMI	$\overline{NMI}$ pulse width	300	—	80	—	70	—	ns
36	TsBUSREQ (Cr)	Set-up time for clock rise	250	—	50	—	50	—	ns
37 *	ThBUSREQ (Cr)	$\overline{BUSREQ}$ hold time after clock rise	10	—	10	—	10	—	ns

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No.	SYMBOL	ITEM	01F (V_{CC} = 2.7V~5.5V fCLK = 1MHz)		01F (fCLK = 4MHz)		02AF-6 (fCLK = 6MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
38	TdCr (BUSACKf)	Time from clock rise to $\overline{BUSACK}$ = "L"	–	400	–	100	–	90	ns
39	TdCf (BUSACKr)	Time from clock fall to $\overline{BUSACK}$ = "H"	–	400	–	100	–	90	ns
40	TdCr (Dz)	Delay from clock rise to data bus float state	–	350	–	90	–	80	ns
41	TdCr (CTz)	Delay from clock rise to control output float state ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$)	–	300	–	80	–	70	ns
42	TdCr (Az)	Delay from clock rise to address bus float state	–	350	–	90	–	80	ns
43	TdCr (A)	Address holding time from $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$	200	–	80	–	35	–	ns
44	TsRESET (Cr)	$\overline{RESET}$ set-up time for clock rise	300	–	60	–	60	–	ns
45 *	ThRESET (Cr)	$\overline{RESET}$ hold time for clock rise	10	–	10	–	10	–	ns
46	TsINTf (Cr)	$\overline{INT}$ set-up time for clock rise	300	–	80	–	70	–	ns
47 *	TsINTr (Cr)	$\overline{INT}$ hold time after clock rise	10	–	10	–	10	–	ns
48 *	TdM1f (IORQf)	$\overline{M1}$ output ("L") definite time prior to $\overline{IORQ}$ fall	2000	–	565	–	365	–	ns
49	TdCf (IORQf)	Delay from clock fall to $\overline{IORQ}$ = "L"	–	300	–	85	–	70	ns
50	TdCr (IORQr)	Delay from clock rise to $\overline{IORQ}$ = "H"	–	300	–	85	–	70	ns
51	TdCf (D)	Delay from clock fall to data output	–	550	–	150	–	150	ns

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No.	SYMBOL	ITEM	01F (V_{CC} = 2.7V~5.5V fCLK = 1MHz)		01F (fCLK = 4MHz)		02AF-6 (fCLK = 6MHz)		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
52	TRST1S	Clock (CLK) restart time by $\overline{INT}$ (STOP mode)	—	(**) (2^{14} + 2.5) × T_{CC}	—	(**) (2^{14} + 2.5) × T_{CC}	—	(**) (2^{14} + 2.5) × T_{CC}	ns
53	TRST2S	Clock (CLK) restart time by $\overline{NMI}$ (STOP mode)	—	(**) (2^{14} + 2.5) × T_{CC}	—	(**) (2^{14} + 2.5) × T_{CC}	—	(**) (2^{14} + 2.5) × T_{CC}	ns
54	TRST1I	Clock (CLK) restart time by $\overline{INT}$ (IDLE1/2 mode)	—	(**) 2.5 T_{CC}	—	(**) 2.5 T_{CC}	—	(**) 2.5 T_{CC}	ns
55	TRST2I	Clock (CLK) restart time by $\overline{NMI}$ (IDLE1/2 mode)	—	(**) 2.5 T_{CC}	—	(**) 2.5 T_{CC}	—	(**) 2.5 T_{CC}	ns

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Note 1 : Test conditions (1) @VCC = 5V ± 10%
VIH = 2.4V, VIL = 0.4V, VIHC = VCC − 0.6V, VILC = 0.6V, VOH = 2.2V, VOL = 0.8V
Test conditions (2) TMPZ84C01F @Low Voltage Operation
VIH = VCC-0.2V, VIL = 0.2V, VIHC = VCC-0.2V, VILC = 0.2V, VOH = VCC/2V, VOL = VCC/2V

Note 2 : Items with an asterisk (*) are non-compatible with NMOS Z80.

Note 3 : **TYPICAL

4.4 CAPACITANCE

TA = 25°C

SYMBOL	ITEM	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CCLOCK	CLOCK input capacitance	f = 1MHz	—	—	8	pF
CIN	input capacitance	All pins except measured	—	—	6	pF
COUT	output capacitance	pin are connected to GND	—	—	10	pF

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4.5 TIMING DIAGRAM

Figures 4.1 to 4.10 show the basic timings of respective operations. Numbers shown in the figures correspond with those in the AC Electrical Characteristics Table in 4.3.

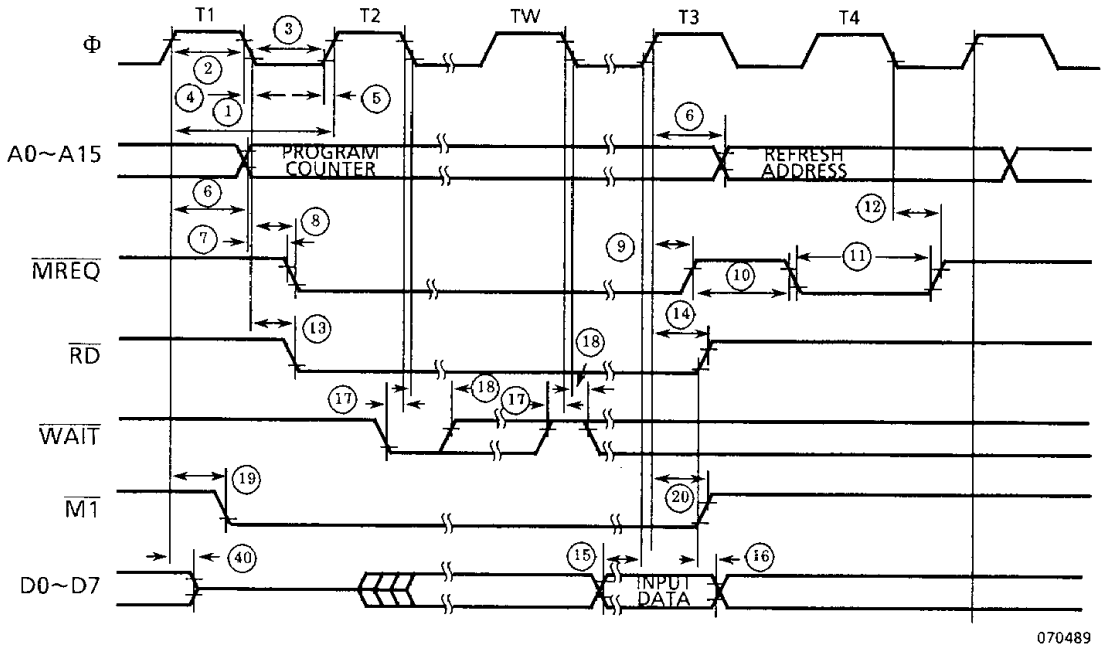


Figure 4.1 Operation Code Fetch Cycle

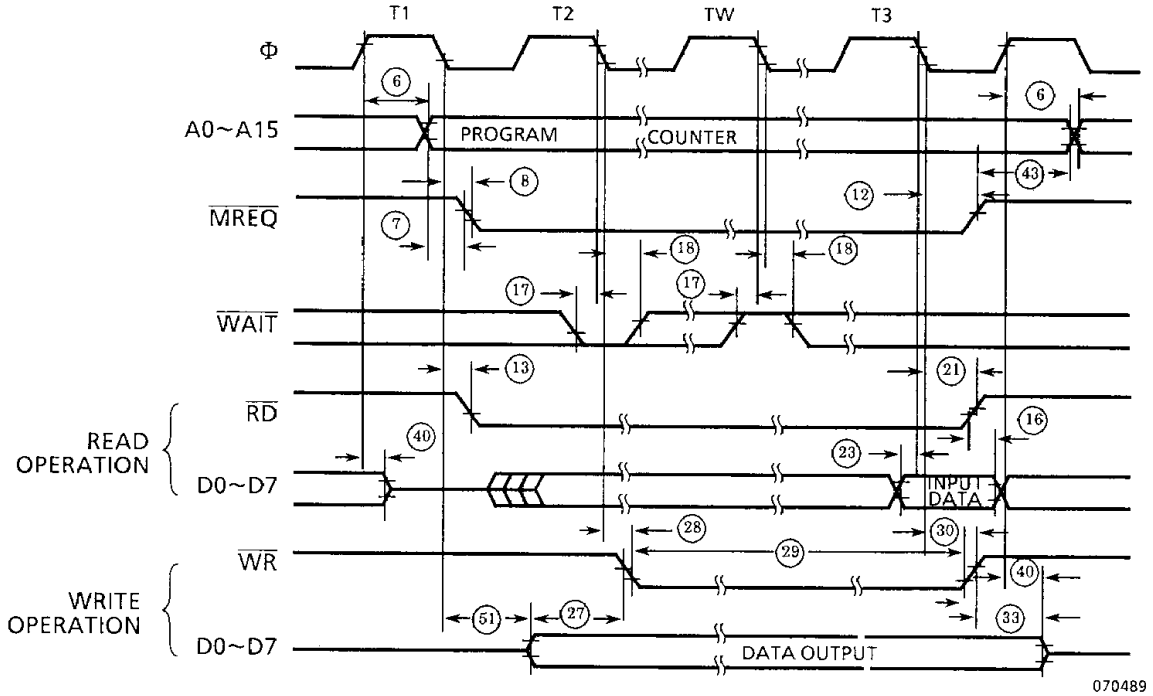
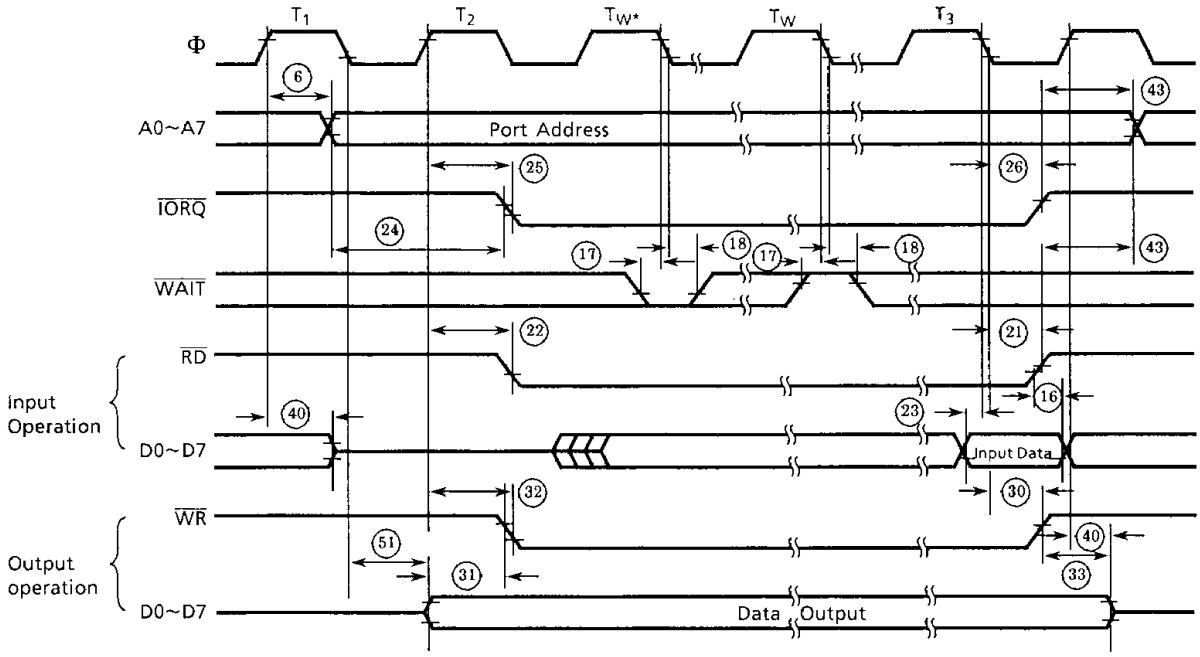


Figure 4.2 Memory Read/Write Cycle



Note : 1 wait state (TW*) is inserted automatically by MPU.

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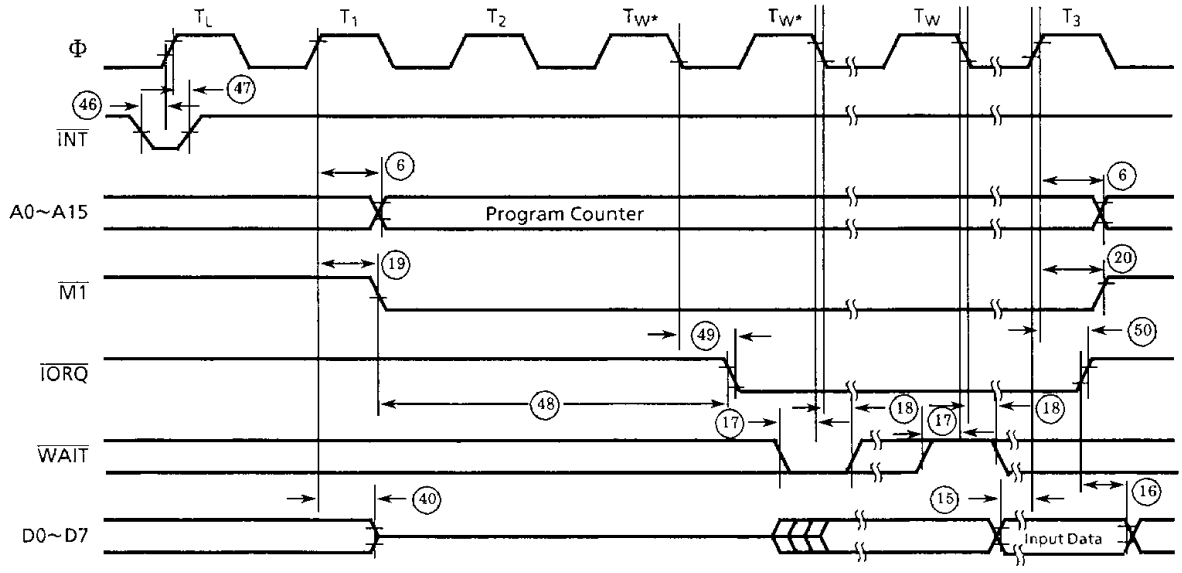
Figure 4.3 Input/Output Cycle



Note 1 TL is the final state of the preceding instruction.

Note 2 2 wait state (TW*) is inserted automatically by MPU.

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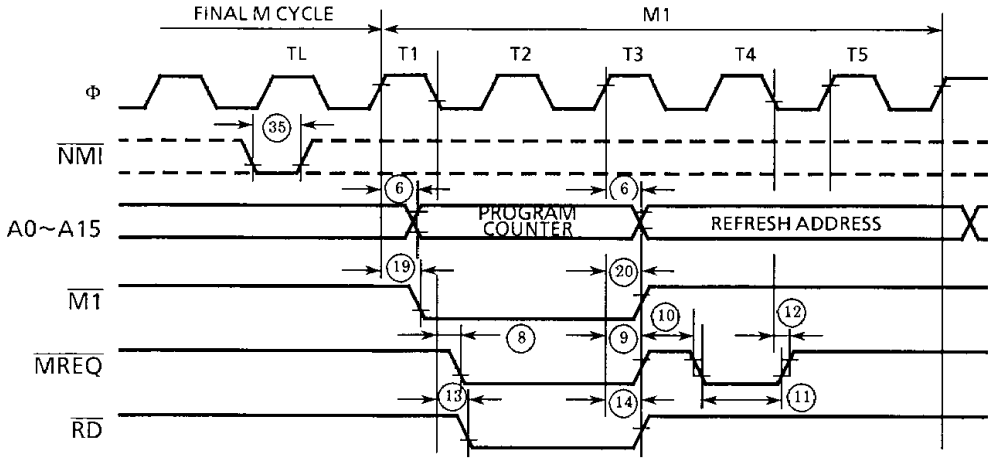
Figure 4.4 Interrupt Request/Acknowledge Cycle



Note : NMI is asynchronous input but in order to assure the positive response in the following cycle, NMI triling edge signal cust be generated keeping abreast of the leading edge of the preceding TL state.

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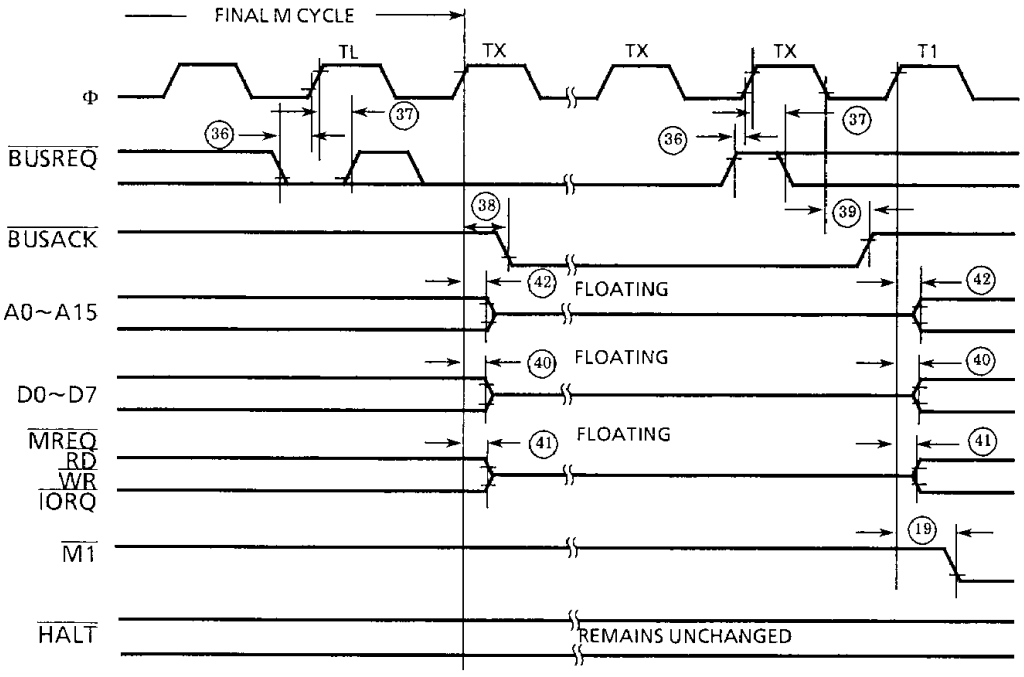
Figure 4.5 Non-maskable Interrupt Request Cycle



Note :
1. TL is the final state of any machine cycle.
2. TX is optional clock used bv requested peripheral LSI.

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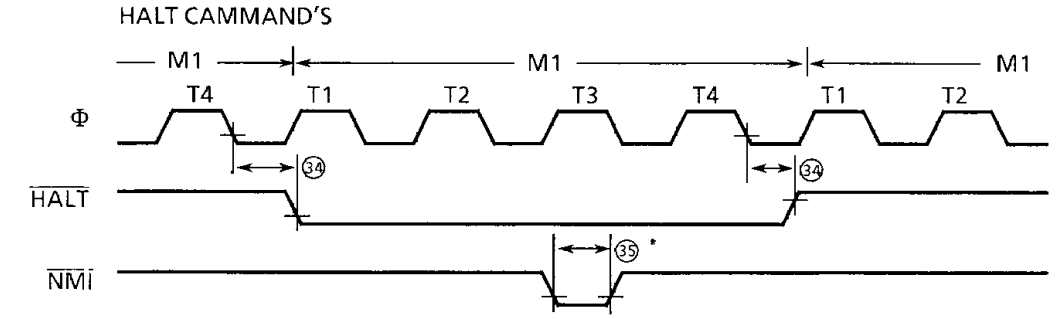
Figure 4.6 Bus Repuest/Acknowledge Cycle



Note : INT signal is also used for releasing from the halt state.

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Figure 4.7 Halt Acknowledge Cycle

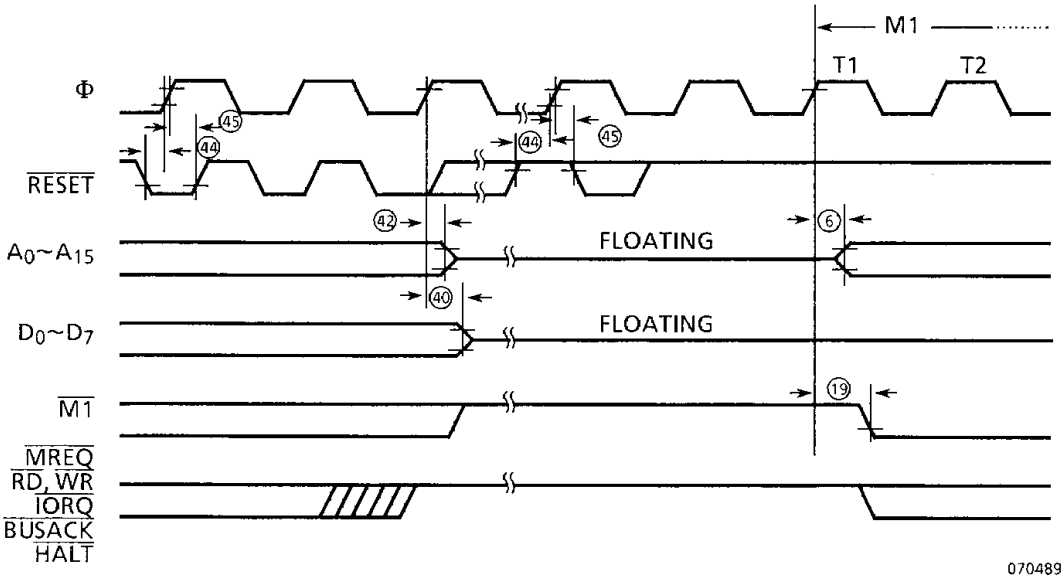

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Figure 4.8 Reset Cycle

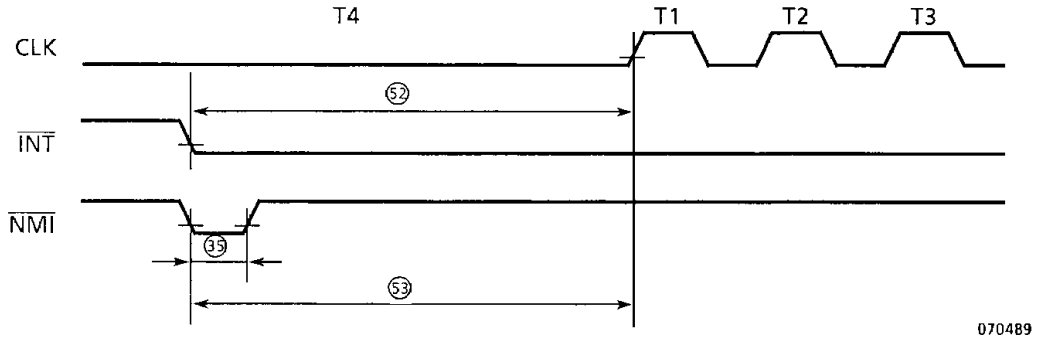


Figure 4.9 Clock Restart Timing (STOP Mode)

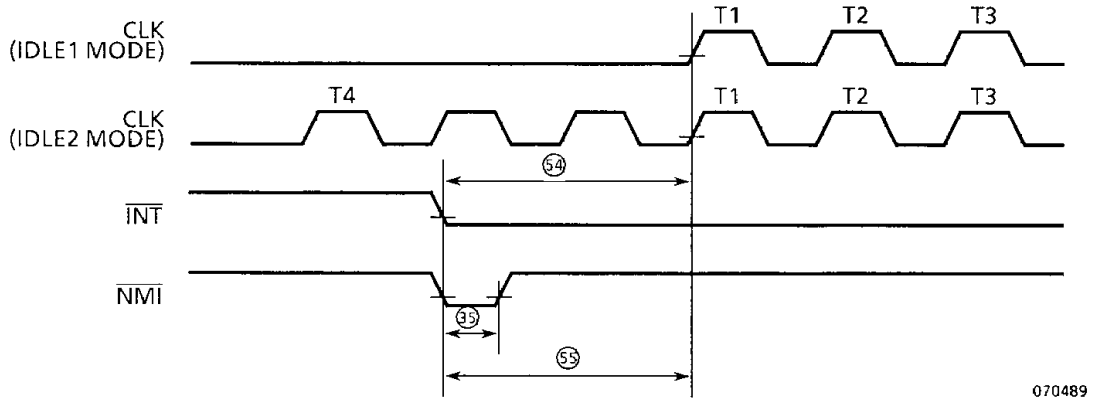


Figure 4.10 Clock Restart Timing (IDLE1/2 Mode)

5. PRECAUTIONS

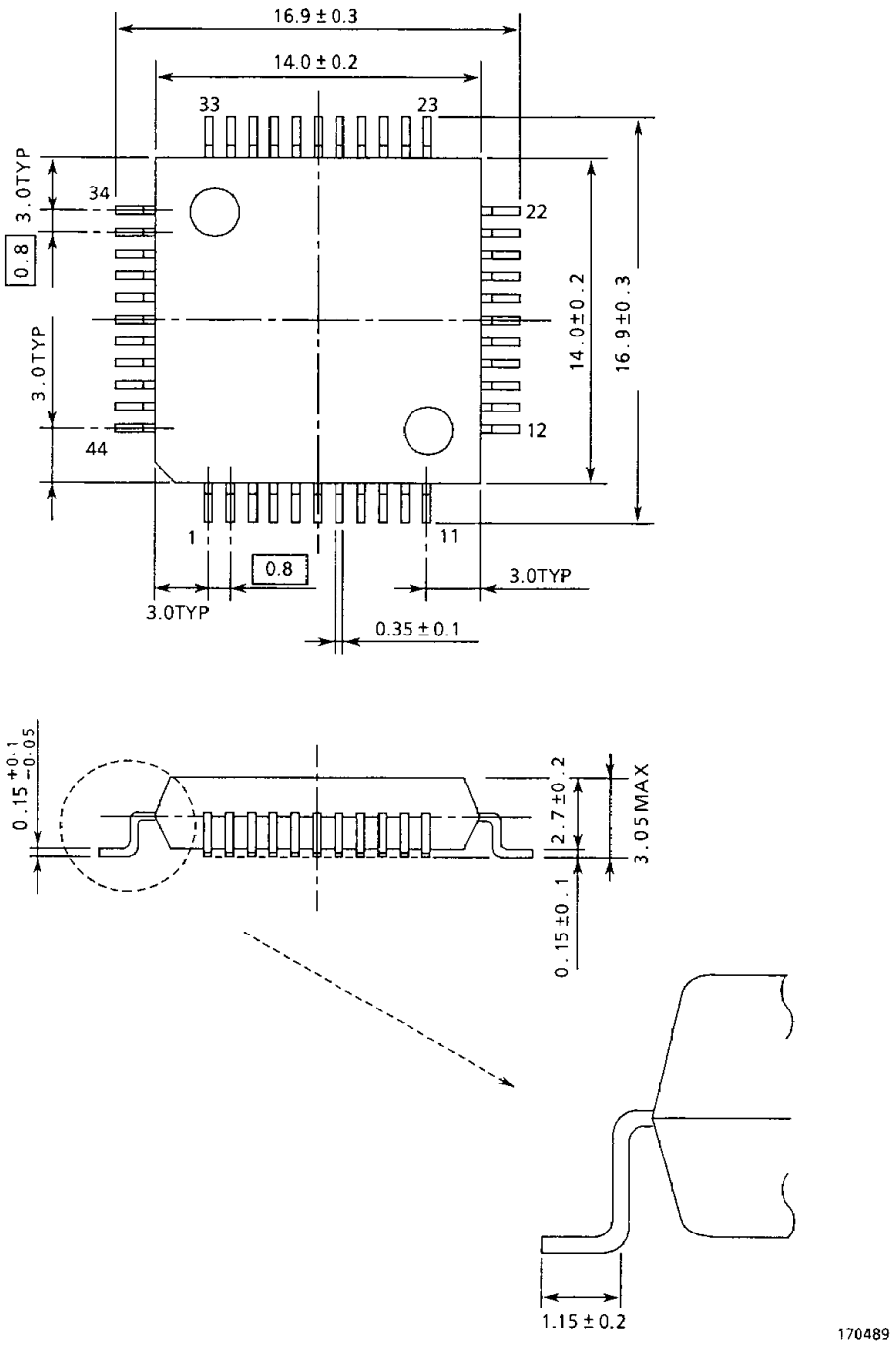
(1) To reset MPU, it is necessary to hold $\overline{\text{RESET}}$ signal input at "0" level for ; least 3 clocks.
In particular, to release the HALT state by $\overline{\text{RESET}}$ signal in STOP Mode, hold $\overline{\text{RESET}}$ signal at "0"level for sufficient time in order to stabilize output from the internal oscillator.

(2) In releasing MPU from the HALT state by interrupt signal in IDLE1/2 Mode and STOP Mode, MPU will not be released from the HALT state and the internal system clock will stop again unless an interrupt signal is accepted during the execution of NOP instruction even when the internal system clock is restarted by the interrupt signal input. In particular, care must be taken when $\overline{\text{INT}}$ is used.
Other precautions are identical to those for the TMPZ84C00A except those for $\overline{\text{RFSH}}$ terminal. Refer to the data sheet for the TMPZ84C00A.

6. OUTLINE DRAWING

QFP44-P-1414F

Unit : mm



Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.