TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95CS66FG

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

Previous Part Number (in Body Text)	New Part Number
TMP95CS66F	TMP95CS66FG

2. Package code and dimensions

Previous Package Code (in Body Text)	New Package Code
P-LQFP100-1414-0.50F	LQFP100-P-1414-0.50F

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Solderability of lead free products

Test Parameter	Test Condition	Note
Solderability	Use of Sn-37Pb solder Bath Solder bath temperature = 230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: Solderability rate until forming ≥ 95%
	Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead free)	

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

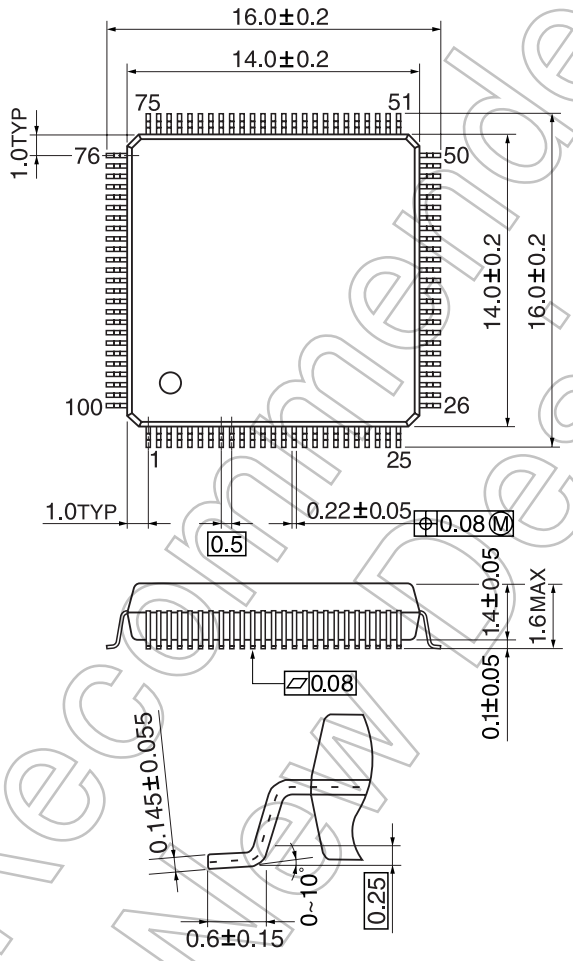
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

LQFP100-P-1414-0.50F

Unit: mm



CMOS 16-Bit Microcontrollers

TMP95CS66F

1. Outline and Features

TMP95CS66 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment. This device is TNP95CS64 function cut. Otherwise, all the functions of the products are the same.
TMP95CS66 comes in a 100-pin flat package.
Listed below are the features.

(1) High-speed 16-bit CPU (900/H CPU)

- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: Four-channels (640 ns / 2 bytes at 25 MHz)

(2) Minimum instruction execution time: 160 ns (at 25 MHz)

(3) Built-in RAM: 2 Kbytes
Built-in ROM: 64 Kbyte

(4) External memory expansion

- Expandable up to 16 Mbytes (shared program/data area)
- External data bus width select pin (AM8/$\overline{16}$)
- Can simultaneously support 8/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 8 channels

- With event counter function: 2 channels

(6) 16-bit timer/event counter: 2 channels

(7) General-purpose serial interface: 1 channels

(8) Watchdog timer

(9) Chip select/wait controller: 4 blocks

(10) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 21 internal interrupts:] Seven selectable priority levels
- 10 external interrupts:]

(11) Input/output ports: 81 pins

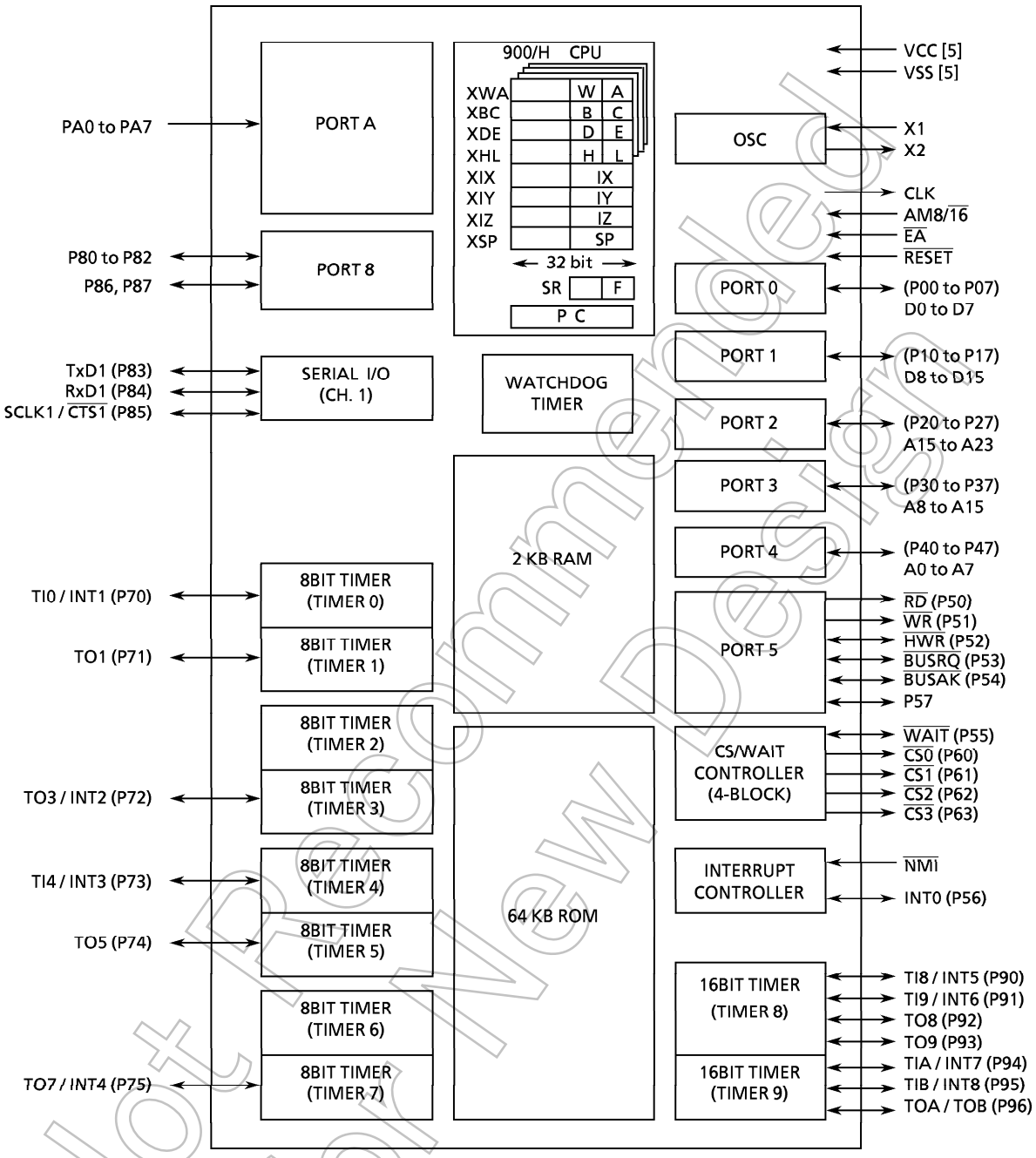
(12) Standby mode
- Four HALT modes: RUN, IDLE2, IDLE1, STOP

(13) Operating voltage
- V_{CC} = 4.5 − 5.5 V

(14) Package: P-LQFP100-1414-0.50F

(15) Differences between TMP95CS64F and TMP95CS66

	TMP95CS64F	TMP95CS66F
10-bit A/D converter	8 channels	—
8-bit D/A converter	8 channels	—
Operating voltage	V_{CC} = 4.5 V to 5.5 V (@ f = 8 to 25 MHz) V_{CC} = 2.7 V to 3.3 V (@ f = 4 to 10 MHz)	V_{CC} = 4.5 V to 5.5 V (@ f = 8 to 25 MHz)



Note: After a reset function in parentheses ( ) are selected for the shared pins.

Product	AM8/16	Pin function after reset
TMP95CS66	Fixed to high level	Multi-use pins can select function in parentheses ( ).

Figure 1 TMP95CS66 Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP95CS66F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1 is a pin assignment diagram for TMP95CS66F.

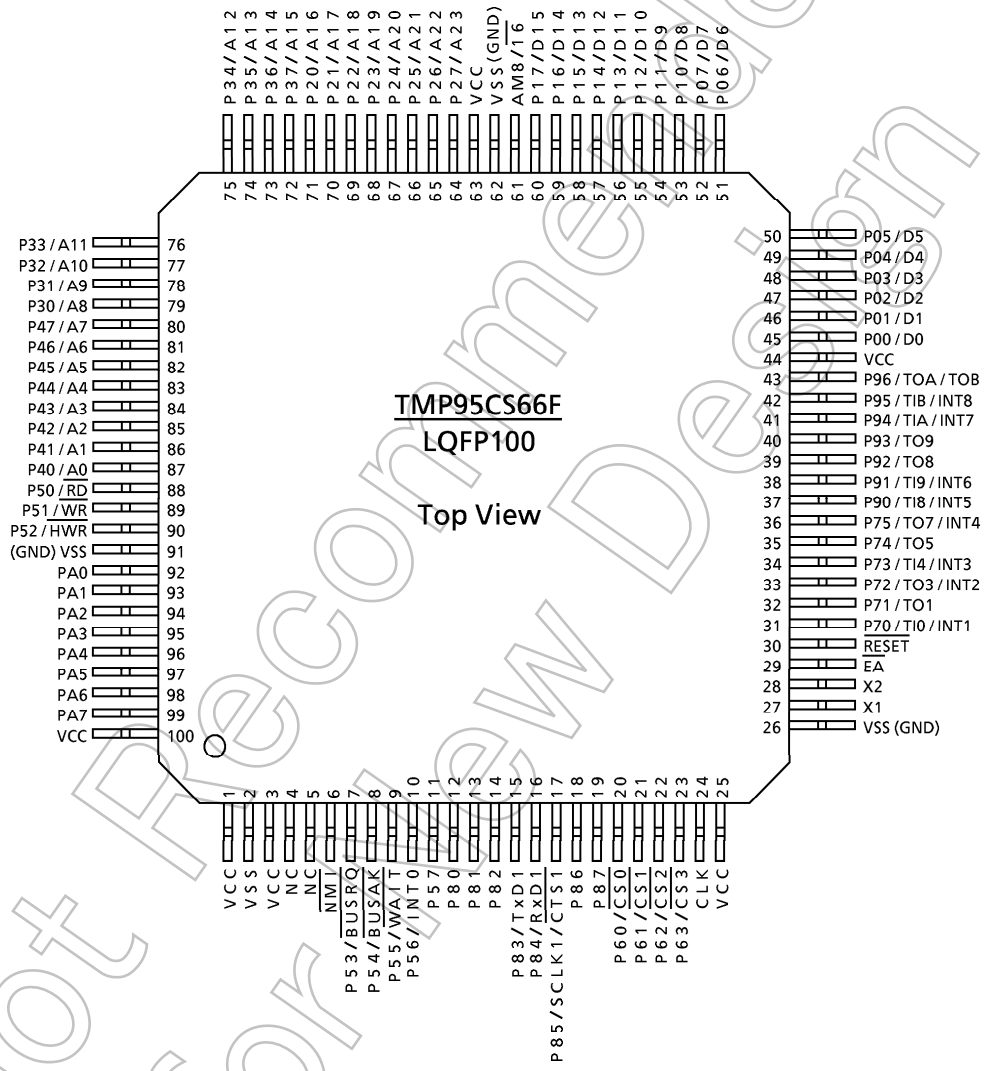


Figure 2.1 Pin Assignment Diagram (100-Pin LQFP)

2.2 Pin Names and Functions

Table 2.2 shows the names and functions of the input/output pins.

Table 2.2 Pin Names and Functions (1/3)

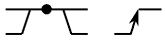
Pin Name	Number of Pins	Input/Output	Function
P00 to P07	8	Input/output	Port 0: I/O port. Input or output specifiable in units of bits
/ D0 to D7		Input/output	Data: Data bus 0 to 7
P10 to P17	8	Input/output	Port 1: I/O port. Input or output specifiable in units of bits
/ D8 to D15		Input/output	Data: Data bus 8 to 15
P20 to P27	8	Input/output	Port 2: I/O port. Input or output specifiable in units of bits
/ A16 to A23		Output	Address: Address bus 16 to 23
P30 to P37	8	Input/output	Port 3: I/O port. Input or output specifiable in units of bits
/ A8 to A15		Output	Address: Address bus 8 to 15
P40 to P47	8	Input/output	Port 4: I/O port. Input or output specifiable in units of bits
/ A0 to A7		Output	Address: Address bus 0 to 7
P50	1	Output	Port 50: Output-only port
/ $\overline{RD}$		Output	Read: Outputs strobe signal to read external memory (setting P5 <P50> = 0 and P5FC <P50F> = 1 outputs strobe signal at all read timings)
P51	1	Output	Port 51: Output-only port.
/ $\overline{WR}$		Output	Write: Outputs strobe signal to write data on pins D0 to D7
P52	1	Input/output	Port 52: I/O port (with built-in pull-up resistor)
/ $\overline{HWR}$		Output	Upper write: Outputs strobe signal to write data on pins D8 to D15
P53	1	Input/output	Port 53: I/O port (with built-in pull-up resistor)
/ $\overline{BUSRQ}$		Input	Bus request: Input pin to request external bus release
P54	1	Input/output	Port 54: I/O port (with built-in pull-up resistor)
/ $\overline{BUSAK}$		Output	Bus acknowledge: Output pin to acknowledge that CPU received $\overline{BUSRQ}$ and released external bus.
P55	1	Input/output	Port 55: I/O port (with built-in pull up resistor)
/ $\overline{WAIT}$		Input	Wait: Bus wait request pin for CPU (Effective when 1 + N WAIT mode, or 0 + N WAIT mode. Set using chip select/wait control register.)
P56	1	Input/output	Port 56: I/O port (with built-in pull-up resistor)
/ INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. 
P57	1	Input/output	Port 57: I/O port (with built-in pull-up resistor)

Table 2.2 Pin Names and Functions (2/3)

Pin Name	Number of Pins	Input/Output	Function
P60	1	Output	Port 60: Output-only port
/ $\overline{CS0}$		Output	Chip select 0: Outputs 0 if address is within specified address range
P61	1	Output	Port 61: Output-only port
/ $\overline{CS1}$		Output	Chip select 1: Outputs 0 if address is within specified address range
P62	1	Output	Port 62: Output-only port
/ $\overline{CS2}$		Output	Chip select 2: Outputs 0 if address is within specified address range
P63	1	Output	Port 63: Output-only port
/ $\overline{CS3}$		Output	Chip select 3: Outputs 0 if address is within specified address range
P70	1	Input/output	Port 70: I/O port
/ TI0		Input	Timer input 0: Input pin for timer 0
/ INT1		Input	Interrupt request pin 1: Rising-edge interrupt request pin
P71	1	Input/output	Port 71: I/O port.
/ TO1		Output	Timer output 1: Output pin for timer 0 or 1
P72	1	Input/output	Port 72: I/O port
/ TO3		Output	Timer output 3: Output pin for timer 2 or 3
/ INT2		Input	Interrupt request pin 2: Rising-edge interrupt request pin
P73	1	Input/output	Port 73: I/O port
/ TI4		Input	Timer input 4: Input pin for timer 4
/ INT3		Input	Interrupt request pin 3: Rising-edge interrupt request pin
P74	1	Input/output	Port 74: I/O port
/ TO5		Output	Timer output 5: Output pin for timer 4 or 5
P75	1	Input/output	Port 75: I/O port
/ TO7		Output	Timer output 7: Output pin for timer 6 or 7
/ INT4		Input	Interrupt request pin 4: Rising-edge interrupt request pin
P80	1	Input/output	Port 80: I/O port (with built-in pull-up resistor)
P81	1	Input/output	Port 81: I/O port (with built-in pull-up resistor)
P82	1	Input/output	Port 82: I/O port (with built-in pull-up resistor)
P83	1	Input/output	Port 83: I/O port (with built-in pull-up resistor)
/ TxD1		Output	Serial transmission data 1
P84	1	Input/output	Port 84: I/O port (with built-in pull-up resistor)
/ RxD1		Input	Serial receive data 1
P85	1	Input/output	Port 85: I/O port (with built-in pull-up resistor)
/ SCLK1		Input/output	Serial clock input/output 1
/ $\overline{CTS1}$		Input	Serial data ready to send 1 (Clear-to-send)
P86	1	Input/output	Port 86: I/O port (with built-in pull-up resistor)
P87	1	Input/output	Port 87: I/O port (with built-in pull-up resistor)

Table 2.2 Pin Names and Functions (3/3)

Pin Name	Number of Pins	Input/Output	Function
P90	1	Input/output	Port 90: I/O port
/ TI8		Input	Timer input 8: Input pin for timer 8
/ INT5		Input	Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge
P91	1	Input/output	Port 91: I/O port
/ TI9		Input	Timer input 9: Input pin for timer 8
/ INT6		Input	Interrupt request pin 6: Rising edge interrupt request pin
P92	1	Input/output	Port 92: I/O port
/ TO8		Output	Timer output 8: Output pin for timer 8
P93	1	Input/output	Port 93: I/O port
/ TO9		Output	Timer output 9: Output pin for timer 8
P94	1	Input/output	Port 94: I/O port
/ TIA		Input	Timer input A: Input pin for timer 9
/ INT7		Input	Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge
P95	1	Input/output	Port 95: I/O port
/ TIB		Input	Timer input B: Input pin for timer 9
/ INT8		Input	Interrupt request pin 8: Rising edge interrupt request pin
P96	1	Input/output	Port 96: I/O port
/ TOA		Output	Timer output A: Output pin for timer 9
/ TOB		Output	Timer output B: Output pin for timer 9
PA0 to PA2	3	Input	Port A0 to A2: Input-only port
PA3	1	Input	Port A3: Input-only port
PA4 to PA7	4	Input	Port A4 to A7: Input-only port
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both falling and rising edge
CLK	1	Output	Clock output: Outputs external clock divided by 4. Pulled up during reset.
$\overline{EA}$	1	Input	External access: Connect to VCC.
AM8 / $\overline{16}$	1	Input	Address mode: External data bus width select pin Connect this pin to VCC. Data bus width at external access can be set by chip select/wait control register.
X1 / X2	2	Input/output	Oscillator connecting pin
VCC	5		Collector supply pin: Connect all VCC pins to power supply
VSS	5		GND pin: Connect all VSS pins to GND (0 V)

Note: Disconnect the pull-up resistors from pins other than $\overline{RESET}$ pin by software.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 6.5	V
Input Voltage	V_{IN}	− 0.5 to Vcc + 0.5	V
Output current (total)	ΣI_{OL}	+ 120	mA
Output current (total)	ΣI_{OH}	− 120	mA
Power Dissipation (Ta = + 70°C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	+ 260	°C
Storage Temperature	T_{STG}	− 65 to + 150	°C
Operating Temperature	T_{OPR}	− 20 to + 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

3.2 DC Electrical Characteristics

(1) Vcc = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

(Typical values are for Ta = + 25°C, VCC = + 5 V.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15)	V_{IL}		−0.3	0.8	V
Port 2 to A (except P56, P70, P72, P73, P75)	V_{IL1}		−0.3	0.3 Vcc	V
$\overline{RESET}$, $\overline{NMI}$, INT0 to 4	V_{IL2}		−0.3	0.25 Vcc	V
$\overline{EA}$, AM8/$\overline{16}$	V_{IL3}		−0.3	0.3	V
X1	V_{IL4}		−0.3	0.2 Vcc	V
Input High Voltage (D0 to 15)	V_{IH}		2.2	Vcc + 0.3	V
Port 2 to A (except P56, P70, P72, P73, P75)	V_{IH1}		0.7 Vcc	Vcc + 0.3	V
$\overline{RESET}$, $\overline{NMI}$, INT0 to 4	V_{IH2}		0.75 Vcc	Vcc + 0.3	V
$\overline{EA}$, AM8/$\overline{16}$	V_{IH3}		Vcc − 0.3	Vcc + 0.3	V
X1	V_{IH4}		0.8 Vcc	Vcc + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA		0.45	V
Output High Voltage	V_{OH}	I_{OH} = − 400 μA	2.4		V
	V_{OH1}	I_{OH} = − 100 μA	0.75 Vcc		V
	V_{OH2}	I_{OH} = − 20 μA	0.9 Vcc		V
Darlington Drive Current (8 Output Pins max.)	I_{DAR}	V_{EXT} = 1.5 V, R_{EXT} = 1.1 kΩ	− 1.0	− 3.5	mA
Input Leakage Current	I_{LI}	0.0 ≦ Vin ≦ Vcc	0.02 (Typ)	± 5	μA
Output Leakage Current	I_{LO}	0.2 ≦ Vin ≦ Vcc − 0.2	0.05 (Typ)	± 10	μA
Operating Current (RUN)	I_{CC}	fc = 25 MHz	40 (Typ)	50	mA
IDLE2			30 (Typ)	40	mA
IDLE1			3.5 (Typ)	10	mA
STOP (Ta = − 20 to + 70°C)		0.2 ≦ Vin ≦ Vcc − 0.2	0.5 (Typ)	50	μA
STOP (Ta = 0 to + 50°C)		0.2 ≦ Vin ≦ Vcc − 0.2		10	μA
Power Down Voltage (@STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0	6.0	V
Pull Up Registance	R_{RP}		45	160	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz		10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0 to 4	V_{TH}		0.4	1.0 (Typ)	V

Note: I_{DAR} guarantees up to eight pins from any output port.

3.3 AC Electrical Characteristics

(1) Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C

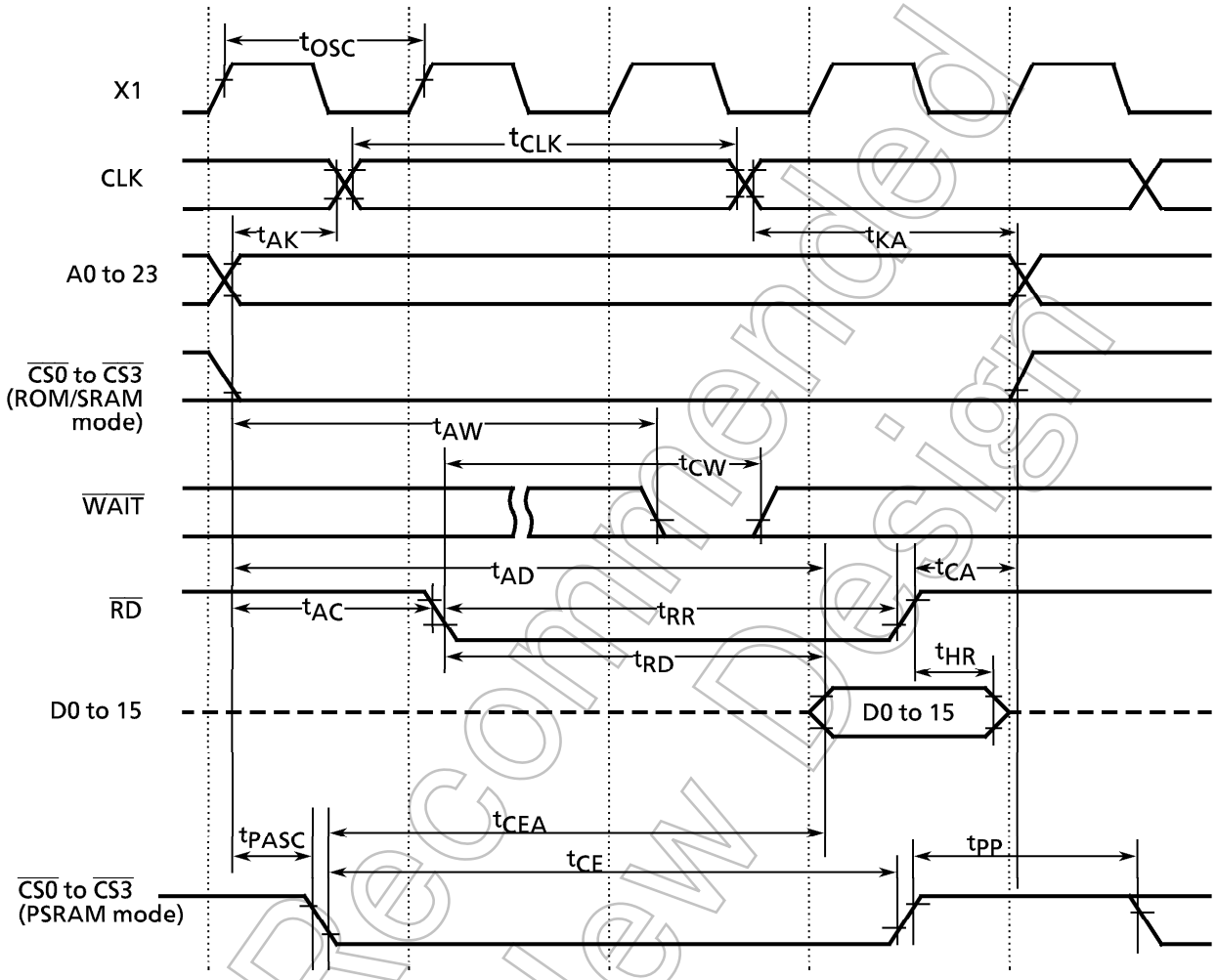
(fc = 8 MHz to 25 MHz)

No.	Parameter	Symbol	Formula		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	40	125	50		40		ns
2	Clock pulse width	t_{CLK}	2.0x – 40		60		40		ns
3	A0 to 23 valid → Clock hold	t_{AK}	0.5x – 20		5		0		ns
4	Clock valid → A0 to 23 hold	t_{KA}	1.5x – 60		15		0		ns
5	A0 to 23 valid → $\overline{RD}/\overline{WR}$ fall	t_{AC}	1.0x – 20		30		20		ns
6	$\overline{RD}/\overline{WR}$ rise → A0 to 23 hold	t_{CA}	0.5x – 20		5		0		ns
7	A0 to 23 valid → D0 to 15 input	t_{AD}		3.5x – 40		135		100	ns
8	$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.5x – 45		80		55	ns
9	$\overline{RD}$ low pulse width	t_{RR}	2.5x – 40		85		60		ns
10	$\overline{RD}$ rise → D0 to 15 hold	t_{HR}	0		0		0		ns
11	$\overline{WR}$ low pulse width	t_{WW}	2.5x – 40		85		60		ns
12	D0 to 15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 40		60		40		ns
13	$\overline{WR}$ rise →D0 to 15 hold	t_{WD}	0.5x – 10		15		10		ns
14	A0 to 23 valid → $\overline{WAIT}$ input ($^{1\ WAIT}_{+\ n\ mode}$)	t_{AW}		3.5x – 90		85		50	ns
	A0 to 23 valid → $\overline{WAIT}$ input ($^{0+n\ WAIT}_{mode}$)	t_{AW}		1.5x – 40		35		20	ns
15	$\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{1\ WAIT}_{+\ n\ mode}$)	t_{CW}	2.5x + 0		125		100		ns
	$\overline{RD}/\overline{WR}$ fall → $\overline{WAIT}$ hold ($^{0+n\ WAIT}_{mode}$)	t_{CW}	0.5x + 0		25		20		ns
16	$\overline{WR}$ rise→ PORT valid	t_{CP}		200		200		200	ns
17	$\overline{CS}$ Low pulse width (PSRAM mode)	t_{CE}	3.0x – 40		110		80		ns
18	$\overline{CS}$ fall→ D0 to 15 input (PSRAM mode)	t_{CEA}		3.0x – 60		90		60	ns
19	Address setup time (PSRAM mode)	t_{PASC}	0.5x – 15		10		5		ns
20	$\overline{CS}$ precharge time (PSRAM mode)	t_{PP}	1.0x – 10		40		30		ns

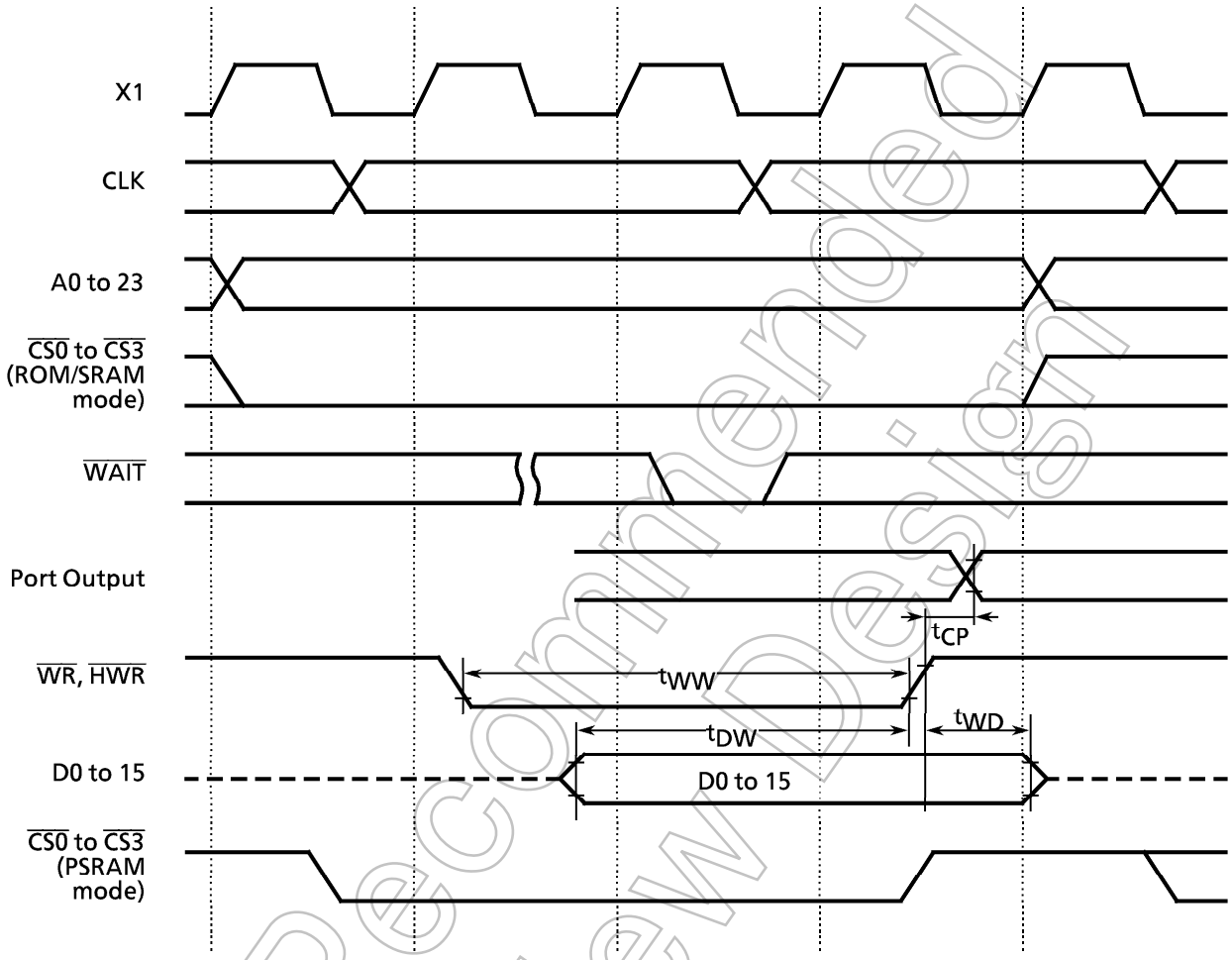
AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
- Input level: High 2.4 V / Low 0.45 V (D0 to D15)
  High 0.8 Vcc / Low 0.2 Vcc (except for D0 to D15)

(2) Read Cycle



(3) Write Cycle



3.4 Serial Channel Timing

(1) I/O interface mode

① SCLK input mode

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)

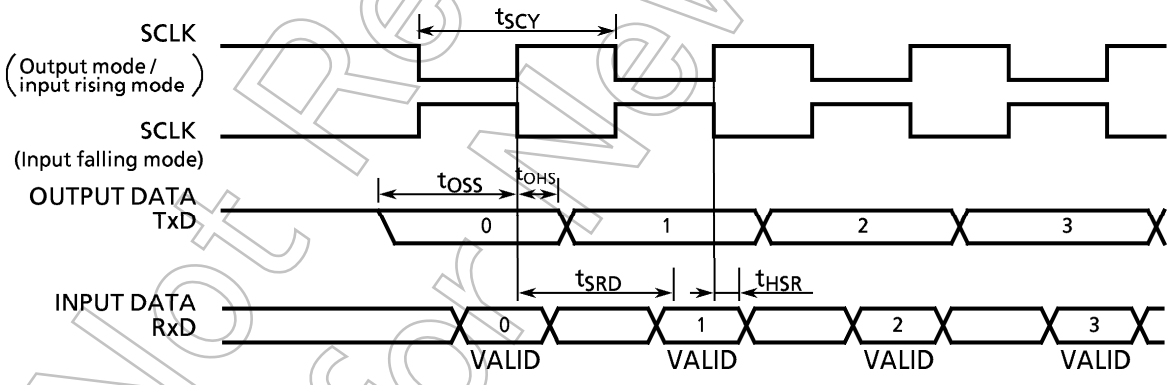
Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16x		1.6		0.64		μs
Output Data →SCLK rise/fall*	t_{OSS}	t_{SCY}/2 – 5x – 50		250		70		ns
SCLK rise/fall* →Output Data hold	t_{OHS}	5x – 100		400		100		ns
SCLK rise/fall* →input data hold	t_{HSR}	0		0		0		ns
SCLK rise/fall* →valid data input	t_{SRD}		t_{SCY} – 5x – 100		1000		340	ns

*) SCLK rise/fall: In SCLK rising edge mode, SCLK rising edge timing; in SCLK falling edge mode, SCLK falling edge timing

② SCLK output mode

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16x	8192x	1.6	819.2	0.64	327.6	μs
Output Data →SCLK rising edge	t_{OSS}	t_{SCY} – 2x – 150		1250		410		ns
SCLK rising edge →Output Data hold	t_{OHS}	2x – 80		120		0		ns
SCLK rising edge →Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge →valid data input	t_{SRD}		t_{SCY} – 2x – 150		1250		410	ns



(2) UART Mode (SCLK1 External Input)

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	4x + 20		420		180		ns
Low-level SCLK pulse width	t_{SCYL}	2x + 5		205		85		ns
High-level SCLK pulse width	t_{SCYH}	2x + 5		205		85		ns

3.5 Event Counter (External Input Clocks: TI0, TI4, TI8, TI9, TIA, TIB)

Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
External input clock cycle	t_{VCK}	8x + 100		900		420		ns
External low-level input clock pulse width	t_{VCKL}	4x + 40		440		200		ns
External high-level input clock pulse width	t_{VCKH}	4x + 40		440		200		ns

3.6 Interrupt Operation

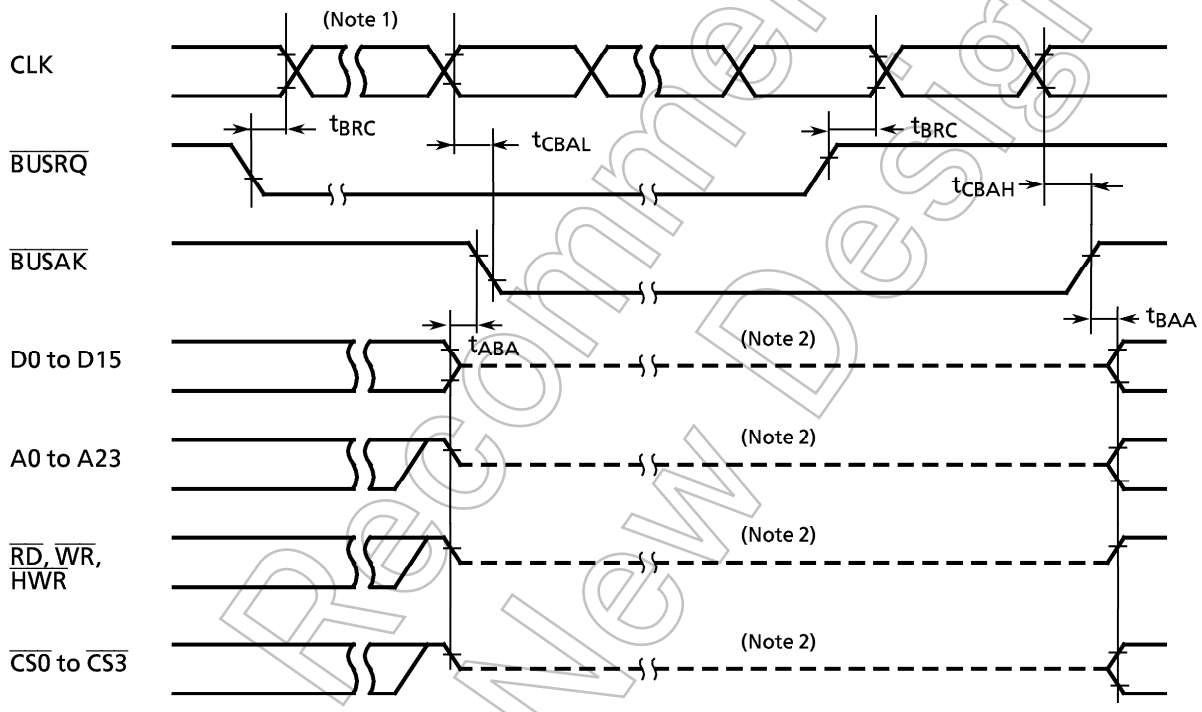
Vcc = + 5 V ± 10%, Ta = – 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 to 4 low-level pulse width	t_{INTAL}	4x		400		160		ns
$\overline{NMI}$, INT0 to 4 high-level pulse width	t_{INTAH}	4x		400		160		ns
INT5 to INT8 low-level pulse width	t_{INTBL}	8x + 100		900		420		ns
INT5 to INT8 high-level pulse width	t_{INTBH}	8x + 100		900		420		ns

3.7 Bus Request/Bus Acknowledge Timing

Vcc = + 5 V ± 10%, Ta = − 20 to + 70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ setup time for CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ fall	t_{CBAL}		2.0x + 120		320		200	ns
CLK→ $\overline{BUSAK}$ rise	t_{CBAH}		0.5x + 40		90		60	ns
Time from output buffer off until $\overline{BUSAK}$ falling edge	t_{ABA}	0	80	0	80	0	80	ns
Time from $\overline{BUSAK}$ rising edge until output buffer on	t_{BAA}	0	80	0	80	0	80	ns



Note 1: When $\overline{BUSRQ}$ goes to low level to request bus release, if the current bus cycle is yet complete due to a wait, the bus is not released until the wait completes.

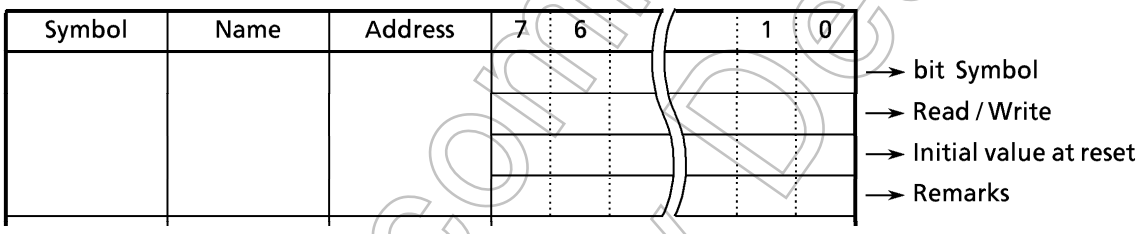
Note 2: The dotted line indicates only that the output buffer is off, not that the signal is at middle level. Immediately after bus release, the signal level prior to the bus release is held dynamically by the external load capacitance. Therefore, designs should allow for the fact that when using an external resistor or similar to fix the signal level while the bus is released, after bus release a delay occurs before the signal goes to its fixed level (due to the CR time constant). The internal programmable pull-up resistor continues to function in accordance with the internal signal level.

4. List of Special Function Registers (SFR)

The special function registers (SFR), which control the input/output ports and peripheral components, are allocated 160 bytes within the 000000H to 00009FH address range.
The registers built into cannot be accessed from outside.

(1) Input/output port
(2) Input/output port control
(3) Timer control
(4) Serial channel control
(5) Interrupt control
(6) Watchdog timer control
(7) Chip select/wait controller
(8) D/A converter control
(9) A/D converter control

Table structure



(Supplement for symbols used in Table)

① Read / Write
- R/W: Both readable and writable
- R: Readable
- W: Writable
- *R/W: Read-modify-write (RMW) instructions are prohibited for controlling ON/OFF of the pull-up resistors.

② RMW prohibited
- Cannot be read, modified, and written. (Cannot use the following instructions: EX, ADD, ADC, SUB, SBC, INC, DEC, AND, OR, XOR, STCF, RES, SET, CHG, TEST, RLC, RRC, RL, RR, SLA, SRA, SLL, SRL, RLD, RRD)

Table 5 List of TMP95CS64/265 Special Function Register Addresses

Address	Register Name	Address	Register Name	Address	Register Name	Address	Register Name
000000H	P0	30H	TREG8L	60H	(Reserved)	90H	B0CS
1H	P1	1H	TREG8H	1H	(Reserved)	1H	B1CS
2H	P0CR	2H	TREG9L	2H	(Reserved)	2H	B2CS
3H	(Reserved)	3H	TREG9H	3H	(Reserved)	3H	B3CS
4H	P1CR	4H	CAP1L	4H	(Reserved)	4H	MSAR0
5H	P1FC	5H	CAP1H	5H	(Reserved)	5H	MAMR0
6H	P2	6H	CAP2L	6H	(Reserved)	6H	MSAR1
7H	P3	7H	CAP2H	7H	(Reserved)	7H	MAMR1
8H	P2CR	8H	T8MOD	8H	(Reserved)	8H	MSAR2
9H	P2FC	9H	T8FFCR	9H	(Reserved)	9H	MAMR2
AH	P3CR	AH	T89CR	AH	SDMACR0	AH	MSAR3
BH	P3FC	BH	T16RUN	BH	SDMACR1	BH	MAMR3
CH	P4	CH	(Reserved)	CH	SDMACR2	CH	BEXCS
DH	P5	DH		DH	SDMACR3	DH	(Reserved)
EH	P4CR	EH		EH	WDMOD	EH	(Reserved)
FH	P4FC	FH		FH	WDCR	FH	(Reserved)
10H	P5CR	40H	TREGAL	70H	INTE0AD		
1H	P5FC	1H	TREGAH	1H	INTE12		
2H	P6	2H	TREGBL	2H	INTE34		
3H	P7	3H	TREGBH	3H	INTE56		
4H	(Reserved)	4H	CAP3L	4H	INTE78		
5H	P6FC	5H	CAP3H	5H	INTET01		
6H	P7CR	6H	CAP4L	6H	INTET23		
7H	P7FC	7H	CAP4H	7H	INTET45		
8H	P8	8H	T9MOD	8H	INTET67		
9H	P9	9H	T9FFCR	9H	INTET89		
AH	P8CR	AH	(Reserved)	AH	INTETAB		
BH	P8FC	BH	(Reserved)	BH	NTETOV		
CH	P9CR	CH	(Reserved)	CH	INTES0		
DH	P9FC	DH	(Reserved)	DH	INTES1		
EH	PA	EH	(Reserved)	EH	INTES2		
FH	(Reserved)	FH	(Reserved)	FH	INTETC01		
20H	T8RUN	50H	SC1BUF	80H	INTETC23		
1H	TRDC	1H	SC1CR	1H	(Reserved)		
2H	TREG0	2H	SC1MOD	2H			
3H	TREG1	3H	BR1CR	3H			
4H	T01MOD	4H	(Reserved)	4H			
5H	T02FFCR	5H	(Reserved)	5H			
6H	TREG2	6H	(Reserved)	6H			
7H	TREG3	7H	(Reserved)	7H			
8H	T23MOD	8H	ODE	8H			
9H	TREG4	9H	IIMC	9H			
AH	TREG5	AH	DMA0V	AH			
BH	T45MOD	BH	DMA1V	BH			
CH	T46FFCR	CH	DMA2V	CH			
DH	TREG6	DH	DMA3V	DH			
EH	TREG7	EH	(Reserved)	EH			
FH	T67MOD	FH	(Reserved)	FH			

(1) Input/Output Ports

Symbol	Name	Address	7	6	5	4	3	2	1	0
P0	Port 0 Register	00H	P07	P06	P05	P04	P03	P02	P01	P00
			R/W							
			Input mode (output latch register undefined)							
			shared with D7 to D0							
P1	Port 1 Register	01H	P17	P16	P15	P14	P13	P12	P11	P10
			R/W							
			Input mode (output latch register cleared to 0)							
			shared with D15 to D8							
P2	Port 2 Register	06H	P27	P26	P25	P24	P23	P22	P21	P20
			R/W							
			Input mode (output latch register cleared to 0)							
			shared with D23 to D16							
P3	Port 3 Register	07H	P37	P36	P35	P34	P33	P32	P31	P30
			R/W							
			Input mode (output latch register cleared to 0)							
			shared with A15 to A8							
P4	Port 4 Register	0CH	P47	P46	P45	P44	P43	P42	P41	P40
			R/W							
			Input mode (output latch register cleared to 0)							
			shared with A7 to A0							
P5	Port 5 Register	0DH	P57	P56	P55	P54	P53	P52	P51	P50
			*R/W							
			Input mode (set to 1 / Pull-up)						Output only (set to 1) (Note)	
				Shared with INT0	Shared with WAIT	Shared with BUSAK	Shared with BUSRQ	Shared with HWR	Shared with WR	Shared with RD
P6	Port 6 Register	12H					P63	P62	P61	P60
							R/W			
							Output mode (set to 1)			
							Shared with CS3	Shared with CS2	Shared with CS1	Shared with CS0
P7	Port 7 Register	13H			P75	P74	P73	P72	P71	P70
					R/W					
					Input mode (output latch register cleared to 0)					
					Shared with TO7/INT4	Shared with TO5	Shared with TI4/INT3	Shared with TO3/INT2	Shared with TO1	Shared with TI0/INT1
P8	Port 8 Register	18H	P87	P86	P85	P84	P83	P82	P81	P80
			*R/W							
			Input mode (set to 1/pulled up)							
					Shared with SCLK1/CTS1	Shared with RxD1	Shared with TxD1			
P9	Port 9 Register	19H		P96	P95	P94	P93	P92	P91	P90
				R/W						
				Input mode (output latch register cleared to 0)						
				Shared with TOA/TOB	Shared with TIB/INT8	Shared with TIA/INT7	Shared with TO9	Shared with TO8	Shared with TI9/INT6	Shared with TI8/INT5
PA	Port A Register	1EH	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
			R							
			Input-only							

Note: When P5<P50> is cleared to 0 with P50 set as an $\overline{RD}$ pin, the P50 $\overline{RD}$ signal is still output even when the internal address area is accessed (for PSRAM).

(2) Input/Output Port Control (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
P0CR	Port 0 Control Register	02H (RMW prohibited)	P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT							
P1CR	Port 1 Control Register	04H (RMW prohibited)	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT							
P1FC	Port 1 Function Register	05H (RMW prohibited)	P17F	P16F	P15F	P14F	P13F	P12F	P11F	P10F
			W							
			0	0	0	0	0	0	0	0
			0: PORT 1: D15 to D8 (P1CR = 00H)							
P2CR	Port 2 Control Register	08H (RMW prohibited)	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT							
P2FC	Port 2 Function Register	09H (RMW prohibited)	P27F	P26F	P25F	P24F	P23F	P22F	P21F	P20F
			W							
			0	0	0	0	0	0	0	0
			0: PORT 1: A23 to A16 (P2CR = FFH)							
P3CR	Port 3 Control Register	0AH (RMW prohibited)	P37C	P36C	P35C	P34C	P33C	P32C	P31C	P30C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT							
P3FC	Port 3 Function Register	0BH (RMW prohibited)	P37F	P36F	P35F	P34F	P33F	P32F	P31F	P30F
			W							
			0	0	0	0		0	0	0
			0: PORT 1: A15 to A8 (P3CR = FFH)							
P4CR	Port 4 Control Register	0EH (RMW prohibited)	P47C	P46C	P45C	P44C	P43C	P42C	P41C	P40C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT							
P4FC	Port 4 Function Register	0FH (RMW prohibited)	P47F	P46F	P45F	P44F	P43F	P42F	P41F	P40F
			W							
			0	0	0	0	0	0	0	0
			0: PORT 1: A7 to A0 (P4CR = FFH)							
P5CR	Port 5 Control Register	10H (RMW prohibited)	P57C	P56C	P55C	P54C	P53C	P52C		
			W							
			0	0	0	0	0	0		
			0: IN 1: OUT							
P5FC	Port 5 Function Register	11H (RMW prohibited)				P54F	P53F	P52F	P51F	P50F
								W		
						0	0	0	0	0
						0: PORT 1: $\overline{BUSAK}$	0: PORT 1: $\overline{BUSRQ}$	0: PORT 1: $\overline{HWR}$	0: PORT 1: $\overline{WR}$	0: PORT 1: $\overline{RD}$

Input/Output Port Control (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
P6FC	Port 6 Function Register	15H (RMW prohibited)					P63F	P62F	P61F	P60F
							W			
							0	0	0	0
							0: PORT 1: $\overline{CS3}$	0: PORT 1: $\overline{CS2}$	0: PORT 1: $\overline{CS1}$	0: PORT 1: $\overline{CS0}$
P7CR	Port 7 Control Register	16H (RMW prohibited)			P75C	P74C	P73C	P72C	P71C	P70C
							W			
					0	0	0	0	0	0
							0: IN	1: OUT		
P7FC	Port 7 Function Register	17H (RMW prohibited)			P75F	P74F		P72F	P71F	
					W			W		
					0	0		0	0	
					0: PORT 1: TO7	0: PORT 1: TO5		0: PORT 1:TO3	0: PORT 1: TO1	
P8CR	Port 8 Control Register	1AH (RMW prohibited)	P87C	P86C	P85C	P84C	P83C	P82C	P81C	P80C
			W							
			0	0	0	0	0	0	0	0
			0: IN				1: OUT			
P8FC	Port 8 Function Register	1BH (RMW prohibited)			P85F		P83F			
					W		W			
					0		0			
					0: PORT 1: SCLK1 /$\overline{CTS1}$		0: PORT 1: TxD1			
P9CR	Port 9 Control Register	1CH (RMW prohibited)		P96C	P95C	P94C	P93C	P92C	P91C	P90C
							W			
				0	0	0	0	0	0	0
						0: IN		1: OUT		
P9FC	Port 9 Function Register	1DH (RMW prohibited)	TOS1	P96F			P93F	P92F		
			W				W			
			0	0			0	0		
			0: TOA 1: TOB	0: PORT 1: TOA / TOB			0: PORT 1: TO9	0: PORT 1: TO8		

(3) Timer Control (1/4)

Symbol	Name	Address	7	6	5	4	3	2	1	0
T8RUN	8 bit Timer Run Control Register	20H	T7RUN	T6RUN	T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN
			R/W							
			0	0	0	0	0	0	0	0
			8-bit timer 7 0: Stop and clear 1: Count	8-bit timer 6 0: Stop and clear 1: Count	8-bit timer 5 0: Stop and clear 1: Count	8-bit timer 4 0: Stop and clear 1: Count	8-bit timer 3 0: Stop and clear 1: Count	8-bit timer 2 0: Stop and clear 1: Count	8-bit timer 1 0: Stop and clear 1: Count	8-bit timer 0 0: Stop and clear 1: Count
TRDC	Timer Register Double Buffer Control Register	21H					TR6DE	TR4DE	TR2DE	TR0DE
							R/W			
							0	0	0	0
							TREG6 double buffer 0: Disable 1: Enable	TREG4 double buffer 0: Disable 1: Enable	TREG2 double buffer 0: Disable 1: Enable	TREG0 double buffer 0: Disable 1: Enable
TREG0	8 bit Timer Register 0	22H (RMW prohibited)	–							
			W							
			Undefined							
TREG1	8 bit Timer Register 1	23H (RMW prohibited)	–							
			W							
			Undefined							
T01 MOD	8 bit Timer 0, 1 Mode Control Register	24H	T01M1	T01M0	PWM01	PWM00	T1CLK1	T1CLK0	T0CLK1	T0CLK0
			R/W							
			0	0	0	0	0	0	0	0
			Timer 0, 1 operating mode setting 00: 8 bit timer 01: 16 bit timer 10: 8 bit PPG 11: 8 bit PWM		PWM0 cycle selection 00: Don't care 01: $2^6 - 1$ 10: $2^7 - 1$ 11: $2^8 - 1$		Timer 1 input clock selection 00: TO0TRG 01: ϕT1 10: ϕT16 11: ϕT256		Timer 0 input clock selection 00: TI0 input 01: ϕT1 10: ϕT4 11: ϕT16	
T02 FFCR	8 bit Timer 0, 2 Flip-Flop Control Register	25H	FF3C1	FF3C0	FF3IE	FF3IS	FF1C1	FF1C0	FF1IE	FF1IS
			W		R/W		W		R/W	
			1	1	0	0	1	1	0	0
			00: Invert TFF3 01: Set TFF3 10: Clear TFF3 11: Don't care		TFF3 inversion control 0: Disable 1: Enable	0: Inversion by timer 2 1: Inversion by timer 3	00: Invert TFF1 01: Set TFF1 10: Clear TFF1 11: Don't care		TFF1 inversion control 0: Disable 1: Enable	0: Inversion by timer 0 1: Inversion by timer 1
TREG2	8 bit Timer Register 2	26H (RMW prohibited)	–							
			W							
			Undefined							
TREG3	8 bit Timer Register 3	27H (RMW prohibited)	–							
			W							
			Undefined							
T23 MOD	8 bit Timer 2, 3 Mode Control Register	28H	T23M1	T23M0	PWM21	PWM20	T3CLK1	T3CLK0	T2CLK1	T2CLK0
			R/W							
			0	0	0	0	0	0	0	0
			Timer 2, 3 operating mode setting 00: 8 bit timer 01: 16 bit timer 10: 8 bit PPG 11: 8 bit PWM		PWM2 cycle selection 00: Don't care 01: $2^6 - 1$ 10: $2^7 - 1$ 11: $2^8 - 1$		Timer 3 input clock selection 00: TO2TRG 01: ϕT1 10: ϕT16 11: ϕT256		Timer 2 input clock selection 00: Don't care 01: ϕT1 10: ϕT4 11: ϕT16	

Timer Control (2/4)

Symbol	Name	Address	7	6	5	4	3	2	1	0
TREG4	8 bit Timer Register4	29H (RMW prohibited)	–							
			W							
			Undefined							
TREG5	8 bit Timer Register5	2AH (RMW prohibited)	–							
			W							
			Undefined							
T45 MOD	8 bit Timer 4, 5 Mode Control Register	2BH	T45M1	T45M0	PWM41	PWM40	T5CLK1	T5CLK0	T4CLK1	T4CLK0
			R/W							
			0	0	0	0	0	0	0	0
			Timer 4, 5 operating mode setting 00: 8 bit timer 01: 16 bit timer 10: 8 bit PPG 11: 8 bit PWM		PWM4 cycle selection 00: Don't care 01: $2^6 - 1$ 10: $2^7 - 1$ 11: $2^8 - 1$		Timer 5 input clock selection 00: TO4TRG 01: ϕT1 10: ϕT16 11: ϕT256		Timer 4 input clock selection 00: TI4 input 01: ϕT1 10: ϕT4 11: ϕT16	
T46 FFCR	8 bit Timer 4, 6 Flip-Flop Control Register	2CH	FF7C1	FF7C0	FF7IE	FF7IS	FF5C1	FF5C0	FF5IE	FF5IS
			W		R/W		W		R/W	
			1	1	0	0	1	1	0	0
			00: Invert TFF7 01: Set TFF7 10: Clear TFF7 11: Don't care		TFF7 inversion control 0: Disable 1: Enable	0: Inversion by timer 6 1: Inversion by timer 7	00: Invert TFF5 01: Set TFF5 10: Clear TFF5 11: Don't care		TFF5 inversion control 0: Disable 1: Enable	0: I inversion by timer 4 1: Inversion by timer 5
TREG6	8 bit Timer Register6	2DH (RMW prohibited)	–							
			W							
			Undefined							
TREG7	8 bit Timer Register7	2EH (RMW prohibited)	–							
			W							
			Undefined							
T67 MOD	8 bit Timer 6, 7 Mode Control Register	2FH	T67M1	T67M0	PWM61	PWM60	T7CLK1	T7CLK0	T6CLK1	T6CLK0
			R/W							
			0	0	0	0	0	0	0	0
			Timer 6, 7 operating mode setting 00: 8 bit timer 01: 16 bit timer 10: 8 bit PPG 11: 8 bit PWM		PWM6 cycle selection 00: Don't care 01: $2^6 - 1$ 10: $2^7 - 1$ 11: $2^8 - 1$		Timer 7 input clock selection 00: TO6TRG 01: ϕT1 10: ϕT16 11: ϕT256		Timer 6 input clock selection 00: Don't care 01: ϕT1 10: ϕT4 11: ϕT16	
TREG8L	16 bit Timer Register8L	30H (RMW prohibited)	–							
			W							
			Undefined							
TREG8H	16 bit Timer Register8H	31H (RMW prohibited)	–							
			W							
			Undefined							
TREG9L	16 bit Timer Register9L	32H (RMW prohibited)	–							
			W							
			Undefined							
TREG9H	16 bit Timer Register9H	33H (RMW prohibited)	–							
			W							
			Undefined							

Timer Control (3/4)

Symbol	Name	Address	7	6	5	4	3	2	1	0
CAP1L	Capture Register1L	34H	–							
			R							
			Undefined							
CAP1H	Capture Register1H	35H	–							
			R							
			Undefined							
CAP2L	Capture Register2L	36H	–							
			R							
			Undefined							
CAP2H	Capture Register2H	37H	–							
			R							
			Undefined							
T8MOD	16 bit Timer 8 Mode Control Register	38H	CAP2T9	EQ9T9	CAP1IN	CAP12M1	CAP12M0	CLE	T8CLK1	T8CLK0
			R/W		W			R/W		
			0	0	1	0	0	0	0	0
			TFF9 inversion trigger 0: Trigger Disable 1: Trigger Enable		0: Software capture 1: Don't care	Capture timing 00: Disable 01: TI8 ↑ TI9 ↑ 10: TI8 ↑ TI8 ↓ 11: TFF1 ↑ TFF1 ↓		Timer 8 up-counter control 0: Clear disabled 1: Clear at match with TREG9	Timer 8 input clock selection 00: TI8 input 01: ϕT1 10: ϕT4 11: ϕT16	
			At loading of up-counter value to CAP2	At match between up-counter and TREG9						
T8FFCR	16 bit Timer 8 Flip-Flop Control Register	39H	TFF9C1	TFF9C0	CAP2T8	CAP1T8	EQ9T8	EQ8T8	TFF8C1	TFF8C0
			W		R/W				W	
			1	1	0	0	0	0	1	1
			00: Invert TFF9 01: Set TFF9 10: Clear TFF9 11: Don't care		TFF8 inversion trigger 0: Trigger Disable 1: Trigger Enable				00: Invert TFF8 01: Set TFF8 10: Clear TFF8 11: Don't care	
					At loading of up-counter value to CAP2	At loading of up-counter value to CAP3	At match between up-counter and TREG9	At match between up-counter and TREG8		
T89CR	Timer 8/9 Control Register	3AH	–					–	DBAEN	DB8EN
			R/W						R/W	
			0					0	0	0
			Note: Always fixed to 0.					Note: Always fixed to 0.	TREGA double buffer 0: Disable 1: Enable	TREG8 double buffer 0: Disable 1: Enable
T16RUN	16 bit Timer Run Control Register	3BH	PRRUN		T9RUN	T8RUN				
			R/W		R/W					
			0		0	0				
			Prescaler 0: Stop and clear 1: Count		16-bit timer 9 0: Stop and clear 1: Count	16-bit timer 8 0: Stop and clear 1: Count				

Timer Control (4/4)

Symbol	Name	Address	7	6	5	4	3	2	1	0
TREGAL	16 bit Timer RegisterAL	40H (RMW prohibited)	–							
			W							
			Undefined							
TREGAH	16 bit Timer RegisterAH	41H (RMW prohibited)	–							
			W							
			Undefined							
TREGBL	16 bit Timer RegisterBL	42H (RMW prohibited)	–							
			W							
			Undefined							
TREGBH	16 bit Timer RegisterBH	43H (RMW prohibited)	–							
			W							
			Undefined							
CAP3L	Capture Register3L	44H	–							
			R							
			Undefined							
CAP3H	Capture Register3H	45H	–							
			R							
			Undefined							
CAP4L	Capture Register4L	46H	–							
			R							
			Undefined							
CAP4H	Capture Register4H	47H	–							
			R							
			Undefined							
T9MOD	16 bit Timer 9 Mode Control Register	48H	CAP4TB	EQBTB	CAP3IN	CAP34M1	CAP34M0	CLE	T9CLK1	T9CLK0
			R/W		W	R/W				
			0	0	1	0	0	0	0	0
			TFFB inversion trigger 0: Trigger Disable 1: Trigger Enable		0: Software capture 1: Don't care	Capture timing 00: Disable 01: TIA ↑ TIB ↑ 10: TIA ↑ TIA ↓ 11: TFF1 ↑ TFF1 ↓		Timer 9 up-counter control 0: Clear disabled 1: Clear at match with TREGB	Timer 8 input clock selection 00: TIA input 01: ϕT1 10: ϕT4 11: ϕT16	
			At loading of up-counter value to CAP4	At match between up-counter and TREGB						
T9FFCR	16 bit Timer 9 Flip-Flop Control Register	49H	TFFBC1	TFFBC0	CAP4TA	CAP3TA	EQBTA	EQATA	TFFAC1	TFFAC0
			W		R/W				W	
			1	1	0	0	0	0	1	1
			00: Invert TFFB 01: Set TFFB 10: Clear TFFB 11: Don't care		TFFA inversion trigger 0: Trigger Disable 1: Trigger Enable				00: Invert TFFA 01: Set TFFA 10: Clear TFFA 11: Don't care	
					At loading of up-counter value to CAP4	At loading of up-counter value to CAP3	At match between up-counter and TREGB	At match between up-counter and TREGA		

(4) Serial Channel Control

Symbol	Name	Address	7	6	5	4	3	2	1	0
SC1BUF	Serial Channel 1 Buffer Register	50H	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
			TB7	TB6	TB5	TB4	TB3	TB2	RB1	TB0
			R (receive) /W (send)							
			Undefined							
SC1CR	Serial Channel 1 Control Register	51H	RB8	EVEN	PE	OERR	PERR	FERR	SCLKS	IOC
			R	R/W		R (cleared to 0 when read)			R/W	
				0	0	0	0	0	0	0
			Bit 8 of receive data	Parity 0: Odd 1: Even	Parity addition 0: Disable 1: Enable	1: Error			0: SCLK1 (↑) 1: SCLK1 (↓)	I/O interface mode clock selection 0: Baud rate generator 1 1: SCLK1 pin input
						Overrun	Parity	Framing		
SC1-MOD	Serial Channel 1 Mode Control Register	52H	TB8	CTSE	RXE	WU	SM1	SM0	SC1	SC0
			R/W							
			Undefined	0	0	0	0	0	0	0
			Bit 8 of send data	Handshake function 0: CTS Disable 1: CTS Enable	Receive control 0: Disable 1: Enable	Wake-up function 0: Disable 1: Enable	Serial transfer mode selection 00: I/O interface mode 01: 7-bit UART mode 10: 8-bit UART mode 11: 9-bit UART mode		UART mode clock selection 00: TO2 trigger 01: Baud rate generator 1 10: Internal clock ϕ1 11: SCLK1 pin input (external clock)	
BR1CR	Baud Rate Generater 1 Control Register	53H	–		BR1CK1	BR1CK0	BR1S3	BR1S2	BR1S1	BR1S0
			R/W			R/W				
			0		0	0	0	0	0	0
			Note: Always fixed to 0.		Baud rate generator 1 input clock selection 00: ϕT0 (4/fc) 01: ϕT2 (16/fc) 10: ϕT8 (64/fc) 11: ϕT32 (256/fc)		Baud rate generator 1 divisor setting 0000: Divide by 16 0001: Divide by 1 (no division) to 1111: Divide by 15			
ODE	Serial Open Drain Enable Register	58H							ODE1	
									R/W	
									0	
									P83 output settings 0: CMOS 1: Open drain	

(5) Interrupt Control (1/3)

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTE-0AD	INT0/AD Enable Register	70H (RMW prohibited)	—				INT0			
							I0C	I0M2	I0M1	I0M0
							R/W Note)		W	
							0	0	0	0
INTE12	INT1/2 Enable Register	71H (RMW prohibited)	INT2				INT1			
			I2C	I2M2	I2M1	I2M0	I1C	I1M2	I1M1	I1M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTE34	INT3/4 Enable Register	72H (RMW prohibited)	INT4				INT3			
			I4C	I4M2	I4M1	I4M0	I3C	I3M2	I3M1	I3M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTE56	INT5/6 Enable Register	73H (RMW prohibited)	INT6				INT5			
			I6C	I6M2	I6M1	I6M0	I5C	I5M2	I5M1	I5M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTE78	INT7/8 Enable Register	74H (RMW prohibited)	INT8				INT7			
			I8C	I8M2	I8M1	I8M0	I7C	I7M2	I7M1	I7M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTET01	INTT0/1 Enable Register	75H (RMW prohibited)	INTT1 (timer 1)				INTT0 (timer 0)			
			IT1C	IT1M2	IT1M1	IT1M0	IT0C	IT0M2	IT0M1	IT0M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTET23	INTT2/3 Enable Register	76H (RMW prohibited)	INTT3 (timer 3)				INTT2 (timer 2)			
			IT3C	IT3M2	IT3M1	IT3M0	IT2C	IT2M2	IT2M1	IT2M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	
INTET45	INTT4/5 Enable Register	77H (RMW prohibited)	INTT5 (timer 5)				INTT4 (timer 4)			
			IT5C	IT5M2	IT5M1	IT5M0	IT4C	IT4M2	IT4M1	IT4M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTET67	INTT6/7 Enable Register	78H (RMW prohibited)	INTT7 (timer 7)				INTT6 (timer 6)			
			IT7C	IT7M2	IT7M1	IT7M0	IT6C	IT6M2	IT6M1	IT6M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTET89	INTTR8/9 Enable Register	79H (RMW prohibited)	INTTR9 (timer 8)				INTTR8 (timer 8)			
			IT9C	IT9M2	IT9M1	IT9M0	IT8C	IT8M2	IT8M1	IT8M0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0
INTETAB	INTTRA/B Enable Register	7AH (RMW prohibited)	INTTRB (timer 9)				INTTRA (timer 9)			
			ITBC	ITBM2	ITBM1	ITBM0	ITAC	ITAM2	ITAM1	ITAM0
			R/W		W		R/W		W	
			0	0	0	0	0	0	0	0

IxxM2	IxxM1	IxxM0	Function (Write)
0	0	0	Disables interrupt request
0	0	1	Sets interrupt request level to 1
0	1	0	Sets interrupt request level to 2
0	1	1	Sets interrupt request level to 3
1	0	0	Sets interrupt request level to 4
1	0	1	Sets interrupt request level to 5
1	1	0	Sets interrupt request level to 6
1	1	1	Disables interrupt request

Note: In INT0 level mode, the interrupt request flag cannot be cleared by writing 0 to <I0C>.

IxxC	Function (Read)	Function (Write)
0	Indicates no interrupt request generated	Clears interrupt request flag
1	Indicates interrupt request generated	----- Don't care -----

Interrupt Control (2/3)

Symbol	Name	Address	7	6	5	4	3	2	1	0
INTEOV	INTTO8/9 Enable Register	7BH (RMW prohibited)	INTTO9				INTTO8			
			ITO9C	ITO9M2	ITO9M1	ITO9M0	ITO8C	ITO8M2	ITO8M1	ITO8M0
			R/W	W			R/W	W		
			0	0	0	0	0	0	0	0
INTES1	INTRX1/ TX1 Enable Register	7DH (RMW prohibited)	INTTX1				INTRX1			
			ITX1C	ITX1M2	ITX1M1	ITX1M0	IRX1C	IRX1M2	IRX1M1	IRX1M0
			R/W	W			R (Note)	W		
			0	0	0	0	0	0	0	0
INTETC 01	INTTC0/1 Enable Register	7FH (RMW prohibited)	INTTC1				INTTC0			
			ITC1C	ITC1M2	ITC1M1	ITC1M0	ITC01C	ITC0M2	ITC0M1	ITC0M0
			R/W	W			R/W	W		
			0	0	0	0	0	0	0	0
INTETC 23	INTTC2/3 Enable Register	80H (RMW prohibited)	INTTC3				INTTC2			
			ITC3C	ITC3M2	ITC3M1	ITC3M0	ITC2C	ITC2M2	ITC2M1	ITC2M0
			R/W	W			R/W	W		
			0	0	0	0	0	0	0	0

IxxM2	IxxM1	IxxM0	Function (Write)
0	0	0	Disables interrupt request
0	0	1	Sets interrupt request level to 1
0	1	0	Sets interrupt request level to 2
0	1	1	Sets interrupt request level to 3
1	0	0	Sets interrupt request level to 4
1	0	1	Sets interrupt request level to 5
1	1	0	Sets interrupt request level to 6
1	1	1	Disables interrupt request

Note: <IRX1C> is read-only, an interrupt request cannot be cleared by writing 0 to these flags.

IxxC	Function (Read)	Function (Write)
0	Indicates no interrupt request generated	Clears interrupt request flag
1	Indicates interrupt request generated	----- Don't care -----

Interrupt Control (3/3)

Symbol	Name	Address	7	6	5	4	3	2	1	0
IIMC	Interrupt Input Mode Contorol Register	59H (RMW prohibited)			–			I0IE	I0LE	NMIREE
					W				W	
					0			0	0	0
					Note: Always set to 0			INT0 input 0: Disable 1: Enable	INT0 0: ↑ edge 1: level	$\overline{\text{NMI}}$ 0: ↓ edge 1: ↑ ↓ edge
DMA0V	Micro DMA 0 Start Vector Register	5AH (RMW prohibited)	DMA0V7	DMA0V6	DMA0V5	DMA0V4	DMA0V3	DMA0V2		
			W							
			0	0	0	0	0	0		
			Micro DMA0 start vector							
DMA1V	Micro DMA 1 Start Vector Register	5BH (RMW prohibited)	DMA1V7	DMA1V6	DMA1V5	DMA1V4	DMA1V3	DMA1V2		
			W							
			0	0	0	0	0	0		
			Micro DMA1 start vector							
DMA2V	Micro DMA 2 Start Vector Register	5CH (RMW prohibited)	DMA2V7	DMA2V6	DMA2V5	DMA2V4	DMA2V3	DMA2V2		
			W							
			0	0	0	0	0	0		
			Micro DMA2 start vector							
DMA3V	Micro DMA 3 Start Vector Register	5DH (RMW prohibited)	DMA3V7	DMA3V6	DMA3V5	DMA3V4	DMA3V3	DMA3V2		
			W							
			0	0	0	0	0	0		
			Micro DMA3 start vector							

Note: The micro DMA software start is activated in the write cycle of SDMACR0/1/2/3 (6AH/6BH/6CH/6DH). (Data values are not affected by a software start.)

(6) Watchdog Timer Control

Symbol	Name	Address	7	6	5	4	3	2	1	0
WD-MOD	Watch Dog Timer Mode Control Register	6EH	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRVE
			R/W							
			1	0	0	0	0	0	0	
			WDT control 0: Disable 1: Enable	WDT detection time selection 00: 2^{16}/fc 01: 2^{18}/fc 10: 2^{20}/fc 11: 2^{22}/fc		Warm-up time 0: 2^{14}/fc 1: 2^{16}/fc	HALT mode selection 00: RUN mode 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode		1: Perform internal reset on runaway detection	1: Drive pins in STOP mode
WDCR	Watch Dog Timer Control Register	6FH (RMW prohibited)	–							
			W							
			–							
			B1H: WDT disable code 4EH: WDT clear code							

(7) Chip Select/Wait Controller (1/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
B0CS	Block 0 CS/WAIT Control Register	90H (RMW prohibited)	B0E		B0OM1	B0OM0	B0BUS	B0W2	B0W1	B0W0
			W		W					
			0		0	0	0	0	0	0
			0: Disable 1: Enable		00: ROM/SRAM 01: PSRAM 10: Don't care 11: Don't care		Data bus width selection 0: 16-bit 1: 8-bit	000: 2WAIT 001: 1WAIT 010: 1WAIT + N 011: 0WAIT	100: NWAIT 101 110 111	Do not set
B1CS	Block 1 CS/WAIT Control Register	91H (RMW prohibited)	B1E		B1OM1	B1OM0	B1BUS	B1W2	B1W1	B1W0
			W		W					
			0		0	0	0	0	0	0
			0: Disable 1: Enable		00: ROM/SRAM 01: PSRAM 10: Don't care 11: Don't care		Data bus width selection 0: 16-bit 1: 8-bit	000: 2WAIT 001: 1WAIT 010: 1WAIT + N 011: 0WAIT	100: NWAIT 101 110 111	Do not set
B2CS	Block 2 CS/WAIT Control Register	92H (RMW prohibited)	B2E	B2M	B2OM1	B2OM0	B2BUS	B2W2	B2W1	B2W0
			W							
			1	0	0	0	0	0	0	0
			0: Disable 1: Enable	0: 16M 1: CS area setting	00: ROM/SRAM 01: PSRAM 10: Don't care 11: Don't care		Data bus width selection 0: 16-bit 1: 8-bit	000: 2WAIT 001: 1WAIT 010: 1WAIT + N 011: 0WAIT	100: NWAIT 101 110 111	Do not set
B3CS	Block 3 CS/WAIT Control Register	93H (RMW prohibited)	B3E		B3OM1	B3OM0	B3BUS	B3W2	B3W1	B3W0
			W		W					
			0		0	0	0	0	0	0
			0: Disable 1: Enable		00: ROM/SRAM 01: PSRAM 10: Don't care 11: Don't care		Data bus width selection 0: 16-bit 1: 8-bit	000: 2WAIT 001: 1WAIT 010: 1WAIT + N 011: 0WAIT	100: NWAIT 101 110 111	Do not set
BEXCS	External CS/WAIT Control Register	9CH (RMW prohibited)					BEXBUS	BEXBUS	BEXW1	BEXW0
							W			
							0	0	0	0
							Data bus width selection 0: 16-bit 1: 8-bit	000: 2WAIT 001: 1WAIT 010: 1WAIT + N 011: 0WAIT	100: NWAIT 101 110 111	Do not set
MSAR0	Memory Start Address Register 0	94H	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16 setting							
MAMR0	Memory Address Mask Register 0	95H	V20	V19	V18	V17	V16	V15	V14 to 9	V8
			R/W							
			1	1	1	1	1	1	1	1
			CS0 area size setting 0: Used for address comparison							
MSAR1	Memory Start Address Register 1	96H	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16 setting							
MAMR1	Memory Address Mask Register 1	97H	V21	V20	V19	V18	V17	V16	V15 to 9	V8
			R/W							
			1	1	1	1	1	1	1	1
			CS1 area size setting 0: Used for address comparison							

Chip Select/Wait Controller (2/2)

Symbol	Name	Address	7	6	5	4	3	2	1	0
MSAR2	Memory Start Address Register 2	98H	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16 setting							
MAMR2	Memory Address Mask Register 2	99H	V22	V21	V20	V19	V18	V17	V16	V15
			R/W							
			1	1	1	1	1	1	1	1
			CS2 area size setting 0: Used for address comparison							
MSAR3	Memory Start Address Register 3	9AH	S23	S22	S21	S20	S19	S18	S17	S16
			R/W							
			1	1	1	1	1	1	1	1
			Start address A23 to A16 setting							
MAMR3	Memory Address Mask Register 3	9BH	V22	V21	V20	V19	V18	V17	V16	V15
			R/W							
			1	1	1	1	1	1	1	1
			CS3 area size setting 0: Used for address comparison							

5. Diagram of Equivalent Circuit in Port Block

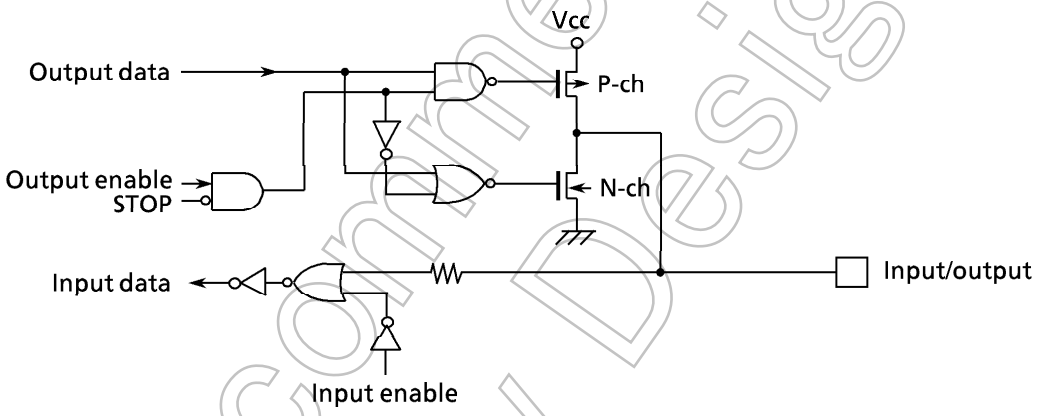
- Reading circuit diagrams

  TMP95CS66 use essentially the same gate symbols as the standard CMOS logic IC (74HCxxx) series. The following lists the special symbols.

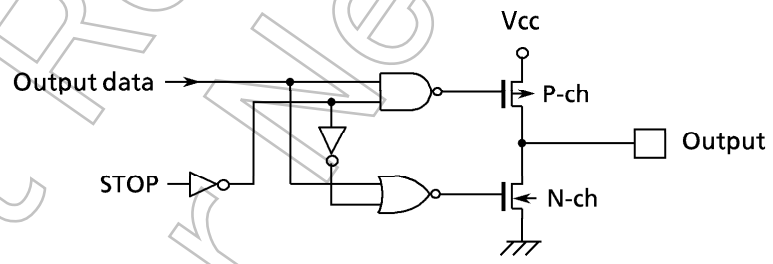
  STOP: This symbol sets the HALT mode setting register to STOP mode (WDMOD<HALTM1:0> = 0,1). When the CPU executes the HALT instruction, STOP is active 1.
  Note that when the drive enable bit WDMOD<DRVE> is set to 1, STOP remains at 0.

- The input protection resistor operates in the range of tens to hundreds of Ω ms.

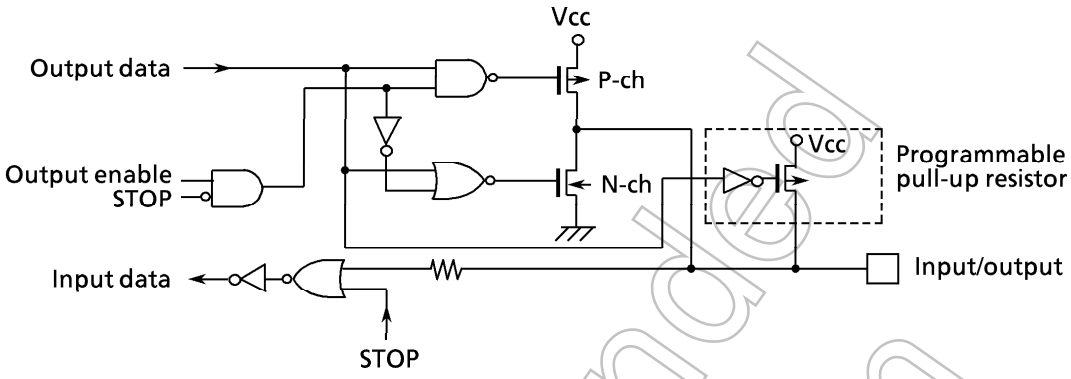
■ P0 (D0 to D7), P1 (D8 to 15), P2 (A16 to A23), P3 (A8 to A15), P4 (A0 to A7)



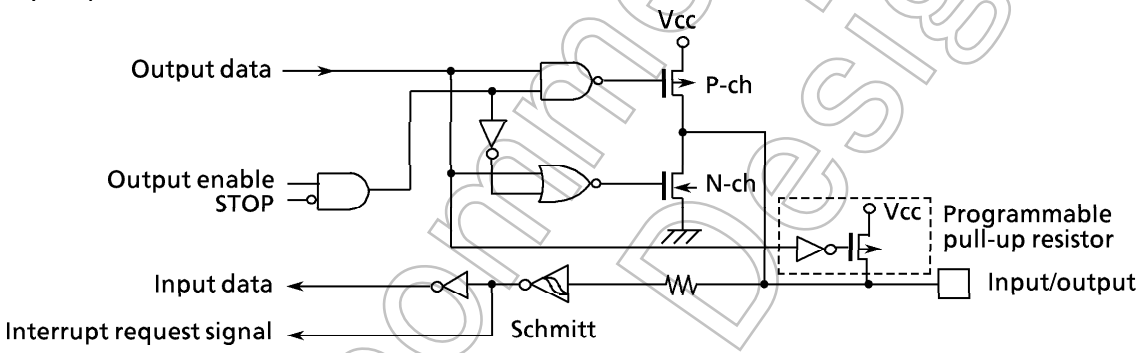
■ P50 ($\overline{RD}$), P51 ($\overline{WR}$), P6 ($\overline{CS0}$ to $\overline{CS3}$)



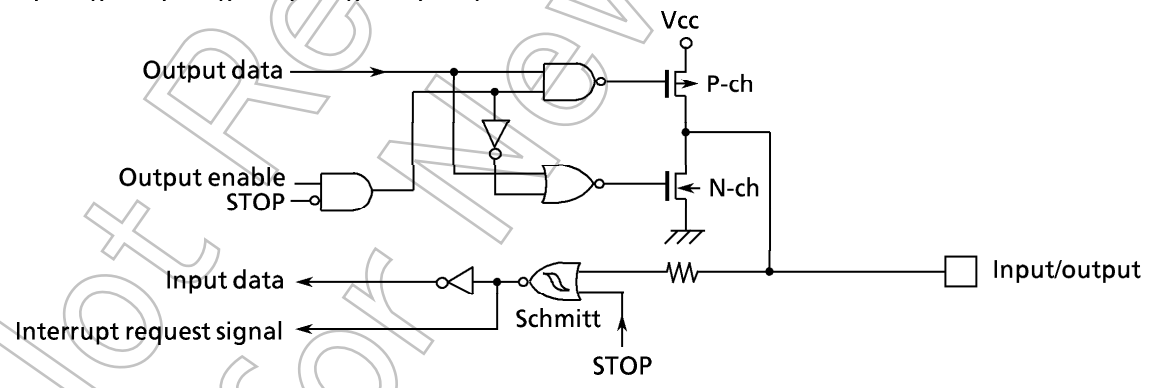
■ P52 to 55, P57, P80 to P82, P84 to P87



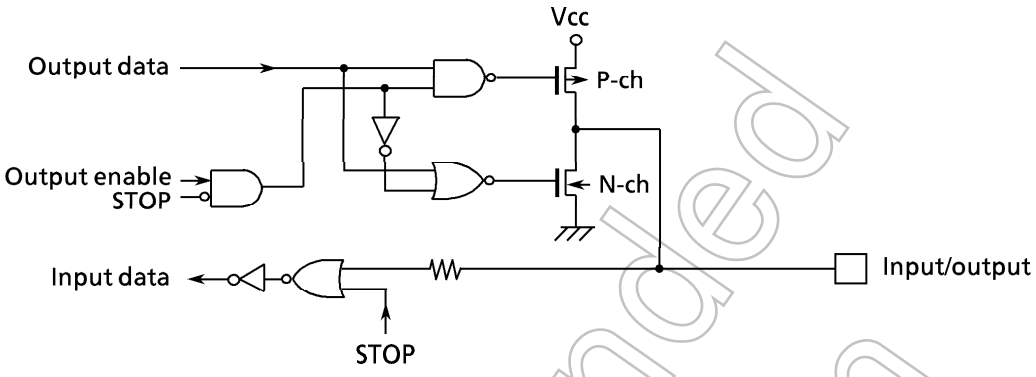
■ P56 (INT0)



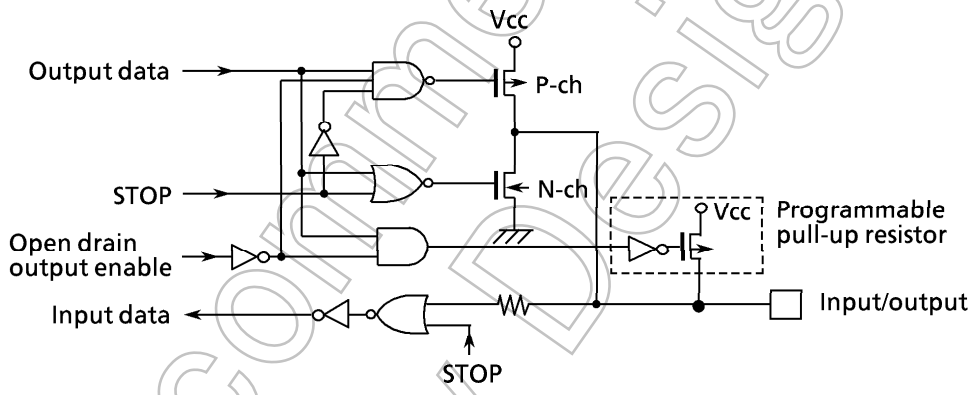
■ P70 (INT1), P72 (INT2), P73 (INT3), P75 (INT4)



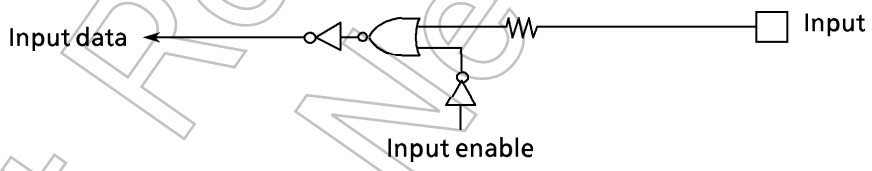
■ P71, P74, P90 to P96



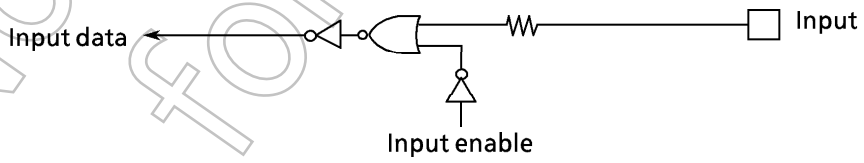
■ P83 (TxD1)



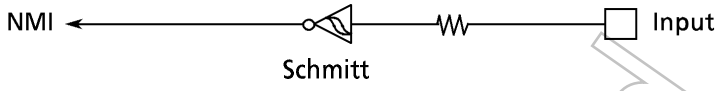
■ PA0 to 2, PA4 to 7



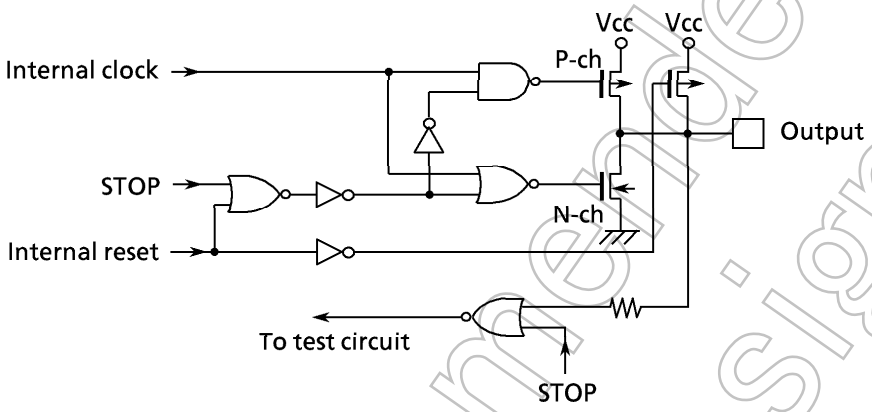
■ PA3 (AN3)



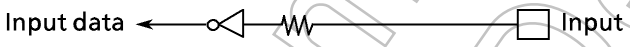
■ $\overline{NMI}$



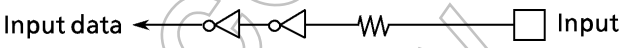
■ CLK



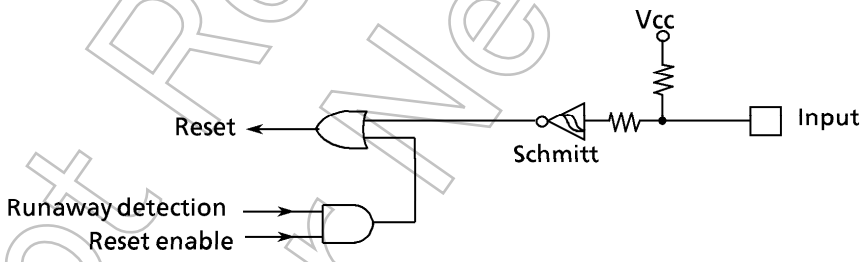
■ $\overline{EA}$



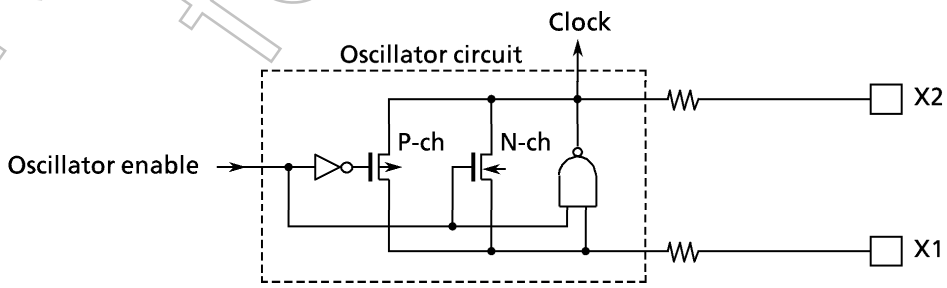
■ AM8/$\overline{16}$



■ $\overline{RESET}$



■ X1, X2



6. Use Precautions and Restrictions

(1) Special Notations and Words

① Description of internal I/O registers: Register symbol<bit symbol>

Example: T8RUN<T0RUN> … The T0RUN bit of the T8RUN register

② Read-modify-write instructions

Instructions which tell the CPU to read the data in memory, manipulate them, then write them back to memory are called read-modify-write instructions.
Example 1) SET 3, (T8RUN) … Sets bit 3 of the T8RUN register.
Example 2) INC 1, (100H) … Adds 1 to the data at address 100H.

- TLCS-900 read-modify-write instructions

Conversion instruction

```
EX   (mem), R
```

Arithmetic operations

```
ADD  (mem), R/#      ADC  (mem), R/#
SUB  (mem), R/#      SBC  (mem), R/#
INC  #3, (mem)       DEC  #3, (mem)
```

Logic operations

```
AND  (mem), R/#      OR   (mem), R/#
XOR  (mem), R/#
```

Bit manipulation

```
STCF #3/A, (mem)     SET  #3, (mem)
RES  #3, (mem)       TEST #3, (mem)
CHG  #3, (mem)
```

Rotate, shift

```
RLC  (mem)           RRC  (mem)
RL   (mem)           RR(mem)
SLA  (mem)           SRA  (mem)
SLL  (mem)           SRL  (mem)
RLD  (mem)           RRD  (mem)
```

③ One state

The single cycle resulting from dividing the oscillation frequency by 2 is called “one state”.
Example: At oscillation frequency 25 MHz
2/25 MHz = 80 ns = 1 state

(2) Points of Note and Restrictions

① $\overline{EA}$ pin, AM8/$\overline{16}$ pin

This pin is connected to the VCC or the GND pin. Do not alter the level while the pin is active.

② Warm-up counter

When releasing STOP mode (by interrupt, for example) in a system that uses an external oscillator, a warm-up time is required until the system clock is output. The warm-up counter operates during the warm-up time.

③ Programmable pull-up resistor

The pull-up resistor of a port can only be set to programmable or non-programmable in input port mode. When using a port as an output port, its pull-up resistor cannot be set to programmable.

④ Watchdog timer

As the watchdog timer is enabled after a reset, disable the watchdog timer when it is not required.
Note that during bus release, the I/O block, including the watchdog timer, still operate.

⑤ CPU (Micro DMA)

Only "LDC cr, r" and "LDC r, cr" can write or read data to or from control registers (eg, transfer source register DMASx) in the CPU.

⑥ As this device does not support minimum mode, do not use the MIN instruction.

⑦ POP SR instruction

Please execute POP SR instruction during DI condition.

⑧ Releasing the HALT mode by requesting an interruption

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{NMI}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)
If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.