

CMOS 16-Bit Microcontrollers

**TMP95CS66F**

**1. Outline and Features**

TMP95CS66 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment. This device is TNP95CS64 function cut. Otherwise, all the functions of the products are the same.

TMP95CS66 comes in a 100-pin flat package.

Listed below are the features.

- (1) High-speed 16-bit CPU (900/H CPU)
  - Instruction mnemonics are upward-compatible with TLCS-90/900
  - 16 Mbytes of linear address space
  - General-purpose registers and register banks
  - 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
  - Micro DMA: Four-channels (640 ns / 2 bytes at 25 MHz)
- (2) Minimum instruction execution time: 160 ns (at 25 MHz)
- (3) Built-in RAM: 2 Kbytes  
Built-in ROM: 64 Kbyte
- (4) External memory expansion
  - Expandable up to 16 Mbytes (shared program/data area)
  - External data bus width select pin (AM8/ $\overline{16}$ )
  - Can simultaneously support 8/16-bit width external data bus  
... Dynamic data bus sizing
- (5) 8-bit timers: 8 channels
  - With event counter function: 2 channels
- (6) 16-bit timer/event counter: 2 channels
- (7) General-purpose serial interface: 1 channels
- (8) Watchdog timer
- (9) Chip select/wait controller: 4 blocks

980910EBP1

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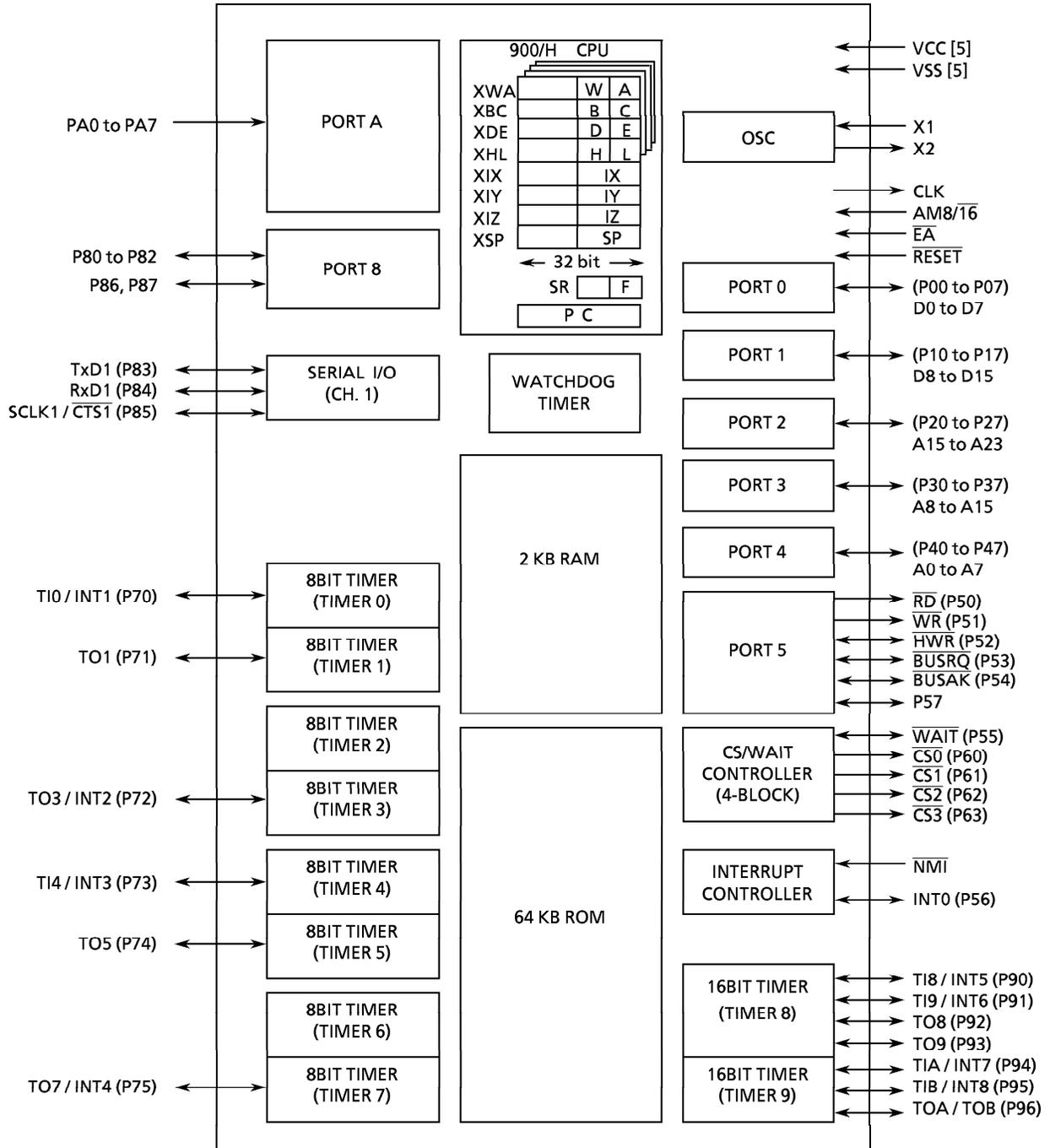
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- (10) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
  - 21 internal interrupts:
  - 10 external interrupts: ] Seven selectable priority levels
- (11) Input/output ports: 81 pins
- (12) Standby mode
- Four HALT modes: RUN, IDLE2, IDLE1, STOP
- (13) Operating voltage
- $V_{CC} = 4.5 - 5.5$  V
- (14) Package: P-LQFP100-1414-0.50D
- (15) Differences between TMP95CS64F and TMP95CS66

	TMP95CS64F	TMP95CS66F
10-bit A/D converter	8 channels	—
8-bit D/A converter	8 channels	—
Operating voltage	$V_{CC} = 4.5$ V to 5.5 V (@ f = 8 to 25 MHz) $V_{CC} = 2.7$ V to 3.3 V (@ f = 4 to 10 MHz)	$V_{CC} = 4.5$ V to 5.5 V (@ f = 8 to 25 MHz)



Note: After a reset function in parentheses ( ) are selected for the shared pins.

Product	AM8/16	Pin function after reset
TMP95CS66	Fixed to high level	Multi-use pins can select function in parentheses ( ).

Figure 1 TMP95CS66 Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP95CS66F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1 is a pin assignment diagram for TMP95CS66F.

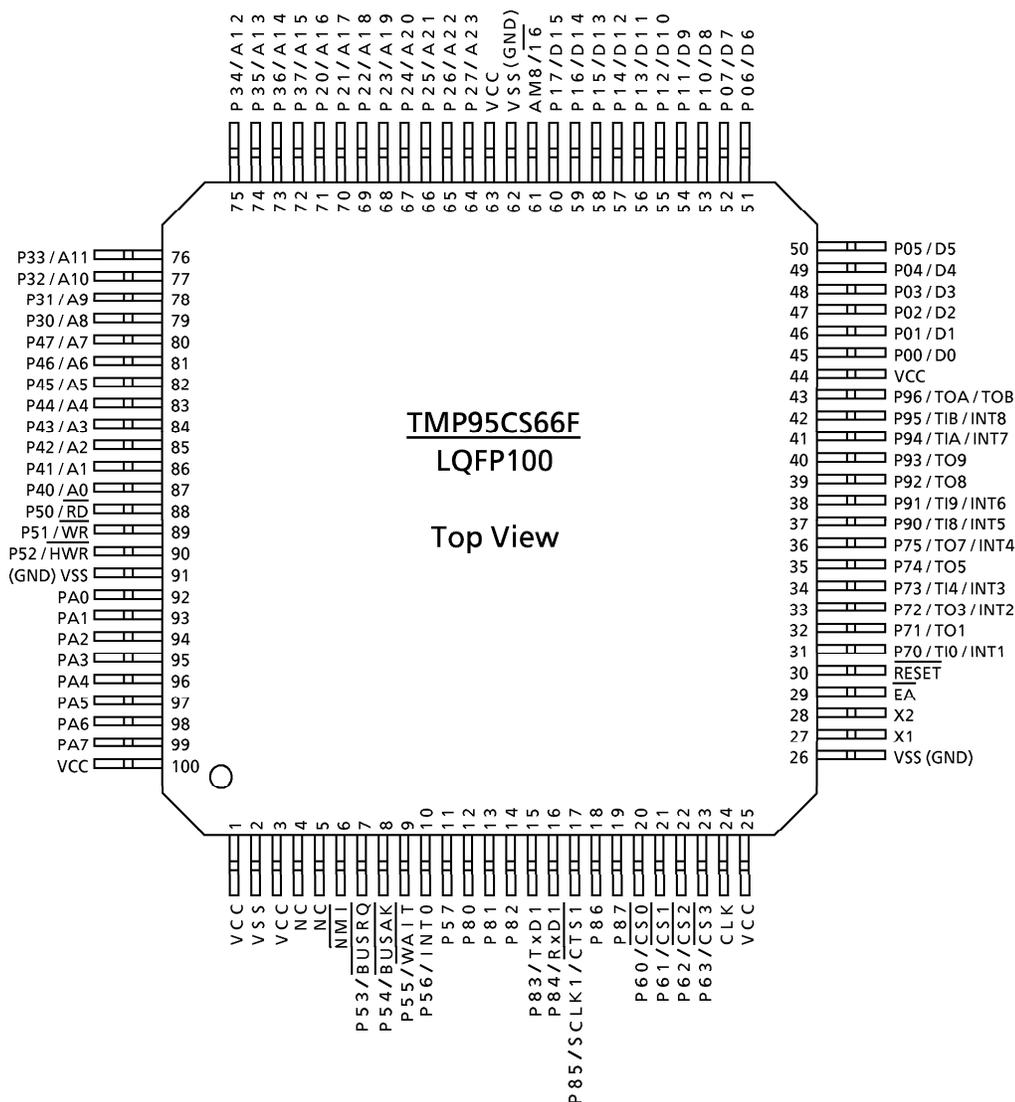


Figure 2.1 Pin Assignment Diagram (100-Pin LQFP)

## 2.2 Pin Names and Functions

Table 2.2 shows the names and functions of the input/output pins.

Table 2.2 Pin Names and Functions (1/3)

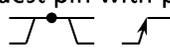
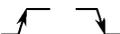
Pin Name	Number of Pins	Input/Output	Function
P00 to P07 / D0 to D7	8	Input/output	Port 0: I/O port. Input or output specifiable in units of bits
		Input/output	Data: Data bus 0 to 7
P10 to P17 / D8 to D15	8	Input/output	Port 1: I/O port. Input or output specifiable in units of bits
		Input/output	Data: Data bus 8 to 15
P20 to P27 / A16 to A23	8	Input/output	Port 2: I/O port. Input or output specifiable in units of bits
		Output	Address: Address bus 16 to 23
P30 to P37 / A8 to A15	8	Input/output	Port 3: I/O port. Input or output specifiable in units of bits
		Output	Address: Address bus 8 to 15
P40 to P47 / A0 to A7	8	Input/output	Port 4: I/O port. Input or output specifiable in units of bits
		Output	Address: Address bus 0 to 7
P50 / $\overline{RD}$	1	Output	Port 50: Output-only port
		Output	Read: Outputs strobe signal to read external memory (setting P5 <P50> = 0 and P5FC <P50F> = 1 outputs strobe signal at all read timings)
P51 / $\overline{WR}$	1	Output	Port 51: Output-only port.
		Output	Write: Outputs strobe signal to write data on pins D0 to D7
P52 / $\overline{HWR}$	1	Input/output	Port 52: I/O port (with built-in pull-up resistor)
		Output	Upper write: Outputs strobe signal to write data on pins D8 to D15
P53 / $\overline{BUSRQ}$	1	Input/output	Port 53: I/O port (with built-in pull-up resistor)
		Input	Bus request: Input pin to request external bus release
P54 / $\overline{BUSAK}$	1	Input/output	Port 54: I/O port (with built-in pull-up resistor)
		Output	Bus acknowledge: Output pin to acknowledge that CPU received $\overline{BUSRQ}$ and released external bus.
P55 / $\overline{WAIT}$	1	Input/output	Port 55: I/O port (with built-in pull up resistor)
		Input	Wait: Buswait request pin for CPU (Effective when 1 + N WAIT mode, or 0 + N WAIT mode. Set using chipselect/wait control register.)
P56 / INT0	1	Input/output	Port 56: I/O port (with built-in pull-up resistor)
		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. 
P57	1	Input/output	Port 57: I/O port (with built-in pull-up resistor)

Table 2.2 Pin Names and Functions (2/3)

Pin Name	Number of Pins	Input/Output	Function
P60 / $\overline{\text{CS0}}$	1	Output	Port 60: Output-only port
		Output	Chip select 0: Outputs 0 if address is within specified address range
P61 / $\overline{\text{CS1}}$	1	Output	Port 61: Output-only port
		Output	Chip select 1: Outputs 0 if address is within specified address range
P62 / $\overline{\text{CS2}}$	1	Output	Port 62: Output-only port
		Output	Chip select 2: Outputs 0 if address is within specified address range
P63 / $\overline{\text{CS3}}$	1	Output	Port 63: Output-only port
		Output	Chip select 3: Outputs 0 if address is within specified address range
P70 / $\text{TI0}$ / $\text{INT1}$	1	Input/output	Port 70: I/O port
		Input	Timer input 0: Input pin for timer 0
		Input	Interrupt request pin 1: Rising-edge interrupt request pin 
P71 / $\text{TO1}$	1	Input/output	Port 71: I/O port.
		Output	Timer output 1: Output pin for timer 0 or 1
P72 / $\text{TO3}$ / $\text{INT2}$	1	Input/output	Port 72: I/O port
		Output	Timer output 3: Output pin for timer 2 or 3
		Input	Interrupt request pin 2: Rising-edge interrupt request pin 
P73 / $\text{TI4}$ / $\text{INT3}$	1	Input/output	Port 73: I/O port
		Input	Timer input 4: Input pin for timer 4
		Input	Interrupt request pin 3: Rising-edge interrupt request pin 
P74 / $\text{TO5}$	1	Input/output	Port 74: I/O port
		Output	Timer output 5: Output pin for timer 4 or 5
P75 / $\text{TO7}$ / $\text{INT4}$	1	Input/output	Port 75: I/O port
		Output	Timer output 7: Output pin for timer 6 or 7
		Input	Interrupt request pin 4: Rising-edge interrupt request pin 
P80	1	Input/output	Port 80: I/O port (with built-in pull-up resistor)
P81	1	Input/output	Port 81: I/O port (with built-in pull-up resistor)
P82	1	Input/output	Port 82: I/O port (with built-in pull-up resistor)
P83 / $\text{TxD1}$	1	Input/output	Port 83: I/O port (with built-in pull-up resistor)
		Output	Serial transmission data 1
P84 / $\text{RxD1}$	1	Input/output	Port 84: I/O port (with built-in pull-up resistor)
		Input	Serial receive data 1
P85 / $\text{SCLK1}$ / $\overline{\text{CTS1}}$	1	Input/output	Port 85: I/O port (with built-in pull-up resistor)
		Input/output	Serial clock input/output 1
		Input	Serial data ready to send 1 (Clear-to-send)
P86	1	Input/output	Port 86: I/O port (with built-in pull-up resistor)
P87	1	Input/output	Port 87: I/O port (with built-in pull-up resistor)

Table 2.2 Pin Names and Functions (3/3)

Pin Name	Number of Pins	Input/Output	Function
P90 / TI8 / INT5	1	Input/output	Port 90: I/O port
		Input	Timer input 8: Input pin for timer 8
		Input	Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge 
P91 / TI9 / INT6	1	Input/output	Port 91: I/O port
		Input	Timer input 9: Input pin for timer 8
		Input	Interrupt request pin 6: Rising edge interrupt request pin 
P92 / TO8	1	Input/output	Port 92: I/O port
		Output	Timer output 8: Output pin for timer 8
P93 / TO9	1	Input/output	Port 93: I/O port
		Output	Timer output 9: Output pin for timer 8
P94 / TIA / INT7	1	Input/output	Port 94: I/O port
		Input	Timer input A: Input pin for timer 9
		Input	Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge 
P95 / TIB / INT8	1	Input/output	Port 95: I/O port
		Input	Timer input B: Input pin for timer 9
		Input	Interrupt request pin 8: Rising edge interrupt request pin 
P96 / TOA / TOB	1	Input/output	Port 96: I/O port
		Output	Timer output A: Output pin for timer 9
		Output	Timer output B: Output pin for timer 9
PA0 to PA2	3	Input	Port A0 to A2: Input-only port
PA3	1	Input	Port A3: Input-only port
PA4 to PA7	4	Input	Port A4 to A7: Input-only port
NM $\bar{I}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both falling and rising edge 
CLK	1	Output	Clock output: Outputs external clock divided by 4. Pulled up during reset.
$\bar{E}A$	1	Input	External access: Connect to VCC.
AM8 / $\bar{16}$	1	Input	Address mode: External data bus width select pin Connect this pin to VCC. Data bus width at external access can be set by chip select/wait control register.
X1 / X2	2	Input/output	Oscillator connecting pin
VCC	5		Collector supply pin: Connect all VCC pins to power supply
VSS	5		GND pin: Connect all VSS pins to GND (0 V)

Note: Disconnect the pull-up resistors from pins other than  $\bar{R}ESET$  pin by software.

### 3. Electrical Characteristics

#### 3.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	$V_{CC}$	- 0.5 to + 6.5	V
Input Voltage	$V_{IN}$	- 0.5 to $V_{CC} + 0.5$	V
Output current (total)	$\Sigma I_{OL}$	+ 120	mA
Output current (total)	$\Sigma I_{OH}$	- 120	mA
Power Dissipation ( $T_a = +70^\circ\text{C}$ )	$P_D$	600	mW
Soldering Temperature (10 s)	$T_{SOLDER}$	+ 260	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	- 65 to + 150	$^\circ\text{C}$
Operating Temperature	$T_{OPR}$	- 20 to + 70	$^\circ\text{C}$

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

#### 3.2 DC Electrical Characteristics

- (1)  $V_{CC} = +5\text{ V} \pm 10\%$ ,  $T_a = -20$  to  $+70^\circ\text{C}$  ( $f_c = 8$  to  $25\text{ MHz}$ )

(Typical values are for  $T_a = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{ V}$ .)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15)	$V_{IL}$		- 0.3	0.8	V
Port 2 to A	$V_{IL1}$		- 0.3	$0.3 V_{CC}$	V
(except P56, P70, P72, P73, P75)					
RESET, NMI, INT0 to 4	$V_{IL2}$		- 0.3	$0.25 V_{CC}$	V
EA, AM8/16	$V_{IL3}$		- 0.3	0.3	V
X1	$V_{IL4}$		- 0.3	$0.2 V_{CC}$	V
Input High Voltage (D0 to 15)	$V_{IH}$		2.2	$V_{CC} + 0.3$	V
Port 2 to A	$V_{IH1}$		$0.7 V_{CC}$	$V_{CC} + 0.3$	V
(except P56, P70, P72, P73, P75)					
RESET, NMI, INT0 to 4	$V_{IH2}$		$0.75 V_{CC}$	$V_{CC} + 0.3$	V
EA, AM8/16	$V_{IH3}$		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
X1	$V_{IH4}$		$0.8 V_{CC}$	$V_{CC} + 0.3$	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 1.6\text{ mA}$		0.45	V
Output High Voltage	$V_{OH}$	$I_{OH} = -400\ \mu\text{A}$	2.4		V
	$V_{OH1}$	$I_{OH} = -100\ \mu\text{A}$	$0.75 V_{CC}$		V
	$V_{OH2}$	$I_{OH} = -20\ \mu\text{A}$	$0.9 V_{CC}$		V
Darlington Drive Current (8 Output Pins max.)	$I_{DAR}$	$V_{EXT} = 1.5\text{ V}$ $R_{EXT} = 1.1\text{ k}\Omega$	- 1.0	- 3.5	mA
Input Leakage Current	$I_{LI}$	$0.0 \leq V_{in} \leq V_{CC}$	0.02 (Typ)	$\pm 5$	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$0.2 \leq V_{in} \leq V_{CC} - 0.2$	0.05 (Typ)	$\pm 10$	$\mu\text{A}$
Operating Current (RUN)	$I_{CC}$	$f_c = 25\text{ MHz}$	40 (Typ)	50	mA
IDLE2			30 (Typ)	40	mA
IDLE1			3.5 (Typ)	10	mA
STOP ( $T_a = -20$ to $+70^\circ\text{C}$ )		$0.2 \leq V_{in} \leq V_{CC} - 0.2$	0.5 (Typ)	50	$\mu\text{A}$
STOP ( $T_a = 0$ to $+50^\circ\text{C}$ )		$0.2 \leq V_{in} \leq V_{CC} - 0.2$		10	$\mu\text{A}$
Power Down Voltage (@STOP, RAM Back up)	$V_{STOP}$	$V_{IL2} = 0.2 V_{CC}$ , $V_{IH2} = 0.8 V_{CC}$	2.0	6.0	V
Pull Up Resistance	$R_{RP}$		45	160	$\text{k}\Omega$
Pin Capacitance	$C_{IO}$	$f_c = 1\text{ MHz}$		10	pF
Schmitt Width	$V_{TH}$		0.4	1.0 (Typ)	V
RESET, NMI, INT0 to 4					

Note:  $I_{DAR}$  guarantees up to eight pins from any output port.

## 3.3 AC Electrical Characteristics

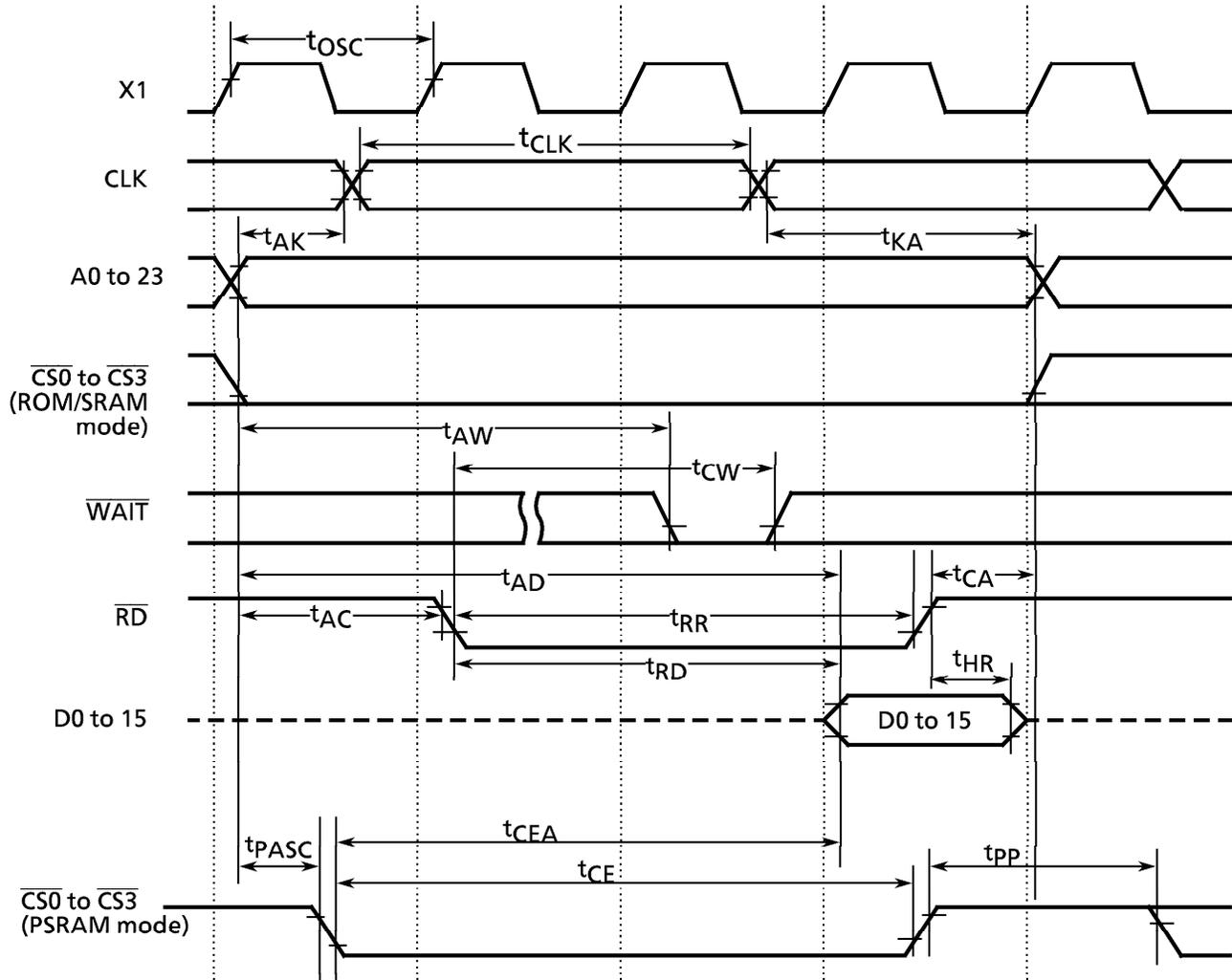
(1)  $V_{CC} = +5V \pm 10\%$ ,  $T_a = -20$  to  $+70^\circ\text{C}$ (f<sub>c</sub> = 8 MHz to 25 MHz)

No.	Parameter	Symbol	Formula		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation cycle (= x)	t <sub>OSC</sub>	40	125	50		40		ns
2	Clock pulse width	t <sub>CLK</sub>	2.0x – 40		60		40		ns
3	A0 to 23 valid → Clock hold	t <sub>AK</sub>	0.5x – 20		5		0		ns
4	Clock valid → A0 to 23 hold	t <sub>KA</sub>	1.5x – 60		15		0		ns
5	A0 to 23 valid → $\overline{\text{RD}}/\overline{\text{WR}}$ fall	t <sub>AC</sub>	1.0x – 20		30		20		ns
6	$\overline{\text{RD}}/\overline{\text{WR}}$ rise → A0 to 23 hold	t <sub>CA</sub>	0.5x – 20		5		0		ns
7	A0 to 23 valid → D0 to 15 input	t <sub>AD</sub>		3.5x – 40		135		100	ns
8	$\overline{\text{RD}}$ fall → D0 to 15 input	t <sub>RD</sub>		2.5x – 45		80		55	ns
9	$\overline{\text{RD}}$ low pulse width	t <sub>RR</sub>	2.5x – 40		85		60		ns
10	$\overline{\text{RD}}$ rise → D0 to 15 hold	t <sub>HR</sub>	0		0		0		ns
11	$\overline{\text{WR}}$ low pulse width	t <sub>WW</sub>	2.5x – 40		85		60		ns
12	D0 to 15 valid → $\overline{\text{WR}}$ rise	t <sub>DW</sub>	2.0x – 40		60		40		ns
13	$\overline{\text{WR}}$ rise → D0 to 15 hold	t <sub>WD</sub>	0.5x – 10		15		10		ns
14	A0 to 23 valid → $\overline{\text{WAIT}}$ input <sup>(1 WAIT + n mode)</sup>	t <sub>AW</sub>		3.5x – 90		85		50	ns
	A0 to 23 valid → $\overline{\text{WAIT}}$ input <sup>(0 + n WAIT mode)</sup>	t <sub>AW</sub>		1.5x – 40		35		20	ns
15	$\overline{\text{RD}}/\overline{\text{WR}}$ fall → $\overline{\text{WAIT}}$ hold <sup>(1 WAIT + n mode)</sup>	t <sub>CW</sub>	2.5x + 0		125		100		ns
	$\overline{\text{RD}}/\overline{\text{WR}}$ fall → $\overline{\text{WAIT}}$ hold <sup>(0 + n WAIT mode)</sup>	t <sub>CW</sub>	0.5x + 0		25		20		ns
16	$\overline{\text{WR}}$ rise → PORT valid	t <sub>CP</sub>		200		200		200	ns
17	$\overline{\text{CS}}$ Low pulse width (PSRAM mode)	t <sub>CE</sub>	3.0x – 40		110		80		ns
18	$\overline{\text{CS}}$ fall → D0 to 15 input (PSRAM mode)	t <sub>CEA</sub>		3.0x – 60		90		60	ns
19	Address setup time (PSRAM mode)	t <sub>PASC</sub>	0.5x – 15		10		5		ns
20	$\overline{\text{CS}}$ precharge time (PSRAM mode)	t <sub>PP</sub>	1.0x – 10		40		30		ns

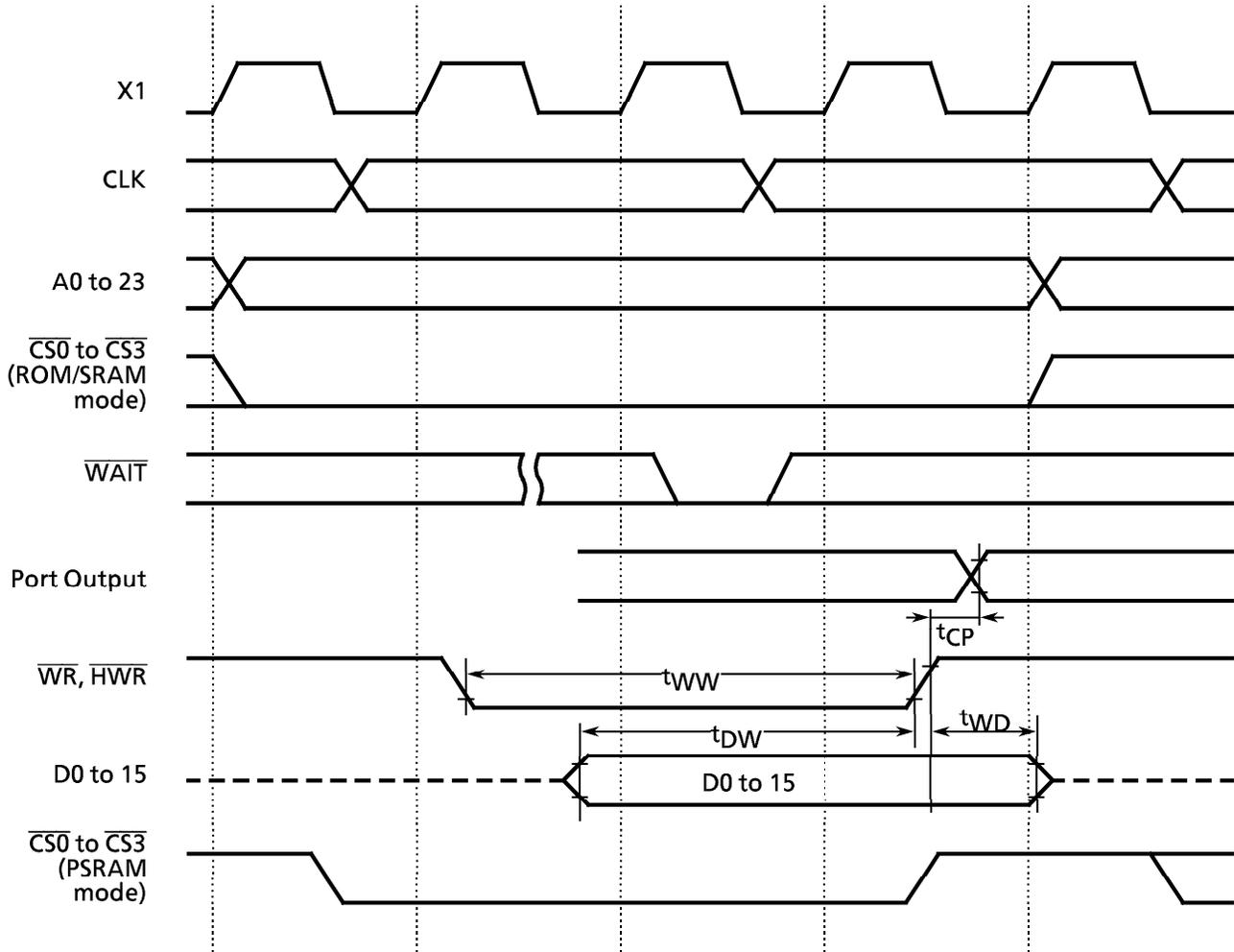
## AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
- Input level: High 2.4 V / Low 0.45 V (D0 to D15)  
High 0.8 V<sub>CC</sub> / Low 0.2 V<sub>CC</sub> (except for D0 to D15)

(2) Read Cycle



(3) Write Cycle



3.4 Serial Channel Timing

(1) I/O interface mode

① SCLK input mode

Vcc = +5 V ± 10%, Ta = -20 to +70°C (fc = 8 to 25 MHz)

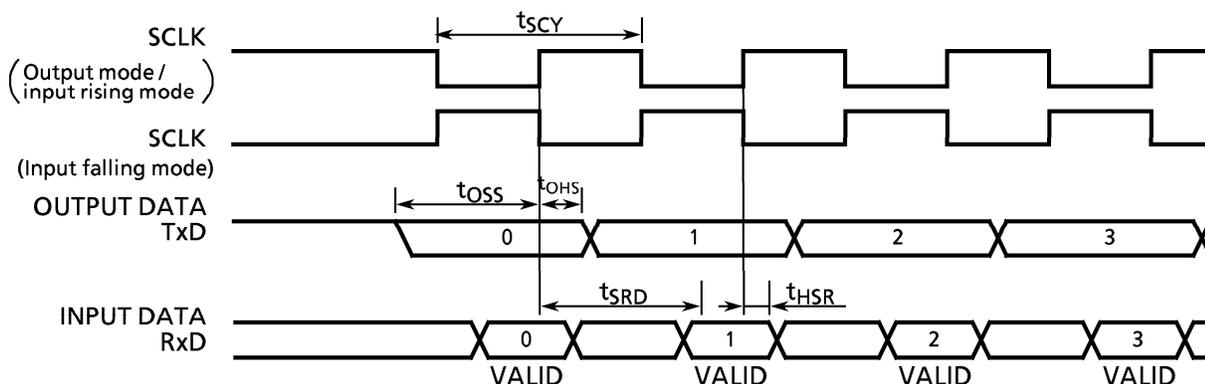
Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t <sub>SCY</sub>	16x		1.6		0.64		μs
Output Data → SCLK rise/fall*	t <sub>OSS</sub>	t <sub>SCY</sub> /2 - 5x - 50		250		70		ns
SCLK rise/fall* → Output Data hold	t <sub>OHS</sub>	5x - 100		400		100		ns
SCLK rise/fall* → input data hold	t <sub>HSR</sub>	0		0		0		ns
SCLK rise/fall* → valid data input	t <sub>SRD</sub>		t <sub>SCY</sub> - 5x - 100		1000		340	ns

\* ) SCLK rise/fall: In SCLK rising edge mode, SCLK rising edge timing; in SCLK falling edge mode, SCLK falling edge timing

② SCLK output mode

Vcc = +5 V ± 10%, Ta = -20 to +70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t <sub>SCY</sub>	16x	8192x	1.6	819.2	0.64	327.6	μs
Output Data → SCLK rising edge	t <sub>OSS</sub>	t <sub>SCY</sub> - 2x - 150		1250		410		ns
SCLK rising edge → Output Data hold	t <sub>OHS</sub>	2x - 80		120		0		ns
SCLK rising edge → Input Data hold	t <sub>HSR</sub>	0		0		0		ns
SCLK rising edge → valid data input	t <sub>SRD</sub>		t <sub>SCY</sub> - 2x - 150		1250		410	ns



(2) UART Mode (SCLK1 External Input)

Vcc = +5 V ± 10%, Ta = -20 to +70°C (fc = 8 to 25 MHz)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t <sub>SCY</sub>	4x + 20		420		180		ns
Low-level SCLK pulse width	t <sub>SCYL</sub>	2x + 5		205		85		ns
High-level SCLK pulse width	t <sub>SCYH</sub>	2x + 5		205		85		ns

### 3.5 Event Counter (External Input Clocks: TI0, TI4, TI8, TI9, TIA, TIB)

$V_{CC} = +5V \pm 10\%$ ,  $T_a = -20$  to  $+70^\circ\text{C}$  ( $f_c = 8$  to  $25$  MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
External input clock cycle	$t_{VCK}$	$8x + 100$		900		420		ns
External low-level input clock pulse width	$t_{VCKL}$	$4x + 40$		440		200		ns
External high-level input clock pulse width	$t_{VCKH}$	$4x + 40$		440		200		ns

### 3.6 Interrupt Operation

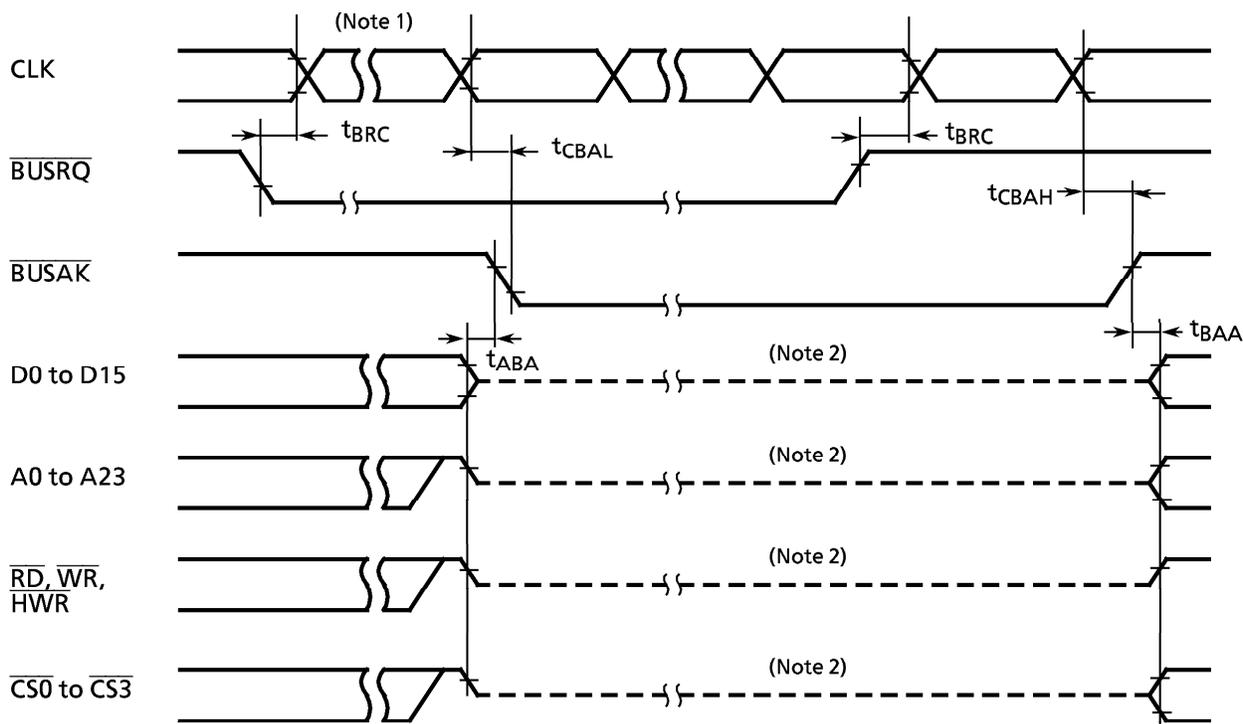
$V_{CC} = +5V \pm 10\%$ ,  $T_a = -20$  to  $+70^\circ\text{C}$  ( $f_c = 8$  to  $25$  MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$ , INT0 to 4 low-level pulse width	$t_{INTAL}$	$4x$		400		160		ns
$\overline{NMI}$ , INT0 to 4 high-level pulse width	$t_{INTAH}$	$4x$		400		160		ns
INT5 to INT8 low-level pulse width	$t_{INTBL}$	$8x + 100$		900		420		ns
INT5 to INT8 high-level pulse width	$t_{INTBH}$	$8x + 100$		900		420		ns

3.7 Bus Request/Bus Acknowledge Timing

V<sub>CC</sub> = +5 V ± 10%, T<sub>a</sub> = -20 to +70°C (f<sub>c</sub> = 8 to 25 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
BUSRQ setup time for CLK	t <sub>BRC</sub>	120		120		120		ns
CLK → BUSAK fall	t <sub>CBAL</sub>		2.0x + 120		320		200	ns
CLK → BUSAK rise	t <sub>CBAH</sub>		0.5x + 40		90		60	ns
Time from output buffer off until BUSAK falling edge	t <sub>ABA</sub>	0	80	0	80	0	80	ns
Time from BUSAK rising edge until output buffer on	t <sub>BAA</sub>	0	80	0	80	0	80	ns



Note 1: When  $\overline{\text{BUSRQ}}$  goes to low level to request bus release, if the current bus cycle is yet complete due to a wait, the bus is not released until the wait completes.

Note 2: The dotted line indicates only that the output buffer is off, not that the signal is at middle level. Immediately after bus release, the signal level prior to the bus release is held dynamically by the external load capacitance. Therefore, designs should allow for the fact that when using an external resistor or similar to fix the signal level while the bus is released, after bus release a delay occurs before the signal goes to its fixed level (due to the CR time constant). The internal programmable pull-up resistor continues to function in accordance with the internal signal level.