TOSHIBA

TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870/X Series

TMP88PU77FG

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP88PU77F	P-QFP100-1420-0.65A	TMP88PU77FG	QFP100-P-1420-0.65A	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

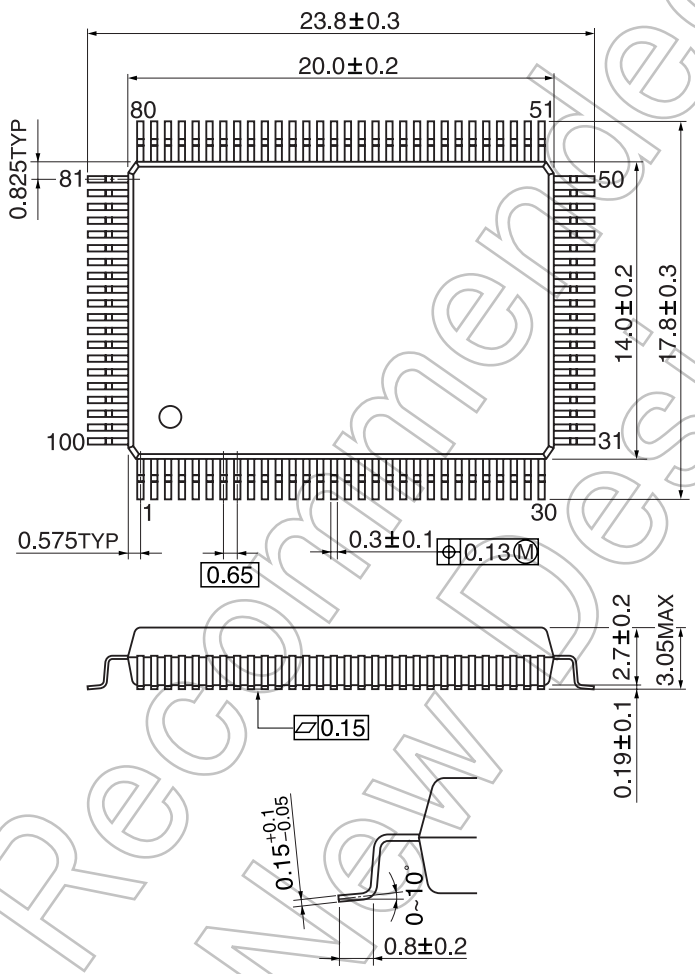
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

QFP100-P-1420-0.65A

Unit: mm



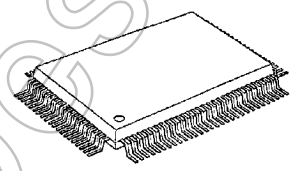
CMOS 8-Bit Microcontroller

TMP88PU77F

The 88PU77 are the high-speed and high performance 8-bit single chip microcomputers which built in a program storage area (96 Kbyte) and the One-Time PROM of bector table storage area (256 byte). The 88PU77 is pin compatible with the 88CP77/S77/U77. The operations possible with the 88PU77 can be performed by writing programs to PROM. The 88PU77 can write and verify in the same way as the TC571000 an EPROM programmer.

PART No.	OTP	RAM	PACKAGE	ADAPTOR SOCKET
TMP88PU77F	96 Kbyte + 256 byte	3 Kbyte	P-QFP100-1420-0.65A	BM11150

P-QFP100-1420-0.65A



TMP88CP77F
TMP88CS77F
TMP88CU77F
TMP88PU77F

070122EBP

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  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc. 021023_A
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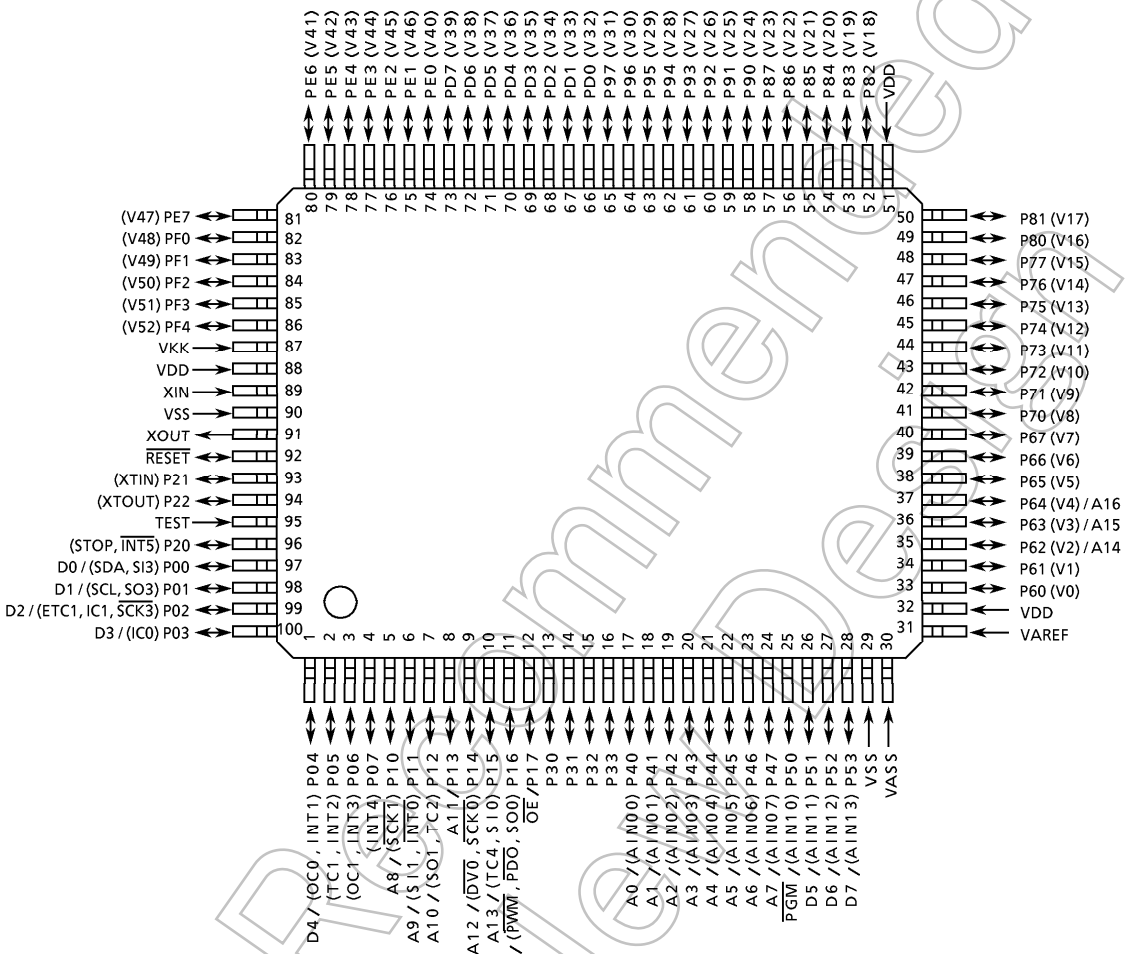
Pin Assignments (Top View)

P-QFP100-1420-0.65A



Note: All VDDs should be connected externally for keeping the same voltage level.

Pin Function

The 88PU77 has two modes: MCU and PROM.

(1) MCU mode
In this mode, the 88PU77 is pin compatible with the 88CP77/S77/U77 (fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16	Input	PROM address inputs	P64
A15 to A8			P63, P62, P15 to P10
A7 to A0			P47 to P40
D7 to D0	I/O	PROM data input/outputs	P53 to P51, P04 to P00
$\overline{CE}$	Input	Chip enable signal input (active low)	P16
$\overline{OE}$		Output enable signal input (active low)	P17
$\overline{PGM}$		Program mode single input	P50
VPP	Power supply	+ 12.75 V / 5 V (Program supply voltage)	TEST
VCC		+ 6.25 V / 5 V	VDD
GND		0 V	VSS
P07 to P05	Input	Pull-up with resistance for input processing	
P33 to P30			
P60		PROM mode setting pin. Be fixed at high level.	
P21			
P67, P66, P61		PROM mode setting pin. Be fixed at low level.	
PF4 to PF0, PE7 to PE0			
$\overline{RESET}$			
P65	Output	Open	
P77 to P70			
P87 to P80			
P97 to P90			
PD7 to PD0			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
VAREF	Power supply	0 V (GND)	
VASS			
VKK		Open	

Operational Description

The configuration and functions of the 88PU77 are the same as those of the 88CP77/S77/U77, except in that a one-time PROM is used instead of an on-chip mask ROM.

1. Operating Mode

The 88PU77 has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST / VPP pin at low level.
In the MCU mode, operation is the same as with the 88CP77/S77/U77 (the TEST / VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program memory

The 88PU77 has a 96 Kbyte (addresses 04000_H to $1BFFF_H$ in the MCU mode, addresses 00000_H to $17FFF_H$ in the PROM mode) of program storage area and 256 byte (addresses FFF00 to $FFFFF_H$ in the MCU mode, addresses 1FF00 to $1FFFF_H$ in the PROM mode) one-time PROM of vector table storage area.

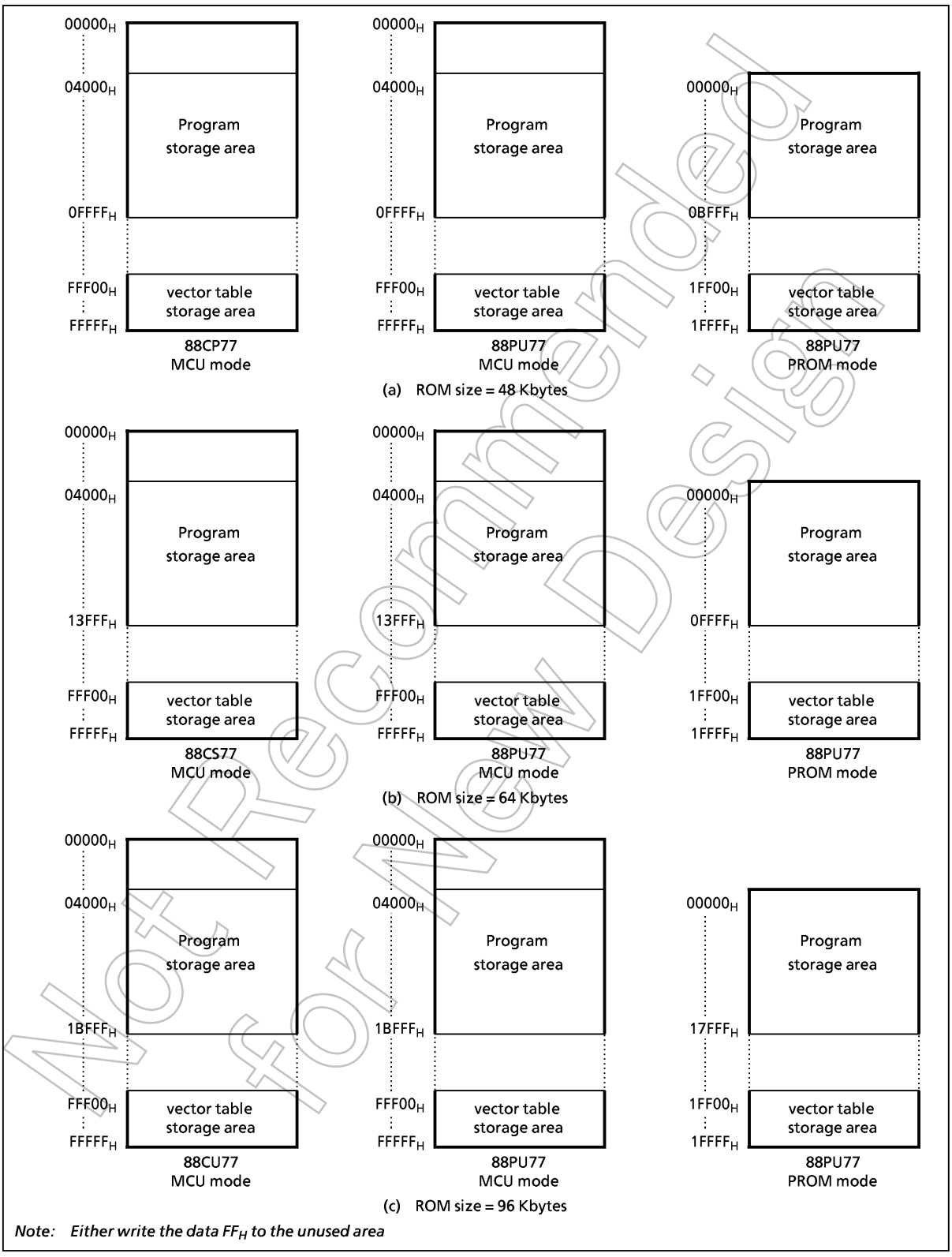


Figure 1-1. Program Storage Area

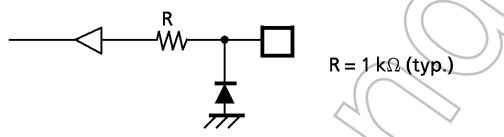
1.1.2 Data memory

The 88PU77 has an on-chip 3 Kbyte data memory (static RAM).

1.1.3 Input/output circuitry

(1) Control pins

The control pins of the 88PU77 are the same as those of the 88CP77/S77/U77 except that the TEST pin has is no built-in pull-down resistance.



Note: TEST pin has no built-in pull-down resistance

Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of 88PU77 I/O ports are the same as the code A type I/O circuitries of the 88CP77/S77/U77.

1.2 PROM Mode

The PROM mode is activated by setting shown in Figure 1-2. The PROM mode is used to write and verify programs with a general-purpose PROM programmer. The high-speed programming mode can be used for program operation.

The 88PU77 is not supported an electric signature mode, so the ROM type must be set to TC571000.

Set the adaptor socket switch to "N".

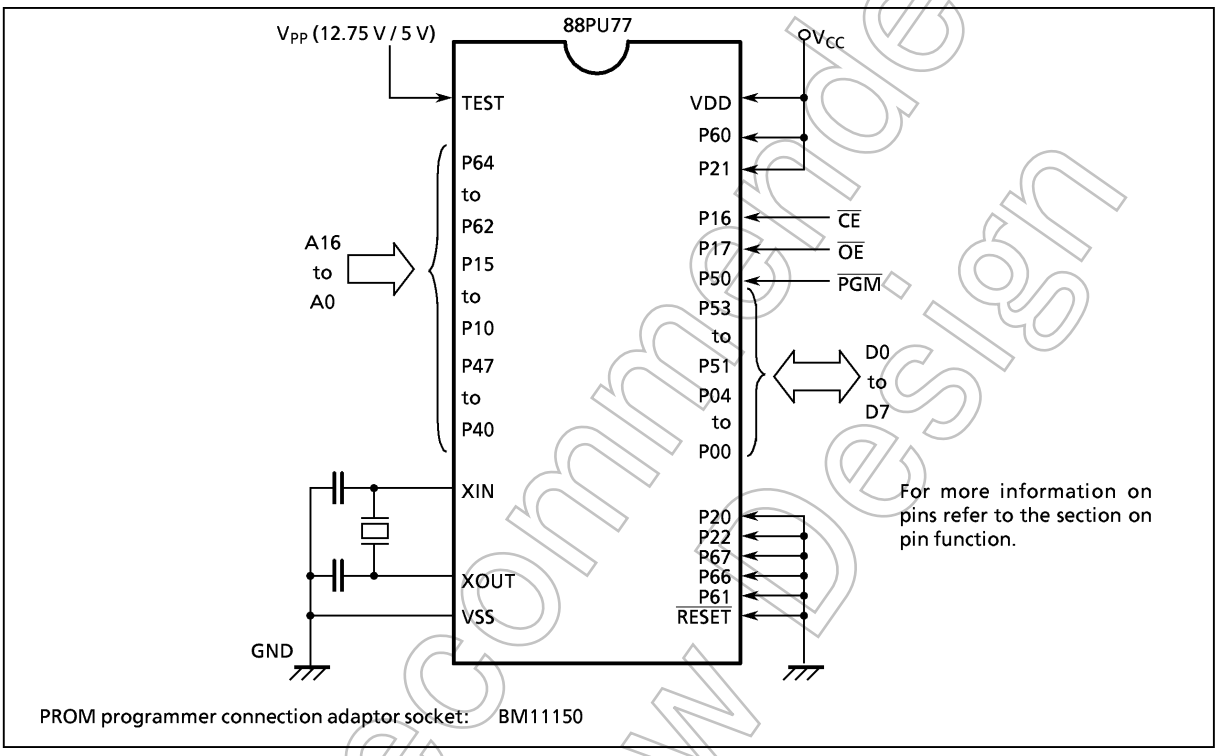


Figure 1-3. Setting for PROM Mode

1.2.1 Programming flowchart (High-speed programming)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{CE}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

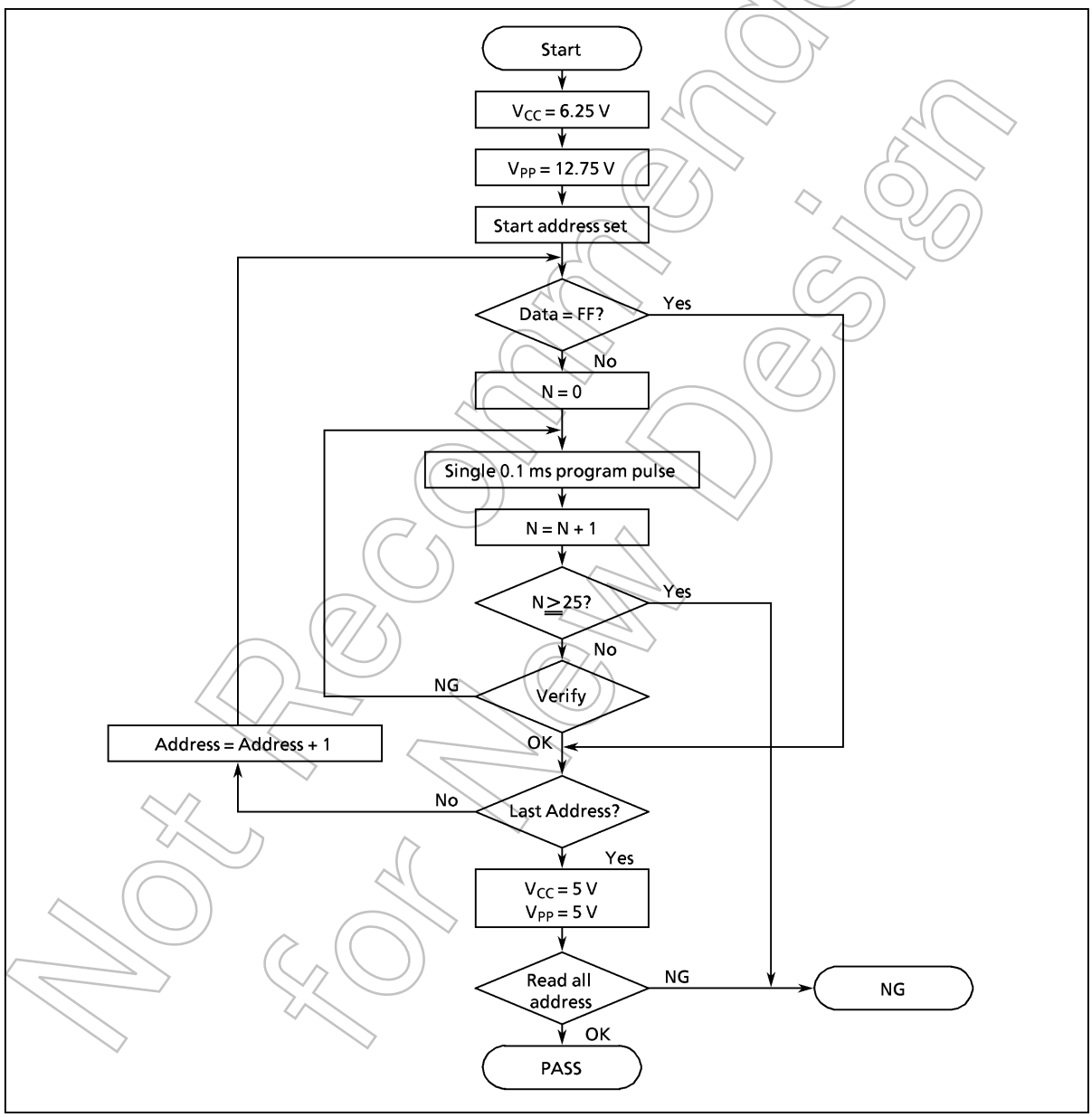


Figure 1-4. Flowchart of High-speed Programming

1.2.2 Writing method for general-purpose PROM program

(1) Adapters
BM11150

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying

i) PROM type is specified to TC571000.
Writing voltage: 12.75 V (high-speed program)

ii) Data transfer (copy) (Note 1)
In TMP88PU77, EPROM is within the addresses 00000_H to $17FFF_H$ and $1FF00_H$ to $1FFFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in Figure 1-1.

Ex. In the block transfer (copy) mode, executed as below.
Program area: transferred addresses 04000_H to $1BFFF_H$ to addresses 00000 to $17FFF_H$
Vector area: transferred addresses $FFF00_H$ to $FFFFF_H$ to 1FF00 to $1FFFF_H$

iii) Writing address is specified. (Note 1)
Start address: 00000_H
End address: $1FFFF_H$

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1: The specifying method is referred to the PROM programmer description. Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.

Note 3: The TMP88PU77 does not support the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12 V ± 0.5 V to the address pin 9 (A9). The signature must not be used.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage (* Note 3)	V_{DD}		– 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST/VPP	– 0.3 to 13.0	V
Input Voltage	V_{IN1}	P1, P2, P3, P4, P5, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{IN2}	P0 port	– 0.3 to 5.5 V	
Output Voltage	V_{OUT1}	P1, P2, P3, P4, P5, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P0 port	– 0.3 to 5.5 V	
	V_{OUT3}	Source open drain ports	V_{DD} – 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P3, P4, P5 ports	3.2	mA
	I_{OUT2}	P6, P7, P80, 81 Ports	– 25	
	I_{OUT3}	P82 to P87, P9, PD, PE, PF ports	– 12	
Output Current (Total)	ΣI_{OUT1}	P1, P3, P4, P5 ports	– 40	mA
	ΣI_{OUT2}	P0, P1, P2, P3, P4, P5 ports	60	
	ΣI_{OUT3}	P6, P7, P8, P9, PD, PE, PF ports	– 120	
Power Dissipation [Topr = 25°C]	PD	note	1200	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.
Note 2: Power Dissipation (PD) ; For PD, it is necessary to decrease -14.3 mW/°C. (Refernce to TMP88CP77/S77/U77)
Note 3: All VDDs should be connected externally for keeping the same voltage level.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min	Max	UNIT
Supply Voltage	V_{DD}		fc = 12.5 MHz	NORMAL1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 V to 5.5 V		1.0	12.5	MHz
	fs	XTIN, XTOUT	V_{DD} = 2.7 V to 5.5 V		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min	Typ.	Max	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
	I_{IN4}	PD, PE, PF ports (Note3)		–	–	80	
Input Resistance	R_{IN3}	$\overline{RESET}$		100	220	450	kΩ
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5 V, V_{KK} = – 30 V	50	80	110	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = – 32 V	–	–	– 2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V	–	–	2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output High current	I_{OH1}	P6, P7, P80, P81 port	V_{DD} = 4.5 V, V_{OH} = 2.4 V	–	– 30	–	mA
	I_{OH2}	P82 to P87, P9, PD, PE, PF ports		–	– 15	–	
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 12.5 MHz fs = 32.768 kHz	–	15	22	mA
modesSupply Current in IDLE 1, 2 modes				–	6	12	
Supply Current in SLOW mode			V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5 V.

Note 2: Input Current I_{IN1},I_{IN3} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Input Current I_{IN4} ; The current when the pull-down register (Rk) is not connected by the mask option.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min	Typ.	Max	UNIT
Analog Reference Voltage	V_{AREF}		4.5	–	V_{DD}	V
	V_{ASS}		V_{SS}			
Analog Reference Voltage Range	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Input Voltage	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Quantizing error is not contained in those errors.

A.C. Characteristics

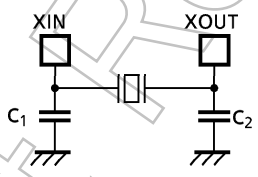
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min	Typ.	Max	UNIT
Machine Cycle Time	tcy	In NORMAL1, 2 modes	0.32	–	10	μs
		In IDLE1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 12.5 MHz	32	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	15.2	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

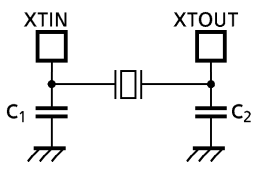
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	12.5 MHz	Murata	CSA12.5MTZ	30 pF	30 pF
		8 MHz	Murata	CSA8.00MTZ	30 pF	30 pF
	Crystal Oscillator	12.5 MHz	NDK	AT-51	10 pF	10 pF
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

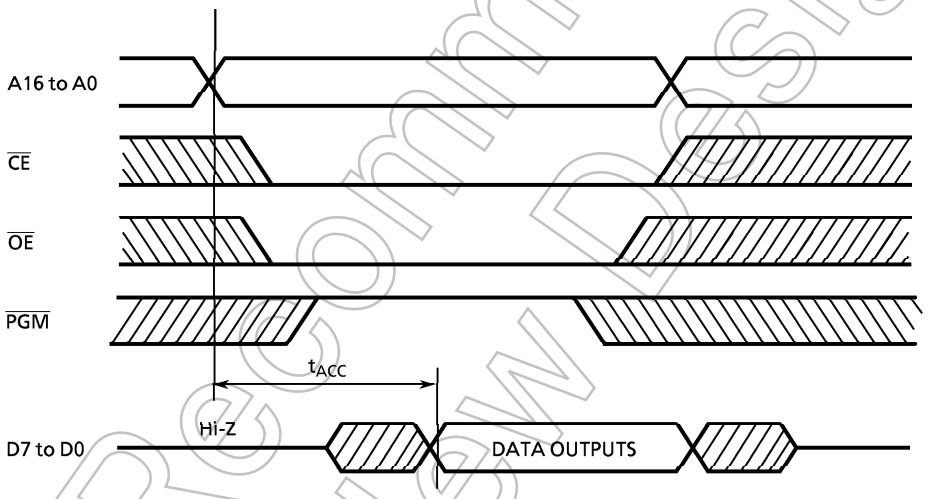
Note: An electrical shield by metal shied plate on the IC package should be recommend able in order to prevent the device from the high electric fieldstress applied for continuous reliable operation.

D.C./A.C. Characteristics (PROM mode) (V_{SS} = 0 V)

(1) Read Operation (VDD = 5.0 ± 0.25 V, Topr = 25 ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	Min	Typ.	Max	UNIT
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH4}		VDD × 0.7	–	VDD	V
Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL4}		0	–	0.8	V
Program Power Supply Voltage	V_{PP}		4.75	5.0	5.25	V
Address Access Time	t_{ACC}		–	1.5tcyc + 300	–	ns

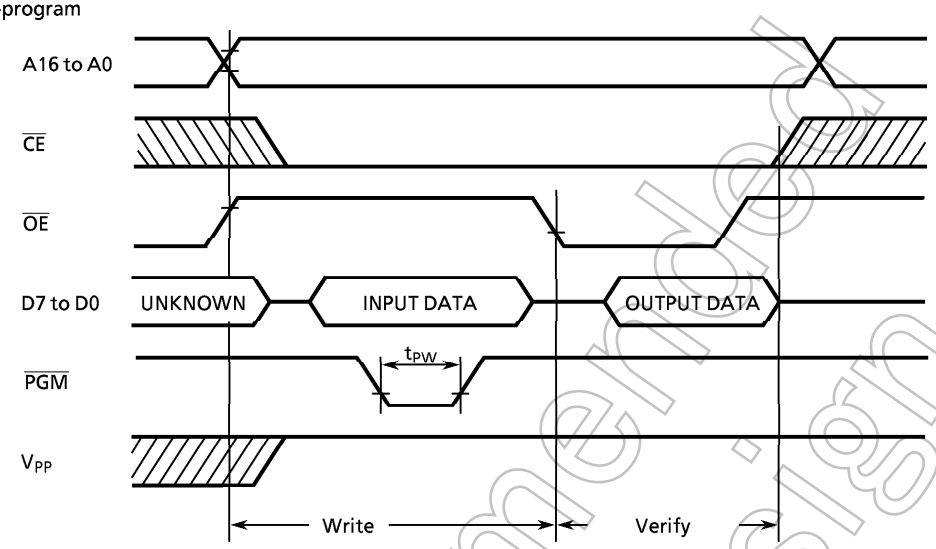
Note: tcyc = 500 ns at 8 MHz



(2) High-Speed Programming Operation (Topr = 25 ± 5°C, VDD = 6.25 ± 0.25 V)

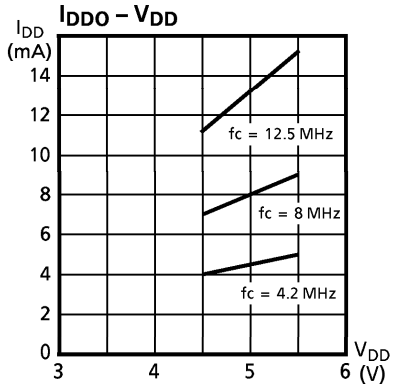
PARAMETER	SYMBOL	CONDITIONS	Min	Typ.	Max	UNIT
Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH4}		VDD × 0.7	–	VDD	V
Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL4}		0	–	0.8	V
Program Power Supply Voltage	V_{PP}		12.5	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{DD} = 6.0 V	0.095	0.1	0.105	ms

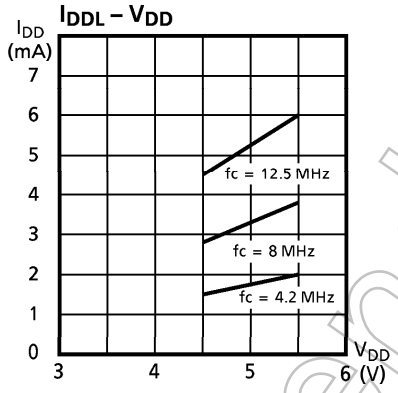
High-program

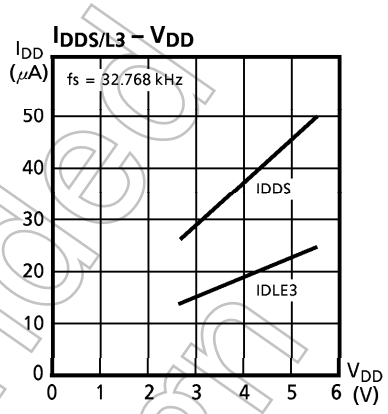


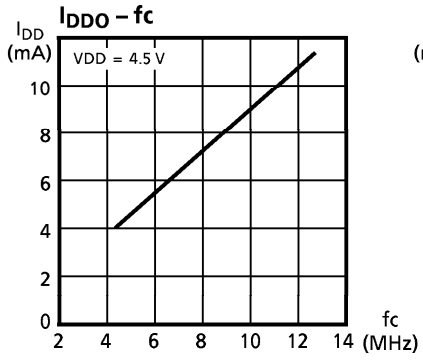
Note1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.
Note2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V ± 0.5 V) to the V_{pp} pin as the device is damaged.
Note3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

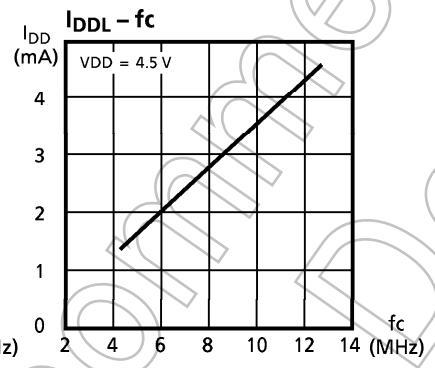
Typical Characteristics (Ta = 25°C)

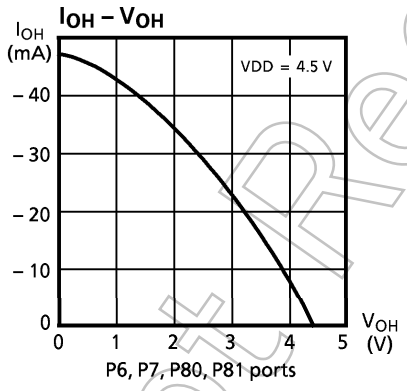




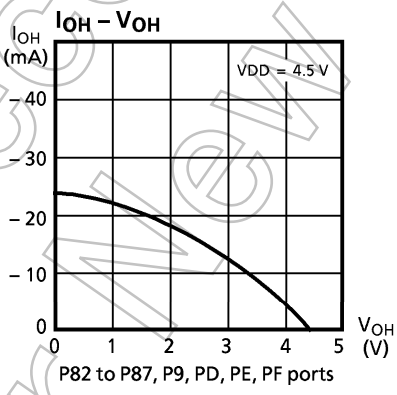




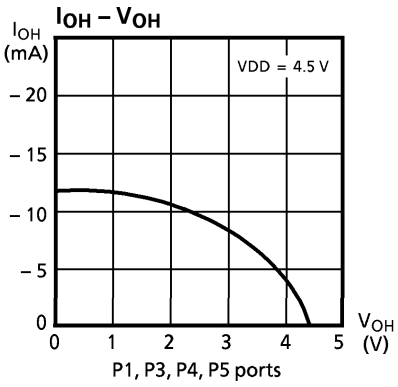




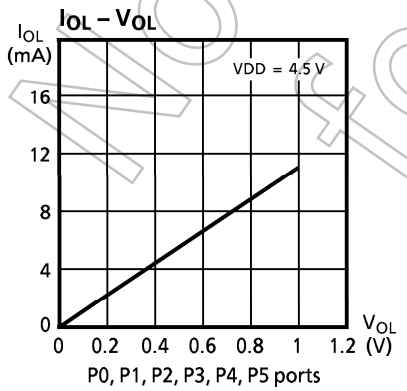
P6, P7, P80, P81 ports



P82 to P87, P9, PD, PE, PF ports



P1, P3, P4, P5 ports



P0, P1, P2, P3, P4, P5 ports

P-QFP100-1420-0.65A

Unit: mm