CMOS 8-Bit Microcontroller

TMP87PH48U/DF, TMP87PM48U/DF

The TMP87PH48 is a one-time PROM microcontroller with low-power 128 Kbits (16 Kbytes) electrically programmable read only memory for the TMP87CH48 system evaluation. The TMP87PM48 is a One-time PROM microcontroller with low-power 256 Kbits (32 Kbytes) electrically programmable read only memory for the TMP87CM48 system evaluation. The TMP87PH48/PM48 are pin compatible with the TMP87CH48/CM48. The operations possible with the TMP87CH48/CM48 can be performed by writing programs to PROM. The TMP87PH48/PM48 can write and verify in the same way as the TC57256AD using an adaptor sockets BM11117/BM11147 and an EPROM programmer.

Product No.	ROM	RAM	Package	Adapter Socket
TMP87PH48U	16 K × 8 bits	512 × 8 bits	P-LQFP64-1010-0.50	BM11117
TMP87PH48DF	IOKXODIG	312 X 6 DILS	P-QFP64-1414-0.80A	BM11147
TMP87PM48U	32 K × 8 bits	1 K × 8 bits	P-LQFP64-1010-0.50	BM11117
TMP87PM48DF	32 K X 8 DITS	I K X 8 DITS	P-QFP64-1414-0.80A	BM11147



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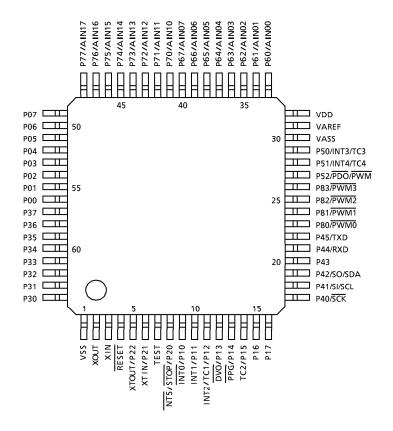
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87PH48-1 2003-07-09

Pin Assignments (Top View)

P-LQFP64-1010-0.50 P-QFP64-1414-0.80A



Pin Function

The TMP87PH48/PM48 have two modes: MCU and PROM.

(1) MCU mode

In this mode, the TMP87PH48/PM48 are pin compatible with the TMP87CH48/CM48 (Fix the TEST pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)			
A14 to A8			P76 to P70			
A7 to A0	Input	PROM address inputs	P81, P80, P45 to P40			
D7 to D0	1/0	PROM data input/outputs	P07 to P00			
CE		Chip enable signal input (active low)	P13			
ŌĒ	Input	Output enable signal input (active low)	P14			
VPP		+ 12.5 V/5 V (Program supply voltage)	TEST			
vcc	Power supply	+5V	VDD			
GND		0 V	VSS			
P37 to P34		Open				
P32 to P30		Pull-up with resistance R1 for input processing				
P52 to P50	1/0					
P83, P82		Pull-up with resistance K1 for input processing				
P67 to P60						
P11, P12, P15						
P21		PROM mode setting pins. Be fixed at high level.	(Pull-up with resistance R2)			
P77						
P17, P16, P10	I/O					
P133		PROM mode setting pins. Be fixed at low level.				
P22, P20		r now mode setting pins. Be fixed at low level.				
RESET						
XIN	Input	Connect an 8 MHz oscillator to stabilize the inter	anal state			
XOUT	Output	Connect an o Minz oscillator to stabilize the Inter	nai sidle.			
VAREF	Dayyon Cumple	OVICND				
VASS	Power Supply	0 V (GND)				

Operational Description

The following explains the TMP87PH48/PM48 hardware configuration and operation. The configuration and functions of the TMP87PH48/PM48 are the same as those of the TMP87CH48/CM48, except in that a one-time PROM is used instead of an on-chip mask ROM.

The TMP87PH48/PM48 are placed in the *single-clock* mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. Operating Mode

The TMP87PH48/PM48 have two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.

In the MCU mode, operation is the same as with the TMP87CH48/CM48 (The TEST/VPP pin cannot be used open because TMP87PH48/PM48 have no built-in pull-down resistance).

1.1.1 Program Memory

The TMP87PH48/PM48 have a $16K \times 8$ -bit (Addresses $C000_H$ to FFFF_H in the MCU mode, addresses 4000_H to 7FFF_H in the PROM mode) the TMP87PM48 has a $32K \times 8$ bit (Address 8000_H to FFFF_H in the MCU mode, addresses 0000_H to 7FFF_H in the PROM mode) of program memory (OTP).

To use the TMP87PH48/PM48 as the system evaluation for the TMP87CH48/CM48, the program should be written to the program memory area as shown in Figure 1-1.

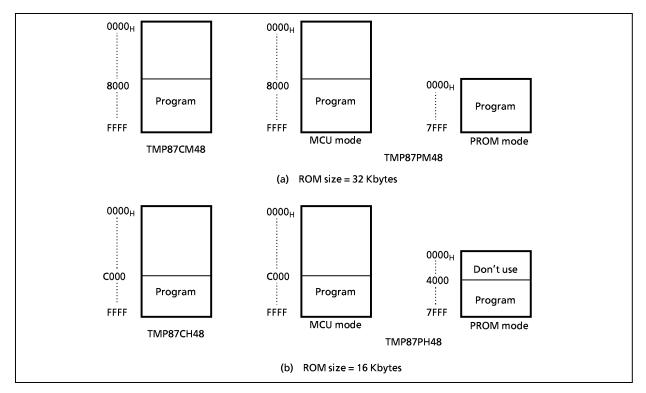


Figure 1-1. Program Memory Area

Note: Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.

1.1.2 Data Memory

The TMP87PH48 have an on-chip 512 \times 8-bit data memory (Static RAM). The TMP87PM48 have an on-chip 1K \times 8-bit data memory (Static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP87PH48/PM48 are the same as those of the TMP87CH48/CM48 except that the TEST pin has no built-in pull-down resistance.

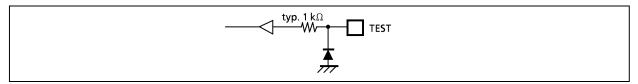


Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of TMP87PH48/PM48 I/O ports are the same as the TMP87CH48/CM48.

1.2 PROM Mode

The PROM mode is activated by setting the TEST, RESET pin and the ports P17 to P10, P22 to P20 and P77 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

The high-speed programming mode can be used for program operation.

The TMP87PH48/PM48 are not supported an *electric signature* mode, so the ROM type must be set to TC57256AD AD.

Set the adaptor socket switch to "N".

Note: Please set the high-speed programming mode according to each manual of PROM programmer.

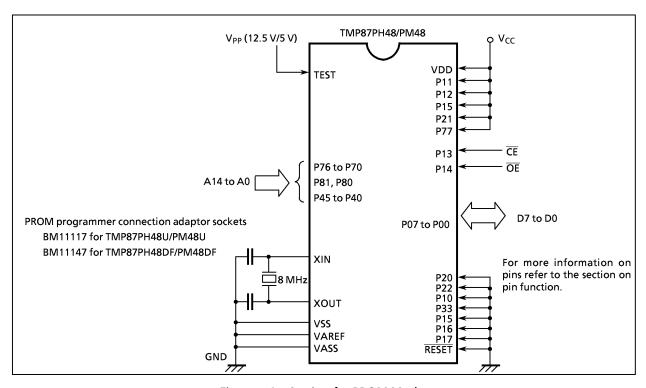


Figure 1-3. Setting for PROM Mode

1.2.1 Programming Flowchart (High-speed programming mode-I)

The high-speed programming mode is achieved by applying the program voltage (\pm 12.5 V) to the Vpp pin when Vcc = 6 V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the \overline{CE} input. The programmed data is verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (Up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (Number of programmed times \times 1 ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

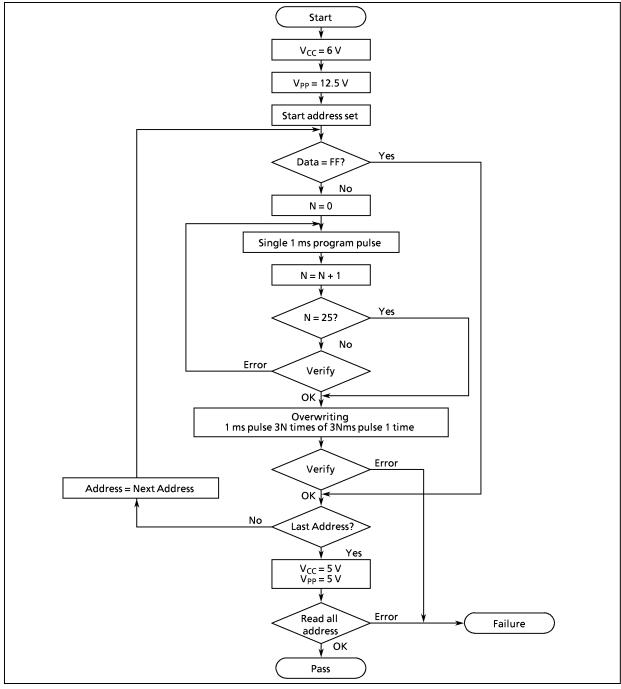


Figure 1-4. Flowchart of High-speed Programming Mode - I

1.2.2 Programming Flowchart (High-speed programming mode-II)

The high-speed programming mode is achieved by applying the program voltage (\pm 12.75 V) to the Vpp pin when Vcc = 6.25 V. After the address and input data are stable, the data is programmed by applying a single 0.1ms program pulse to the $\overline{\text{CE}}$ input. The programmed data is verified. If incorrect, another 0.1ms program pulse is applied and then the programmed data is verified. This process should be repeated (Up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

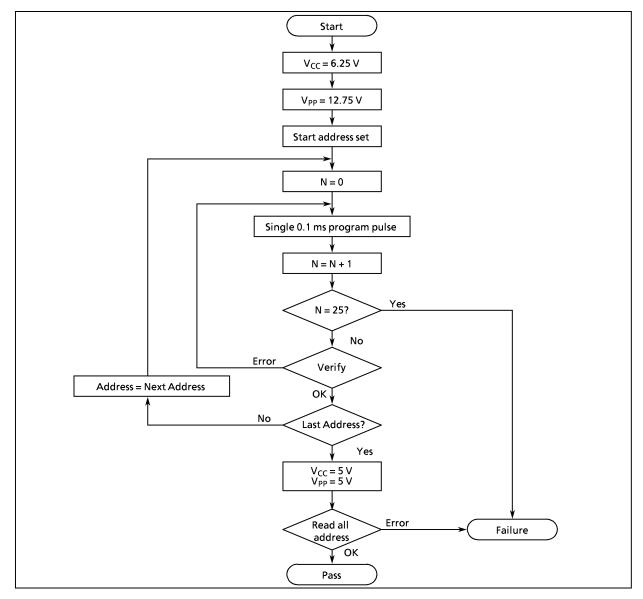


Figure 1-5. Flowchart of High-speed Programming Mode - II

1.2.3 Writing Method for General-purpose PROM Program

(1) Adapters

BM11117: TMP87PH48U, TMP87PM48U BM11147: TMP87PH48DF, TMP87PM48DF

(2) Adapter setting

Switch (SW1) is set to side N.

- (3) PROM programmer specifying
 - i) PROM type is specified to TC57256AD.

Writing voltage: 12.5 V (High-speed program I mode)

12.75 V (High-speed program II mode)

ii) Data transfer (Copy) (Note 1)

In TMP87PH48, EPROM is within the addresses 4000 to 7FFFH. In TMP87PM48, EPROM is within the addresses 0000 to FFFH. Data is required to be transferred (Copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in figure 1-1.

Ex. In the block transfer (Copy) mode, executed as below.

ROM capacity of 16KB: transferred addresses C000 to FFFFH to addresses 4000 to 7FFFH

iii) Writing address is specified (Note 1)

(4) Writing

Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

- Note 1: The specifying method is referred to the PROM programmer description. The data in addresses 0000 to 3FFFH must be specified to FFH.
- Note 2: When MCU is set to an adapter or the adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reversed, MCU, the adapter and PROM program is damaged.
- Note 3: TMP87PH48, TMP87PM48 don't support the electric signature mode (Hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying $12V \pm 0.5V$ to the address pin 9 (A9). The signature must not be used.

Input/Output Circuitry

(1) Control pins
The input/output circuitries of the TMP87PH48/PM48 control pins are shown below.

Control Pin	I/O	Input/Output Circuitry	Remarks
XIN XOUT	Input Output	Osc. enable fc VDD O Rf RO NOUT	Resonator connecting pins (high-frequency) $R_f = 1.2 \ M\Omega \ (typ.)$ $R_O = 1.5 \ k\Omega \ (typ.)$
XTIN XTOUT	Input Output	Osc. enable XTEN Fs VDD Rf SW XTIN XTOUT RO Initial "High-Z"	$ \begin{array}{lll} \text{XTIN, XTOUT} \\ \text{Resonator connecting pins} \\ & \text{(low-frequency)} \\ \text{R}_f &= 6 \text{ M}\Omega \text{ (typ.)} \\ \text{R}_O &= 220 \text{ k}\Omega \text{ (typ.)} \\ \\ \text{XTEN (Initial: 0)} \\ \text{SW (XTEN = 0: OFF)} \\ & \text{(XTEN = 1: ON)} \\ \end{array} $
P21 P22	1/O 1/O	P21 Output P22 R P22 R P22 Input	P21, P22 Sink open drain output Hysteresis input $R = 1 \ k\Omega \ (typ.)$
RESET	1/0	Address-trap-reset Watchdog-timer-reset System-clock-reset	Sink open drain output Hysteresis input $Pull-up \ resistor \\ R_{IN} = 220 \ k\Omega \ (typ.)$ $R = 1 \ k\Omega \ (typ.)$
STOP/INT5 (P20)	I/O	P20 Output R (P20) STOP/INT5	Hysteresis input $R = 1 \text{ k}\Omega \text{ (typ.)}$
TEST	Input	Input R D1	R = 1 kΩ (typ.)

Note 1: The TMP87PH48/PM48 don't have a pull-down resistor (R_{IN}) and a diode (D_1) for TEST pin.

Note 2: The TMP87PH48/PM48/CH48/CM48 are placed in the single-clock mode during reset.

(2) Input/Output Ports

The input/output circuitries of the TMP87PH48/PM48 input/output ports are shown below.

Port	1/0	Input/Output Circuitry	Remarks
P0 P6 P7 P8	1/0	Output Initial "High-Z" Disable Input	Tri-state I/O $R=1~k\Omega~(typ.)$
P1	1/0	Output Initial "High-Z" Disable R	Tri-state I/O Hysteresis input $R = 1 \text{ k}\Omega$ (typ.)
P3	1/0	Output R	Hligh current output only P3 Sink open drain output $R=1\ k\Omega\ (typ.)$
P4 P5	I/O	Output R Input	Sink open drain output $Hysteresis\ input \\ R=1\ k\Omega\ (typ.)$

Electrical Characteristics

(1) TMP87PH48

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		- 0.3 to 6.5	٧
Input voltage	V_{IN}		- 0.3 to V _{DD} + 0.3	V
Output voltage	V _{OUT}		- 0.3 to V _{DD} + 0.3	V
Output suggest (Day 1 min)	I _{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2	4
Output current (Per 1 pin)	I _{OUT2}	Port P3	30	mA
O to the west (Tetal)	Σ l _{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	120	
Output current (Total)	Σ I _{OUT2}	Port P3	120	mA
Power dissipation	PD		350	mW
Soldering temperature (Time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		– 55 to 125	°C
Operating temperature	Topr		- 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins		Conditions	Min	Max	Unit
			fc = 8 MHz	NORMAL1/2 modes IDLE1/2 modes	4.5		
			fc =	NORMAL1/2 modes			
Supply voltage	V_{DD}		4.2 MHz	IDLE1/2 modes	2.7	5.5	V
			fs =	SLOW mode	2.,		
			32.768 kHz	SLEEP mode			
				STOP mode	2.0		
	V _{IH1}	Except hysteresis input] ,	. > 4.5.4	$V_{DD} \times 0.70$		
Input high voltage	V _{IH2}	Hysteresis input	$V_{DD} \ge 4.5 V$		$V_{DD} \times 0.75$	V_{DD}	V
	V _{IH3}		\	/ _{DD} < 4.5 V	$V_{DD} \times 0.90$		
	V _{IL1}	Except hysteresis input		/ _{DD} ≧ 4.5 V		$V_{DD} \times 0.30$	
Input low voltage	V _{IL2}	Hysteresis input	V	7DD ≅ 4.3 V	0	$V_{DD} \times 0.25$	V
	V _{IL3}		V	/ _{DD} < 4.5 V		V _{DD} × 0.10	
	fc	VIN VOUT	V _{DD}	= 4.5 to 5.5 V	0.4	8.0	MHz
Clock frequency	I C	XIN, XOUT	V _{DD}	= 2.7 to 5.5 V	0.4	4.2	IVITIZ
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: The condition of clock frequency is in NORMAL1/2 modes and IDLE1/2 modes.

DC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis voltage	V _{HS}	Hysteresis inputs	VDD = 5.0 V	_	0.9	_	٧
	I _{IN1}	TEST					
Input current	I _{IN2}	Open drain ports, Tri-state ports	VDD = 5.5 V V _{IN} = 5.5 V/0 V	-	_	± 2	μA
	I _{IN3}	RESET, STOP					
Input resistance	R _{IN2}	RESET	VDD = 5.0 V	100	220	450	kΩ
Output leakage		Sink open drain ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	_	_	2	
current	I _{LO}	Tri-state ports	V _{DD} = 5.5 V, V _{OUT} = 5.5/0 V	_	_	± 2	μA
Output high voltage	V _{OH2}	Tri-state ports	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	_	_	V
Output low voltage	V _{OL}	Except for XOUT and P3	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	-	_	0.4	mA
Output low current	I _{OL3}	P3	V _{DD} = 4.5 V, V _{OL} = 1.0 V	_	20	_	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	_	4.5	5.5	mA
Supply current in IDLE 1, 2 modes			fc = 8 MHz fs = 32.768 kHz	_	2.5	4.0	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 3.0 \text{ V}, V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$ $V_{IN} = 4.19 \text{ MHz}$	_	1.75	3.0	mA
Supply current in IDLE 1, 2 modes] ,		fs = 32.768 kHz	_	1.25	2.0	mA
Supply current in SLOW mode	I _{DD}		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$	-	20	30	μΑ
Supply current in SLEEP mode			fs = 32.768 kHz	_	10	20	μΑ
Supply current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V	-	0.5	10	μΑ

Note 1: Typical values show those at Topr = 25° C

Note 2: Input Current $I_{\text{IN1},l_{\text{IN3}}}$. The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

Note 3: IDD except for I_{REF}.

AD Conversion Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

					Max			
Parameter	Symbol	Conditions	Min	Тур.	ADCDR1	ADO	DR2	Unit
					ADCDIT	ACK = 0	ACK = 1	
Analan mafananaa walta wa	V_{AREF}	., , , , , , , , , , , , , , , , , , ,	2.7	_		V_{DD}		V
Analog reference voltage	V _{ASS}	$V_{AREF} - V_{ASS} \ge 2.5 V$	V _{SS}	_		1.5		V
Analog input voltage	V _{AIN}		V _{ASS}	_		V_{AREF}		>
Analog supply current	I _{REF}	V _{AREF} = 5.5 V, V _{ASS} = 0.0 V	-	0.5		1.2		mA
Nonlinearity error		V _{DD} = 5.0, V _{SS} = 0.0 V V _{AREF} = 5.000 V	_	_	± 1	± 3	± 2	
Zero point error		VAREF = 3.000 V VASS = 0.000 V	_	_	± 1	± 3	± 2	LCD
Full scale error		$V_{DD} = 2.7, V_{SS} = 0.0 \text{ V}$	_	_	± 1	± 3	± 2	LSB
Total error		V _{AREF} = 2.700 V V _{ASS} = 0.000 V	_	_	± 2	± 6	± 4	

Note 1: $\triangle V_{AREF} = V_{AREF} - V_{ASS}$ ADCDR1: 8 bits - AD conversion result (1LSB = $\triangle V_{AREF}$ /256) ADCDR2: 10 bits - AD conversion result (1LSB = $\triangle V_{AREF}$ /1024)

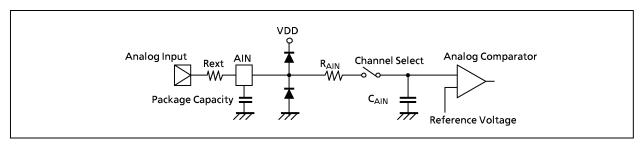
Note 2: Quantizing error is not contained in those errors.

AD Input Characteristics

(Topr = $-40 \text{ to } 85^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Innut impodence (Pecistence)	В	VDD = 5.0 V, Conversion time 23 μ s (fc = 8 MHz)	-	5	-	1.0
Input impedance (Resistance)	R _{AIN}	$V_{DD} = 2.7 \text{ V}$, Conversion time 43.8 μ s (fc = 4.2 MHz)	-	20	_	kΩ
Inner time and an an (Compaits)	_	$V_{DD} = 5.0 \text{ V}$, Conversion time 23 μ s (fc = 8 MHz)	-	7	-	
Input impedance (Capacity)	C _{AIN}	$V_{DD} = 2.7 \text{ V}$, Conversion time 43.8 μ s (fc = 4.2 MHz)	-	7	-	pF
Carrier in a dame.	David	$V_{DD} = 5.0 \text{ V}$, Conversion time 23 μ s (fc = 8 MHz)	-	-	5	1.0
Source impedance	Rext	$V_{DD} = 2.7 \text{ V}$, Conversion time 43.8 μ s (fc = 4.2 MHz)	-	-	5	kΩ

Note: Input current (Output leak current) error (Max $\pm 2 \mu$ A) and quantizing error (Max ± 4 LSB) for AD are contained.



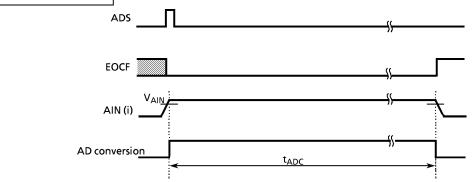
AD Pin Mode

AC Characteristics

(Vcc	_	٥v	Tonr	_	- 40 to	85°C)
(V SS	=	υν,	ropr	=	- 40 to	05 C)

Parameter	Symbol	Conditions	V _{DD}	Min	Тур.	Max	Unit
		In NORMAL 1, 2 mode	4.5 to	0.5		40	
Machina avelatima	_	In IDLE 1, 2 mode	5.5 V	0.5	-	10	
Machine cycle time	t _{cy}	In SLOW mode	2.7 to	447.6		422.2	μ S
		In SLEEP mode 5.		117.6	_	133.3	
High level clock pulse width	t _{WCH}	For external clock operation	4.5 to	62.5			
Low level clock pulse width	t _{WCL}	(XIN input), fc = 8 MHz	5.5 V	62.5	-	_	ns
High level clock pulse width	t _{WSH}	For external clock operation	2.7 to	44.7			
Low level clock pulse width	t _{WSL}	(XTIN input), fs = 32.768 kHz	5.5 V	14.7	-	_	μ S
AB		ADCCR bit 4; ACK = 0	-	-	49 tcy	-	
AD conversion time	t _{ADC}	ADCCR bit 4; ACK = 1	-	-	196 tcy	-	ns

Timing of AD Conversion



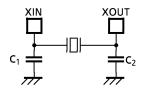
Note 1: During AD conversion, make the level of V_{AIN} stable.

Note 2: i = 17 to 10, 07 to 00

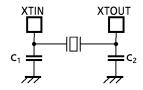
Recommended Oscillating Conditions

$$(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

_		Oscillation		_		Recommended Constant		
Parameter	arameter Oscillator		VDD	Recommended Oscillator		C ₁	C ₂	
	Ceramic		4.5 to 5.5 V	KYOCERA	KBR8.0 M			
High-frequency resonator			2.7 to 5.5 V	KYOCERA	KBR4.0 MS	30 pF	30 pF	
oscillation		4 MHz		MURATA	CSA4.00 MG			
		8 MHz	4.5 to 5.5 V	тоуосом	210B 8.0000			
	Crystal oscillator	4 MHz	2.7 to 5.5 V	тоуосом	204B 4.0000	20 pF	20 pF	
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 to 5.5 V	NDK	MX-38T	15 pF	15 pF	



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.
- Note 2: TOYAMA MURATA MFG. CO., LTD (JAPAN)

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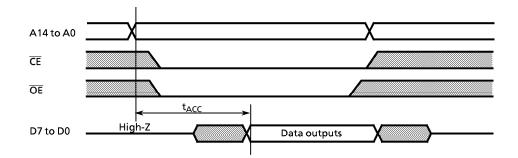
DC/AC Characteristics (PROM mode)

 $(V_{SS} = 0 \ V)$

(1) Read operation

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input high voltage	V _{IH4}		2.2	-	V _{CC}	V
Input low voltage	V _{IL4}		0	-	0.8	<
Power supply voltage	V _{CC}		4.75		6.5	\ \
Program power supply voltage	V_{PP}		4.75	_	0.5	'
Address access time	t _{ACC}	V _{CC} = 5.0 ± 0.25 V	_	1.5 tcyc + 300	-	ns

Note: tcyc = 500 ns at 8 MHz

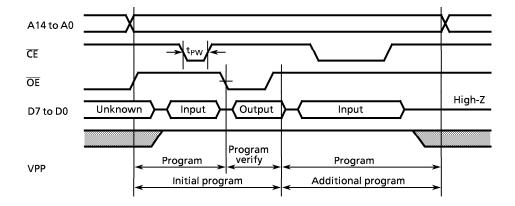


Timing Waveforms of Read Operation

2003-07-09

(2) Program Operation (High-speed write mode - I) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input high voltage	V _{IH4}		2.2	-	V _{CC}	V
Input low voltage	V _{IL4}		0	-	0.8	٧
Power supply voltage	V _{CC}		5.75	_	6.5	٧
Program power supply voltage	V _{PP}		12.0	12.5	13.0	V
Initial program pulse width	t _{PW}	$V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V},$ $V_{PP} = 12.5 \text{ V} \pm 0.5 \text{ V}$	0.95	1.0	1.05	ms



Timing Waveforms of Programming Operation

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.

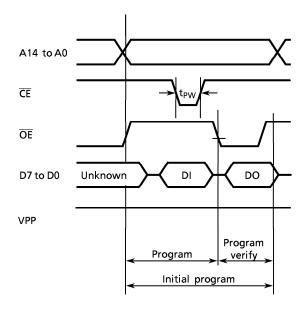
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.

Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V \pm 0.5 V) to the V_{pp} pin as the device is damaged.

Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

(3) Program operation (High-speed write mode -II) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input high voltage	V_{IH4}		2.2	_	V _{CC}	V
Input low voltage	V_{IL4}		0	_	0.8	V
Supply voltage	V_{CC}		6.00	6.25	6.50	V
Program supply voltage	V_{PP}		12.50	12.75	13.0	V
Initial program pulse width	t _{PW}	$V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V},$ $V_{PP} = 12.75 \text{ V} \pm 0.25 \text{ V}$	0.095	0.1	0.105	ms



Note: DO: Data output (10 to 17) DI: Data input (10 to 17)

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.

When V_{cc} power supply is turned off or before, V_{pp} must be decreased.

Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V \pm 0.25 V) to the V_{pp} pin as the device is damaged.

Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Electrical Characteristics

(2) TMP87PM48

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V_{DD}		- 0.3 to 6.5	٧	
Input voltage	V_{IN}		- 0.3 to V _{DD} + 0.3	٧	
Output voltage	V _{OUT}		- 0.3 to V _{DD} + 0.3	V	
Output current (Per 1 pin)	I _{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	3.2	4	
	I _{OUT2}	Port P3	30	mA	
O to the second (Testall)	Σ l _{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8	120		
Output current (Total)	Σ I _{OUT2}	Port P3	120	mA	
Power dissipation	PD		350	mW	
Soldering temperature (Time)	Tsld		260 (10 s)	°C	
Storage temperature	Tstg		– 55 to 125	°C	
Operating temperature	Topr		– 40 to 85	°C	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

$$(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$$

Parameter	Symbol	Pins		Conditions	Min	Max	Unit
			fc = 8 MHz	NORMAL1/2 modes IDLE1/2 modes	4.5		
Supply voltage	V _{DD}		fc = 4.2 MHz fs = 32.768 kHz	NORMAL1/2 modes IDLE1/2 modes	2.7	5.5	V
				SLOW mode SLEEP mode			
				STOP mode	2.0		
	V _{IH1}	Except hysteresis input	V _{DD} ≧ 4.5 V		$V_{DD} \times 0.70$	V_{DD}	
Input high voltage	V _{IH2}	Hysteresis input			$V_{DD} \times 0.75$		V
	V _{IH3}		V _{DD} < 4.5 V		$V_{DD} \times 0.90$		
	V _{IL1}	Except hysteresis input	$V_{DD} \ge 4.5 V$			$V_{DD} \times 0.30$	
Input low voltage	V_{IL2}	Hysteresis input			0	$V_{DD} \times 0.25$	V
	V _{IL3}		\	/ _{DD} < 4.5 V		$V_{DD} \times 0.10$	
		VIII. VOLIT	V _{DD} = 4.5 to 5.5 V			8.0	D411-
Clock frequency	fc	XIN, XOUT	V _{DD} = 2.7 to 5.5 V		0.4	4.2	MHz
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: The condition of clock frequency is in NORMAL1/2 modes and IDLE1/2 modes.

DC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Conditions	Min	Тур.	Max	Unit
Hysteresis voltage	V _{HS}	Hysteresis inputs	VDD = 5.0 V	-	0.9	_	٧
	I _{IN1}	TEST					
Input current	I _{IN2}	Open drain ports, Tri-state ports	VDD = 5.5 V V _{IN} = 5.5 V/0 V	-	_	± 2	μΑ
	I _{IN3}	RESET, STOP					
Input resistance	R _{IN2}	RESET	VDD = 5.0 V	100	220	450	kΩ
Output leakage Sink open drain ports V _{DD}		V _{DD} = 5.5 V, V _{OUT} = 5.5 V	_	-	2		
current	ILO	Tri-state ports	V _{DD} = 5.5 V, V _{OUT} = 5.5/0 V	_	_	± 2	μ A
Output high voltage	V _{OH2}	Tri-state ports	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	-	-	٧
Output low voltage	V _{OL}	Except for XOUT and P3	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	-	_	0.4	mA
Output low current	I _{OL3}	P3	V _{DD} = 4.5 V, V _{OL} = 1.0 V	_	20	_	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 5.5 \text{ V}$ $V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$	_	4.75	6.4	mA
Supply current in IDLE 1, 2 modes			fc = 8 MHz fs = 32.768 kHz	_	3.25	4.65	mA
Supply current in NORMAL 1, 2 modes			$V_{DD} = 3.0 \text{ V}, V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$ $V_{IN} = 4.19 \text{ MHz}$	_	1.87	3.2	mA
Supply current in IDLE 1, 2 modes] ,		fs = 32.768 kHz	_	1.35	2.2	mA
Supply current in SLOW mode	I _{DD}		$V_{DD} = 3.0 \text{ V}$ $V_{IN} = 2.8 \text{ V}/0.2 \text{ V}$	_	20	30	μΑ
Supply current in SLEEP mode			fs = 32.768 kHz	-	10	20	μΑ
Supply current in STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V	-	0.5	10	μΑ

Note 1: Typical values show those at Topr = 25° C

Note 2: Input Current I_{IN1} , I_{IN3} : The current through resistor is not included, when the input resistor (pull-up or pull-down) is contained.

Note 3: IDD except for I_{REF}.

AD Conversion Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 5.5 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

						Max		
Parameter	Symbol	Conditions	Min	Тур.	ADCDR1		DR2	Unit
						ACK = 0	ACK = 1	
A +	V_{AREF}	., , , , , , , , , , , , , , , , , , ,	2.7	_		V_{DD}		V
Analog reference voltage	V _{ASS}	$V_{AREF} - V_{ASS} \ge 2.5 V$	V _{SS}	-		1.5		٧
Analog input voltage	V _{AIN}		V _{ASS}	_		V_{AREF}		٧
Analog supply current	I _{REF}	$V_{AREF} = 5.5 \text{ V},$ $V_{ASS} = 0.0 \text{ V}$	_	0.5		1.2		mA
Nonlinearity error		V _{DD} = 5.0, V _{SS} = 0.0 V V _{AREF} = 5.000 V	_	_	± 1	± 3	± 2	
Zero point error		VAREF = 3.000 V VASS = 0.000 V	_	_	± 1	± 3	± 2	1.60
Full scale error		$V_{DD} = 2.7, V_{SS} = 0.0 \text{ V}$	_	_	± 1	± 3	± 2	LSB
Total error		V _{AREF} = 2.700 V V _{ASS} = 0.000 V	_	_	± 2	± 6	± 4	

Note 1: $\triangle V_{AREF} = V_{AREF} - V_{ASS}$ ADCDR1: 8 bits - AD conversion result (1LSB = $\triangle V_{AREF}$ /256) ADCDR2: 10 bits - AD conversion result (1LSB = $\triangle V_{AREF}$ /1024)

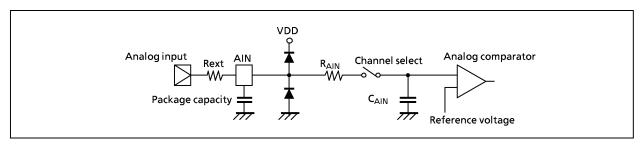
Note 2: Quantizing error is not contained in those errors.

AD Input Characteristics

(Topr = $-40 \text{ to } 85^{\circ}\text{C}$)

Parameter	Symbol	Conditions		Тур.	Max	Unit
Input impedance (Resistance)	В	VDD = 5.0 V, Conversion time 23 μ s (fc = 8 MHz)	-	5	-	I.O
	R _{AIN}	$V_{DD} = 2.7 \text{ V}$, Conversion time 43.8 μ s (fc = 4.2 MHz)	-	20	_	kΩ
	_	$V_{DD} = 5.0 \text{ V}$, Conversion time 23 μ s (fc = 8 MHz)		7	-	4.5
Input impedance (Capacity)	C _{AIN}	$V_{DD} = 2.7 \text{ V}$, Conversion time 43.8 μ s (fc = 4.2 MHz)		7	-	pF
Source impedance	David	$V_{DD} = 5.0 \text{ V}$, Conversion time 23 μ s (fc = 8 MHz)	-	-	5	I.O
	Rext	$V_{DD} = 2.7 \text{ V}$, Conversion time 43.8 μ s (fc = 4.2 MHz)		_	5	kΩ

Note: Input current (Output leak current) error (Max $\pm 2 \mu$ A) and quantizing error (Max ± 4 LSB) for AD are contained.



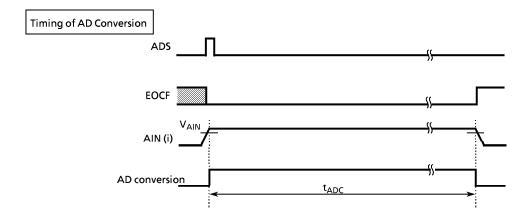
AD Pin Mode

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AC Characteristics

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Conditions	V _{DD}	Min	Тур.	Max	Unit
		In NORMAL 1, 2 mode	4.5 to	0.5		10	
Machine cycle time	_	In IDLE 1, 2 mode	5.5 V		-	10	
iviachine cycle unie	t _{cy}	In SLOW mode	2.7 to	447.6		133.3	μ S
		In SLEEP mode	5.5 V	117.6	-		
High level clock pulse width	t _{WCH}	For external clock operation	4.5 to	- CO -			
Low level clock pulse width	t _{WCL}	(XIN input), fc = 8 MHz	5.5 V	62.5	_	_	ns
High level clock pulse width	t _{WSH}	For external clock operation	2.7 to	44.7			
Low level clock pulse width	t _{WSL}	(XTIN input), fs = 32.768 kHz	5.5 V	14.7	-	_	μS
	t _{ADC}	ADCCR bit 4; ACK = 0			49 tcy	-	
AD conversion time		ADCCR bit 4 ; ACK = 1	-	-	196 tcy	-	ns



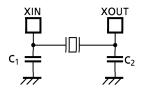
Note 1: During AD conversion, make the level of V_{AIN} stable.

Note 2: i = 17 to 10, 07 to 00

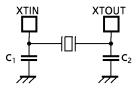
Recommended Oscillating Conditions

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

		Oscillation		_		Recommended Constant		
Parameter	Oscillator	Frequency	VDD	Recommend	ded Oscillator	C ₁	C ₂	
Ceramic	Ceramic	8 MHz	4.5 to 5.5 V	KYOCERA	KBR8.0 M			
High-frequency	resonator		2.7 to 5.5 V	KYOCERA	KBR4.0 MS	30 pF	30 pF	
oscillation		4 MHz		MURATA	CSA4.00 MG			
		8 MHz	4.5 to 5.5 V	тоуосом	210B 8.0000			
	Crystal oscillator	rystal oscillator 4 MHz		тоуосом	204B 4.0000	20 pF	20 pF	
Low-frequency oscillation	Crystal oscillator	32.768 kHz	2.7 to 5.5 V	NDK	MX-38T	15 pF	15 pF	



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

- Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.
- Note 2: TOYAMA MURATA MFG. CO., LTD (JAPAN)

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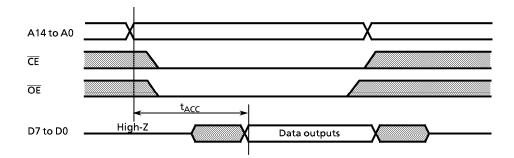
DC/AC Characteristics (PROM mode)

 $(V_{SS} = 0 \ V)$

(1) Read operation

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input high voltage	V _{IH4}		2.2	-	V _{CC}	٧
Input low voltage	V _{IL4}		0	-	0.8	٧
Power supply voltage	V _{CC}		4.75	_	6.5	V
Program power supply voltage	V_{PP}		4.75	_	0.5	
Address access time	t _{ACC}	V _{CC} = 5.0 ± 0.25 V	_	1.5 tcyc + 300	-	ns

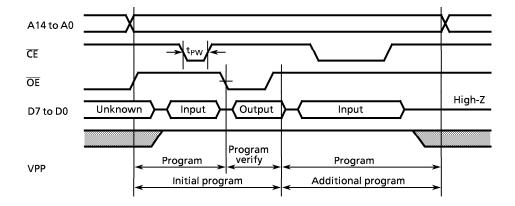
Note: tcyc = 500 ns at 8 MHz



Timing Waveforms of Read Operation

(2) Program Operation (High-speed write mode - I) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input high voltage	V _{IH4}		2.2	-	V _{CC}	٧
Input low voltage	V_{IL4}		0	_	0.8	٧
Power supply voltage	V _{CC}		5.75	6.0	6.25	٧
Program power supply voltage	V_{PP}		12.0	12.5	13.0	٧
Initial program pulse width	t _{PW}	$V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V},$ $V_{PP} = 12.5 \pm 0.5 \text{ V}$	0.95	1.0	1.05	ms



Timing Waveforms of Programming Operation

Note 1: When V_{cc} power supply is turned on or after, V_{pp} must be increased.

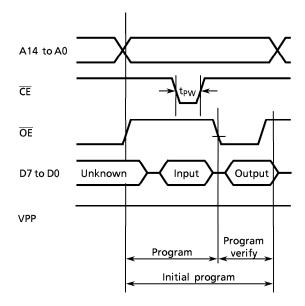
When V_{cc} power supply is turned off or before, V_{pp} must be decreased.

Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.5 V \pm 0.5 V) to the V_{pp} pin as the device is damaged.

Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

(3) Program operation (High-speed write mode -II) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
Input high voltage	V _{IH4}		2.2	-	V _{CC}	V
Input low voltage	V _{IL4}		0	-	0.8	٧
Supply voltage	V _{CC}		6.00	6.25	6.50	V
Program supply voltage	V_{PP}		12.50	12.75	13.0	٧
Initial program pulse width	t _{PW}	$V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V},$ $V_{PP} = 12.75 \text{ V} \pm 0.25 \text{ V}$	0.095	0.1	0.105	ms



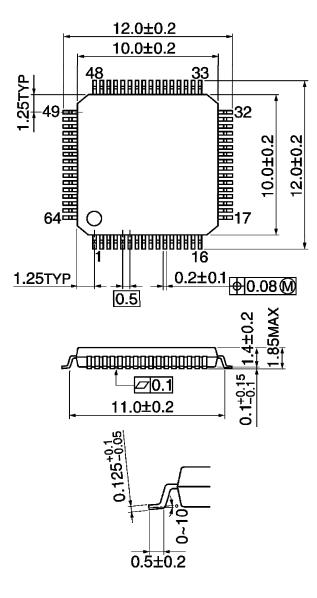
Note 1: When V_{CC} power supply is turned on or after, V_{pp} must be increased. When V_{CC} power supply is turned off or before, V_{pp} must be decreased.

Note 2: The device must not be set to the EPROM programmer or picked up from it under applying the program voltage (12.75 V \pm 0.25 V) to the V_{pp} pin as the device is damaged.

Note 3: Be sure to execute the recommended programing mode with the recommended programing adaptor. If a mode or an adaptor except the above, the misoperation sometimes occurs.

Package Dimensions

P-LQFP64-1010-0.50 Unit: mm



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P-QFP64-1414-0.80A Unit: mm

