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For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions. 030619_S

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Revision History

Date	Revision	
2007/8/31	1	First Release
2007/10/15	2	Contents Revised
2008/8/29	3	Contents Revised

Caution in Setting the UART Noise Rejection Time

When UART is used, settings of RXDNC are limited depending on the transfer clock specified by BRG. The combination "O" is available but please do not select the combination "–".

 (\Box)

The transfer clock generated by timer/counter interrupt is calculated by the following equation :

Transfer clock [Hz] = Timer/counter source clock [Hz] ÷ TTREG set value

			$\langle \rangle$	$\langle \langle \vee \rangle \rangle$					
	Transfer clock [Hz]	RXDNC setting							
BRG setting		00 (No noise rejection)	01 (Reject pulses shorter than 31/fc[s] as noise)	10 (Reject pulses shorter than 63/fc[s] as noise)	11 (Reject pulses shorter than 127/fc[s] as noise)				
000	fc/13	0	0	0	<u> </u>				
110	fc/8	0	(7/)	- 6	- >>				
(When the transfer clock gen- erated by timer/counter inter-	fc/16	0	Q Q		$\langle \rangle \rangle$ -				
rupt is the same as the right side column)	fc/32	0	0	0	<u> </u>				
The setting except the above		0			0				

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13. Package Dimensions

This is a technical document that describes the operating functions and electrical

specifications of the 8-bit microcontroller series TLCS-870/C (LSI).

CMOS 8-Bit Microcontroller

TMP86P203MG

The TMP86P203MG is a single-chip 8-bit high-speed and high-functionality microcomputer incorporating 2048 bytes of One-Time PROM.

Product No.	ROM (EPROM)	RAM	Package	Emulation Chip
TMP86P203MG	2048 bytes	128 bytes	SOP20-P-300-1.27	TMP86C908XB

1.1 Features

- 1. 8-bit single chip microcomputer TLCS-870/C series
 - Instruction execution time :

1.60 µs (at 2.5 MHz)

- 132 types & 731 basic instructions
- 2. 11interrupt sources (External : 3 Internal : 8)
- 3. Input / Output ports (14 pins)

Large current output: 2pins (Typ. 20mA), LED direct drive

- 4. Watchdog Timer
- 5. Prescaler
 - Time base timer
 - Divider output function
- 6. 8-bit timer counter : 2 ch
 - Timer, Event counter,
 - Programmable divider output (PDO),
 - Pulse width modulation (PWM) output,
 - Programmable pulse generation (PPG) modes
- 7. 8-bit successive approximation type AD converter (with sample hold)
 - Analog inputs: 4ch
- 8. Low power consumption operation
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STOP mode: Oscillation stops. (Battery/Capacitor back-up.)

IDLE0 mode: CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using high frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>.

IDLE1 mode: CPU stops and peripherals operate using high frequency clock. Release by interruputs(CPU restarts).

9. RC oscillation

10. Operation voltage:

 $4.5\ V$ to $5.5\ V$ at $\ 2.5\ MHz$

1.2 Pin Assignment



1.3 Block Diagram



1.4 Pin Names and Functions

The TMP86P203MG has MCU mode and PROM mode. Table 1-1 shows the pin functions in MCU mode. The PROM mode is explained later in a separate chapter.

Table 1-1Pin Names and Functions

	1		
Pin Name	Pin Number	Input/Output	Functions
P01	7	IO	PORT01
P00	6	IO	PORT00
P12 DVO	12	10 0	PORT12 Divider Output
P11	44	IO	PORTA
INT1	11		External interrupt 1 input
P10 INTO	10		PORT10 External interrupt 0 input
P20 STOP	9	O	PORT20 STOP mode release signal input
INT5			External interrupt 5 input
P37 AIN5	20	IO	PORT37 AD converter analog input 5
P36 AIN4	19	10	PORT36 AD converter analog input 4
D25			
AIN3	18		AD converter analog input 3
P34 AIN2	17		PORT34 AD converter analog input 2
P33	16	01	PORT33
P32	15		PORT32
P31		10	PORT31
TC4 PDO4/PWM4/PPG4	14		TC4 input PDO4/PWM4/PPG4 output
P30	~	OI	PORT30
TC3 PDO3/PWM3	13		TC3 input PDO3/PWM3 output
	2	-	Resonator connecting pins for high-frequency clock
XOUT)) o	Resonator connecting pins for high-frequency clock
RESET	8	-	Reset signal
TEST	4	I	Test pin for out-going test. Normally, be fixed to low.
VDD	5	I	+5V
VSS	1	I	0(GND)

2. Operational Description

2.1 CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

2.1.1 Memory Address Map

The TMP86P203MG memory is composed OTP RAM, and SFR(Special function register). They are all mapped in 64-Kbyte address space. Figure 2-1 shows the TMP86P203MG memory address map.



2.1.2 Program Memory (OTP)

The TMP86P203MG has a 2048 bytes (Address F800H to FFFFH) of program memory (OTP).

2.1.3 Data Memory (RAM)

The TMP86P203MG has 128 bytes (Address 0040H to 00BFH) of internal RAM. The internal RAM are located in the direct area; instructions with shorten operations are available against such an area.

The data memory contents become unstable when the power supply is turned on; therefore, the data memory should be initialized by an initialization routine.

Example :Clears RAM to "00H". (TMP86P203MG)

	LD	HL, 0040H
	LD	Α, Η
	LD	BC, 007FH
SRAMCLR:	LD	(HL), A
	INC	HL
	DEC	BC
	JRS	F, SRAMCLR

2.2 System Clock Controller

The system clock controller consists of a clock generator, a timing generator, and a standby controller.

; Start address setup ; Initial value (00H) setup



The clock generator generates the basic clock which provides the system clocks supplied to the CPU core and peripheral hardware.

The high-frequency (fc) clock can easily be obtained by connecting a resonator between the XIN and XOUT pins. Clock input from an external oscillator is also possible. In this case, external clock is applied to XIN pin with XOUT pin not connected.



Figure 2-3 Examples of Resonator Connection

Note: The function to monitor the basic clock directly at external is not provided for hardware, however, with disabling all interrupts and watchdog timers, the oscillation frequency can be adjusted by monitoring the pulse which the fixed frequency is outputted to the port by the program. The system to require the adjustment of the oscillation frequency should create the program for the adjustment in advance.

2.2.2 Timing Generator

The timing generator generates the various system clocks supplied to the CPU core and peripheral hardware from the basic clock (fc). The timing generator provides the following functions.

- 1. Generation of main system clock
- 2. Generation of divider output (DVO) pulses
- 3. Generation of source clocks for time base timer
- 4. Generation of source clocks for watchdog timer
- 5. Generation of internal source clocks for timer/counters
- 6. Generation of warm-up clocks for releasing STOP mode

2.2.2.1 Configuration of timing generator

The timing generator consists of a 2-stage prescaler, a 21-stage divider, a main system clock generator, and machine cycle counters.

As reset and STOP mode started/canceled, the prescaler and the divider are cleared to "0".



2.2.2.2 Machine cycle

Instruction execution and peripheral hardware operation are synchronized with the main system clock.

The minimum instruction execution unit is called an "machine cycle". There are a total of 10 different types of instructions for the TLCS-870/C Series: Ranging from 1-cycle instructions which require one machine cycle for execution to 10-cycle instructions which require 10 machine cycles for execution. A machine cycle consists of 4 states (S0 to S3), and each state consists of one main system clock.



2.2.3 Operation Mode Control Circuit

The operation mode control circuit starts and stops the oscillation circuit for the high-frequency clock. There are two operating modes: Single clock mode and STOP mode. These modes are controlled by the system control registers (SYSCR1 and SYSCR2). Figure 2-6 shows the operating mode transition diagram.

2.2.3.1 Single-clock mode

The oscillation circuit for the high-frequency clock is used. The main-system clock is obtained from the high-frequency clock. In the single-clock mode, the machine cycle time is 4/fc [s].

(1) NORMAL1 mode

In this mode, both the CPU core and on-chip peripherals operate using the high-frequency clock. The TMP86P203MG is placed in this mode after reset.

(2) JDLE1 mode

In this mode, the internal oscillation circuit remains active. The CPU and the watchdog timer are halted; however on-chip peripherals remain active (Operate using the high-frequency clock).

IDLE1 mode is started by SYSCR2<IDLE> = "1", and IDLE1 mode is released to NORMAL1 mode by an interrupt request from the on-chip peripherals or external interrupt inputs. When the IMF (Interrupt master enable flag) is "1" (Interrupt enable), the execution will resume with the acceptance of the interrupt, and the operation will return to normal after the interrupt service is completed. When the IMF is "0" (Interrupt disable), the execution will resume with the instruction which follows the IDLE1 mode start instruction.

(3) IDLE0 mode

In this mode, all the circuit, except oscillator and the timer-base-timer, stops operation.

This mode is enabled by SYSCR2<TGHALT> = "1".

When IDLE0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with TBTCR<TBTCK>, the timing generator starts feeding the clock to all peripheral circuits.

When returned from IDLE0 mode, the CPU restarts operating, entering NORMAL1 mode back again. IDLE0 mode is entered and returned regardless of how TBTCR<TBTEN> is set. When IMF = "1", EF6 (TBT interrupt individual enable flag) = "1", and TBTCR<TBTEN> = "1", interrupt processing is performed. When IDLE0 mode is entered while TBTCR<TBTEN> = "1", the INTTBT interrupt latch is set after returning to NORMAL1 mode.

2.2.3.2 STOP mode

In this mode, the internal oscillation circuit is turned off, causing all system operations to be halted. The internal status immediately prior to the halt is held with a lowest power consumption during STOP mode.

STOP mode is started by the system control register 1 (SYSCR1), and STOP mode is released by a inputting (Either level-sensitive or edge-sensitive can be programmably selected) to the STOP pin. After the warm-up period is completed, the execution resumes with the instruction which follows the STOP mode start instruction.



Note 1: The mode is released by falling edge of TBTCR<TBTCK> setting.

Figure 2-6 Operating Mode Transition Diagram

		\sim			5
Tahla 2-1	Operating	Mode	and	Conditions	ſ
	Operating	INIGAC (anu	Contaitionia	/

	Opera	ting Mode	Oscillator High Frequency	CPU Core	твт	Other Peripherals	Machine Cycle Time
		RESET		Reset	Reset	Reset	
		NORMAL1	Oscillation	Operate		Oporato	
	Single clock	IDLE1	Oscillation		Operate	Operate	4/10 [5]
\sim		IDLE0		Halt		Halt	
		STOP	Stop		Halt	Tidit	_
$\langle -$		\sim	\bigcirc				

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System Control Register 1

SYSCR1	7	6	5	4	3	2	1	0		
(0038H)	STOP	RELM	0	OUTEN	W	UT	1		(Initial value: 0000 00**)	
	STOP	STO	P mode star	t	0: CPI 1: CPI	U core and U core and	peripherals peripherals	remain acti are halted	ive (Start STOP mode)	R/W
	RELM	Rele mod	ase method e	for STOP	0: Edg 1: Lev	ge-sensitive el-sensitive	release release			R/W
	OUTEN	I Port	Port output during STOP mode			uring STOP mode 0: High impedance 1: Output kept				R/W
								Return t	to NORMAL mode	
		Wor	n un timo at	rologging	00			\sim	3 x 2 ¹⁶ /fc	1
	WUT	STOP mode		01		_		2 ¹⁶ /fc	R/W	
					10		\leq	$\langle \ \rangle$	3 x 2 ¹⁴ /fc	
					11		\bigcirc		2 ¹⁴ /fc	
								$\left(\right)$	\sim (\bigcirc)	

Note 1: When STOP mode is released with RESET pin input, a return is made to NORMAL1.

Note 2: fc: High-frequency clock [Hz], *; Don't care

Note 3: Bits 1 and 0 in SYSCR1 are read as undefined data when a read instruction is executed.

- Note 4: As the hardware becomes STOP mode under OUTEN = "0", input value is fixed to "0"; therefore it may cause external interrupt request on account of falling edge.
- Note 5: Port P20 is used as STOP pin. Therefore, when stop mode is started, OUTEN does not affect to P20, and P20 becomes High-Z mode.
- Note 6: Always set bit5 in SYSCR1 to "0".
- Note 7: The warmig-up time should be set correctly for using oscillator.

System Control Register 2



XEN	High-frequency oscillator control	0: Turn of escillation 1: Turn on escillation	R/W
IDLE	CPU and watchdog timer control (IDLE1 mode)	0: CPU and watchdog timer remain active 1: CPU and watchdog timer are stopped (Start IDLE1 mode)	R/M/
TGHALT	TG control (IDLE0 mode)	0: Feeding clock to all peripherals from TG (Start IDLE0 mode)	11/10

Note 1: When SYSCR2<XEN> is cleard to "0", the device is reset.

Note 2: *: Don't care, TG: Timing generator, *; Don't care

Note 3: Bits 3, 1 and 0 in SYSCR2 are always read as undefined value.

Note 4: Do not set IDLE and TGHALT to "1" simultaneously.

Note 5: Because returning from IDLE0 to NORMAL1 is executed by the asynchronous internal clock, the period of IDLE0 mode might be shorter than the period setting by TBTCR<TBTCK>.

Note 6: When IDLE1 mode is released, IDLE is automatically cleared to "0".

Note 7: When IDLE0 mode is released, TGHALT is automatically cleared to "0".

Note 8: Always clear bit6 and 5 in SYSCR2 to "0".

Note 9: Before setting TGHALT to "1", be sure to stop peripherals. If peripherals are not stopped, the interrupt latch of peripherals may be set after IDLE0 mode is released.

2.2.4 Operating Mode Control

2.2.4.1 STOP mode

STOP mode is controlled by the system control register 1, the STOP pin input.

The STOP pin is also used both as a port P20 and an INT5 (external interrupt input 5) pin. STOP mode is started by setting SYSCR1<STOP> to "1". During STOP mode, the following status is maintained.

- 1. Oscillations are turned off, and all internal operations are halted.
- 2. The data memory, registers, the program status word and port output latches are all held in the status in effect before STOP mode was entered.
- 3. The prescaler and the divider of the timing generator are cleared to "0".
- 4. The program counter holds the address 2 ahead of the instruction (e.g., [SET (SYSCR1).7]) which started STOP mode.

STOP mode includes a level-sensitive mode and an edge-sensitive mode, either of which can be selected with the SYSCR1<RELM>.

- Note 1: During STOP period (from start of STOP mode to end of warm up), due to changes in the external interrupt pin signal, interrupt latches may be set to "1" and interrupts may be accepted immediately after STOP mode is released. Before starting STOP mode, therefore, disable interrupts. Also, before enabling interrupts after STOP mode is released, clear unnecessary interrupt latches.
- (1) Level-sensitive release mode (RELM = "1")

In this mode, STOP mode is released by setting the <u>STOP</u> pin high. This mode is used for capacitor backup when the main power supply is cut off and long term battery backup.

Even if an instruction for starting STOP mode is executed while STOP pin input is high, STOP mode does not start but instead the warm-up sequence starts immediately. Thus, to start STOP mode in the level-sensitive release mode, it is necessary for the program to first confirm that the STOP pin input is low. The following two methods can be used for confirmation.

1. Testing a port.

2. Using an external interrupt input INT5 (INT5 is a falling edge-sensitive input).

Example 1 :Starting STOP mode from NORMAL mode by testing a port P20.



Example 2 :Starting STOP mode from NORMAL mode with an INT5 interrupt.

PINT5:	TEST	(P2PRD). 0	; To reject noise, STOP mode does not start if		
	JRS	F, SINT5	port P20 is at high		
	LD	(SYSCR1), 01010000B	; Sets up the level-sensitive release mode.		
	DI		; $IMF \leftarrow 0$		
	SET	(SYSCR1). 7	; Starts STOP mode		
SINT5:	RETI				



STOP mode is released by the following sequence.

- 1. The high-frequency clock oscillator is turned on.
- 2. A warm-up period is inserted to allow oscillation time to stabilize. During warm up, all internal operations remain halted. Four different warm-up times can be selected with the SYSCR1<WUT> in accordance with the resonator characteristics.
- 3. When the warm-up time has elapsed, normal operation resumes with the instruction following the STOP mode start instruction.

- Note 1: When the STOP mode is released, the start is made after the prescaler and the divider of the timing generator are cleared to "0".
- Note 2: STOP mode can also be released by inputting low level on the RESET pin, which immediately performs the normal reset operation.
- Note 3: When STOP mode is released with a low hold voltage, the following cautions must be observed. The power supply voltage must be at the operating voltage level before releasing STOP mode. The RESET pin input must also be "H" level, rising together with the power supply voltage. In this case, if an external time constant circuit has been connected, the RESET pin input voltage will increase at a slower pace than the power supply voltage. At this time, there is a danger that a reset may occur if input voltage level of the RESET pin drops below the non-inverting high-level input voltage (Hysteresis input).

Table 2-2 Warm-up Time Example (at fc = 2.5 M	up Time Example (at fc = 2.5 MHz)
---	-----------------------------------

WUT	Warm-up Time [ms]
00	78.64
01	26.21
10	19.66
11	6.554
1	

Note 1: The warm-up time is obtained by dividing the basic clock by the divider. Therefore, the warm-up time may include a certain amount of error if there is any fluctuation of the oscillation frequency when STOP mode is released. Thus, the warm-up time must be considered as an approximate value.



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2.2.4.2 IDLE1 mode

IDLE1 mode is controlled by the system control register 2 (SYSCR2) and maskable interrupts. The following status is maintained during this mode.

- 1. Operation of the CPU and watchdog timer (WDT) is halted. On-chip peripherals continue to operate.
- 2. The data memory, CPU registers, program status word and port output latches are all held in the status in effect before this mode were entered.
- 3. The program counter holds the address 2 ahead of the instruction which starts this mode.



• Start the IDLE1 mode

After IMF is set to "0", set the individual interrupt enable flag (EF) which releases IDLE1 mode. To start IDLE1 mode, set SYSCR2<IDLE> to "1".

• Release the IDLE1 mode

IDLE1 mode includes a normal release mode and an interrupt release mode. These modes are selected by interrupt master enable flag (IMF). After releasing IDLE1 mode, the SYSCR2<IDLE> is automatically cleared to "0" and the operation mode is returned to the mode preceding IDLE1 mode.

IDLE1 mode can also be released by inputting low level on the RESET pin. After releasing reset, the operation mode is started from NORMAL1 mode

(1) Normal release mode (IMF = "0")

IDLE1 mode is released by any interrupt source enabled by the individual interrupt enable flag (EF). After the interrupt is generated, the program operation is resumed from the instruction following the IDLE1 mode starts instruction. Normally, the interrupt latches (IL) of the interrupt source used for releasing must be cleared to "0" by load instructions.

(2) Interrupt release mode (IMF \neq "1")

IDLE1 mode are released by any interrupt source enabled with the individual interrupt enable flag (EF) and the interrupt processing is started. After the interrupt is processed, the program operation is resumed from the instruction following the instruction, which starts IDLE1 mode.

Note: When a watchdog timer interrupts is generated immediately before IDLE1 mode are started, the watchdog timer interrupt will be processed but IDLE1 mode will not be started.





2.2.4.3 IDLE0 mode (IDLE0)

IDLE0 mode is controlled by the system control register 2 (SYSCR2) and the time base timer control register (TBTCR). The following status is maintained during IDLE0 mode.

- 1. Timing generator stops feeding clock to peripherals except TBT.
- 2. The data memory, CPU registers, program status word and port output latches are all held in the status in effect before IDLE0 mode was entered.
- 3. The program counter holds the address 2 ahead of the instruction which starts IDLE0 mode.

Note: Before starting IDLE0 mode, be sure to stop (Disable) peripherals.



Figure 2-12 IDLE0 Mode

• Start the IDLE0 mode

Stop (Disable) peripherals such as a timer counter.

To start IDLE0 mode, set SYSCR2<TGHALT> to "1".

· Release the IDLE0 mode

IDLE0 mode include a normal release mode and an interrupt release mode.

This mode is selected by interrupt master flag (IMF), the individual interrupt enable flag of TBT and TBTCR<TBTEN>.

After releasing IDLE0 mode, the SYSCR2<TGHALT> is automatically cleared to "0" and the operation mode is returned to the mode preceding IDLE0 mode. Before starting the IDLE mode, when the TBTCR<TBTEN> is set to "1", INTTBT interrupt latch is set to "1".

IDLE0 mode can also be released by inputting low level on the **RESET** pin. After releasing reset, the operation mode is started from NORMAL1 mode.

Note: IDLE0 mode start/release without reference to TBTCR<TBTEN> setting.

(1) Normal release mode (IMF•EF6•TBTCR<TBTEN> = "0")

IDLE0 mode are released by the source clock falling edge, which is setting by the TBTCR<TBTCK>. After the falling edge is detected, the program operation is resumed from the instruction following the IDLE0 mode start instruction. Before starting the IDLE mode, when the TBTCR<TBTEN> is set to "1", INTTBT interrupt latch is set to "1".

(2) Interrupt release mode (IMF•EF6•TBTCR<TBTEN> = "1")

IDLE0 mode are released by the source clock falling edge, which is setting by the TBTCR<TBTCK> and INTTBT interrupt processing is started.

Note 1: Because returning from IDLE0 to NORMAL1 is executed by the asynchronous internal clock, the period of IDLE0 mode might be the shorter than the period setting by TBTCR<TBTCK>. Note 2: When a watchdog timer interrupt is generated immediately before IDLE0 mode is started, the watchdog timer interrupt will be processed but IDLE0 mode will not be started.

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2.3 Reset Circuit

The TMP86P203MG has four types of reset generation procedures: An external reset input, an address trap reset, a watchdog timer reset and a system clock reset. Of these reset, the address trap reset, the watchdog timer and the system clock reset are a malfunction reset. When the malfunction reset request is detected, reset occurs during the maximum 24/fc[s].

The malfunction reset circuit such as watchdog timer reset, address trap reset and system clock reset is not initialized when power is turned on. Therefore, reset may occur during maximum 24/fc[s] (9.6µs at 2.5 MHz) when power is turned on.

Table 1-3 shows on-chip hardware initialization by reset action.

On-chip Hardware		Initial Value	On-chip Hardware	Initial Value	
Program counter	(PC)	(FFFEH)	$\mathcal{A}(\mathbb{N})$		
Stack pointer	(SP)	Not initialized	Prescaler and divider of timing generator		
General-purpose registers (W, A, B, C, D, E, H, L, IX, IY)		Not initialized			
Jump status flag	(JF)	Not initialized	Watchdog timer	Enable	
Zero flag	(ZF)	Not initialized			
Carry flag	(CF)	Not initialized		\mathcal{O}	
Half carry flag	(HF)	Not initialized			
Sign flag	(SF)	Not initialized	Output latches of I/O ports	Refer to I/O port circuitry	
Overflow flag	(VF)	Not initialized			
Interrupt master enable flag	(IMF)	(0)			
Interrupt individual enable flags	(EF)	0		Refer to each of control	
Interrupt latches	(IL)	(0)	Control registers	register	
	(RAM	Not initialized	

 Table 2-3
 Initializing Internal Status by Reset Action

2.3.1 External Reset Input

The RESET pin contains a Schmitt trigger (Hysteresis) with an internal pull-up resistor.

When the $\overline{\text{RESET}}$ pin is held at "L" level for at least 3 machine cycles (12/fc [s]) with the power supply voltage within the operating voltage range and oscillation stable, a reset is applied and the internal state is initialized.

When the $\overline{\text{RESET}}$ pin input goes high, the reset operation is released and the program execution starts at the vector address stored at addresses FFFEH to FFFFH.



Figure 2-14 Reset Circuit

2.3.2 Address trap reset

If the CPU should start looping for some cause such as noise and an attempt be made to fetch an instruction from the on-chip RAM (when WDTCR1<ATAS> is set to "1") or the SFR area, address trap reset will be generated. The reset time is maximum 24/fc[s] (9.6µs at 2.5 MHz).

Note: The operating mode under address trapped is alternative of reset or interrupt. The address trap area is alternative.



Interrupt Control Circuit 3.

The TMP86P203MG has a total of 11 interrupt sources excluding reset. Interrupts can be nested with priorities. Four of the internal interrupt sources are non-maskable while the rest are maskable.

Interrupt sources are provided with interrupt latches (IL), which hold interrupt requests, and independent vectors. The interrupt latch is set to "1" by the generation of its interrupt request which requests the CPU to accept its interrupts. Interrupts are enabled or disabled by software using the interrupt master enable flag (IMF) and interrupt enable flag (EF). If more than one interrupts are generated simultaneously, interrupts are accepted in order which is dominated by hardware. However, there are no prioritized interrupt factors among non-maskable interrupts.

				1	ĩ
	Interrupt Factors	Enable Condition	Interrupt Latch	Vector Address	Priority
Internal/External	(Reset)	Non-maskable	- (FFFE	1
Internal	INTSWI (Software interrupt)	Non-maskable	- 41	FFFC	2
Internal	INTUNDEF (Executed the undefined instruction interrupt)	Non-maskable	6	FFFC	2
Internal	INTATRAP (Address trap interrupt)	Non-maskable	IL2	FFFA	2
Internal	INTWDT (Watchdog timer interrupt)	Non-maskable	IL3	FFF8	2
External	INTO	IMF• EF4 = 1, INT0EN = 1	IL4	FFF6	5
External	INT1	IMF• EF5 = 1	IL5	FFF4	6
Internal	INTTBT	IMF• EF6 = 1	IL6	FFF2	7
-	Reserved	IMF• EF7 = 1	IL7	FFF0	8
-	Reserved	IMF• EF8 = 1	IL8	FFEE	9
-	Reserved	IMF• EF9 = 1	IL9	FFEC	10
Internal	INTTC3	IMF• EF10 = 1	IL10	FFEA	11
Internal	INTTC4	IMF• EF11 = 1	IL11	FFE8	12
Internal	INTADC	IMF• EF12 = 1	IL12	FFE6	13
-	Reserved	IMF•EF13 = 1	IL13	FFE4	14
-	Reserved (IME• EF14 = 1	IL14	FFE2	15
External	INT5	IMF• EF15 = 1	IL15	FFE0	16

Note 1: To use the address trap interrupt (INTATRAP), clear WDTCR1<ATOUT> to "0" (It is set for the "reset request" after reset is cancelled). For details, see "Address Trap"

Note 2: To use the watchdog timer interrupt (INTWDT), clear WDTCR1<WDTOUT> to "0" (It is set for the "Reset request" after reset is released). For details, see "Watchdog Timer".

Interrupt latches (IL15 to IL2) 3.1

An interrupt latch is provided for each interrupt source, except for a software interrupt and an executed the undefined instruction interrupt. When interrupt request is generated, the latch is set to "1", and the CPU is requested to accept the interrupt if its interrupt is enabled. The interrupt latch is cleared to "0" immediately after accepting interrupt. All interrupt latches are initialized to "0" during reset.

The interrupt latches are located on address 003CH and 003DH in SFR area. Each latch can be cleared to "0" individually by instruction. However, IL2 and IL3 should not be cleared to "0" by software. For clearing the interrupt latch, load instruction should be used and then IL2 and IL3 should be set to "1". If the read-modify-write instructions such as bit manipulation or operation instructions are used, interrupt request would be cleared inadequately if interrupt is requested while such instructions are executed.

Interrupt latches are not set to "1" by an instruction.

Since interrupt latches can be read, the status for interrupt requests can be monitored by software.

Note: In main program, before manipulating the interrupt enable flag (EF) or the interrupt latch (IL), be sure to clear IMF to "0" (Disable interrupt by DI instruction). Then set IMF newly again as required after operating on the EF or IL (Enable interrupt by EI instruction)

In interrupt service routine, because the IMF becomes "0" automatically, clearing IMF need not execute normally on
interrupt service routine. However, if using multiple interrupt on interrupt service routine, manipulating EF or IL should be executed before setting IMF="1".



3.2 Interrupt enable register (EIR)

The interrupt enable register (EIR) enables and disables the acceptance of interrupts, except for the non-maskable interrupts (Software interrupt, undefined instruction interrupt, address trap interrupt and watchdog interrupt). Non-maskable interrupt is accepted regardless of the contents of the EIR.

The EIR consists of an interrupt master enable flag (IMF) and the individual interrupt enable flags (EF). These registers are located on address 003AH and 003BH in SFR area, and they can be read and written by an instructions (Including read-modify-write instructions such as bit manipulation or operation instructions).

3.2.1 Interrupt master enable flag (IMF)

The interrupt enable register (IMF) enables and disables the acceptance of the whole maskable interrupt. While IMF = "0", all maskable interrupts are not accepted regardless of the status on each individual interrupt enable flag (EF). By setting IMF to "1", the interrupt becomes acceptable if the individuals are enabled. When an interrupt is accepted, IMF is cleared to "0" after the latest status on IMF is stacked. Thus the maskable interrupts which follow are disabled. By executing return interrupt instruction [RETI/RETN], the stacked data, which was the status before interrupt acceptance, is loaded on IMF again.

The IMF is located on bit0 in EIRL (Address: 003AH in SFR), and can be read and written by an instruction. The IMF is normally set and cleared by [EI] and [DI] instruction respectively. During reset, the IMF is initialized to "0".

3.2.2 Individual interrupt enable flags (EF15 to EF4)

Each of these flags enables and disables the acceptance of its maskable interrupt. Setting the corresponding bit of an individual interrupt enable flag to "1" enables acceptance of its interrupt, and setting the bit to "0" disables acceptance. During reset, all the individual interrupt enable flags (EF15 to EF4) are initialized to "0" and all maskable interrupts are not accepted until they are set to "1".

Note: In main program, before manipulating the interrupt enable flag (EF) or the interrupt latch (IL), be sure to clear IMF to "0" (Disable interrupt by DI instruction). Then set IMF newly again as required after operating on the EF

or IL (Enable interrupt by EI instruction)

In interrupt service routine, because the IMF becomes "0" automatically, clearing IMF need not execute normally on interrupt service routine. However, if using multiple interrupt on interrupt service routine, manipulating EF or IL should be executed before setting IMF="1".

; IMF \leftarrow 0

; EF15 to EF13, EF11, EF5 - 1

Note: IMF should not be set.

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: EI ; $IMF \leftarrow 1$ Example 2 :C compiler description example unsigned int _io (3AH) EIRL; _DI(); EIRL = 10100000B; : _EIRL); _EIRL); _EIRL); _EIRL); _EIRL); _EIRL); _CI(); _CI()

(EIRL), 1110100000100000B

Example 1 :Enables interrupts individually and sets IMF

DI

LDW

:



An interrupt request, which raised interrupt latch, is held, until interrupt is accepted or interrupt latch is cleared to "0" by resetting or an instruction. Interrupt acceptance sequence requires 8 machine cycles (12.8 μ s @2.5 MHz) after the completion of the current instruction. The interrupt service task terminates upon execution of an interrupt return instruction [RETI] (for maskable interrupts) or [RETN] (for non-maskable interrupts). Figure 3-1 shows the timing chart of interrupt acceptance processing.

3.3.1 Interrupt acceptance processing is packaged as follows.

- a. The interrupt master enable flag (IMF) is cleared to "0" in order to disable the acceptance of any following interrupt.
- b. The interrupt latch (IL) for the interrupt source accepted is cleared to "0".
- c. The contents of the program counter (PC) and the program status word, including the interrupt master enable flag (IMF), are saved (Pushed) on the stack in sequence of PSW + IMF, PCH, PCL. Meanwhile, the stack pointer (SP) is decremented by 3.

- d. The entry address (Interrupt vector) of the corresponding interrupt service program, loaded on the vector table, is transferred to the program counter.
- e. The instruction stored at the entry address of the interrupt service program is executed.

Note: When the contents of PSW are saved on the stack, the contents of IMF are also saved.



Note 1: a: Return address entry address, b: Entry address, c: Address which RETI instruction is stored

Note 2: On condition that interrupt is enabled, it takes 38/fc [s] at maximum (If the interrupt latch is set at the first machine cycle on 10 cycle instruction) to start interrupt acceptance processing since its interrupt latch is set.

Figure 3-1 Timing Chart of Interrupt Acceptance/Return Interrupt Instruction

Example: Correspondence between vector table address for INTTBT and the entry address of the interrupt service program



A maskable interrupt is not accepted until the IMF is set to "1" even if the maskable interrupt higher than the level of current servicing interrupt is requested.

In order to utilize nested interrupt service, the IMF is set to "1" in the interrupt service program. In this case, acceptable interrupt sources are selectively enabled by the individual interrupt enable flags.

To avoid overloaded nesting, clear the individual interrupt enable flag whose interrupt is currently serviced, before setting IMF to "1". As for non-maskable interrupt, keep interrupt service shorten compared with length between interrupt requests; otherwise the status cannot be recovered as non-maskable interrupt would simply nested.

3.3.2 Saving/restoring general-purpose registers

During interrupt acceptance processing, the program counter (PC) and the program status word (PSW, includes IMF) are automatically saved on the stack, but the accumulator and others are not. These registers are saved by software if necessary. When multiple interrupt services are nested, it is also necessary to avoid using the same data memory area for saving registers. The following methods are used to save/restore the general-purpose registers.

3.3.2.1 Using PUSH and POP instructions

If only a specific register is saved or interrupts of the same source are nested, general-purpose registers can be saved/restored using the PUSH/POP instructions.



PINT



xx:	LD	(GSAVA), A processing)	; Save A register		
	LD	A, (GSAVA)	; Restore A register		
	RETI		; RETURN		



Saving/Restoring general-purpose registers using PUSH/POP data transfer instruction

Figure 3-4 Saving/Restoring General-purpose Registers under Interrupt Processing

3.3.3 Interrupt return

Interrupt return instructions [RETI]/[RETN] perform as follows.

[RET]]/[RETN] Interrupt Return 1. Program counter (PC) and program status word (PSW, includes IMF) are restored from the stack. 2. Stack pointer (SP) is incremented by 3.

As for address trap interrupt (INTATRAP), it is required to alter stacked data for program counter (PC) to restarting address, during interrupt service program.

Note: If [RETN] is executed with the above data unaltered, the program returns to the address trap area and INTATRAP occurs again. When interrupt acceptance processing has completed, stacked data for PCL and PCH are located on address (SP + 1) and (SP + 2) respectively.

Example 1 :Returning from address trap interrupt (INTATRAP) service program

PINTxx:	POP	WA	; Recover SP by 2
	94	WA, Return Address	;
	PUSH	WA	; Alter stacked data
(())	(interrupt proc	essing)	
	RETN	\sim	; RETURN
		\bigcirc	

Example 2 :Restarting without returning interrupt

(In this case, PSW (Includes IMF) before interrupt acceptance is discarded.)

\sim		\checkmark			
PINTxx:	INC	SP	; Recover SP by 3		
	INC	SP	• 7		
	INC	SP	• •		
	(interrupt proce	essing)			
	LD	EIRL, data	; Set IMF to "1" or clear it to "0"		
	JP	Restart Address	; Jump into restarting address		

Interrupt requests are sampled during the final cycle of the instruction being executed. Thus, the next interrupt can be accepted immediately after the interrupt return instruction is executed.

- Note 1: It is recommended that stack pointer be return to rate before INTATRAP (Increment 3 times), if return interrupt instruction [RETN] is not utilized during interrupt service program under INTATRAP (such as Example 2).
- Note 2: When the interrupt processing time is longer than the interrupt request generation time, the interrupt service task is performed but not the main task.

3.4 Software Interrupt (INTSW)

Executing the SWI instruction generates a software interrupt and immediately starts interrupt processing (INTSW is highest prioritized interrupt).

Use the SWI instruction only for detection of the address error or for debugging,

3.4.1 Address error detection

FFH is read if for some cause such as noise the CPU attempts to fetch an instruction from a non-existent memory address during single chip mode. Code FFH is the SWI instruction, so a software interrupt is generated and an address error is detected. The address error detection range can be further expanded by writing FFH to unused areas of the program memory. Address trap reset is generated in case that an instruction is fetched from RAM or SFR areas.

3.4.2 Debugging

Debugging efficiency can be increased by placing the SWI instruction at the software break point setting address.

3.5 Undefined Instruction Interrupt (INTUNDEF)

Taking code which is not defined as authorized instruction for instruction causes INTUNDEF. INTUNDEF is generated when the CPU fetches such a code and tries to execute it. INTUNDEF is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTUNDEF interrupt process starts, soon after it is requested.

Note: The undefined instruction interrupt (INTUNDEF) forces CPU to jump into vector address, as software interrupt (SWI) does.

3.6 Address Trap Interrupt (INTATRAP)

Fetching instruction from unauthorized area for instructions (Address trapped area) causes reset output or address trap interrupt (INTATRAP). INTATRAP is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTATRAP interrupt process starts, soon after it is requested.

Note: The operating mode under address trapped, whether to be reset output or interrupt processing, is selected on watchdog timer control register (WDTCR).

3.7 External Interrupts

The TMP86P203MG has 3 external interrupt inputs. These inputs are equipped with digital noise reject circuits (Pulse inputs of less than a certain time are eliminated as noise).

Edge selection is also possible with INT1. The INT0/P10 pin can be configured as either an external interrupt input pin or an input/output port, and is configured as an input port during reset.

Edge selection, noise reject control and $\overline{INT0}/P10$ pin function selection are performed by the external interrupt control register (EINTCR).

Source	Pin	Enable Conditions	Release Edge	Digital Noise Reject
INT0	ĪNTO	IMF + EF4 + INT0EN=1	Falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 7/fc [s] or more are considered to be signals.
INT1	INT1	IMF + EF5 = 1	Falling edge or Rising edge	Pulses of less than 15/fc or 63/fc [s] are elimi- nated as noise. Pulses of 49/fc or 193/fc [s] or more are considered to be signals.
INT5	ĪNT5	IMF + EF15 = 1	Falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 7/fc [s] or more are considered to be signals.

Note 1: In NORMAL1 or IDLE1 mode, if a signal with no noise is input on an external interrupt pin, it takes a maximum of "signal establishment time + 6/fs[s]" from the input signal's edge to set the interrupt latch.

Note 2: When INT0EN = "0", IL4 is not set even if a falling edge is detected on the INT0 pin input.

Note 3: When a pin with more than one function is used as an output and a change occurs in data or input/output status, an interrupt request signal is generated in a pseudo manner. In this case, it is necessary to perform appropriate processing such as disabling the interrupt enable flag.

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External Interrupt Control Register

EINTCR	7	6	5	4	3	2	1	0	
(0037H)	INT1NC	INT0EN	-	-	-	-	INT1ES		(Initial value: 00** **0*)

INT1NC	Noise reject time select	0: Pulses of less than 63/fc [s] are eliminated as noise 1: Pulses of less than 15/fc [s] are eliminated as noise	R/W
INTOEN	P10/INT0 pin configuration	0: P10 input/output port 1: INT0 pin (Port P10 should be set to an input mode)	R/W
INT1 ES	INT1 edge select	0: Rising edge 1: Falling edge	R/W

Note 1: fc: High-frequency clock [Hz], *: Don't care

Note 2: When the system clock frequency is switched between high and low or when the external interrupt control register (EINTCR) is overwritten, the noise canceller may not operate normally. It is recommended that external interrupts are disabled using the interrupt enable register (EIR).

Note 3: The maximum time from modifying INT1NC until a noise reject time is changed is 2^{6} /fc.

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4. Special Function Register (SFR)

The TMP86P203MG adopts the memory mapped I/O system, and all peripheral control and data transfers are performed through the special function register (SFR). The SFR is mapped on address 0000H to 003FH.

This chapter shows the arrangement of the special function register (SFR) for TMP86P203MG.

4.1 SFR

Address	Read
0000H	PODR
0001H	P1DR
0002H	P2DR
0003H	P3DR
0004H	Reserved
0005H	Reserved
0006H	Reserved
0007H	Reserved
0008H	Reserved
0009H	P1CR
000AH	P3CR
000BH	POOUTCR
000CH	POPRD -
000DH	P2PRD -
000EH	ADCCR1
000FH	ADCCR2
0010H	Reserved
0011H	Reserved
0012H	Reserved
0013H	Reserved
0014H	Reserved
0015H	Reserved
0016H	Reserved
0017H	Reserved
0018H	Reserved
0019H	Reserved
001AH	TC3CR
001BH (())	TC4CR
001CH	TTREG3
001DH	TTREG4
001EH	PWREG3
001FH	PWREG4
0020H	ADCDR1 -
0021H	ADCDR2 -
0022H	Reserved
0023H	Reserved
0024H	Reserved
0025H	Reserved
0026H	Reserved
0027H	Reserved

Address	Read	Write
0028H	Res	erved
0029H	Res	erved
002AH	Res	erved
002BH	Res	erved
002CH	Res	erved
002DH	Res	erved
002EH	Res	erved
002FH	Res	erved
0030H	Res	erved (
0031H	Res	erved
0032H	Res	erved
0033H	Res	erved
0034H	-	WDTCR1
0035H	(WDTCR2
0036H	TB	ÎÇR
0037H	EIN	TCR
0038H	SYS	CR1
0039H	SYS	iCR2
003AH		RL ()
003BH	EI	RH
003CH		
003DH		.#
003EH	Res	erved
003FH	R	SW /

Note 1: Do not access reserved areas by the program.

Note 2: -; Cannot be accessed.

Note 3: Write-only registers and interrupt latches cannot use the read-modify-write instructions (Bit manipulation instructions such as SET, CLR, etc. and logical operation instructions such as AND, OR, etc.).

5. I/O Ports

The TMP86P203MG has 4 parallel input/output ports as follows.

	Primary Function	Secondary Functions
Port P0	2-bit I/O port	-
Port P1	3-bit I/O port	External interrupt input and divider output.
Port P2	1-bit I/O port	External interrupt input and STOP mode release signal input.
Port P3	8-bit I/O port	Analog input and Timer/Counter input/output.

Each output port contains a latch, which holds the output data. All input ports do not have latches, so the external input data should be externally held until the input data is read from outside or reading should be performed several timer before processing. Figure 5-1 shows input/output timing examples.

External data is read from an I/O port in the S1 state of the read cycle during execution of the read instruction. This timing cannot be recognized from outside, so that transient input such as chattering must be processed by the program.

Output data changes in the S2 state of the write cycle during execution of the instruction which writes to an I/O port.



5.1 P0 (P01 to P00) Port (High Current)

The P0 port is an 2-bit input/output port. When using this port as an input port set the output latch to 1.

When using this port as an output port, the output latch data (PODR) is output to the PO port.

When reset, the output latch (P0DR) and the push-pull control register (P0OUTCR) are initialized to 1 and 0, respectively.

The P0 port allows its output circuit to be selected between N-channel open-drain input/output or push-pull output by the P0OUTCR register.

When using this port as an input port, set the POOUTCR register's corresponding bit to 0 after setting the PODR to 1.

The P0 port has independent data input registers. To inspect the output latch status, read the P0DR register. To inspect the pin status, read the P0PRD register.



5.2 P1 (P12 to P10) Port

The P1 port is a 3-bit input/output port that can be specified for input or output bitwise. The P1 Port Input/output Control Register (P1CR) is used to specify this port for input or output. When reset, the P1CR register is initialized to 0, with the P1 port set for input mode. The P1 port output latch is initialized to 0.

The P1 port is shared with external interrupt input and divider output. When using the P1 port as function pin, set its input pins for input mode. For the output pins, first set their output latches to 1 before setting the pins for output mode.

Note that the P11 pin is an external interrupt input. (When used as an output port, its interrupt latch is set at the rising or falling edge.) The P10 pin can be used as an input/output port or an external interrupt input by selecting its function with the External Interrupt Control Register (INT0EN). When reset, the P10 pin is chosen to be an input port.



5.3 P2 (P20) Port

The P2 port is a 1-bit input/output port shared with external interrupt input, and STOP canceling signal input. When using this port as an input port or function pin, set the output latch to 1. The output latch is initialized to 1 when reset.

We recommend using the P20 pin for external interrupt input or STOP canceling signal input or as an input port. (When used as an output port, the interrupt latch is set by a falling edge.)

The P2 port has independent data input registers. To inspect the output latch status, read the P2DR register. To inspect the pin status, read the P2PRD register. When the P2DR or P2PRD read instruction is executed for the P2 port, the values read from bits 7 to 1 are indeterminate.



5.4 P3 (P37 to P30) Port

The P3 port is an 8-bit input/output port that can be specified for input or output bitwise, and is shared with analog input and 8-bit timer counter input/output. The P3 Port Input/output Control Register (P3CR) and AINDS (ADCCR1 register bit 4) are used to specify this port for input or output. When reset, the P3CR register and P3DR are cleared to 0, while AINDS is set to 1, so that P37 to P30 function as input port.

When using the P3 port as an input port, set AINDS = 1 while at the same time setting the P3CR register to 0.

When using the P3 port for analog input, set AINDS = 0 and the pins selected with SAIN (ADCCR1 register bits 3 to 0) are set for analog input no matter what values are set in the P3DR and P3CR. When using the P3 port as an output port, set the P3CR to 1 and the pin associated with that bit is set for output mode, so that P3DR (output latch data) is output from that pin.

When an input instruction is executed for the P3 port while using the AD converter, the pins selected for analog input read in the P3DR value into the internal circuit and those not selected for analog input read in a 1 or 0 according to the logic level on each pin. Even when an output instruction is executed, no latch data are forwarded to the pins selected for analog input.

Any pins of the P3 port which are not used for analog input can be used as input/output ports. During AD conversion, however, avoid executing output instructions on these ports, because this is necessary to maintain the accuracy of conversion. Also, during AD conversion, take care not to enter a rapidly changing signal to any port adjacent to analog input.



Note 1: P30 and P31 are hysteresis inputs.

Note 2: Input status on ports set for input mode are read in into the internal circuit. Therefore, when using the ports in a mixture of input and output modes, the contents of the output latches for the ports that are set for input mode may be rewritten by execution of bit manipulating instructions.

6. Watchdog Timer (WDT)

The watchdog timer is a fail-safe system to detect rapidly the CPU malfunctions such as endless loops due to spurious noises or the deadlock conditions, and return the CPU to a system recovery routine.

The watchdog timer signal for detecting malfunctions can be programmed only once as "reset request" or "interrupt request". Upon the reset release, this signal is initialized to "reset request".

When the watchdog timer is not used to detect malfunctions, it can be used as the timer to provide a periodic interrupt.

Note: Care must be taken in system design since the watchdog timer functions are not be operated completely due to effect of disturbing noise.

6.1 Watchdog Timer Configuration



6.2 Watchdog Timer Control

The watchdog timer is controlled by the watchdog timer control registers (WDTCR1 and WDTCR2). The watchdog timer is automatically enabled after the reset release.

6.2.1 Malfunction Detection Methods Using the Watchdog Timer

The CPU malfunction is detected, as shown below.

- 1. Set the detection time, select the output, and clear the binary counter.
- 2. Clear the binary counter repeatedly within the specified detection time.

If the CPU malfunctions such as endless loops or the deadlock conditions occur for some reason, the watchdog timer output is activated by the binary-counter overflow unless the binary counters are cleared. When WDTCR1<WDTOUT> is set to "1" at this time, the reset request is generated and then internal hardware is initialized. When WDTCR1<WDTOUT> is set to "0", a watchdog timer interrupt (INTWDT) is generated.

The watchdog timer temporarily stops counting in the STOP mode including the warm-up or IDLE mode, and automatically restarts (continues counting) when the STOP/IDLE mode is inactivated.

Note: The watchdog timer consists of an internal divider and a two-stage binary counter. When the clear code 4EH is written, only the binary counter is cleared, but not the internal divider. The minimum binary-counter overflow time, that depends on the timing at which the clear code (4EH) is written to the WDTCR2 register, may be 3/ 4 of the time set in WDTCR1<WDTT>. Therefore, write the clear code using a cycle shorter than 3/4 of the time set to WDTCR1<WDTT>.

Example :Setting the watchdog timer detection time to 2²¹/fc [s], and resetting the CPU malfunction detection



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Watchdog Timer Control Register 1

WDTCR1	7	6	5	4	3		2	1	0		
(0034H)			(ATAS)	(ATOUT)	WDTEN	١	WD	ΓT	WDTOUT	(Initial value: **11	1001)
		-									
	WDTEN	Watchdog	g timer enable	e/disable	0: Disable 1: Enable	(Writin	g the disa	ble code to	WDTCR2 is I	required.)	Write only
								NORM	IAL1 mode		
					00 2 ²⁵ /fc				5		
	WDTT Vatchdog time		og timer detection time		01			:	2 ²³ /fc		Write only
		[-]	-		10			\sim	2 ²¹ fc		,
				ſ	11				2 ¹⁹ /fc		
	WDTOUT	Watchdog	g timer outpu	t select	0: Interrup 1: Reset re	t reque equest	st		$\bigcirc \searrow$		Write only
								$\left \right\rangle$			

Note 1: After clearing WDTOUT to "0", the program cannot set it to "1".

Note 2: fc: High-frequency clock [Hz], *: Don't care

- Note 3: WDTCR1 is a write-only register and must not be used with any of read-modify-write instructions. If WDTCR1 is read, a don't care is read.
- Note 4: To activate the STOP mode, disable the watchdog timer or clear the counter immediately before entering the STOP mode. After clearing the counter, clear the counter again immediately after the STOP mode is inactivated.
- Note 5: To clear WDTEN, set the register in accordance with the procedures shown in "6.2.3 Watchdog Timer Disable".

Watchdog Timer Control Register 2

Write
only
-

Note 1: The disable code is valid only when WDTCR1<WDTEN> = 0.

Note 2: *: Don't care

Note 3: The binary counter of the watchdog timer must not be cleared by the interrupt task.

Note 4: Write the clear code 4EH using a cycle shorter than 3/4 of the time set in WDTCR1<WDTT>.

6.2.2 Watchdog Timer Enable

Setting WDTCR1<WDTEN> to "1" enables the watchdog timer. Since WDTCR1<WDTEN> is initialized to "1" during reset, the watchdog timer is enabled automatically after the reset release.

6.2.3 Watchdog Timer Disable

To disable the watchdog timer, set the register in accordance with the following procedures. Setting the register in other procedures causes a malfunction of the microcontroller.

- 1. Set the interrupt master flag (IMF) to "0".
- 2. Set WDTCR2 to the clear code (4EH).
- 3. Set WDTCR1<WDTEN> to "0".
- 4. Set WDTCR2 to the disable code (B1H).

Note: While the watchdog timer is disabled, the binary counters of the watchdog timer are cleared.

Example :Disabling the watchdog timer



: Clears the binary couthe

Table 6-1 Watchdog Timer Detection Time (Example; fc = 2.5MHz)

 $IMF \leftarrow 0$



6.2.4 Watchdog Timer Interrupt (INTWDT)

When WDTCR1<WDTOUT> is cleared to "0", a watchdog timer interrupt request (INTWDT) is generated by the binary-counter overflow.

A watchdog timer interrupt is the non-maskable interrupt which can be accepted regardless of the interrupt master flag (IMF).

When a watchdog timer interrupt is generated while the other interrupt including a watchdog timer interrupt is already accepted, the new watchdog timer interrupt is processed immediately and the previous interrupt is held pending. Therefore, if watchdog timer interrupts are generated continuously without execution of the RETN instruction, too many levels of nesting may cause a malfunction of the microcontroller.

To generate a watchdog timer interrupt, set the stack pointer before setting WDTCR1<WDTOUT>.

Example :Setting watchdog timer interrupt

LD	SP, 00BFH	: Sets the stack pointer
LD	(WDTCR1), 00001000B	: WDTOUT \leftarrow 0

6.2.5 Watchdog Timer Reset

When a binary-counter overflow occurs while WDTCR1<WDTOUT> is set to "1", a watchdog timer reset request is generated. When a watchdog timer reset request is generated, the internal hardware is reset. The reset time is maximum 24/fc [s] (9.6 μ s @ fc = 2.5 MHz).



6.3 Address Trap

The Watchdog Timer Control Register 1 and 2 share the addresses with the control registers to generate address traps.



6.3.1 Selection of Address Trap in Internal RAM (ATAS)

WDTCR1<ATAS> specifies whether or not to generate address traps in the internal RAM area. To execute an instruction in the internal RAM area, clear WDTCR1<ATAS> to "0". To enable the WDTCR1<ATAS> setting, set WDTCR1<ATAS> and then write D2H to WDTCR2.

Executing an instruction in the SFR area generates an address trap unconditionally regardless of the setting in WDTCR1<ATAS>.

6.3.2 Selection of Operation at Address Trap (ATOUT)

When an address trap is generated, either the interrupt request or the reset request can be selected by WDTCR1<ATOUT>.

6.3.3 Address Trap Interrupt (INTATRAP)

When a binary-counter overflow occurs during WDTCR1<ATOUT> set to "0", an address trap interrupt request (INTATRAP) is generated.

An address trap interrupt is a non-maskable interrupt which can be accepted regardless of the interrupt master flag (IMF).

When an address trap interrupt is generated while the other interrupt including a watchdog timer interrupt is already accepted, the new address trap is processed immediately and the previous interrupt is held pending. Therefore, if address trap interrupts are generated continuously without execution of the RETN instruction, too many levels of nesting may cause a malfunction of the microcontroller.

To generate address trap interrupts, set the stack pointer beforehand.

6.3.4 Address Trap Reset

While WDTCR1<ATOUT> is "1", if the CPU should start looping for some cause such as noise and attempt be made to fetch an instruction from the on-chip RAM (while WDTCR1<ATAS> is "1") or the SFR area, address trap reset will be generated. When an address trap reset request is generated, the internal hardware is reset. The reset time is maximum 24/fc [s] (9.6 μ s @ fc = 2.5 MHz).

7. Time Base Timer (TBT)

The time base timer generates time base for key scanning, dynamic displaying, etc. It also provides a time base timer interrupt (INTTBT).

7.1 Time Base Timer

7.1.1 Configuration



Figure 7-1 Time Base Timer configuration

7.1.2 Control

Time Base Timer is controled by Time Base Timer control register (TBTCR).

Time Base Timer Control Register

	_	7	6	5	4	3	\sim	2	1	0				
ТВТС (0036	CR iH)		DEN) (DVOC	K)	"0"	твт	EN		ТВТСК		(Initial Value: 0000 0000)			
_			\searrow	.((>	\sim								
\langle	твте	Z	Time Base Timer enable / disable	Cal		0: Disable 1: Enable	e e							
	//	//		$\left(\left(\right) \right)$					NO	RMAL1 Mo	ode			
$\langle \langle \langle \langle \rangle \rangle$		\supset			000				fc/223					
	\searrow				001				fc/2 ²¹	'2 ²¹				
	\sim			\sim		010				fc/216				
	TBTC	к	Time Base Timer in Frequency select : [terrupt Hz]		011				fc/214		R/W		
					100				fc/213					
						101				fc/212				
					ſ	110				fc/211				
						111				fc/2 ⁹				

Note 1: fc; High-frequency clock [Hz], *; Don't care

Note 2: The interrupt frequency (TBTCK) must be selected with the time base timer disabled (TBTEN="0"). (The interrupt frequency must not be changed with the disable from the enable state.) Both frequency selection and enabling can be performed simultaneously. Example :Set the time base timer frequency to $fc/2^{16}$ [Hz] and enable an INTTBT interrupt.

LD	(TBTCR), 00000010B	; TBTCK \leftarrow 010	
LD	(TBTCR), 00001010B	; TBTEN \leftarrow 1	~
DI		; $IMF \leftarrow 0$	
SET	(EIRL) . 6		
EI			
			\sim

Table 7-1 Time Base Timer Interrupt Frequency (Example : fc = 2.5MHz)

TRTCK	Time Base Timer Interrupt Frequency [Hz]	
IBICK	NORMAL1 Mode	
000	0.29	$\mathcal{A}(\mathbb{N})$
001	1/19	
010	38.1	
011	153	90
100	305	>
101	610	
110	1220	
111	4880	

7.1.3 Function

An INTTBT (Time Base Timer Interrupt) is generated on the first falling edge of source clock (The divider output of the timing generato which is selected by TBTCK.) after time base timer has been enabled.

The divider is not cleared by the program; therefore, only the first interrupt may be generated ahead of the set interrupt period (Figure 7-2).



Figure 7-2 Time Base Timer Interrupt

7.2 Divider Output (\overline{DVO})

Approximately 50% duty pulse can be output using the divider output circuit, which is useful for piezoelectric buzzer drive. Divider output is from $\overline{\text{DVO}}$ pin.

7.2.1 Configuration



Note: Selection of divider output frequency (DVOCK) must be made while divider output is disabled (DVOEN="0"). Also, in other words, when changing the state of the divider output frequency from enabled (DVOEN="1") to disable(DVOEN="0"), do not change the setting of the divider output frequency.

Example :0.305 kHz pulse output (fc = 2.5 MHz)

 LD
 (TBTCR), 0000000B
 ; DVOCK ← "00"

 LD
 (TBTCR), 1000000B
 ; DVOEN ← "1"

DVOCK	Divider Output Frequency [Hz]	
DVOCK	NORMAL1 Mode	
00	0.305 k	$\langle \rangle$
01	0.610 k	
10	1.22 k	(\bigcirc)
11	2.44 k	77~

Table 7-2 Divider Output Frequency (Example : fc = 2.5 MHz)

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8. 8-Bit TimerCounter (TC3, TC4)

8.1 Configuration



8.2 TimerCounter Control

The TimerCounter 3 is controlled by the TimerCounter 3 control register (TC3CR) and two 8-bit timer registers (TTREG3, PWREG3).



- Note 1: fc: High-frequency clock [Hz]
- Note 2: Do not change the TC3M, TC3CK and TFF3 settings while the timer is running.
- Note 3: To stop the timer operation (TC3S= $1 \rightarrow 0$), do not change the TC3M, TC3CK and TFF3 settings. To start the timer operation (TC3S= $0 \rightarrow 1$), TC3M, TC3CK and TFF3 can be programmed.
- Note 4: To use the TimerCounter in the 16-bit mode, set the operating mode by programming TC4CR<TC4M>, where TC3M must be fixed to 011.
- Note 5: To use the TimerCounter in the 16-bit mode, select the source clock by programming TC3CK. Set the timer start control and timer F/F control by programming TC4CR<TC4S> and TC4CR<TFF4>, respectively.
- Note 6: The operating clock settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 8-1.
- Note 7: The timer register settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 8-2.

The TimerCounter 4 is controlled by the TimerCounter 4 control register (TC4CR) and two 8-bit timer registers (TTREG4 and PWREG4).





- Note 1: fc: High-frequency clock [Hz]
- Note 2: Do not change the TC4M, TC4CK and TFF4 settings while the timer is running.
- Note 3: To stop the timer operation (TC4S= 1 \rightarrow 0), do not change the TC4M, TC4CK and TFF4 settings.
 - To start the timer operation (TC4S= 0 \rightarrow 1), TC4M, TC4CK and TFF4 can be programmed.
- Note 4: When TC4M= 1** (upper byte in the 16-bit mode), the source clock becomes the TC4 overflow signal regardless of the TC3CK setting.
- Note 5: To use the TimerCounter in the 16-bit mode, select the operating mode by programming TC4M, where TC3CR<TC3 M> must be set to 011.
- Note 6: To the TimerCounter in the 16-bit mode, select the source clock by programming TC3CR<TC3CK>. Set the timer start control and timer F/F control by programming TC4S and TFF4, respectively.

Note 7: The operating clock settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 8-1.

Note 8: The timer register settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 8-2.

Table 8-1 Operating Mode and Selectable Source Clock (NORMAL1 and IDLE1 Modes)

Operating mode	fc/2 ¹¹	fc/27	fc/2 ⁵	fc/2 ³	fc/2	fc	TC3 pin input	TC4 pin input
8-bit timer	0	0	0	0	-	-	-	-
8-bit event counter	-	-	-	-	-	((-)	> o	0
8-bit PDO	0	0	О	0	- (/ _	-
8-bit PWM	О	0	О	0 <	o((/	0	-	-
16-bit timer	0	0	0	0			-	-
16-bit event counter	-	-	-	-	((-))	> -	0	-
16-bit PWM	О	0	О	9	¢	О	0	-
16-bit PPG	0	0	0	 O 	\searrow	-	$\mathcal{A}(0)$	> -

Note 1: For 16-bit operations (16-bit timer/event counter, warm-up counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bit (TC3CK).

Note 2: O : Available source clock

Table 8-2 Constraints on Register Values Being Compared

Operating mode	Register Value				
8-bit timer/event counter	1≤ (TTREGn) ≤255				
8-bit PDO	1≤ (TTREGn) ≤255				
8-bit PWM	2≤ (PWREGn) ≤254				
16-bit timer/event counter	1≤ (TTREG4, 3) ≤65535				
16-bit PWM	2≤ (PWREG4, 3) ≤65534				
16-bit PPG	1≤ (PWREG4, 3) < (TTREG4, 3) ≤65535 and (PWREG4, 3) + 1 < (TTREG4, 3)				
	\wedge ((// $))$				

Note: n = 3 to 4

8.3 Function

The TimerCounter 3 and 4 have the 8-bit timer, 8-bit event counter, 8-bit programmable divider output (PDO), 8bit pulse width modulation (PWM) output modes. The TimerCounter 3 and 4 (TC3, 4) are cascadable to form a 16bit timer. The 16-bit timer has the operating modes such as the 16-bit timer, 16-bit pulse width modulation (PWM) output and 16-bit programmable pulse generation (PPG) modes.

8.3.1 8-Bit Timer Mode (TC3 and 4)

In the timer mode, the up-counter counts up using the internal clock. When a match between the up-counter and the timer register j (TTREGj) value is detected, an INTTCj interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting.

Note 1: In the timer mode, fix TCjCR<TFFj> to 0. If not fixed, the PDOj, PWMj and PPGj pins may output pulses.

Note 2: In the timer mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the timer mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 3, 4

Table 8-3 Internal Source Clock for TimerCounter 3, 4 (Internal Clock)

Source Clock	Resolution	Maximum Setting time		
NORMAL1, IDLE1 mode	fc = 2.5 MHz	fc = 2.5 MHz		
fc/2 ¹¹ [Hz]	819 µs	208.8 ms		
fc/2 ⁷	51.2 μs	13.06 ms		
fc/2 ⁵	12.8 μs	3.204 ms		
fc/2 ³	3.20 μs	0.816 ms		

Example :Setting the timer mode with source clock $fc/2^7$ Hz and generating an interrupt 512 μ s later (TimerCounter4, fc = 2.5 MHz)



Figure 8-2 8-Bit Timer Mode Timing Chart (TC4)

8.3.2 8-Bit Event Counter Mode (TC3, 4)

In the 8-bit event counter mode, the up-counter counts up at the falling edge of the input pulse to the TCj pin. When a match between the up-counter and the TTREGj value is detected, an INTTCj interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting at the falling edge of the input pulse to the TCj pin. Two machine cycles are required for the low- or high-level pulse input to the TCj pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1 or IDLE1 mode.

- Note 1: In the event counter mode, fix TCjCR<TFFj> to 0. If not fixed, the PDOj, PWMj and PPGj pins may output pulses.
- Note 2: In the event counter mode, do not change the TTREG setting while the timer is running. Since TTREG is not in the shift register configuration in the event counter mode, the new value programmed in TTREG is in effect immediately after the programming. Therefore, if TTREG is changed while the timer is running, an expected operation may not be obtained.



Figure 8-3 8-Bit Event Counter Mode Timing Chart (TC4)

8.3.3 8-Bit Programmable Divider Output (PDO) Mode (TC3, 4)

This mode is used to generate a pulse with a 50% duty cycle from the \overline{PDOj} pin.

In the PDO mode, the up-counter counts up using the internal clock. When a match between the up-counter and the TTREGj value is detected, the logic level output from the \overline{PDOj} pin is switched to the opposite state and the up-counter is cleared. The INTTCj interrupt request is generated at the time. The logic state opposite to the timer F/Fj logic level is output from the \overline{PDOj} pin. An arbitrary value can be set to the timer F/Fj by TCjCR<TFFj>. Upon reset, the timer F/Fj value is initialized to 0.

To use the programmable divider output, set the output latch of the I/O port to 1.

Example :Generating 160 Hz pulse using TC4 (fc = 2.5 MHz)

$(\langle \rangle \rangle$	Setting port	
LD	(TTREG4), 3DH	$: 1/160 \div 2^7/\text{fc} \div 2 = 3\text{DH}$
LD	(TC4CR), 00010001B	: Sets the operating clock to $\ensuremath{\text{fc}/2^7}\xspace$, and 8-bit PDO mode.
LD	(TC4CR), 00011001B	: Starts TC4.

- Note 1: In the programmable divider output mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the programmable divider output mode, the new value programmed in TTREGj is in effect immediately after programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.
- Note 2: When the timer is stopped during PDO output, the PDOj pin holds the output status when the timer is stopped. To change the output status, program TCjCR<TFFj> after the timer is stopped. Do not change the TCjCR<TFFj> setting upon stopping of the timer.

Example: Fixing the PDOj pin to the high level when the TimerCounter is stopped

CLR (TCjCR).3: Stops the timer. CLR (TCjCR).7: Sets the PDOj pin to the high level.

Note 3: j = 3, 4


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8.3.4 8-Bit Pulse Width Modulation (PWM) Output Mode (TC3, 4)

This mode is used to generate a pulse-width modulated (PWM) signals with up to 8 bits of resolution. The up-counter counts up using the internal clock.

When a match between the up-counter and the PWREGj value is detected, the logic level output from the timer F/Fj is switched to the opposite state. The counter continues counting. The logic level output from the timer F/Fj is switched to the opposite state again by the up-counter overflow, and the counter is cleared. The INTTCj interrupt request is generated at this time.

Since the initial value can be set to the timer F/Fj by TCjCR<TFFj>, positive and negative pulses can be generated. Upon reset, the timer F/Fj is cleared to 0.

(The logic level output from the PWMj pin is the opposite to the timer F/Fj logic level.)

Since PWREGj in the PWM mode is serially connected to the shift register, the value set to PWREGj can be changed while the timer is running. The value set to PWREGj during a run of the timer is shifted by the INTTCj interrupt request and loaded into PWREGj. While the timer is stopped, the value is shifted immediately after the programming of PWREGj. If executing the read instruction to PWREGj during PWM output, the value in the shift register is read, but not the value set in PWREGj. Therefore, after writing to PWREGj, the reading data of PWREGj is previous value until INTTCj is generated.

For the pin used for PWM output, the output latch of the I/O port must be set to 1.

- Note 1: In the PWM mode, program the timer register PWREGj immediately after the INTTCj interrupt request is generated (normally in the INTTCj interrupt service routine.) If the programming of PWREGj and the interrupt request occur at the same time, an unstable value is shifted, that may result in generation of the pulse different from the programmed value until the next INTTCj interrupt request is generated.
- Note 2: When the timer is stopped during PWM output, the PWMj pin holds the output status when the timer is stopped. To change the output status, program TCjCR<TFFj> after the timer is stopped. Do not change the TCjCR<TFFj> upon stopping of the timer.

Example: Fixing the PWMj pin to the high level when the TimerCounter is stopped CLR (TCjCR).3: Stops the timer. CLR (TCjCR).7: Sets the PWMj pin to the high level.

- Note 3: To enter the STOP mode during PWM output, stop the timer and then enter the STOP mode. If the STOP mode is entered without stopping the timer when fc or fc/2 is selected as the source clock, a pulse is output from the PWMj pin during the warm-up period time after exiting the STOP mode.
- Note 4: j = 3, 4

_							
	Source Clock	Resolution	Repeated Cycle				
	NORMAL1, IDLE1 mode	fc = 2.5 MHz	fc = 2.5 MHz				
\sim	fc/2 ¹¹ [Hz]	819 μs	209.7 ms				
	fc/2 ⁷	51.2 μs	13.11 ms				
\sim (C	fc/2 ⁵	12.8 μs	3.277 ms				
	fc/2 ³	3.20 μs	819.2 μs				
$\langle = \rangle$	fc/2	800 ns	204.8 μs				
	fc	400 ns	102.4 μs				

Table 8-4 PWM Output Mode



8.3.5 16-Bit Timer Mode (TC3 and 4)

In the timer mode, the up-counter counts up using the internal clock. The TimerCounter 3 and 4 are cascadable to form a 16-bit timer.

When a match between the up-counter and the timer register (TTREG3, TTREG4) value is detected after the timer is started by setting TC4CR<TC4S> to 1, an INTTC4 interrupt is generated and the up-counter is cleared. After being cleared, the up-counter continues counting. Program the lower byte and upper byte in this order in the timer register. (Programming only the upper or lower byte should not be attempted.)

Note 1: In the timer mode, fix TCjCR<TFFj> to 0. If not fixed, the PDOj, PWMj, and PPGj pins may output a pulse.

Note 2: In the timer mode, do not change the TTREG setting while the timer is running. Since TTREG is not in the shift register configuration in the timer mode, the new value programmed in TTREG is in effect immediately after programming of TTREG. Therefore, if TTREG is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 3, 4

Table 0-3 Source Clock for To-Bit Timer Mode						
Source Clock	Resolution	Maximum Setting Time				
NORMAL1, IDLE1 mode	fc = 2.5 MHz	fc = 2.5 MHz				
fc/2 ¹¹	819 µs	53.69 s				
fc/2 ⁷	51.2 µs	3.355 s				
fc/2 ⁵	12.8 μs	0.839 ms				
fc/2 ³	3.2 µs	0.210 ms				

Table 8-5 Source Clock for 16-Bit Timer Mode

Example :Setting the timer mode v	with source clock fc/27	Hz, and generating	an interrupt 1.92 s later
(fc = 2.5 MHz)	(\land	



Figure 8-6 16-Bit Timer Mode Timing Chart (TC3 and TC4)

8.3.6 16-Bit Event Counter Mode (TC3 and 4)

In the event counter mode, the up-counter counts up at the falling edge to the TC3 pin. The TimerCounter 3 and 4 are cascadable to form a 16-bit event counter.

When a match between the up-counter and the timer register (TTREG3, TTREG4) value is detected after the timer is started by setting TC4CR<TC4S> to 1, an INTTC4 interrupt is generated and the up-counter is cleared.

After being cleared, the up-counter restarts counting at the falling edge of the input pulse to the TC3 pin. Two machine cycles are required for the low- or high-level pulse input to the TC3 pin.

Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1 or IDLE1 mode. Program the lower byte (TTREG3), and upper byte (TTREG4) in this order in the timer register. (Programming only the upper or lower byte should not be attempted.)

- Note 1: In the event counter mode, fix TCjCR<TFFj> to 0. If not fixed, the PDO; PWMj and PPGj pins may output pulses.
- Note 2: In the event counter mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the event counter mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGj is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 3, 4

8.3.7 16-Bit Pulse Width Modulation (PWM) Output Mode (TC3 and 4)

This mode is used to generate a pulse-width modulated (PWM) signals with up to 16 bits of resolution. The TimerCounter 3 and 4 are cascadable to form the 16-bit PWM signal generator.

The counter counts up using the internal clock or external clock.

When a match between the up-counter and the timer register (PWREG3, PWREG4) value is detected, the logic level output from the timer F/F4 is switched to the opposite state. The counter continues counting. The logic level output from the timer F/F4 is switched to the opposite state again by the counter overflow, and the counter is cleared. The INTTC4 interrupt is generated at this time.

Two machine cycles are required for the high- or low-level pulse input to the TC3 pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1 or IDLE1 mode.

Since the initial value can be set to the timer F/F4 by TC4CR<TFF4>, positive and negative pulses can be generated. Upon reset, the timer F/F4 is cleared to 0.

(The logic level output from the $\overline{PWM4}$ pin is the opposite to the timer F/F4 logic level.)

Since PWREG4 and 3 in the PWM mode are serially connected to the shift register, the values set to PWREG4 and 3 can be changed while the timer is running. The values set to PWREG4 and 3 during a run of the timer are shifted by the INTTCj interrupt request and loaded into PWREG4 and 3. While the timer is stopped, the values are shifted immediately after the programming of PWREG4 and 3. Set the lower byte (PWREG3) and upper byte (PWREG3) in this order to program PWREG4 and 3. (Programming only the lower or upper byte of the register should not be attempted.)

If executing the read instruction to PWREG4 and 3 during PWM output, the values set in the shift register is read, but not the values set in PWREG4 and 3. Therefore, after writing to the PWREG4 and 3, reading data of PWREG4 and 3 is previous value until INTTC4 is generated.

For the pin used for PWM output, the output latch of the I/O port must be set to 1.

Note 1: In the PWM mode, program the timer register PWREG4 and 3 immediately after the INTTC4 interrupt request is generated (normally in the INTTC4 interrupt service routine.) If the programming of PWREG and the interrupt request occur at the same time, an unstable value is shifted, that may result in generation of pulse different from the programmed value until the next INTTC4 interrupt request is generated.

Note 2: When the timer is stopped during PWM output, the PWM4 pin holds the output status when the timer is stopped. To change the output status, program TC4CR<TFF4> after the timer is stopped. Do not program TC4CR<TFF4> upon stopping of the timer. Example: Fixing the PWM4 pin to the high level when the TimerCounter is stopped

CLR (TC4CR).3: Stops the timer.

CLR (TC4CR).7 : Sets the $\overline{PWM4}$ pin to the high level.

Note 3: To enter the STOP mode, stop the timer and then enter the STOP mode. If the STOP mode is entered without stopping of the timer when fc or fc/2 is selected as the source clock, a pulse is output from the PWM4 pin during the warm-up period time after exiting the STOP mode.

Source Clock	Resolution	Repeated Cycle
NORMAL1, IDLE1 mode	fc = 2.5 MHz	fc = 2.5 MHz
fc/2 ¹¹	819 μs	53.69 s
fc/2 ⁷	51.2 μs	3.355 s
fc/2 ⁵	12.8 μs	0.839 ms
fc/2 ³	3.20 μs	0.210 ms
fc/2	800 ns	0.105 ms
fc	400 ns	52.43 ms

Table 8-6 16-Bit PWM Output Mode

Example :Generating a pulse with 6.4-ms high-level width and a period of 0.210 ms (fc = 2.5 MHz

		Setting ports	
L	_DW	(PWREG3), 07D0H	: Sets the pulse width.
L	_D	(TC3CR), 33H	: Sets the operating clock to $fc/2^3$, and 16-bit PWM output mode (lower byte).
L	_D	(TC4CR), 056H	: Sets TFF4 to the initial value 0, and 16-bit PWM signal generation mode (upper byte).
		(TC4CR), 05EH	: Starts the timer.
\sim		\checkmark	



Figure 8-7 16-Bit PWM Mode Timing Chart (TC3 and TC4)

8.3.8 16-Bit Programmable Pulse Generate (PPG) Output Mode (TC3 and 4)

This mode is used to generate pulses with up to 16-bits of resolution. The timer counter 3 and 4 are cascadable to enter the 16-bit PPG mode.

The counter counts up using the internal clock or external clock. When a match between the up-counter and the timer register (PWREG3, PWREG4) value is detected, the logic level output from the timer F/F4 is switched to the opposite state. The counter continues counting. The logic level output from the timer F/F4 is switched to the opposite state again when a match between the up-counter and the timer register (TTREG3, TTREG4) value is detected, and the counter is cleared. The INTTC4 interrupt is generated at this time.

Two machine cycles are required for the high- or low-level pulse input to the TC3 pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1 or IDLE1 mode.

Since the initial value can be set to the timer F/F4 by TC4CR<TFF4>, positive and negative pulses can be generated. Upon reset, the timer F/F4 is cleared to 0.

(The logic level output from the $\overline{PPG4}$ pin is the opposite to the timer F/F4.)

Set the lower byte and upper byte in this order to program the timer register. (TTREG3 \rightarrow TTREG4, PWREG3 \rightarrow PWREG4) (Programming only the upper or lower byte should not be attempted.)

For PPG output, set the output latch of the I/O port to 1.

Example :Generating a pulse with 6.4-ms high-level width and a period of 104.86 ms (fc = 2.5 MHz)

	Setting ports	
LDW	(PWREG3), 07D0H	: Sets the pulse width.
LDW	(TTREG3), 8002H	: Sets the cycle period.
LD	(TC3CR), 33H	: Sets the operating clock to fc/2 ³ , and16-bit PWM mode (lower byte).
LD	(TC4CR), 057H	: Sets TFF4 to the initial value 0, and 16-bit PWM mode (upper byte).
LD	(TC4CR), 05FH	: Starts the timer.

Note 1: In the PPG mode, do not change the PWREGi and TTREGi settings while the timer is running. Since PWREGi and TTREGi are not in the shift register configuration in the PPG mode, the new values programmed in PWREGI and TTREGi are in effect immediately after programming PWREGi and TTREGi. Therefore, if PWREGi and TTREGi are changed while the timer is running, an expected operation may not be obtained.

Note 2: When the timer is stopped during PPG output, the PPG4 pin holds the output status when the timer is stopped. To change the output status, program TC4CR<TFF4> after the timer is stopped. Do not change TC4CR<TFF4> upon stopping of the timer.

Example: Fixing the PPG4 pin to the high level when the TimerCounter is stopped

CLR (TC4CR).3: Stops the timer

CLR (TC4CR).7: Sets the PPG4 pin to the high level

Note 3: i = 3, 4



Figure 8-8 16-Bit PPG Mode Timing Chart (TC3 and TC40)

9. 8-Bit AD Converter (ADC)

The TMP86P203MG have a 8-bit successive approximation type AD converter.

Note: AD conversion characteristics are guaranteed with limited supply voltage range (4.5V to 5.5V).

If supply voltage is less than 4.5V then AD conversion accuracy can not be guaranteed.

9.1 Configuration

The circuit configuration of the 8-bit AD converter is shown in Figure 9-1.

It consists of control registers ADCCR1 and ADCCR2, converted value registers ADCDR1 and ADCDR2, a DA converter, a sample-and-hold circuit, a comparator, and a successive comparison circuit.



9.2 Control

The AD converter consists of the following four registers:

1. AD converter control register 1 (ADCCR1)

This register selects the analog channels in which to perform AD conversion and controls the AD converter as it starts operating.

2. AD converter control register 2 (ADCCR2)

This register selects the AD conversion time and controls the connection of the DA converter (ladder resistor network).

3. AD converted value register 1 (ADCDR1)

This register is used to store the digital value after being converted by the AD converter.

4. AD converted value register 2 (ADCDR2)

This register monitors the operating status of the AD converter.

AD Converter Control Register 1

ADCCR1	7	6	5	4	3	2 1 0	90	
(000EH)	ADRS	"0"	"1"	AINDS		SAIN	(Initial value: 0001 0000)	
						$\langle \rangle \rangle$		
	ADRS	ADRS AD conversion start 0: 1: Start						
	AINDS	Analog input control			0: 1:	Analog input enable Analog input disable	\bigcirc	
	SAIN	Analog input channel select		Î select	0000: 0001: 0010: 0010: 0100: 0101: 0100: 1011: 1000: 1011: 1000: 1011: 1000: 1011: 1100: 1111:	Reserved Reserved AIN2 AIN3 AIN4 AIN5 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved		R/W

Note 1: Select analog input when AD converter stops (ADCDR2<ADBF> = "0").

Note 2: When the analog input is all use disabling, the ADCCR1<AINDS> should be set to "1".

- Note 3: During conversion, do not perform output instruction to maintain a precision for all of the pins. And port near to analog input, do not input intense signaling of change.
- Note 4: The ADRS is automatically cleared to "0" after starting conversion.
- Note 5: Do not set ADCCR1<ADRS> newly again during AD conversion. Before setting ADCCR1<ADRS> newly again, check ADCDR2<EOCF> to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).
- Note 6: After STOP mode is started, AD converter control register 1 (ADCCR1) is all initialized and no data can be written in this register. Therefore, to use AD converter again, set the ADCCR1 newly after returning to NORMAL1 or NORMAL2 mode.
- Note 7: Although ADCCR1<SAIN> is initialized to "Reserved value" after reset, set the suitable analog input channel when using AD converter.
- Note 8: Always set bit 5 in ADCCR1 to "1" and set bit 6 in ADCCR1 to "0".

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AD Converter Control Register 2

ADCCR2	7	6	5	4	3	2	1	0		
(000FH)			IREFON	"1"		ACK		"0"	(Initial value: **0* 000*)	
	IREFON	DA con	verter (ladde	er resistor)	0:	Connec	ted only du	uring AD co	onversion	R/W
		connect	tion control		1:	Always	connected			
				000: 001: 010: 011:	Reserve Reserve 78/fc 156/fc	ed ed				
	ACK	AD con	version time	select	100: 101: 110: 111:	312/fc Reserve Reserve Reserve	ed ed ed			R/W

Note 1: Always set bit 0 in ADCCR2 to "0" and set bit 4 in ADCCR2 to "1".

Note 2: When a read instruction for ADCCR2, bit 6 to 7 in ADCCR2 read in as undefined data.

Note 3: After STOP mode is started, AD converter control register 2 (ADCCR2) is all initialized and no data can be written in this register. Therefore, to use AD converter again, set the ADCCR2 newly after returning to NORMAL1 or NORMAL2 mode.

 Table 9-1
 ACK Setting and Conversion Time

Conversion time	2.5 MHz	2 MHz
	Reserved	
	Reserved	(\mathcal{O})
78/fc	31.2 μs	39.0 μs
156/fc	62.4 μ s	78.0 μs
312/fc	124.8 μ s	156.0 μs
())	Reserved	
	Reserved	\sim
	Reserved	
	Conversion time 78/fc 156/fc 312/fc	Conversion time 2.5 MHz Reserved Reserved 78/fc 31.2 μs 156/fc 62.4 μs 312/fc 124.8 μs Reserved Reserved Reserved Reserved

Note 1: fc: High-frequency clock [Hz]

Note 2: Set conversion time by Supply Voltage(VDD) as follows.

- VDD = 4.5 to 5.5 V (15.6 µs or more)

AD Converted Value Register1

ADCDR1	7	6	5	4	3	2	1	0		
(0020H)	AD07	AD06	AD05	AD04	AD03	AD02	AD01	AD00	(Initial value: 0000 0000)	
AD Conve ADCDR2 (0021H)	erted Value	Regi 6	ster2 5 EOQF	4 ADBF	3	2	1	0	(Initial value: **00 ****)	
	EOCF	AD conversion end flag		0: Befo 1: Cor	0: Before or during conversion 1: Conversion completed				Read	
	ADBF	AD co	nversion b	usy flag	0: During stop of AD conversion 1: During AD conversion				only	

Note 1: The ADCDR2<EOCF> is cleared to "0" when reading the ADCDR1.

Therefore, the AD conversion result should be read to ADCDR2 more first than ADCDR1.

Note 2: ADCDR2<ADBF> is set to "1" when AD conversion starts and cleared to "0" when the AD conversion is finished. It also is cleared upon entering STOP mode.

Note 3: If a read instruction is executed for ADCDR2, read data of bits 7, 6 and 3 to 0 are unstable.

9.3 Function

9.3.1 AD Converter Operation

When ADCCR1<ADRS> is set to "1", AD conversion of the voltage at the analog input pin specified by ADCCR1<SAIN> is thereby started.

After completion of the AD conversion, the conversion result is stored in AD converted value registers (ADCDR1) and at the same time ADCDR2<EOCF> is set to "1", the AD conversion finished interrupt (INTADC) is generated.

ADCCR1<ADRS> is automatically cleared after AD conversion has started. Do not set ADCCR1<ADRS> newly again (restart) during AD conversion. Before setting ADRS newly again, check ADCDR<EOCF> to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).

-			75) .	
ADCCR1 <adrs></adrs>	AD conversion	start AD conversion	n start	
ADCDR2 <adbf></adbf>				
ADCDR1 status	Indeterminate	1st conversion result	2nd convers	sion result
ADCDR2 <eocf></eocf>	(OCF cleared by reading onversion result
INTADC interrupt	G			
Reading ADCDR1		Conversion result read		Conversion result read
		$\sim 0^{5}$	>	



9.3.2 AD Converter Operation

- 1. Set up the AD converter control register 1 (ADCCR1) as follows:
 - Choose the channel to AD convert using AD input channel select (SAIN).
 - Specify analog input enable for analog input control (AINDS).
 - Set up the AD converter control register 2 (ADCCR2) as follows:
 - Set the AD conversion time using AD conversion time (ACK). For details on how to set the conversion time, refer to Table 9-1.
 - Choose IREFON for DA converter control.
- 3. After setting up 1. and 2. above, set AD conversion start (ADRS) of AD converter control register 1 (ADCCR1) to "1".
- 4. After an elapse of the specified AD conversion time, the AD converted value is stored in AD converted value register 1 (ADCDR1) and the AD conversion finished flag (EOCF) of AD converted value register 2 (ADCDR2) is set to "1", upon which time AD conversion interrupt INTADC is generated.
- 5. EOCF is cleared to "0" by a read of the conversion result. However, if reconverted before a register read, although EOCF is cleared the previous conversion result is retained until the next conversion is completed.

Example :After selecting the conversion time of 124.8 µs at 2.5 MHz and the analog input channel AIN3 pin, perform AD conversion once. After checking EOCF, read the converted value and store the 8-bit data in address 009FH on RAM.

	; AIN SELECT		\sim
	:	:	; Before setting the AD converter register, set each port register
	:	:	suitably (For detail, see chapter of I/O port.)
	LD	(ADCCR1), 00100011B	; Select AIN3
	LD	(ADCCR2), 11011000B	; Select conversion time (312/fc) and operation mode
	:		
	SET	(ADCCR1). 7	; ADRS = 1 (Start AD conversion)
SLOOP:	TEST	(ADCDR2). 5	; EOCF = 1 ?
	JRS	T, SLOOP	
	:		$\mathcal{A}(\rightarrow)$
	LD	A, (ADCDR1)	Read conversion result
	LD	(9FH), A	$(\vee/)$ \diamond (\bigcirc)
		(

9.3.3 STOP Mode during AD Conversion

When the STOPmode is entered forcibly during AD conversion, the AD convert operation is suspended and the AD converter is initialized (ADCCR1 and ADCCR2 are initialized to initial value.). Also, the conversion result is indeterminate. (Conversion results up to the previous operation are cleared, so be sure to read the conversion results before entering STOPmode.) When restored from STOPmode, AD conversion is not automatically restarted, so it is necessary to restart AD conversion. Note that the DA converter (Ladder resistor) is automatically disconnect.

9.3.4 Analog Input Voltage and AD Conversion Result

The analog input voltage is corresponded to the 8-bit digital value converted by the AD as shown in Figure 9-3.



Figure 9-3 Analog Input Voltage and AD Conversion Result (typ.)

9.4 Precautions about AD Converter

9.4.1 Analog input pin voltage range

Make sure the analog input pins (AIN2 to AIN5) are used at voltages within VSS below VDD. If any voltage outside this range is applied to one of the analog input pins, the converted value on that pin becomes uncertain. The other analog input pins also are affected by that.

9.4.2 Analog input shared pins

The analog input pins (AIN2 to AIN5) are shared with input/output ports. When using any of the analog inputs to execute AD conversion, do not execute input/output instructions for all other ports. This is necessary to prevent the accuracy of AD conversion from degrading. Not only these analog input shared pins, some other pins may also be affected by noise arising from input/output to and from adjacent pins.

9.4.3 Noise countermeasure

The internal equivalent circuit of the analog input pins is shown in Figure 9-4. The higher the output impedance of the analog input source, more easily they are susceptible to noise. Therefore, make sure the output impedance of the signal source in your design is 5 k Ω or less. Toshiba also recommends attaching a capacitor external to the chip.



Figure 9-4 Analog Input Equivalent Circuit and Example of Input Pin Processing

10. OTP operation

10.1 Operating mode

The TMP86P203MG has MCU mode and PROM mode.

10.1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resistor).

10.1.1.1 Program Memory

The TMP86P203MG has 2K bytes built-in one-time-PROM (addresses F800 to FFFFH in the MCU mode, addresses 0000 to 07FFH in the PROM mode).



Note: The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

10.1.1.2 Data Memory

TMP86P203MG has a built-in 128 bytes Data memory (static RAM).

10.1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$ pin, TEST pin and other pins as shown in Table 10-1 and Figure 10-2. The programming and verification for the internal PROM is acheived by using a general-purpose PROM programmer with the adaptor socket.

Pin name (PROM mode)	I/O	Function	Pin name (MCU mode)
A16	Input	Program memory address input	XOUT
A15 to A8	Input	Program memory address input	P37 to P30
A7 to A0	Input	Program memory address input	P37 to P30
D7 to D0	Input/Output	Program memory data input/output	P37 to P30
CE	Input	Chip enable signal input	P00
ŌĒ	Input	Output enable signal input	P20
PGM	Input	Program mode signal input	P01
DIDS	Input	PROM mode control signal input	P12
VPP	Power supply	+12.75V/5V (Power supply of program)	TEST
VCC	Power supply	+6.25V/5V	VDD
GND	Power supply	ov	VSS
VCC	Input	Fix to "H" level in PROM mode	P11
RESET	Input	Fix to "L" level in PROM mode	RESET
CLK	Input	Input a clock from the outside	XIN

Table 10-1 Pin name in PROM mode

Note 1: The high-speed program mode can be used. The setting is different according to the type of PROM pro-grammer to use, refer to each description of PROM programmer. TMP86P203MG does not support the electric signature mode, apply the ROM type of PROM programmer

to TC571000D/AD.

Always set the adapter socket switch to the "N" side when using TOSHIBA's adaptor socket.



10.1.2.1 Programming Flowchart (High-speed program writing)



The high-speed programming mode is set by applying Vpp=12.75V (programming voltage) to the Vpp pin when the Vcc = 6.25 V. After the address and data are fixed, the data in the address is written by applying 0.1[msec] of low level program pulse to \overline{PGM} pin. Then verify if the data is written.

If the programmed data is incorrect, another 0.1[msec] pulse is applied to PGM pin. This programming procedure is repeated until correct data is read from the address (maximum of 25 times).

Subsequently, all data are programmed in all address. When all data were written, verfy all address under the condition Vcc=Vpp=5V.

10.1.2.2 Program Writing using a General-purpose PROM Programmer

(1) Recommended OTP adaptor

BM11704 for TMP86P203MG

(2) Setting of OTP adaptor

Set the switch (SW1) to "N" side.

- (3) Setting of PROM programmer
 - a. Set PROM type to TC571000D/AD.

Vpp: 12.75 V (high-speed program writing mode)

b. Data transmission (or Copy) (Note 1)

The PROM of TMP86P203MG is located on different address; it depends on operating mode: MCU mode and PROM mode. When you write the data of ROM for mask ROM products, the data shuold be transferred (or copied) from the address for MCU mode to that for PROM mode before writing operation is executed. For the applicable program areas of MCU mode and PROM mode are different, refer to TMP86P203MG" Figure 10-1 Program Memory Area ".

Example: In the block transfer (copy) mode, executed as below.

2KB ROM capacity : $0F800~0FFFFH \rightarrow 00000~007FFH$

c. Setting of the program address (Note 1)

Start address: 0000H

End address: 07FFH

(4) Writting

(5)

Write and verify according to the above procedure "Setting of PROM programmer".

Security bit

The TMP86P203MG has a security bit in PROM cell.

If the security bit is programmed to 0, the content of the PROM is disable to be read (FFH data) in PROM mode.

How to program the security bit

The difference from the programming procedures described in section 10.1.2.2 are follows.

1. Setting OTP adapter

Set the switch (SW1) to the "S" side.

2. Setting PROM programmer

i)Setting of programming address

The security bit is in bit 0 of address 1101H. Set the start address 1101H and the end address 1101H. Set the data FEH at the address 1101H.

- Note 1: For the setting method, refer to each description of PROM programmer. Make sure to set the data of address area that is not in use to FFH.
- Note 2: When setting MCU to the adaptor or when setting the adaptor to the PROM programmer, set the first pin of the adaptor and that of PROM programmer socket matched. If the first pin is conversely set, MCU or adaptor or programmer would be damaged.
- Note 3: The TMP86P203MG does not support the electric signature mode. If PROM programmer uses the signature, the device would be damaged because of applying voltage of 12±0.5V to pin 9(A9) of the address. Don't use the signature.
- Note 4: Do not alter the contents of register at 1101H after programming the security bit to 0.

11. Input/Output Circuitry

11.1 Control Pins



11.2 Input/Output Ports



Note: Input staturs on pins set for input mode are read in into the internal circuit. Therefore, when using the ports in a mixture of input and output modes, the contents of the output latches for the ports that are set for input mode may be rewritten by execution of bit manipulating instructions.

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12. Electrical Characteristics

12.1 Absolute Maximum Ratings

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

			(U)	√ _{SS} = 0 V)
Parameter	Symbol	Pins	Ratings	Unit
Supply voltage	V _{DD}		-0.3 to 6.5	
Program voltage	V _{PP}	TEST/V _{PP}	-0.3 to 13.0	
Input voltage	V _{IN}		–0.3 to V _{DD} + 0.3	V
Output voltage	V _{OUT}	(7/5)	-0.3 to V _{DD} + 0.3	
	I _{OUT1}	P0, P1, P3 port	-1.8	
Output current (Per 1 pin)	I _{OUT2}	P1, P2, P3 port	12	
	I _{OUT3}	P0 port	30	
	ΣI_{OUT1}	P0, P1, P3 port	-12	mA
Output current (Total)	ΣI_{OUT2}	P1, P2, P3 port	40	
	ΣI_{OUT3}	P0 port	60	
Power dissipation [Tenr - 95°C]	Pa	DIP	250	m\\/
		SOP	180	IIIVV
Soldering temperature (Time)	Tsld		260 (10 s)	
Storage temperature	Tstg		-55 to 150	°C
Operating temperature	Topr		-40 to 85	

12.2 Operating Condition

The Operating Conditions show the conditions under which the device be used in order for it to operate normally while maintaining its quality. If the device is used outside the range of Operating Conditions (power supply voltage, operating temperature range, or AC/DC rated values), it may operate erratically. Therefore, when designing your application equipment, always make sure its intended working conditions will not exceed the range of Operating Conditions.

				(V _{SS}	= 0 V, Topr = -4	0 to 85°C)
Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage			NORMAL1 mode			
	V _{DD}		IDLE0, 1 mode		5.5	V
			STOP mode) / 2.0		
Input high lovel	V _{IH1}	Except hysteresis input		V _{DD} × 0.70		
Input high level	V _{IH2}	Hysteresis input	$\langle \langle \rangle$	V _{DD} × 0.75	V DD	V
Input low level	V _{IL1}	Except hysteresis input		0	$V_{DD} \times 0.30$	v
	V _{IL2}	Hysteresis input		\diamond (\bigcirc)	$V_{DD} \times 0.25$	
Clock frequency	fc	XIN, XOUT	V _{DD} = 4.5 V to 5.5 V	0.4	2.5	MHz

Note: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

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12.3 DC Characteristics

					$(V_{SS} =$	0 V, Topr = -40	0 to 85°C)
Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis voltage	V _{HS}	Hysteresis input		- <	0.9	-	V
	I _{IN1}	TEST					
Input current	I _{IN2}	Sink open drain, Tri-state port	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V			±2	μΑ
	I _{IN3}	RESET, STOP	<	$\langle \langle \rangle \rangle$	$\langle \rangle$		
Input resistance	R _{IN}	RESET pull-up		100	220	450	kΩ
Output leakage current	I _{LO}	Sink open drain, Tri-state port	V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V	(-)	_	±2	μΑ
Output high voltage	V _{OH}	P0, P1, P3 port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	- (/	V
Output low voltage	V _{OL}	P1, P2, P3 port	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	_	-21	0.4	v
Output low current	I _{OL}	Middle current port (except XOUT, P0)	V _{DD} = 4.5 V, V _{OL} = 1.0 V	- 4	8		
Output low current	I _{OL}	High current port (P0 port)	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$		20)) -	
Supply current in NORMAL 1 mode			$V_{DD} = 5.5 V$	-(C	3.0	5.5	mA
Supply current in IDLE 0, 1 mode	I _{DD}		fc = 8.0 MHz		1.9	4.0	
Supply current in STOP mode		Å	$V_{DD} = 5.5 V$ $V_{IN} = 5.3 V/0.2 V$		0.5	10.0	μΑ

Note 1: Typical values show those at Topr = 25° C, V_{DD} = 5 V

Note 2: Input current (I_{IN1} , I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

12.4 AD Conversion Characteristics

$(v_{SS} = 0.0 v$	$v_{\rm DD} = 4.5 \ 10$	5.5 v, topt = -4	40 10 85°C)
Min	Тур.	Max	Unit

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog input voltage	V _{AIN}		V _{SS}	-	V _{DD}	V
Power supply current of analog reference voltage	IREF	V _{DD} = 5.5 V V _{SS} = 0.0 V	_	0.6	1.0	mA
Non linearity error			-	-	<u>+2</u>	
Zero point error		$V_{PP} = 5.0 \text{ V}$ $V_{PP} = 0.0 \text{ V}$	_	_	±2	I SB
Full scale error	() ()	100 - 0.0 V, VSS - 0.0 V	-	-	±2	LOD
Total error		/	-	-	±4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

- Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to section of "Control" of the chapter "8-bit AD Converter".
- Note 3: Please use input voltage to AIN input Pin in limit of V_{DD} to V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: The relevant pin for I_{REF} is V_{DD} , so that the current flowing into V_{DD} is the power supply current $I_{DD} + I_{REF}$.
- Note 5: AD conversion characteristics are guaranteed with limited supply voltage range 4.5 V to 5.5 V. If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

12.5 AC Characteristics

			(v _{SS} = 0 v	, v _{DD} = 4.5 to s	5.5 V, TOPT =	FO 10 05 C)
Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Machine cycle time	tcy	NORMAL1 mode	1.6		10	μs
		IDLE0, 1 mode				
High level clock pulse width	t _{WCH}	For external clock operation	000	$\left(\right)$	7	
Low level clock pulse width	t _{WCL}	fc = 8 MHz	200		_	ns

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = -40 to $85^\circ C$)

12.6 Recommended Oscillation Conditions







- Note 1: The oscillation characteristics shown in Figure 12-1 and Figure 12-2 above are those of a particular lot (sample) and are not guaranteed data. The target oscillation frequency should be obtained by adjusting the external capacitor capacitance (CXIN) and resistor value (Rx).
- Note 2: Even under the same external conditions (supply voltage, resistor value (Rx), capacitor capacitance (CXIN), temperature (°C)), variations in a lot (sample) may cause a maximum of plus or minus 15 % of fluctuations in the oscillation frequency (fc).

12.7 DC Characteristics, AC Characteristics (PROM mode)

12.7.1 Read operation in PROM mode



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12.7.2 Program operation (High-speed) (Topr = $25 \pm 5^{\circ}$ C)



- Note 3: Use the recommended adapter and mode.
 - Using other than the above condition may cause the trouble of the writting.

12.8 Handling Precaution

- The solderability test conditions for lead-free products (indicated by the suffix G in product name) are shown below.
 - 1. When using the Sn-37Pb solder bath
 - Solder bath temperature = $230 \,^{\circ}\text{C}$
 - Dipping time = 5 seconds
 - Number of times = once
 - R-type flux used
 - 2. When using the Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245 °C Dipping time = 5 seconds Number of times = once

R-type flux used

Note: The pass criteron of the above test is as follows:

- Solderability rate until forming ≥ 95 %
- When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

13. Package Dimensions



This is a technical document that describes the operating functions and electrical specifications of the 8-bit microcontroller series TLCS-870/C (LSI).

Toshiba provides a variety of development tools and basic software to enable efficient software development.

These development tools have specifications that support advances in microcomputer hardware (LSI) and can be used extensively. Both the hardware and software are supported continuously with version updates.

The recent advances in CMOS LSI production technology have been phenomenal and microcomputer systems for LSI design are constantly being improved. The products described in this document may also be revised in the future. Be sure to check the latest specifications before using.

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