TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT
TMP8243P/TMP8243PI
N-CHANNEL SILICON GATE MOS

INPUT/OUTPUT EXPANDER

GENERAL DESCRIPTION

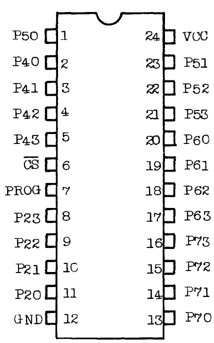
The TMP8243P is an input/output expander designed specifically to provide a low cost means of I/O expansion for the TLCS-84 family.

The I/O ports of the TMP8243P serve as a direct extension of the resident I/O facilities of the TLCS-84 microcomputers and are accessed by their own MOVD, ANLD, and ORLD instructions.

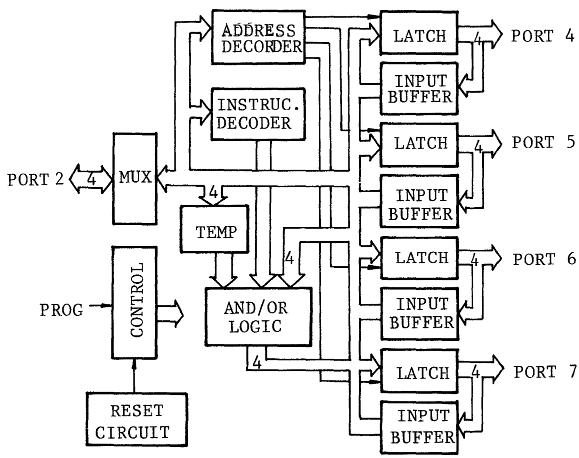
FEATURES

- o Low cost
- o Simple interface to TLCS-84 microcomputers
- o Four 4-bit I/O ports
- o AND and OR directly to ports
- o Single 5V supply
- o High output drive
- o Direct extension of resident TMP8048P/TMP8049P I/O ports.
- o Compatible with intel's 8243
- o -40°C to +85°C Operation (TMP8243PI: Industrial Specification)

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES AND PIN DESCRIPTION

PROG (Input)

Clock Input. A high to low transistion on PROG signifies that address and control are available on P20-23, and a low to high transition signifies that data is available on P20-23.

$\overline{\text{CS}}$ (Input)

Chip Select Input. A high on CS inhibits any change of output or internal status.

P20-23 (Input/Output, 3-state)

Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition contains the data for a selected output port if a write oepration, or the data from a selected port before the low to high transition if a read operation.

P40-43, P50-53, P60-63, P70-73 (Input/Output, 3-state)

Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a 3-state (after read). Data on pins P20-23 may be directly written, ANDed or ORed with previous data.

V_{CC} (Power)

+5 volt supply

GND (Power)

0 volt supply

FUNCTIONAL DESCRIPTION

General Operation

The TMP8243P contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports.

- o Transfer accumulator to port
- o Transfer port to accumulator
- o AND accumulator to port
- o OR accumulator to port

All communication between the TMP8048P and the TMP8243P occurs over Port 2 (P20-23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional TMP8243P'S may be added to the 4-bit bus and chip selected using additional output lines from the TMP8048P/8035P.

Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

Write Modes

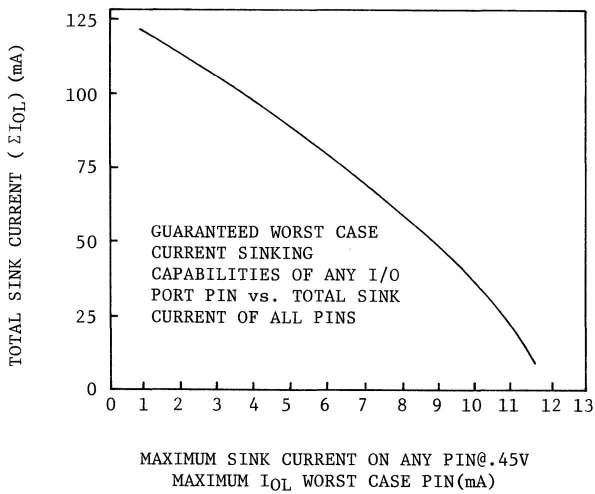
The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are 3-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the 3-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the TMP8243P output. A read of any port will leave that port in a high impedance state.



Sink Capability

The TMP8243P can sink 5 mA@.45V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA@.45V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA

εI_{OL} = 60 mA from curve

#pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 9 I/O lines of the TMP8243P.

Example: This examples shows now the use of the 20 mA sink capability of port 7 affects the sinking capability of the other I/O lines.

An TMP8243P will drive the following loads simultaneously.

2 loads - 20 mA@1V (port 7 only)

8 loads - 4 mA@.45V

6 loads - 3.2 mA@.45V

Is this within the specified limits?

εI_{OL} = (2 x 20) + (8 x 4) + (6 x 3.2) = 91.2 mA. From the curve: for I_{OL} = 4 mA, εI_{OL} = 93 mA since 91.2 mA < 93 mA the loads are within specified limits.

Although the 20 mA@1V load are used in calculating εI_{OL}, it is the largest current required @.45V which determines the maximum allowable εI_{OL}.

TMP8243P

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to GND	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to GND	-0.5V to +7.0V
V_{OUT}	Output Voltage with Respect to GND	-0.5V to +7.0V
P_D	Power Dissipation	800mW
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to +150°C
T_{OPR}	Operating Temperature	0°C to +70°C

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL1}	Output Low Voltage Ports 4-7	I_{OL} = 5mA*			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL} = 20mA			1	V
V_{OL3}	Output Low Voltage Port 2	I_{OL}=0.6mA			0.45	V
V_{OH1}	Output High Voltage Ports 4-7	I_{OH}=-240μA	2.4			V
V_{OH2}	Output High Voltage Port 2	I_{OH}=-100μA	2.4			
I_{IL1}	Input Leakage Port 4-7	0V≤V_{IN}≤V_{CC}	-10		20	μA
I_{IL2}	Input Leadage Port 2, $\overline{CS}$, PROG	0V≤V_{IN}≤V_{CC}	-10		10	μA
I_{CC}	V_{CC} Supply Current			10	20	mA
I_{OL}	Sum of all I_{OL} of 16 Outputs	5 mA Each Pin			80	mA

* See following graph for additional sink current capability

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_A	Code Valid Before PROG	C_L = 80pF	100			ns
t_B	Code Valid After PROG	C_L = 20pF	60			ns
t_C	Data Valid Before PROG	C_L = 80pF	200			ns
t_D	Data Valid After PROG	C_L = 20pF	20			ns
t_H	Floating After PROG	C_L = 20pF	0		150	ns
t_K	PROG Negative Pulse Width		700			ns
t_{CS}	$\overline{CS}$ Valid Before/After PROG		50			ns
t_{PO}	Ports 4-7 Valid After PROG	C_L = 100pF			700	ns
t_{LP1}	Ports 4-7 Valid Before/After PROG		100			ns
t_{ACC}	Port 2 Valid After PROG	C_L = 80pF			650	ns

TMP8243PI : INDUSTRIAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	V_{CC} Supply Voltage with Respect to GND	-0.5V to +7.0V
V_{IN}	Input Voltage with Respect to GND	-0.5V to +7.0V
V_{OUT}	Output Voltage with Respect to GND	-0.5V to +7.0V
P_D	Power Dissipation	800mW
T_{SOLDER}	Soldering Temperature (Soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	-55°C to +150°C
T_{OPR}	Operating Temperature	-40°C to +85°C

D.C. CHARACTERISTICS TA=-40°C to 85°C, V_{CC}=5V±10%

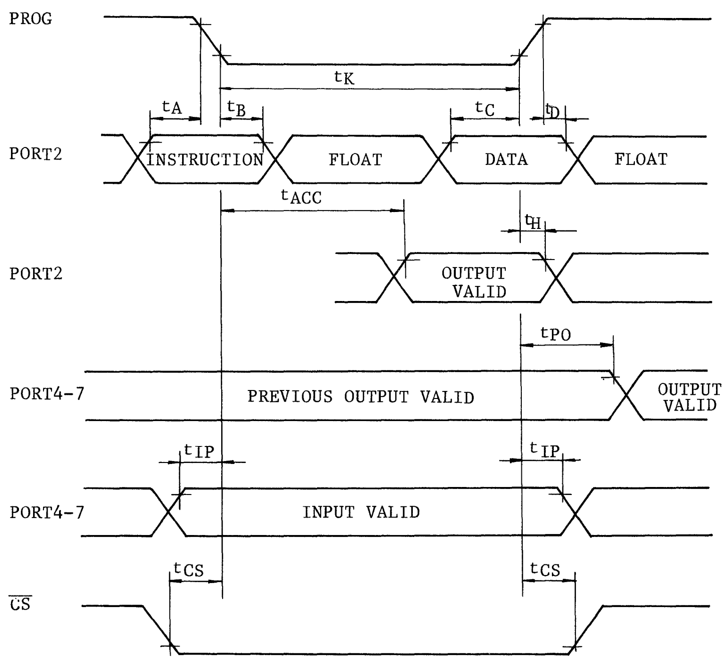
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+0.5	V
V_{OL1}	Outptu Low Voltage Ports 4-7	I_{OL}=4.5mA			0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL}=20mA			1	V
V_{OL3}	Output Low Voltage Port 2	I_{OL}=0.6mA			0.45	V
V_{OH1}	Output High Voltage Ports 4-7	I_{OH}=-240μA	2.4			V
V_{OH2}	Output High Voltage Port 2	I_{OH}=-100μA	2.4			
I_{IL1}	Input Leakage Ports 4-7	$0V \le V_{IN} \le V_{CC}$	-10		20	μA
I_{IL2}	Input Leakage Port 2, $\overline{CS}$,PROG	$0V \le V_{IN} \le V_{CC}$	-10		10	μA
I_{CC}	V_{CC} Supply Current			10	20	mA
I_{OL}	Sum of all I_{OL} of 16 outputs	4.5mA each pin			72	mA

* See following graph for additional sink current capability

A.C. CHARACTERISTICS TA=-40°C to 85°C, V_{CC}=5V±10%

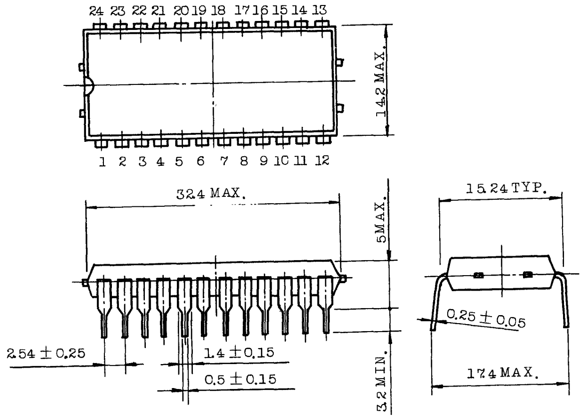
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_A	Code Valid before PROG	C_L = 80pF	100			ns
t_B	Code Valid after PROG	C_L = 20pF	60			ns
t_C	Data Valid before PROG	C_L = 80pF	200			ns
t_D	Data Valid after PROG	C_L = 20pF	20			ns
t_H	Floating after PROG	C_L = 20pF	0		150	ns
t_K	PROG Negative Pulse Width		700			ns
t_{CS}	$\overline{CS}$ Valid before/after PROG		50			ns
t_{PO}	Ports 4-7 Valid after PROG	C_L = 100pF			700	ns
t_{LP1}	Ports 4-7 Valid before/after PROG		100			ns
t_{ACC}	Port 2 Valid after PROG	C_L = 80pF			650	ns

TIMING WAVEFORM



OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.