CMOS 8-BIT SINGLE-CHIP MICROCOMPUTER (TLCS-48C)

TMP80C50AP/TMP80C50AP-6
TMP80C40AP/TMP80C40AP-6
TMP80C50AU/TMP80C50AU-6

1. GENERAL DESCRIPTION AND FEATURES

The TMP80C50A is a single chip microcomputer fabricated in Silicon Gate CMOS technology which provides internal 8-bit parallel architecture.
The following basic architectural functions of a computer have been included in a single chip; an 8-bit CPU, 256×8 RAM data memory, 4K×8 ROM program memory, 27 I/O lines and an 8-bit timer/event counter.

The TMP80C50A is particularly efficient as a controller. It has extensive bit handling capability as well as facilities for both binary and BCD arithmetic.

The TMP80C40A/-6 is the equivalent of a TMP80C50A/-6 without ROM program memory on chip. By using this device with external EPROM or RAM, software debugging becomes easy.

The TMP80C50AP/-6 and TMP80C40AP/-6 are in a standard Dual Inline Package.

The TMP80C50AU/-6 is in a 44-pin Micro Flat Package.

FEATURES

- TMP80C50AP/TMP80C40AP/TMP80C50AU
  1.36μs Instruction Cycle Time −40°C to 85°C, 5V ± 10%
- TMP80C50AP-6/TMP80C40AP-6/TMP80C50AU-6
  2.5μs Instruction Cycle Time −40°C to 85°C, 5V ± 20%
- Software Upward Compatible with TMP8049AP/INTEL's 8049.
- 4K×8 masked ROM / 256×8 RAM
- Low Power
  10mA MAX. in Normal Operation (V_{CC}=5V, f_{XTAL}=6MHz)
  10μA MAX. in Power Down Mode (V_{CC}=5V, f_{XTAL} : DC)
- Power Down Mode (Stand-by Mode)
- Halt Mode (Idle Mode)

MCU48-53

2. PIN CONNECTIONS AND PIN FUNCTIONS

2.1 Pin Connections (Top View)

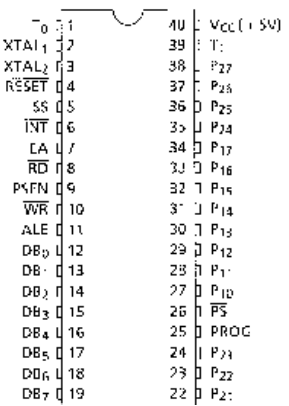


Figure 2-1 (1) DIP Pin Connections

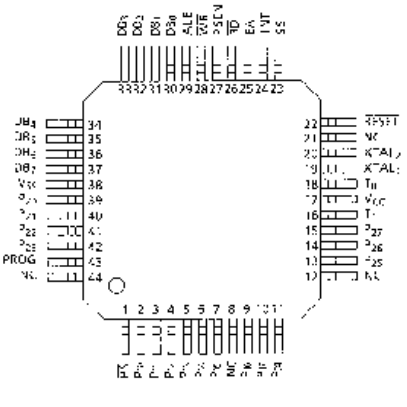


Figure 2-1 (2) Micro Flat Package Pin Connections

2.2 Pin Names And Pin Descript on

- V_{SS} (Power Supply)

  Circuit GND potential

- V_{CC} (Power Supply)

  +5V during, operation

- $\overline{PS}$ (Input)

  The control signal for the power saving at the power down mode (Active Low)

- PROG (Output)

  Output strobe for the TMP82C43P I/O expander.

- P_{10}-P_{17} (Input/Output) Port1

  8-bit quasi-bidirectional port (Internal Pullup=50KΩ).

- P_{20}-P_{27} (Input/Output) Port2

  8-bit quasi-bidirectional port (Internal Pullup=50KΩ).
  P_{20}-P_{25} contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for the TMP82C43P.

- DB_0-DB_7 (Input/Output, Tri-State)

  True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$.
  Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.

- T_0 (Input/Output)

  Input pin testable using the conditional transfer instructions JT0 and JNT0. T_0 can be designated as a clock output using ENT0 CLK instruction.

- T_1 (Input)

  Input pin testable using the JT1 and JNT1 instruction. Can be designated the event counter input using the STRT CNT instruction.

- $\overline{INT}$ (Input)

  External interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

- $\overline{RD}$ (Output)

  Output strobe activated during a Bus read. Can be used to enable data onto the Bus from an external device. Used as a Read Strobe to External Data Memory (Active Low).

- $\overline{WR}$ (Output)

Output strobe during a Bus write (Active Low). Used as a Write Strobe to External Data Memory.

- $\overline{\text{RESET}}$ (Input)

  Active Low signal which is used to initialize the Processor. Also used during the power down mode.

- ALE (Output)

  Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.

- $\overline{\text{PSEN}}$ (Output)

  Program Store Enable. This output occurs only during a fetch to external program memory (Active Low).

- $\overline{\text{SS}}$ (Input)

  Single step input can be used in conjunction with ALE to "single step" processor through each instruction when $\overline{\text{SS}}$ is low the CPU is placed into a wait state after it has completed the instruction being executed. Also used during the power down mode.

- EA (Input)

  External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug and essential for testing and program verification. (Active High)

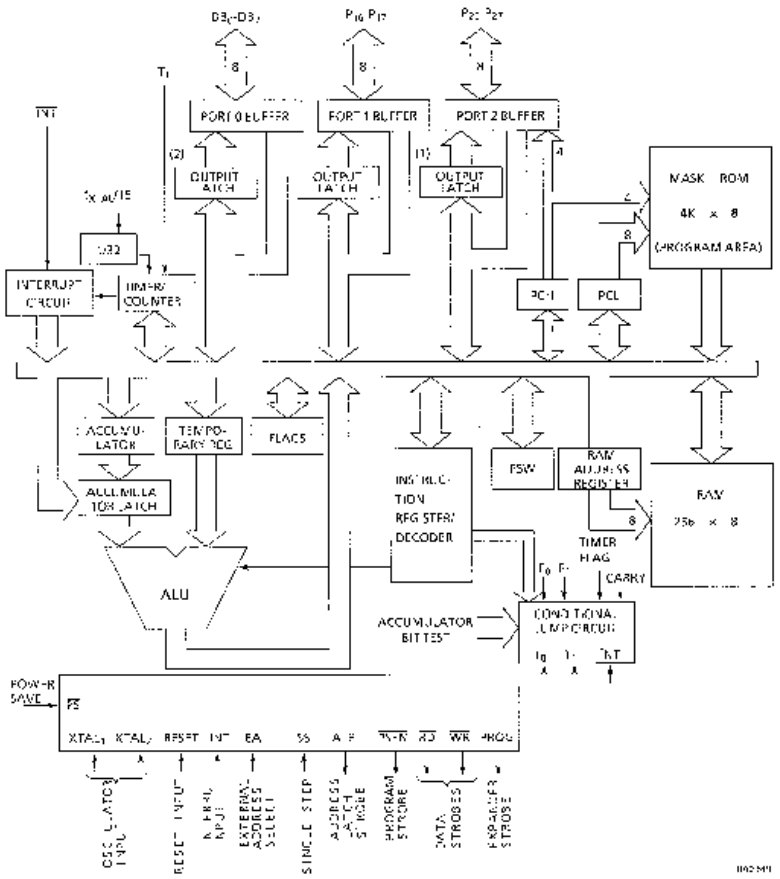
- $XTAL_1$ (Input)

  One side of crystal input for internal oscillator. Also input for external source.

- $XTAL_2$ (Input)

  Other side of crystal input.

2.3 Block Diagram



Note 1 : The lower order 4 bit of port 2 output latch are used also for input/output operations with the I/O expander.

Note 2 : The output latch of port 0 is also used for address output.

Figure 2.3 Block Diagram

Plik z chomika:

datasheets

Inne pliki z tego folderu:

MAB80xx (Philips).pdf (1461 KB)
MSM80Cxx (OKI Semiconductor).pdf (144 KB)
TMP80C35, TMP80C48 (Toshiba).pdf (1073 KB)
TMP80C39, TMP80C49 (Toshiba).pdf (1074 KB)
TMP80C40, TMP80C50 (Toshiba).pdf (1081 KB)

Inne foldery tego chomika:

51 family
arm family
avr family
pic family
st6 family