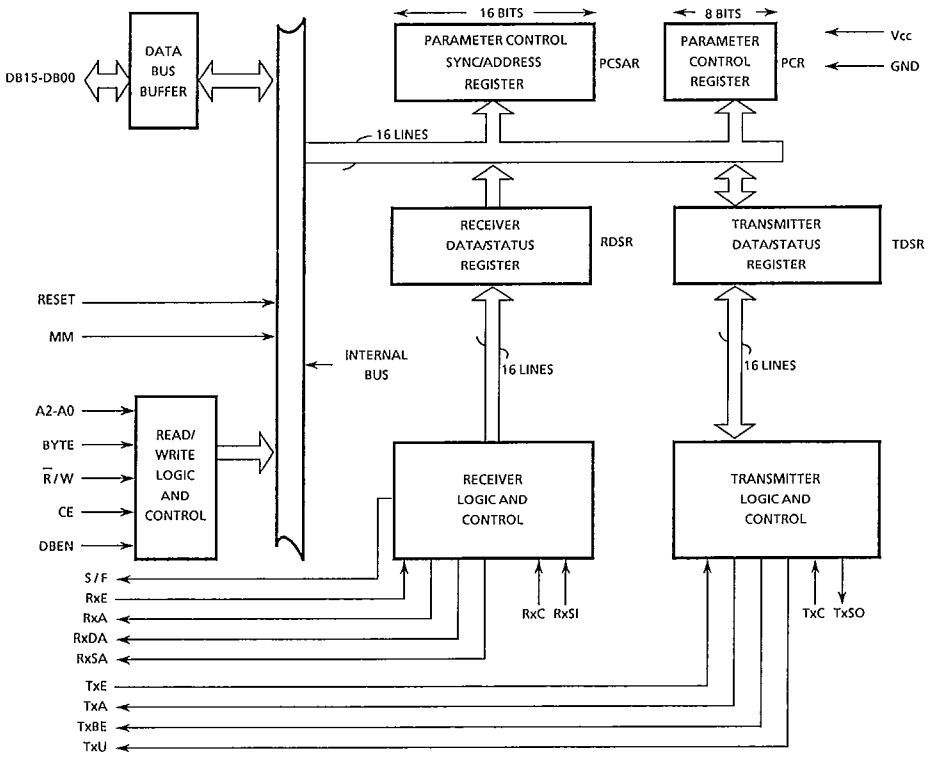
1. INTRODUCTION

The TMP68652 MPCC formats, transmits, and receives synchronous serial data while supporting bit-oriented protocols (BOP) or byte-control protocols (BCP). The parallel bus of the MPCC readily interfaces with the 6800 and TLCS-68000 Microprocessor Families as well as many other 8- or 16-bit processors. Typical applications include intelligent terminals, front-end communications, remote-data concentrators, communication test equipment, and computer-to-computer links.

- DC to 2 Mbps Data Rate
- Bit-Oriented Protocols (BOP) : SCLC, ADCCP, HDLC, X.25
  - Character Length — 1-to-8-bits
  - Address Comparison
  - Automatic Detection and Generation of Special Control Characters, i.e., FLAG, ABORT, GA
  - Automatic Zero Insertion and Deletion
  - Short Last Character
  - Idle Transmission of FLAG or ABORT Characters
- Byte-Control Protcols (BCP), DDCMP, BISYNC (External CRC)
  - Character Length — 5-to-8-bits
  - SYNC Generation Detection and Stripping
  - Automatic Generation and Checking of CRC-16 or VRC
- Maintenance Mode for Self-Checking
- Bidirectional, Three-State, 8 or 16-bit Data Bus
- TTL Compatible

BLOCK DIAGRAM



2. SIGNAL DESCRIPTION

The following paragraphs provide a brief description of the input and output signals.

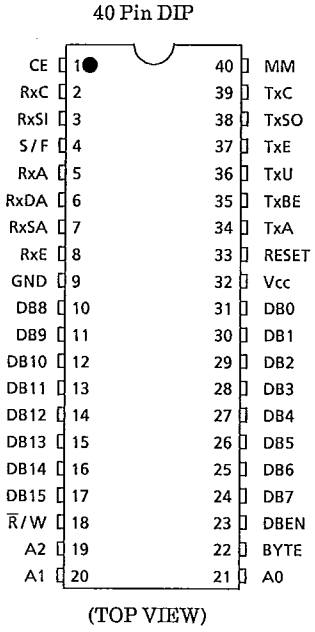


Figure 2.1 Pin Assignments

Note : The terms assertion and negation are used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term negate or negation is used to indicate that a signal is inactive or false.

2.1 DATA BUS (DB0~DB15)

These bidirectional three-state data lines transfer data, control, and status information between the CPU and the MPCC. The DB0~DB7 signal lines contain data while the DB8~DB15 signal lines contain control and status information. Corresponding bits of the high and low order bytes can be wire-ORed onto an 8-bit bus. These lines are three-stated if either chip enable (CE) or data bus enable (DBEN) are negated.

2.2 ADDRESS BUS (A0~A2)

These inputs select the internal register being addressed. The four 16-bit registers can be addressed on a word or byte basis. Accesses of the four addressable registers can be either word accesses (16-bit data transfers) or byte accesses (8-bit data transfers) depending upon the state of BYTE.

2.3 BYTE

Single byte (8-bits) data bus transfers are specified when this input is asserted. When negated, word (16-bits) data bus transfers are specified.

2.4 CHIP ENABLE (CE)

This active-high input permits a data bus operation when asserted.

2.5 READ/WRITE ($\overline{R}$/W)

This input signal controls the direction of data bus transfer. A high level on this pin indicates the transfer of data from the data bus to the addressed register. A low level on the pin indicates the transfer of data from the addressed register to the data bus.

2.6 DATA BUS ENABLE (DBEN)

The active-high input signal should be asserted after A0~A2, CE, BYTE and $\overline{R}$/W are valid. During a read, the three-stated data bus (DB) is enabled with information from the addressed register. During a write, the data appearing on the data bus is loaded into the addressed register and transmitter buffer empty (TxBE) will be negated if the transmit data/status register (TDSR) was addressed.

2.7 RESET

This active-high input, when asserted, initializes all internal registers (to zero) and timing.

2.8 MAINTENANCE MODE (MM)

This active-high input signal, when asserted, internally gates the transmitter serial output (TxSO) to the receiver serial input (RxSI) and the transmitter clock input (TxC) to the receiver clock input (RxC), thus placing the MPCC in a maintenamce mode (for off-line diagnostic purposes). When in this mode, the RxC and RxSI inputs are ignored and the TxSO output is held in the mark (high) state.

2.9 RECEIVER ENABLE (RxE)

This active-high input, when asserted, permits the processing of RxSI data. When negated, receiver logic is disabled and all receiver registers and timing are intialized.

2.10 RECEIVER ENABLE (RxA)

This active-high output signal is asserted when the first data character of a message is ready for the processor. In the BOP mode, this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC parameter control sync/address register (PCSAR bit 13) is set, the first non-SYNC character is the first data character ; if strip-SYNC is the first data character. In the BOP mode, the closing FLAG negates RxA. In the BCP mode, RxA is negated by the negation of RxE.

2.11 RECEIVER DATA AVAILABLE (RxDA)

This active-high output signal is asserted when an assembled character is in the receive data/status register ($RDSR_L$) and is ready to be presented to the processor. RxDA is negated when $RDSR_L$ is read. Note that RxDA is a possible interrupt signal.

2.12 RECEIVER CLOCK (RxC)

The RxC (1×) input provides timing for logic. The positive going edge shifts serial data into the receiver shift register (RxSR) from the receiver serial input (RxSI).

2.13 SYNC/FLAG (S/F)

This active-high output signal is asserted when a SYNC or FLAG character has been detected. This signal is negated one RxC clock cycle later.

2.14 RECEIVER STATUS AVAILABLE (RxSA)

This active-high output signal is asserted when there is a zero-to-one trnasition of any bit in $RDSR_H$ except for the receiver start of message (RSOM) bit. It is negated when $RDSR_H$ is read. Note that RxSA is a possible interrupt signal.

2.15 RECEIVER SERIAL INPUT (RxSI)

This input signal is the received serial data (mark = 1, space = 0).

2.16 TRANSMITTER ENABLE (TxE)

This active-high input signal, when asserted, enables the transmitter data path between the transmit data/status register (TDSR) and the transmitter serial output pin (TxSO). When negated, TxSO is driven to the mark (high) state and the tranmitter active output pin (TxA) is negated after the closing FLAG (BOP) or last character (TCP) is sent out the TxSO pin.

2.17 TRANSMITTER ACTIVE (TxA)

This active-high output signal is asserted after TSOM (TSDR bit 8) is set and TxE is asserted. TxA is negated when TxE is negated and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.

2.18 TRANSMITTER BUFFER EMPTY (TxBE)

This active-high output signal is asserted when TDSR is ready to be loaded with new control information or data. TxBE is negated when new control information or data is loaded into TDSR. Note that TxBE is a possible interrupt signal.

2.19 TRANSMITTER UNDERRUN (TxU)

This active-high output signal is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the trnasmitter. Line fill depends on bit 11 of PCSAR. TxU is negated by asserting RESET or setting TSOM (TDSR bit 8), followed by the falling edge of TxC. Note that TxU is a possible interrupt signal.

2.20 TRANSMITTER CLOCK (TxC)

TxC (1×) provides timing for the taransmitter logic. The positive going edge of this input shifts data out of the TxSR to TxSO.

2.21 TRANSMITTER SERIAL OUTPUT (TxSO)

This output is the transmitted serial data (mark = 1, space = 0).

2.22 Vcc AND GND

Power is supplied to the MPCC using these pins. V_{CC} is the +5 volt power supply and GND is the 0 volt reference ground.

3. FUNCTIONAL DESCRIPTION

The MPCC can be functionally paritioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. Table 3.1 provides a description of the registers, Table 3.2 outlines the error control, and Table 3.3 highlights the special characters found in the MPCC.

The register bit formats are shown in Figure 3.1 while the receiver and transmitter data paths are depicted in Figures 3.2 and 3.3.

Table 3.1 Register Description

Registers		No. of Bits	Description*
• Addressable			
PCSAR	Parameter Control Sync/Address Register	16 8	$PSCAR_H$ and PCR contain parameters common to the receiver and transmitter. $PCSAR_L$ contains a programmable SYNC character (BCP) or secondary station address (BOP).
PCR	Parameter Control Register		
RDSR	Receive Data/Status Register	16	$RDSR_H$ contains receiver status information. $RDSR_L$ = RxDB contains the received assembled character.
TDSR	Transmit Data/Status Register	16	$TDSR_H$ contains transmitter command and status information. $TDSR_L$ = TxDB contains the character to be transmitted.
• Internal			
CCSR	Control Character Shift Register	8	These registers are used for character assembly (CCSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding Shift Register	16	
RxSR	Receiver Shift Register	8	
TxSR	Transmitter Shift Register	8	
RxCRC	Receiver CRC Accumulation Register	16	
TxCRC	Transmitter CRC Generation Register	16	

* H = High Byte (Bits 8~15)
L = Low Byte (Bits 0~7)

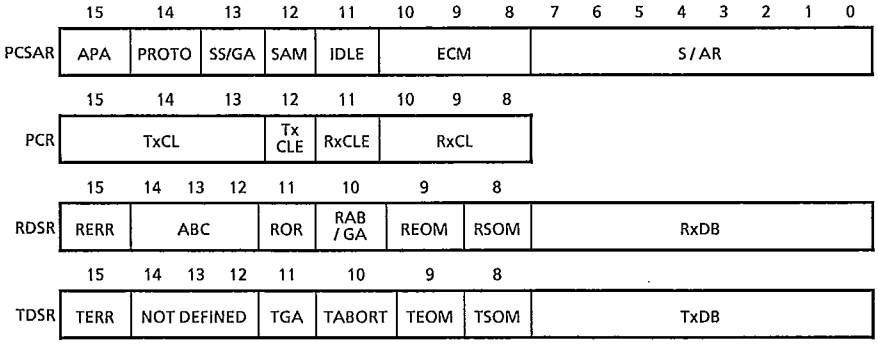
Table 3.2 Error Control

Character	Description
FCS	Frame Check Sequence is transmitted/received as 16 bits following the last data character of a BOP message. The divisor is usually CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) with dividend preset to 1s but can be otherwise determined by ECM. The inverted remainder is transmitted as the FCS.
BCC	Block Check Character is transmitted/received as two successive characters following the last data character of a BCP message. The polynomial is CRC-16 ($X^{16} + X^{15} + X^2 + 1$) or CRC-CCITT with dividend preset to 0s (as specified by ECM). The true remainder is transmitted as the BCC.

Table 3.3 Special Characters

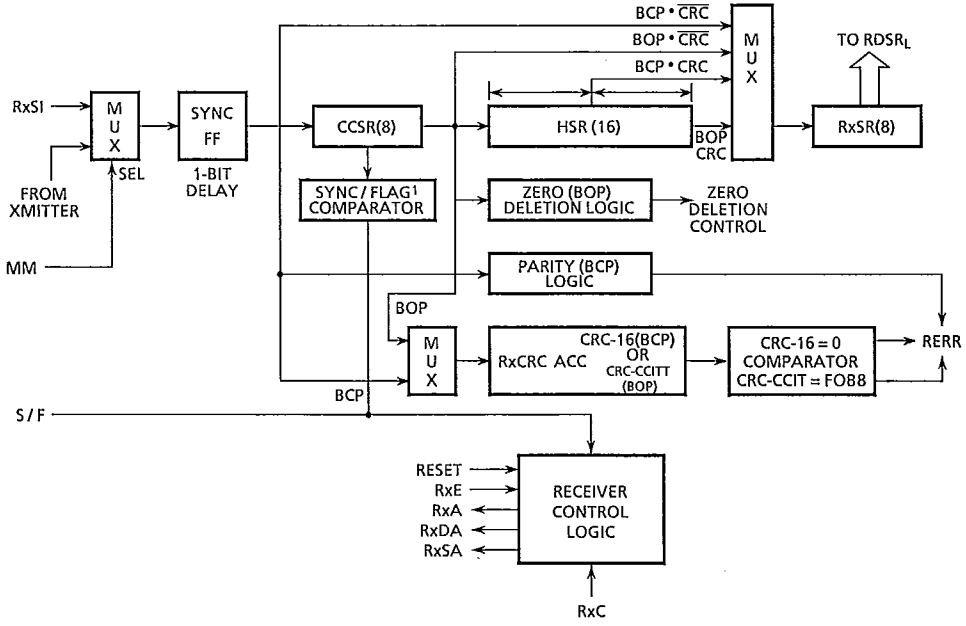
Operation	Bit Pattern	Function
• BOP		
FLAG	01111110	Frame Message
ABORT	1111111 Generation 01111111 Detection	Terminate Communication
GA	01111111	Terminate Loop Mode Repeater Function
Address	($PCSAR_L$)[1]	Secondary Station Address
• BCP		
SYNC	($PCSAR_L$) or (TXDB)[2] Generation	Character Syncronization

Note 1 : (δ) refers to contents of δ.
2 : For IDLE = 0 or 1 respectively.



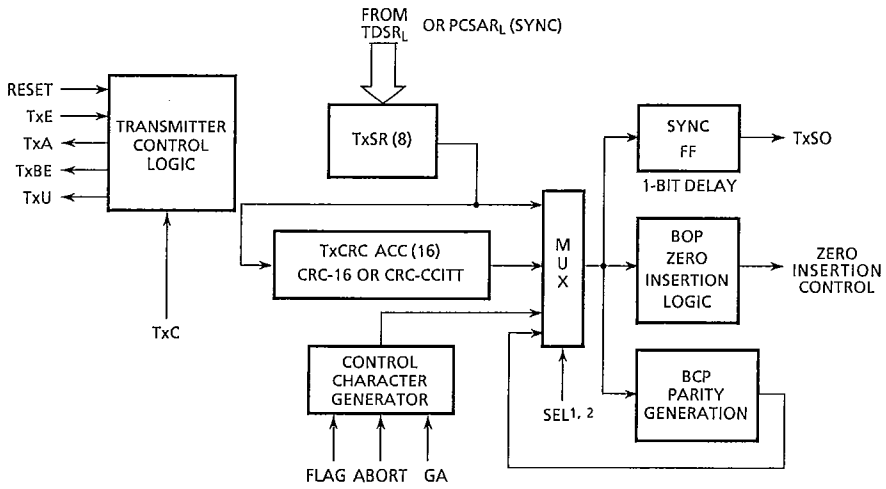
Note : Refer to Table 3.1 for mnemonics and description.

Figure 3.1 Short Form Register Bit Formats



Note 1 : Detected in SYNC FF and 7 MS bits of CCSR.
2 : In BOP mode, a minimum of two data characters must be received to activate the receiver.

Figure 3.2 MPCC Receiver Data Path



Note 1 : TxCRC is selected if TEOM = 1 and the last data character has been shifted out of TxSR.
2 : In BCP, parity selected will be generated after each character is shifted out of TxSR.

Figure 3.3 MPCC Transmitter Data Path

3.1 RECEIVER OPERATION

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be asserted to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit control character shift register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) characters is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit holding shift register (HSR) is enabled. The receiver then operates as described in the following paragraphs.

3.1.1 BOP Mode

A flowchart of receiver operation in BOP mode appears in Figure 3.4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through CCSR, HSR, and into RxSR. A character will be assembled in the RxSR and transferred to the RDSR$_L$ for presentation to the processor. At that time the RxDA output well be asserted and the processor must take the character no later than one RxC time after the next character is assembled in the RxSR. If not, an overrun (RSDR bit 11 = 1) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If MPCC is a secondary station (PCSAR bit 12=1), the contents of RxSR are compared with the address stored in $PCSAR_L$. A match indicates the forthcoming message intended for the station ; the RxA output is asserted, the character is loaded into $RDSR_L$, RxDA is asserted, and the receive start of message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

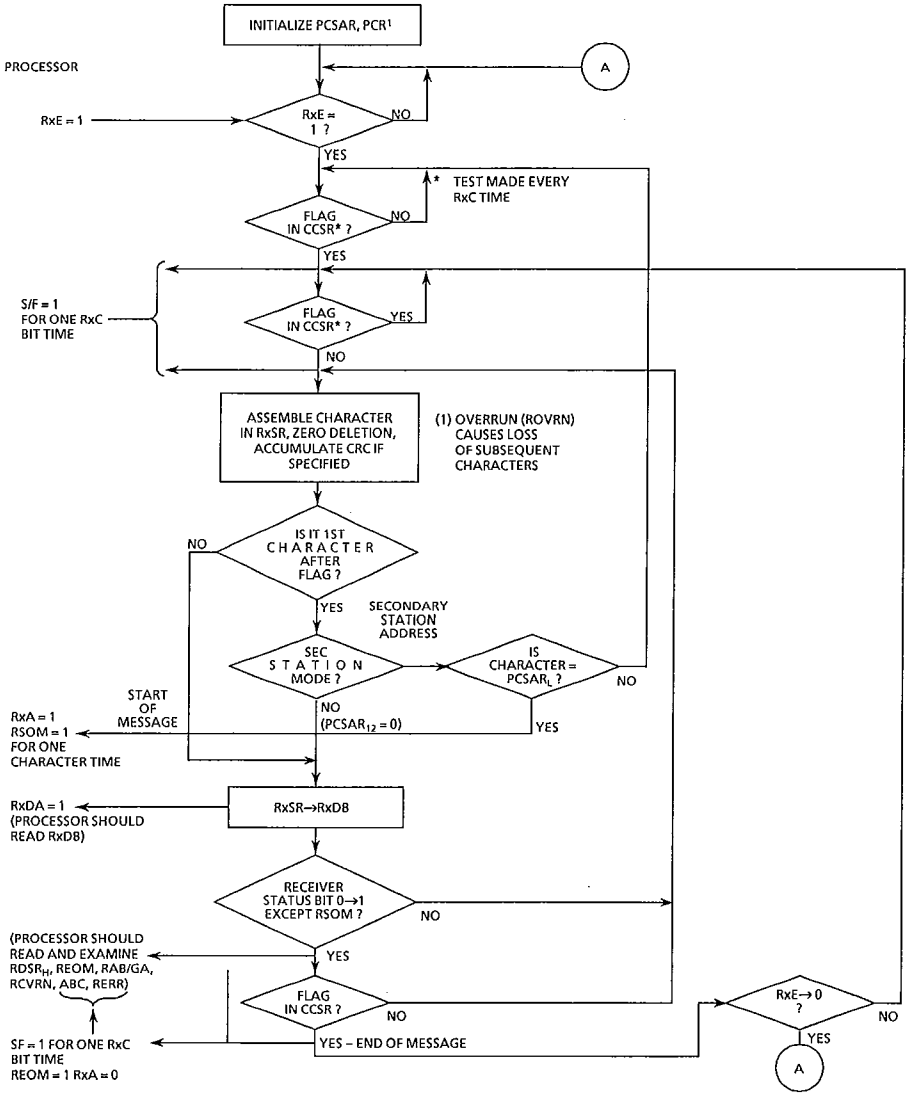
If the MPCC is a primary station (PCSAR bit 12=0), no secondary address check is made ; RxA is asserted and RSOM is set once the first non-FLAG character has been loaded into $FDSR_L$ and RxDA has been asserted. Extended address field can be supported by software if $PCSAR_{12}=0$.

When the eight bits following the address character have been loaded into $RDSR_L$ and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the control field.

Received serial data that follows is read and interpreted as the information field by the processor. It will be assembled into character lengths as specified by PCR bits 8~10. As before, RxDA is asserted each time a character has been transferred into $RDSR_L$ and is negated when $RDSR_L$ is read by the processor. $RDSR_H$ should only be read when RxSA is asserted. This occurs on a zero-to-one trnasition of any bit in $RDSR_H$ except for RSOM. RxSA and all bits in $RDSR_H$ except RSOM are cleared when $RDSR_H$ is read. The processor should check RDSR bits 9~15 each time RxSA is asserted. If RDSR bit 9 is set, then RDSR bits 12~15 should be examined.

Receiver character length may be changed dynamically in response to RxDA ; read the character in RxDB and write the new character length into RxCL. The character length will be changed on the next receiver character boundary. A received residual (short) character will be transferred into RxDB after the previous character in RxDB has been read, i.e., there will not be an overrun. In general the last two characters are protected from underrun.

The CRC-CCITT, if specified by PCSAR bits 8~10 is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is the 16-bit HSR. At that time, the receive end of message bit (REOM) will be set ; RxSA and RxDA will be asserted. The processor should read the last data character in $RDSR_L$ and the receiver status in RDSR bits 9~15. If RSDR bit 15 equals one, there has been a transmission error ; the accumulated CRC-CCITT is incorrect. If RDSR bits 12~15 equal zero, the received CRC nor closing FLAG are presented to the processor. The processor may negate RxE or leave it asserted at the end of the received message.



Note : RxE must be negated during initialization of PCSAR and PCR.

Figure 3.4 BOP Receiver Flowchart

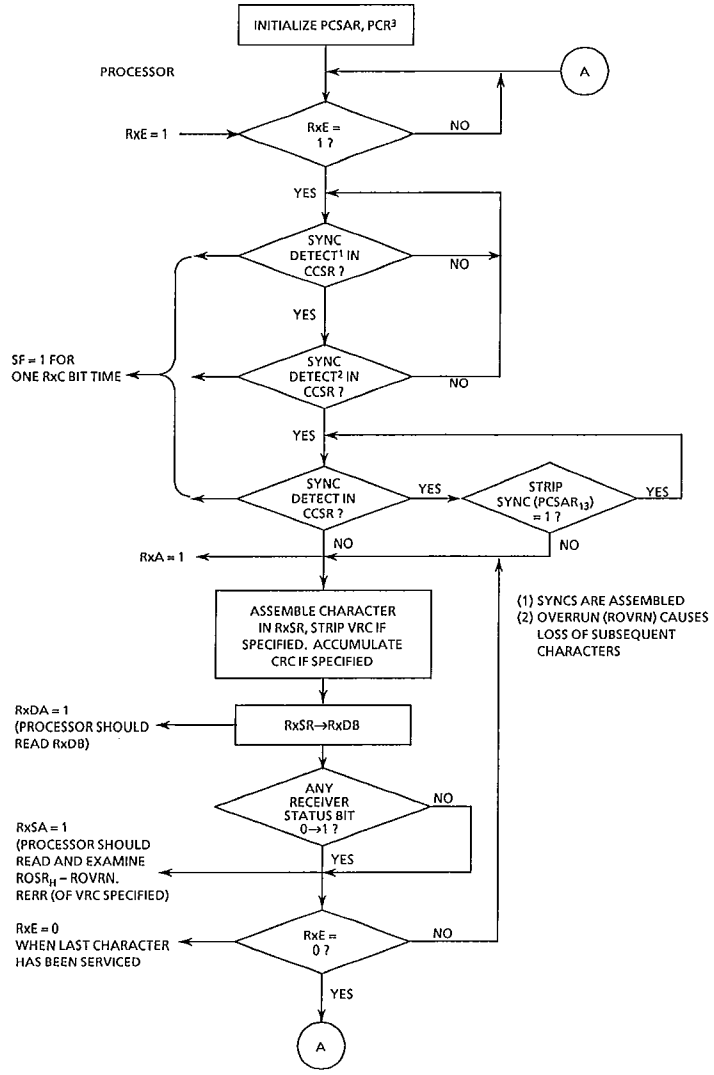
3.1.2 BCP Mode

The operation of the receiver in BCP mode is shown in Figure 3.5. The receiver initially searches for two successive SYNC characters, of length specified by PCR bits 8~10, that match the contents of $PCSAR_L$. The next non-SYNC character or next SYNC character, if stripping is not specified (PCSAR bit 13=0), causes RxA to be asserted, and enables the receiver data path. Once enabled, all characters are assembled in RxSR and loaded in $RDSR_L$. RxDA is asserted when a character is available in $RDSR_L$. RxSA is asserted on a zero-to-one transition of any bit in $RDSR_H$. The signals are negated when $RDSR_L$ or $RDSR_H$ are read respectively.

If CRC-16 error control is specified by PCSAR bits 8~10, the processor must determine the last character received prior to the CRC field. When that character is loaded into $RDSR_L$ and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a trnasmission error, the processor must read the receiver status ($RDSR_H$) and examine RDSR bit 15. This bit will be set for one character time if an error-free message has been received. If RDSR bit 15 equals zero, the CRC-16 is in error. The state of RDSR bit 15 in BCP CRC mode does not assert RxSA. Note that this bit should be examined only at the end of a message. The accumulated CRC will include all characters starting with the first non-SYNC character if PCSAR bit 13 equals one, or the character after the opening two SYNC's if PCSAR bit 13 equals zero. This necessitates external CRC generation/checking when supporting IBM's BISYNC. This can be accomplished using the MC68653 polynomial generator/checker.

If VRC had been selected for error control, parity (odd or even) is regenerated on each character and checked when the parity bit is received. A discrepancy causes RDSR bit 15 to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor.

When the processor has read the last character of the message, it should negate RxE which disables the receiver logic and initializes all receiver registers and timing.



Note 1 : Test made every RxC time.
2 : Test made on Rx character boundary.
3 : RxE must be negated during initialization of PCSAR and PCR.

Figure 3.5 BCP Receiver Flowchart

3.2 TRANSMITTER OPERATION

After the parameter control registers (PCSAR and PCR) have been initialized, TxSO is held at mark until transmit start of message (TSOM) (TDSR bit 8) is set and TxE is asserted. Then, transmitter operation depends on protocol mode.

3.2.1 BOP Mode

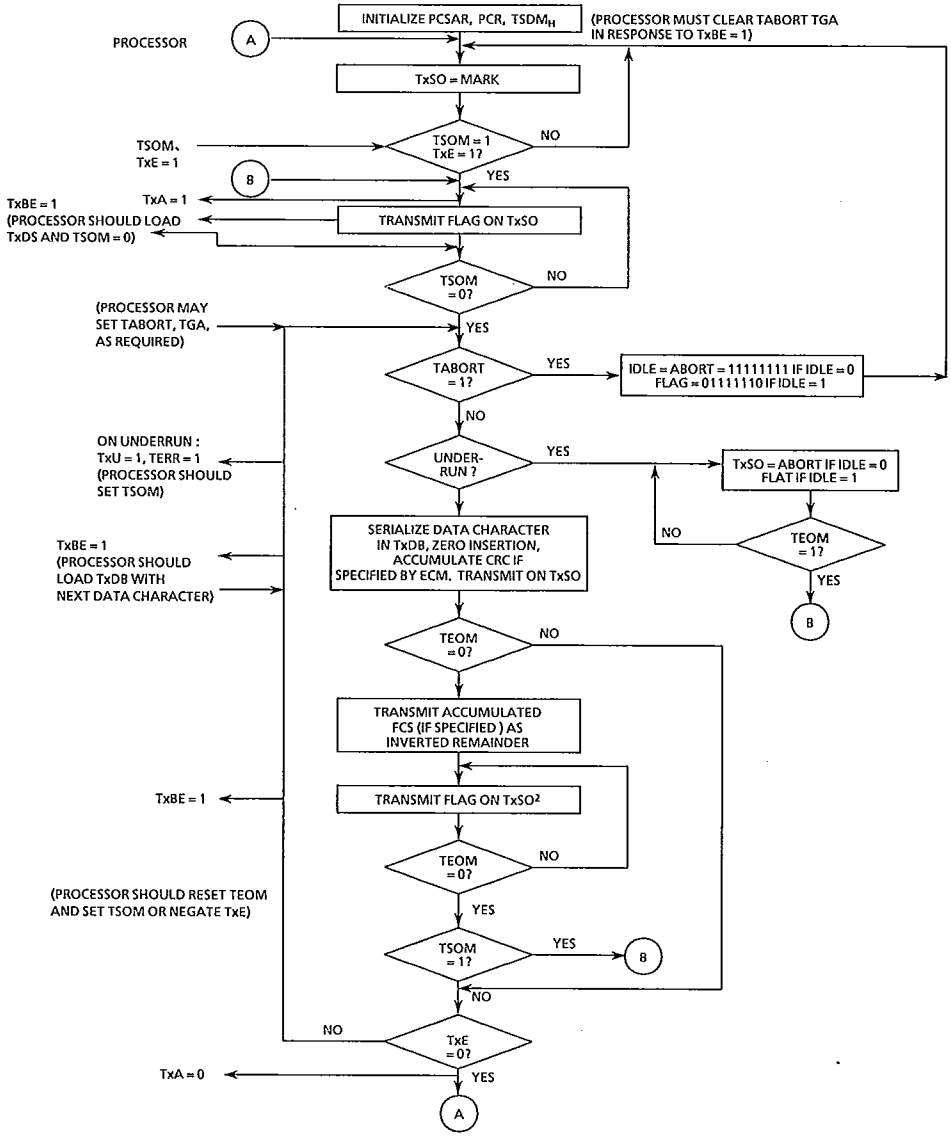
Transmitter operation for BOP mode is shown in Figure 3.6. A FLAG is sent after the processor sets the transmit start of message bit (TSOM) and asserts TxE. The FLAG is used to synchronize the message that follows. TxA will also be asserted. When TxBE is asserted by the MPCC, the processor should load $TDSR_L$ with the first character of the message. TSOM should be cleared at the same time $TDSR_L$ is loaded (16-bit data bus) or immediately thereafter (8-bit data bus), FLAGs are sent as long as TSOM equals one. For counting the number of FLAGs, the processor should set TSOM in response to the assertion of TxBE.

All succeeding characters are loaded into $TDSR_L$ by the processor when TxBE equals one. Each character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a zero into the serial bit stream after five successive ones are sent. This ensures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is terminated, the frame check sequence (FCS) is generated as specified by error control mode (PCSAR bits 8~10). The FCS should be the CRC-CCITT polynomial ($X^{16}+X^{12}+X^5+1$) preset to ones. If an underrun occurs (processor is not keeping up with the transmitter), TxU and transmitter error (TERR) (TDSR bit 15) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE (PCSAR bit 11). The processor must set TSOM to reset the underrun condition. To retransmit the message, the processor should proceed with the normal start of message sequence.

A residual character of one to seven bits may be transmitted at the end of the information field. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence. The character length will be changed on the next transmit character boundary.

After the last data character has been loaded into $TDSR_L$ and sent to TxSR (TxBE=1), the processor should set TEOM (TDSR bit 9). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and negate TxE when the next TxBE has been negated, TxA will be negated one and one-half bit times after the first bit of the closing FLAG has been transmitted. TxSO will marked after the closing FLAG has been transmitted.

If TxE is asserted and TEOM is high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading $TDSR_L$ with a data character and then simply resetting TEOM (without setting TSOM).



Note 1 : TxE must be negated during initialization of PCSAR and PCR.
2 : GA will be transmitted if TGA is set together with TEOM.

Figure 3.6 BOP Transmitter Flowchart

3.2.2 BCP Operation

Transmitter operation for BCP mode is shown in Figure 3.7. TxA will be asserted after TSOM=1 and TxE is asserted. At that time SYNC characters are sent from $PCSAR_L$ or $TDSR_L$ (IDLE=0 or 1) as long as TSOM=1. TxBE is asserted at the start of transmission of the first SYNC character. For counting the number of SYNC's, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM=0 transmission is from $TDSR_L$, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the TxSO line fill depends on IDLE (PCSAR bit 11). The processor must set TSOM and retransmit the message to recover. This is not compatible with IBM's BISYNC, so that the user must not underrun when IBM's BISYNC, so that the user must not underrun when supporting that protocol.

CRC-16, if specified by PCSAR bits 8~10, is generated on each character transmitted from $TDSR_L$ when TSOM=0. The processor must set to TEOM=1 after the last data character has been set to TxSR (TxBE=1). The MPCC will finish transmitting the last data character and the CRC-16 transmission, the processor should clear TEOM and negate TxE when the TxBE corresponding to the start of CRC-16 transmission, the processor should clear TEOM and negate TxE when the TxBE corresponding to the start of CRC-16 transmission is asserted. When TEOM=0, the line is marked and a new message may be initiated by setting TSOM and asserting TxE.

If VRC is specified, it is generated on each data character and the data character length must not exceed seven bits. For software LRC or CRC, TEOM should be set only if SYNC's are required at the end of the message block.

3.2.3 Special Case

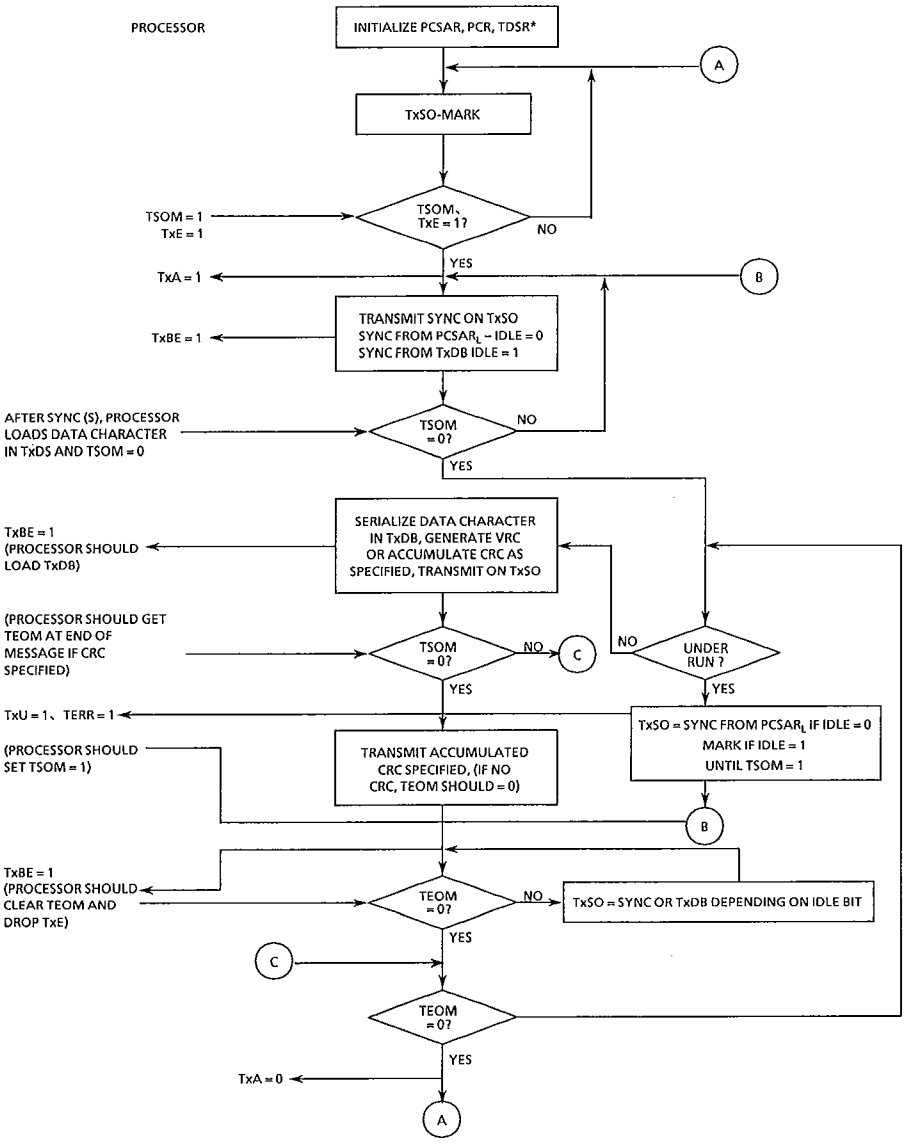
The capability to transmit 16 spaces is provided for line turnaround in half-duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE is asserted, and proceeding as required.

3.3 PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCM must be loaded with control information from the processor. The contents of these registers will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is desabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS=CRC-CCITT preset to ones.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be eight bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character.



* TxE must be asserted during initialization of PCSAR and PCR.

Figure 3.7 BCP Transmit Flowchart

3.4 DATA BUS CONTROL

The processor must set up the MPCC register address (A0~A2), chip enable (CE), byte select (BYTE), and read/write ($\overline{R}/W$) inputs before each data bus transfer operation.

During a read operation ($\overline{R}/W = 0$), the asserting edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE is asserted, the 8-bit byte is placed on DB8~DB15 or DB0~DB7 depending on the H/L status of the register addressed. Unused bits in $RDSR_L$ are zero. If BYTE is negated, all 16-bits (DB0~DB15) contain MPCC information. The negating edge of DBEN will negate RxDA and/or RxSA if $RDSR_L$ or $RDSR_H$ is addressed respectively. Refer to Table 3.4.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation ($\overline{R}/W = 1$), the data must be stable on DB15~DB8 and/or DB7~DB0 prior to the asserting edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be negated if the addressed register was $TDSR_H$ or $TDSR_L$.

Tables 3.5, 3.6, 3.7 and 3.8 describe the functions of the parameter control register, the parameter control SYNC/address register, the transmit data/status register, and the receiver data/status register, respectively.

Table 3.4 MPCC Register Addressing

	A2	A1	A0	Register
BYTE = 0	16-BIT DATA BUS = DB_{15}~DB_{00}			
	0	0	X	PDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
BYTE = 1	8-BIT DATA BUS = $DB_{7\sim0}$ or $DB_{15\sim8}$**			
	0	0	0	$PDSR_L$
	0	0	1	$PDSL_H$
	0	1	0	$TDSR_L$
	0	1	1	$TDSR_H$
	1	0	0	$PCSAR_L$
	1	0	1	$PCSAR_H$
	1	1	0	PCR_L *
	1	1	1	PCR_H

* PCR lower byte does not exist. It will be all "0" s when read.

** Corresponding high and low order pins must be tied together.

Table 3.5 Parameter Control Register (PCR) - ($\overline{R}$/W)

Bit	Name	Mode	Function
00~07	Not Defined		
08~10	RxCL	BOP/BCP	Receiver character length is loaded by the processor when RxCLE = 0. The character length is valid after transmission of single byte address and control fields have been received. 10 9 8 — Character Length (Bits) 0 0 0 — 8 0 0 1 — 1 0 1 0 — 2 0 1 1 — 3 1 0 0 — 4 1 0 1 — 5 1 1 0 — 6 1 1 1 — 7
11	RxCLE	BOP/BCP	Reaceiver character length enable should be zero when the processor loads RxCL. The remaining bits of PCR are not afffected during loading. Always 0 when read.
12	TxCLE	BOP/BCP	Transmitter character length enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
13~15	TxCL	BOP/BCP	Transmitter character length is loaded by the processor when TxCLE = 0. Character bit length specification format is identical to RxCL. It is valid after transmission of single byte address and control fields.

Table 3.6 Parameter Control SYNC/Address Register (PCSAR) ($\overline{R}$/W)

Bit	Name	Mode	Function
00~07	S/AR	BOP	SYNC Register. Contains the secondary station address if the MPCC is a secondary station. The contents of this reagister is compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.
08~10	ECM	BOP/BCP	Error Control Mode — 10 9 8 — Suggested Mode — Character Length CRC-CCITT present ot 1's — 0 0 0 — BOP — 1-8 CRC-CCITT present to 0's — 0 0 1 — BCP — 8 Not used — 0 1 0 — – CRC-16 present to 0's — 0 1 1 — BCP — 8 VRC odd — 1 0 0 — BCP — 5-7 VRC even — 1 0 1 — BCP — 5-7 Not used — 1 1 0 — – No error control — 1 1 1 — BCP/BOP — 5-8 ECM should be loaded by the processor during initialization or when both data paths are idle.
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1. IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1.
		BCP	IDLE = 0, transmit initial SYNC characters and underrun line fill characters from the S/AR. IDLE = 1, transmit initial SYNC characters from TxDB and marks TxSO during underrun.
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.
13	SS/GA		Strip SYNC/Go Ahead. Operation depends on mode.
		BOP	SS/GA = 1 is used for loop mode only and enables GA detection. When a GA is detected as a closing character, REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 is the normal mode which enables ABORT detection. It causes the receiver to terminate the frame upon detection of and ABORT or FLAG.
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.
14	PROTO		Determines MPCC Protocol mode
		BOP	PROTO = 0
		BCP	PROTO = 1
15	APA	BOP	All Parties Address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.

Table 3.7 Transmit Data/Status Register (TDSR)($\overline{R}$/W except TDSR Bit 15)

Bit	Name	Mode	Function
00~07	TxDB	BOP/BCP	Transmit Data Buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM	BOP	Transmitter Start of Message. Set by the processor to initiate message transmission provided TxE = 1. TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation (if specified) begins. FCS, as specified by $PCSAR_{8-10}$, should be CRC-CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.
09	TEOM	BOP	Transmit End of Message. Used to terminate a transmitted message. TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0 ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC-16 to be transmitted (if selected) followed by SYNCs from $PCSAR_L$ or TxDB (IDLE = 0 or1). Clearing TEOM prior to the end of CRC-16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC-16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter Abort = 1 will causes ABORT or FLAG to be sent (IDLE = 0 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit Go Ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12~14	Not Defined		
15	TERR	(Read Only)	Transmitter Error = 1 indicates the TxDB has not been loaded in time (one character time – 1/2 TxC period after TxBE is asserted) to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. See timing diagram.
		BOP	ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1)
		BCP	SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 3.8 Receiver Data/Status Register (RDSR) (Read Only)

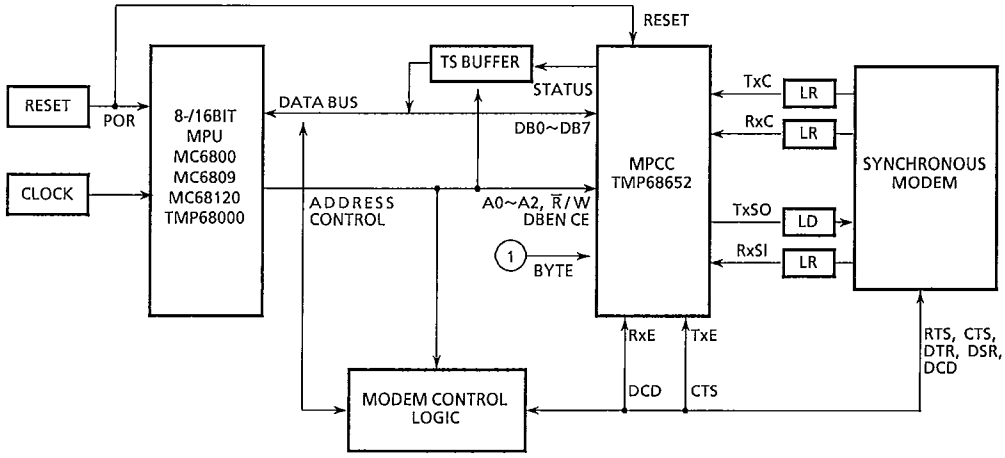
Bit	Name	Mode	Function
00~07	RxDB	BOP/BCP	Receiver Data Buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver Start of Message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station address if SAM = 1 RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no effect on RxSA.
09	REOM	BOP	Receiver End of Message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received REOM is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading $RDSR_H$, reset operation, or dropping of RxE. A received ABORT does not set RxDA.
11	ROR	BOP/BCP	Receiver Overrun = 1 indicates the processor has not read last character in the RxDB within one character time + 1/2 RxC period after RxDA is asserted. Subsequent characters will be lost. ROR is cleared on reading $RDSR_H$, reset operation, on dropping of RxE.
12~14	ABC	BOP	Assembled Bit Count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1 (RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a FLAG or GA) on a character boundary as specified by PCR_{8-10}. Otherwise, ABC = number of bits in the last data character. ABC is cleared when $RDSR_H$ is read, reset operation, or dropping RxE. The residual character is right justified in $RDSR_L$.
15	RERR	BOP/BCP	Receiver Error indicator should be examined by the processor when REOM = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC-CCITT preset to 1's/-0's as specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ FOB8 ≠ 0) RERR = 0 indicates FCS received correctly (CRC = FOB8/ = 0) CRC-16 preset to 0's on 8-bit data characters specified by $PSCAR_{8-10}$ RERR = 1 indicates CRC-16 received correctly (CRC = 0). RERR = 0 indicates CRC-16 error (CRC ≠ 0). VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VCR error RERR = 0 indicates VRC is correct.

4. TMP68000-TO-TMP68652 INTERFACE CIRCUIT

The TMP68000-to-TMP68652 interface circuit is shown in Figure 4.1. It will generate the DBEN select signal required by the TMP68652 multiple protocol communications controller (MPCC) and the $\overline{\text{DTACK}}$ signal required by the TMP68000. This allows the MPCC to interface with the TMP68000's asynchronous bus.

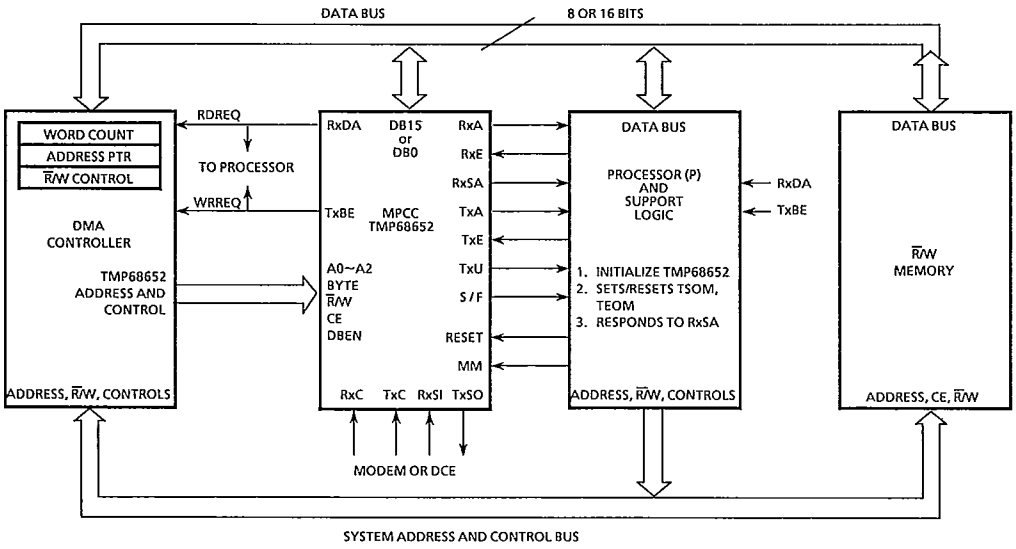
The MPCC has a 16-bit data bus (D0-D15), three register select signals (A0, A1, and A2), a chip enable (CE), and a read/write signal ($\overline{\text{R}}$/W). The data bus is connected directly to the MPU data bus and the register seleclts are connected to the A1 and A2 address lines of the processor. A0 of the MPCC is generated from $\overline{\text{LDS}}$. Together $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ determine the width of the transfer on the data bus. If $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ are both asserted, the BYTE input is negated and a word is transferred; otherwise the byte input is asserted, indicating byte transfers. The MPU's $\overline{\text{R}}$/W line is inverted and connected to the $\overline{\text{R}}$/W pin of the MPCC. Since DBEN controls all data transfers and operations internal to the MPCC, CE is held asserted and DBEN is used as the chip select.

An access begins when $\overline{\text{AS}}$ is asserted by the MPU, indicating a valid address on the address bus. $\overline{\text{UDS}}$ and/or $\overline{\text{LDS}}$ are then asserted, enabling flip-flop U2 to assert DBEN on the next rising edge of the system clock. The one clock cycle delay between $\overline{\text{SELECT}}$ and DBEN allows the MPCC setup time to be met. $\overline{\text{DTACK}}$ is then asserted on the next rising edge, forcing the processor to insert four wait states. This guarantees that the MPCC access time is met. At the end of the cycle, $\overline{\text{AS}}$ and th data strobes are negated, causing DBEN to be negated. The timing for a MPU write cycle is shown in Figure 4.2.



Note 1 : Possible MPU interrupt requests are : RxDA, RxSA, TxBE, and TxU.
2 : Other TMP68652 status signals and possible uses are :
S/F line : idle indicator, frame delimiter.
RxA handshake on RxE, line turn around control
TxA handshake on TxE, line turn around control.
3 : Line drivers/receivers (LD/LR) convert EIA to TTL voltages and vice versa.
4 : RTS should be cleared after the CRC (BCP) or FLAG (BOP) has been transmitted. This forces CTS low and TxE low.
5 : Corresponding high and low order bits of DB must be OR tied.

Figure 4.1 TMP68652 MPCC Microprocessor Interface



Note : For non-DMA operation, TxBE and RxDA are sent to the processor which then loads or reads data characters as required.

Figure 4.2 DMA/Processor Interface

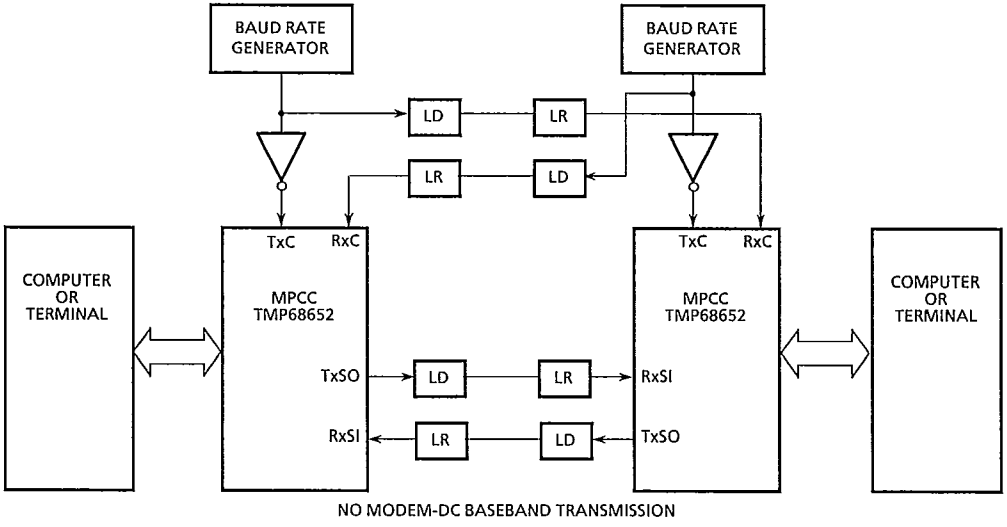


Figure 4.3 Channel Interface

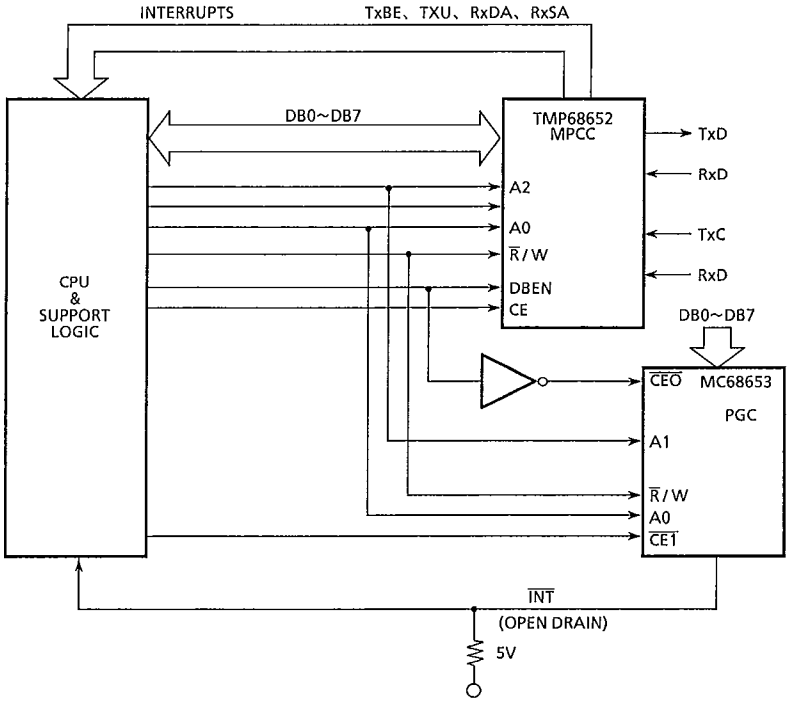


Figure 4.4 TMP68652 Interface Typical Protocols : BISYNC, DDCMP, SDLC, HDLC

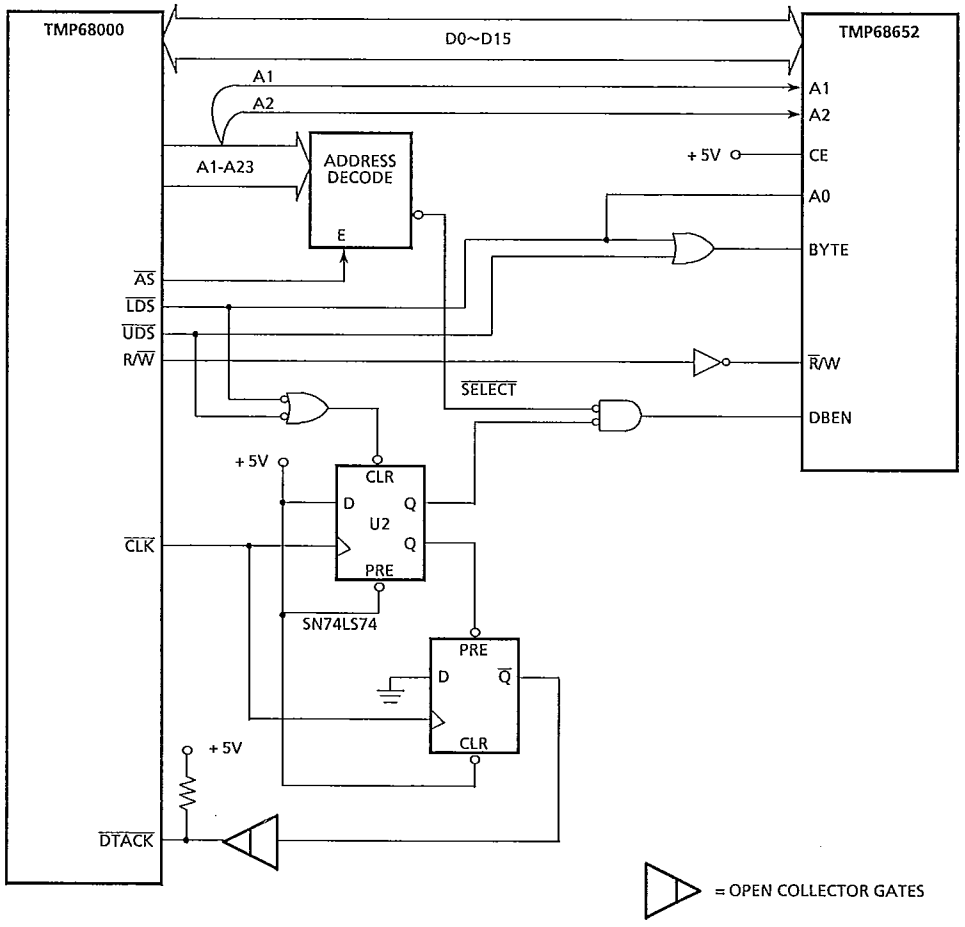


Figure 4.5 TMP68000/TMP68652 Interface Circuit

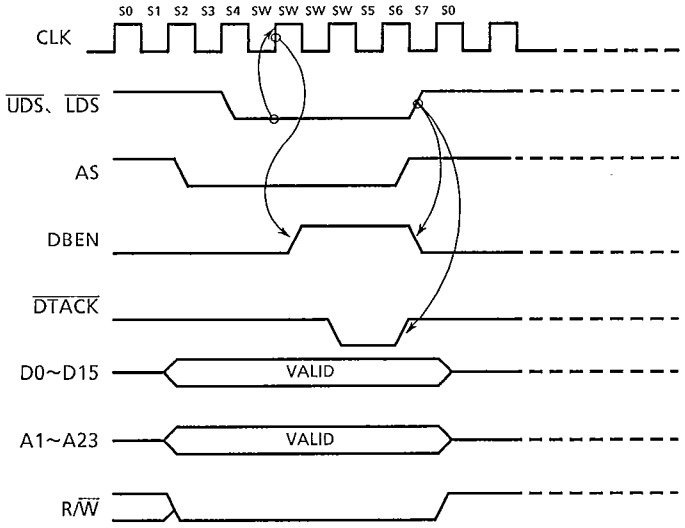


Figure 4.6 TMP68000 Write Cycle Timing

5. ELECTRICAL SPECIFICATIONS

5.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3~+0.7	V
Input Voltage	V_{in}	−0.3~+15.0	V
Output Voltage	V_{out}	−0.3~+15.0	V
Operating Temperature Range	T_a	0 ~70	°C
Storage Temperature Range	T_{stg}	−65~150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

5.2 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, GND = 0V, C_L = 100pF, Ta = 0 ~ 70 °C)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	–	V
Input Low Voltage	V_{IL}	–	0.8	V
Input Leakage Current (V_{in} = 0 to 5.25V)	I_{IL}	–	1.0	μA
Output High Voltage (I_{Load} = −100 μA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{Load} = −1.6mA)	V_{OL}	–	0.4	V
Output Leakage Current (Off-State) (V_{out} = 0V to 5.25V)	I_{OL}	–	10	μA
Internal Power Dissipation (V_{CC} = 5.25V, T_a = 0℃)	P_{INT}	–	750	mW
Input Capacitance (V_{in} = 0V, f = 1.0MHz)	C_{in}	–	20	pF
Output Capaciatance (V_{out} = 0V, f = 1.0MHz)	C_{out}	–	20	pF

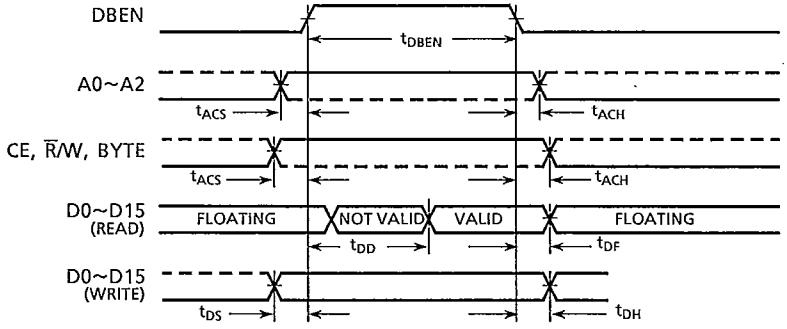
5.3 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V ±5%, GND = 0 V, C_L = 100pF, Ta = 0 ~ 70 °C)

Characteristic	Symbol	TMP68652P-2		Unit
		Min	Max	
Pulse Width, Clock Low	PW_{CL}	240	–	ns
Pulse Width, Clock High MM = 0 MM = 1	PW_{CH}	165 240	– –	ns ns
Pulse Width, RESET	PW_{RES}	250	–	ns
Pulse Width, DBEN	PW_{DBEN}	200	m*	ns
Receiver Serial Data Setup Time	t_{RXS}	150	–	ns
Receiver Serial Data Hold Time	t_{RXH}	150	–	ns
Address/Control Setup Time	t_{ACS}	50	–	ns
Address/Control Hold Time	t_{ACH}	0	–	ns
Data Bus Set up Time (Write)	t_{DS}	50	–	ns
Data Bus Hold Time (Write)	t_{DH}	0	–	ns
Data Bus Delay Time (Read)	t_{DD}	–	170	ns
Transmit Serial Data Delay Time	t_{TXD}	–	250	ns
DBEN to DBEN Delay Time	t_{DBEND}	200	–	ns
Data Bus Float Time (Read)	t_{DF}	–	150	ns
Serial Data Clock Frequency (TxC, RxC)	f_C	–	2.0	MHz

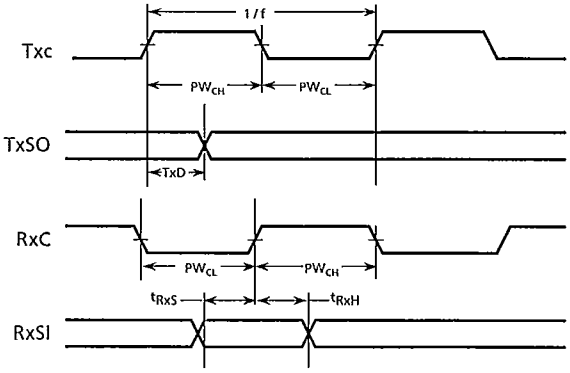
*m = TxC negated and applines to writing to $TDSR_H$ only.

Figure 5.1 Reset Timing Diagram



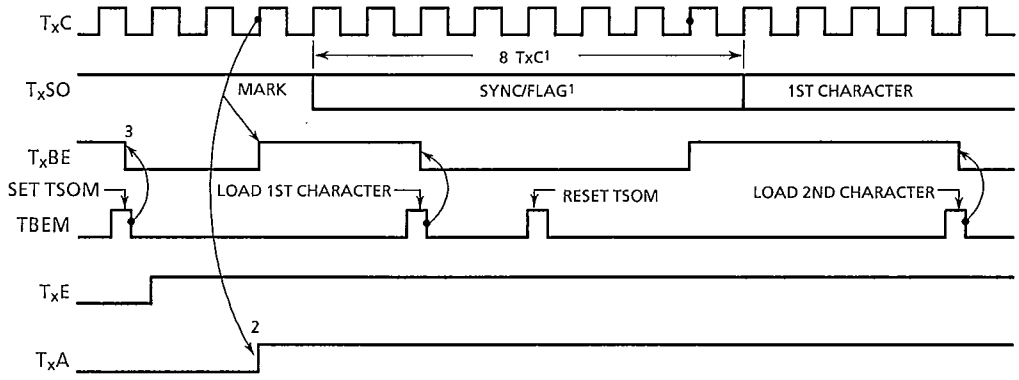
Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 5.2 Read/Write Bus Timing Diagram



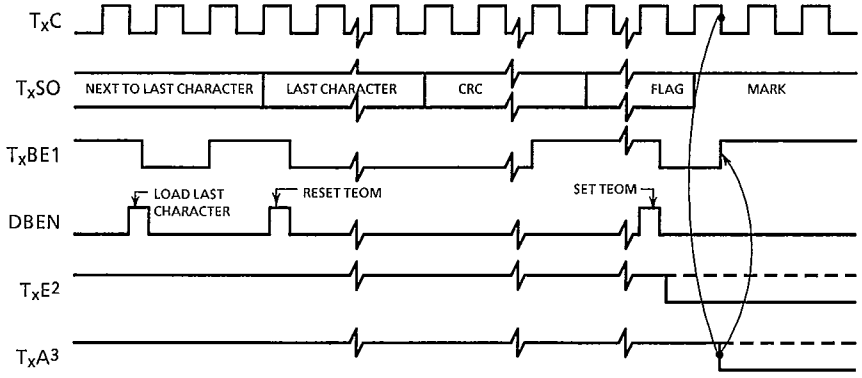
Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside, and pass through, the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

Figure 5.3 Serial Clock and Data Timing Diagram



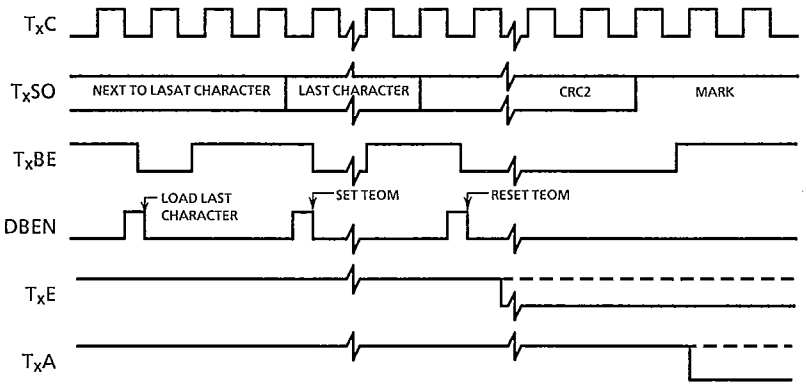
Note 1 : SYNC may be 5 to 8 bits and will contain parity bit as specified.
2 : TxA is asserted relative to TxC rising edge after TSOM has been set and TxE has been asserted.
3 : TxBE is negated relative to DBEN falling edge on the first write transfer into TDSR. It is reasserted one TxC time before the first bit of the transmitted SYNC/FLAG. TxBE is then negated relative to DBEN falling edge when writing into $TDSR_H$ and/or $TDSR_L$. It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character except in BOP mode when the CRC is sent as the next character.

Figure 5.4 Transmit-Start of Message Timing Diagram



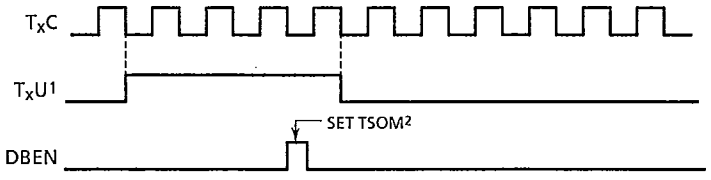
Note 1 : Txbe is negated relative to the falling edge of DBEN corresponding to loading $TDSR_{H/L}$. It is asserted one TxC cycle before character taransmission begins and also when TxA is negated.
2 : TxE can be negated before clearing TEOM if TxBE(corresponding to the closing FLAG) is asserted. Alternatively TxE can remain asserted and a new message initiated.
3 : TxA is negated after TxE is negated and 11/2 TxC cycles after the last bit of the closing FLAG has been transmitted.

Figure 5.5 Transmit-End of BOP Message Timing Diagram



Note 1 : When TMP68652-generated CRC is not required, TEOM should only be set if SYNCs are to follow the message block. In that case, TxE should be negated in response to TxBE (which corresponds to the start of transmission of the last character). When CRC is required, TxE must be negated before CRC transmission is complete. Otherwise, the contents of TxDB will be shifted out on TxSO. This facilitates transmission of contiguous messages.

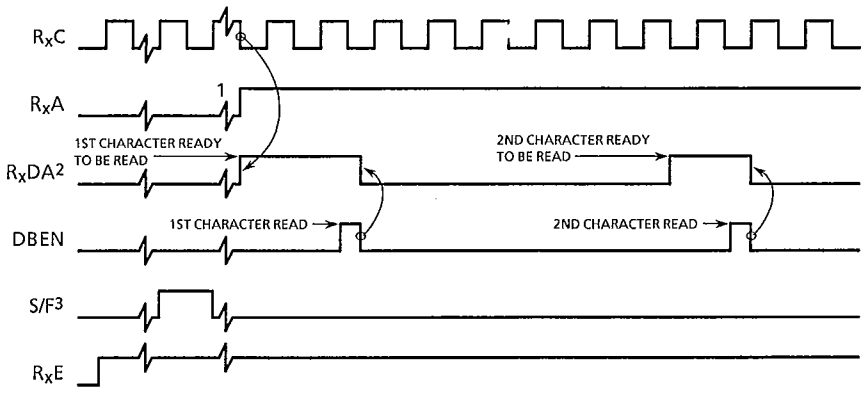
Figure 5.6 Transmit—End of BCP Message Timing Diagram



Note 1 : TxU is asserted relative to TxC falling edge if TxBE has not be serviced after n-1/2 TxC times (where n equals transmit character length). TxU is negated on the TxC falling edge following setting of the TSOM command.

2 : An underrun will occur at the next character boundary if TEOM is cleared and the transmitter remains enabled, unless the TSOM command is set or a character is loaded into the TxDB.

Figure 5.7 Transmit-Underrun Timing Diagram

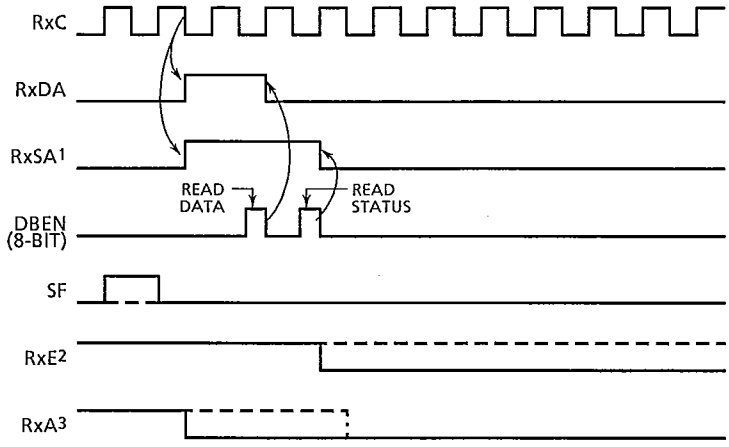


Note 1 : RxA is asserted relative to the falling edge of RxC when RxE is asserted and :
- a. A data character following two SYNC's is in RxDB (BCP mode).
- b. The character following FLAG is in RxDB (BOP primary station mode).
- c. The character following FLAG is in RxDB and matches the secondary station address or all parties address (BOP secondary station mode).

2 : TxDA is asserted on RxC falling edge when a character in RxDB is ready to be read. It is asserted before RxSA is negated on the falling edge of DBEN when RxDB is read.

3 : S/F is asserted relative to the rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected.

Figure 5.8 Receive-Start of Message Timing Diagram



Note 1 : At the end of a BOP message, RxSA is asserted when FLAG detection (S/F = 1) forces the setting of REOM. The processor should read the last data character ($RDSR_L$) and status ($RDSR_L$) which negates RxDA and RxSA, respectively. For BCP end of message, RxSA must not be asserted and S/F must equal zero. The processor should read the last data character and status.

2 : RxE must be negated for BCP with non-contiguous messages. It may be left asserted at the end of a BOP message (see BOP Mode).

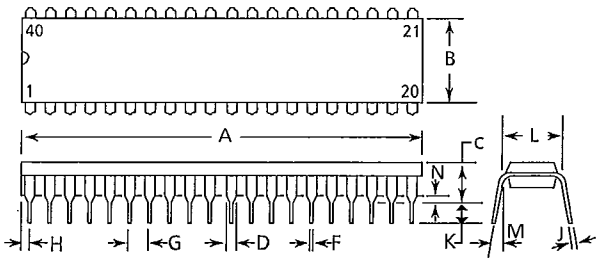
3 : RxA is negated relative to the falling edge of RxC after the closing FLAG of a BOP message (REOM = 1 and RxSA is asserted) or when RxE is negated.

Figure 5.9 Receive-End of Message Timing Diagram

6. MECHANICAL DATA

6.1 PACKAGE DIMENSIONS

PLASTIC PACKAGE



Unit : mm

Dim	Min	Max
A	51.69	52.45
B	13,72	14.22
C	3.94	5.08
D	0.36	0.56
F	1.02	1.52
G	2.54BSC	
H	1.65	2.16
J	0.20	0.36
K	2.92	3.43
L	15.24BSC	
M	0°	15°
N	0.51	1.02