CMOS 4-BIT MICROCONTROLLER

TMP47C475AN

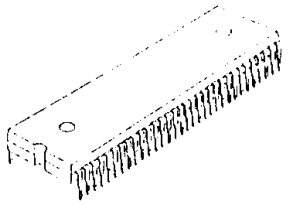
The 47C475A is the high speed and high performance 4-bit single chip microcomputer with VFT (Vacuum Fluorescent Tube Display) driver, Watchdog Timer and 14-bit D/A converter (Pulse width modulation) output. The 47C475A has two osillation circuits. It is possible to switch the operation mode ; high speed operation and low power cousumption operation.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C475AN	4096 × 8-bit	256 × 4-bit	SDIP64	TMP47C975AE

FEATURES

- ◆4-bit Single chip microcomputer
- ◆Instruction exection time : 1.9μs (at 4.2MHz), 244μs (at 32.8KHz)
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All source have independent latches each, and multiple interrupt control is available.
- ◆I/O port (55 pins)
  - Input 1 port 4pins
  - Output 8 ports 32pins
  - I/O 5 ports 19pins
- ◆Interval Timer
- ◆Two 12 bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Watchdog timer
- ◆Serial Interface with 4-bit buffer
  External/Internal clock, and leading/trailing edge shift mode
- ◆D/A converter (pulse width modulation) output
  14-bit resolution (1 channel)
- ◆VFT drive circuit (automatic display)
  - Max. 16-digit × 8-segment
  - High breakdown voltage output ports
    (42V max. × 24-bit)
- ◆Key scan control
  Key matrix constructed by segment outputs.
- ◆LED direct drive capability (typ. 20mA × 8 bits)
- ◆Dual clock operation
  High-speed / low-power-consumption operating mode
- ◆Real Time Emulator : BM47211A

SDIP64



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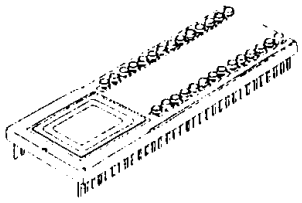

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PIN ASSIGNMENT (TOP VIEW)

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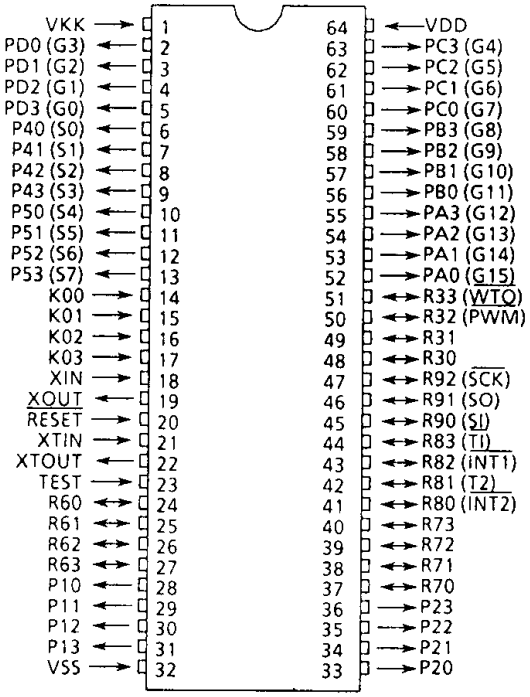
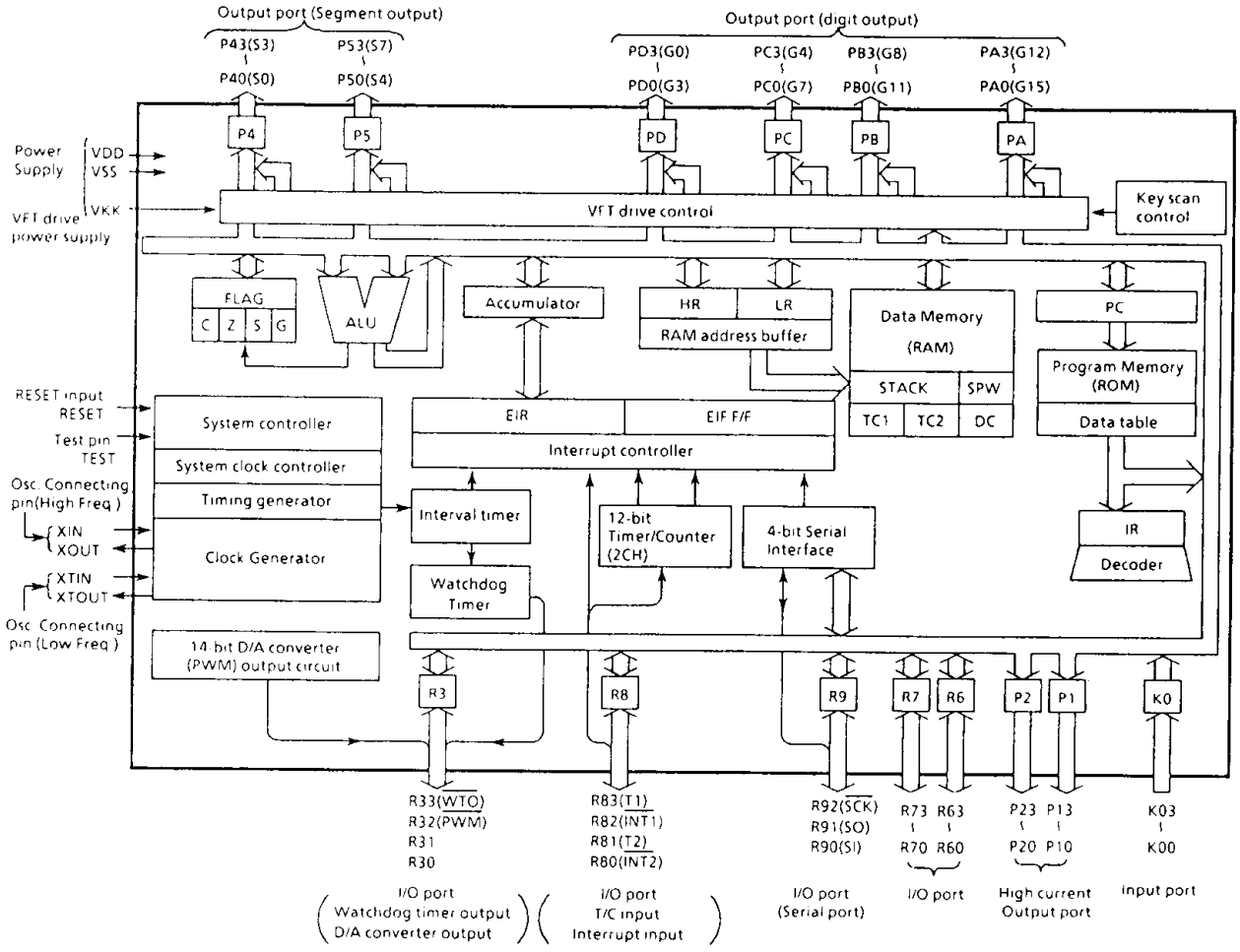


BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch.	
P23 - P20		8-bit data are output by the 5-bit to 8-bit data conversion instruction. [OUTB @HL].	
R33 ($\overline{WTO}$)	I/O (Output)	4-bit I/O port with latch. When using as input port or watchdog timer output or PWM output, the latch must be set to "1".	Watchdog timer output
R32 (PWM)	I/O (Output)		Pulse Width Modulation output
R31 - R30	I/O		
P53 (S7) -P40 (S0)	Output (Output)	4-bit output port with latch.	VFT segment output
R63 - R60	I/O	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	
R73 - R70			
PD3 (G0) -PA0 (G15)	Output (Output)	4-bit output port with latch	VFT digit output
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When using as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pin (High-Frequency).	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
XTIN	Input	Resonator connecting pin (Low-Frequency).	
XTOUT	Output	For inputting external clock, XTIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VKK		VFT drive power supply	

OPERATIONAL DESCRIPTION

Concerning the 47C475A the configuration and functions of hardwares are described. As the description is provided with priority on these ports differing from the 47C400A, the technical data sheets for the 47C400A, shall also be referred to. In addition, the hold function and KE port have been built-in the 47C475A.

1. SYSTEM CONFIGURATION

(1) I/O port
(2) System Clock Controller
(3) Interval Timer
(4) Timer/Counter
(5) Serial Interface
(6) Vacuum Fluorescent Tube Drive circuit
(7) D/A Converter (Pulse Width Modulation Output)
(8) Watchdog Timer

2. PERIPHERAL HARDWARE FUNCTION

2.1 I/O port

The 47C475A has 14 ports (55 pins) each as follows :

① K0	;4-bit input	
② P1, P2	;4-bit output	
③ R3	;4-bit input/output	(Shared with PWM and watchdog timer output)
④ P4, P5	;4-bit input/output	(Shared with VFT segment output)
⑤ R6, R7	;4-bit input/output	
⑥ R8	;4-bit input/output	(Shared with external interrput input and timer / counter input)
⑦ R9	;3-bit input/output	(Shared with serial port)
⑧ PA, PB, PC, PD	;4-bit output	(Shared with VFT digit output)

This section describes ports of ③, ④, and ⑧ which are changed from the 47C400A.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

※ Connecting VKK (power supply for driving Vacume Fluorescent Tube) pin.
The 24 pins of ports P5, P6 and PA to PD have a P-channel open-drain construction with pull-down resistor. Each pin is connected to a VKK pin through a pull-down resistor (typ. 80kΩ). Consequently, it is possible to drive a Vacume Fluorescent Tube (VFT) by applying a negative voltage (– 35V max.) to the VKK pin without external resistor.

(1) Port R3 (R33-R30)

The 4-bit I/O port with latch. R30 and R31 are normal I/O ports. When used as input ports, the latches should be set to "1". R32 is used for pulse width modulation ($\overline{PWM}$) output and R33 is used for watchdog timer ($\overline{WTO}$) output. When using R32 for $\overline{PWM}$ output and R33 for watchdog output, the output latches should be set to "1". The latches are initialized to "1" during reset.

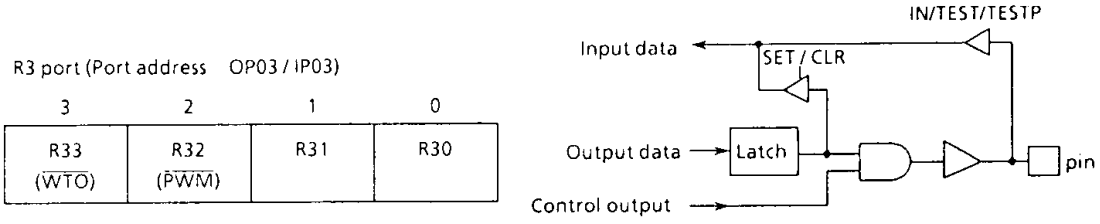


Figure 2-1. Port R3

(2) Ports P4 (P43-P40), P5 (P53-P50)

The 4-bit high breakdown voltage output ports with latch, which can directly drive Vacume Fluorescent Tube (VFT). Latch data can be read out by input instructions. During reset, the latches are initialized to "0". Ports P4 and P5 are also used for segment output, at which time the latches must be cleared to "0". When used as normal output ports, however, VFT display must be set blanking mode (access by instruction is not possible while display is enabled).

Ports P4, P5, R6, and R7 can be set, cleared and tested for each bit as specified by L-register indirect addressing bit manipulation instructions ([SET @L], [CLR @L], and [TEST @L]).

Port P5 (Port address OP05/IP05)

3	2	1	0
P53 (S7)	P52 (S6)	P51 (S5)	P50 (S4)

Port P4 (Port addrerss OP04/IP04)

3	2	1	0
P43 (S3)	P42 (S2)	P41 (S1)	P40 (S0)

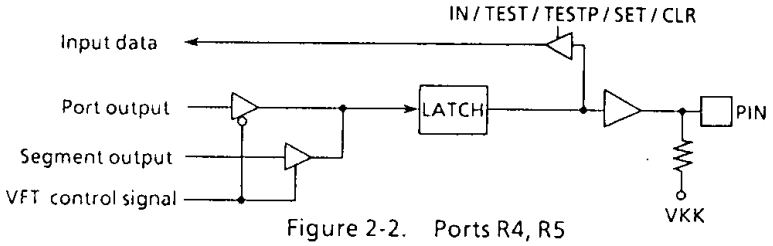


Figure 2-2. Ports R4, R5

(3) PA (PA3-PA0), PB (PB3-PB0), PC (PC3-PC0), PD (PD3-PD0) port

The 4-bit high breakdown voltage output ports with latch, which can directly drive Vacuum Fluorescent Tube (VFT). Latch data can be read out by input instructions. During reset, latches are initialized to "0". The 16 pins of these 4 ports are also used for digit output, at which time the latches must be cleared to "0".

Also, the pins not connected to a VFT can be used as normal output ports. In this case, however, the port output instruction is effective even when the VFT display is enabled. Consequently, caution must be exercised since the output data for the display can be destroyed when an output instruction is sent to a pin being used for display.

PD port (Port address OP0D/IP0D)

3	2	1	0
PD3 (G0)	PD2 (G1)	PD1 (G2)	PD0 (G3)

PC port (Port addres OP0C/IP0C)

3	2	1	0
PC3 (G4)	PC2 (G5)	PC1 (G6)	PC0 (G7)

PBport (Port address OP0B/IP0B)

3	2	1	0
PB3 (G8)	PB2 (G9)	PB1 (G10)	PB0 (G11)

PA port (Port address OP0A/IP0A)

3	2	1	0
PA3 (G12)	PA2 (G13)	PA1 (G14)	PA0 (G15)

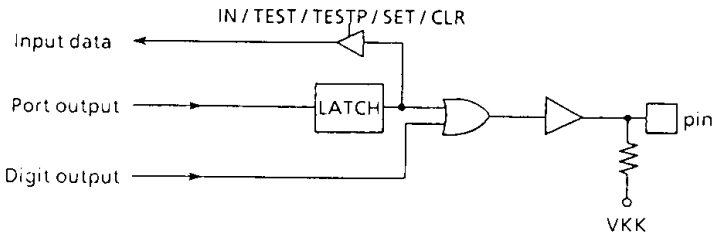


Figure 2-3. Ports PA, PB, PC, PD

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Input (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT@HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	R3 input port	R3 〃	○	○	○	–	○	○	–
04	P4 output latch	R4 output port (Segment output)	○	○	○	–	○	○	○
05	P5 〃	R5 output port (Segment output)	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port (Note 3)	R9 output port	○	○	○	–	○	○	–
0A	PA output latch	PA output port (Digit output)	○	○	○	–	○	○	–
0B	PB output latch	PB output port (Digit output)	○	○	○	–	○	○	–
0C	PC output latch	PC output port (Digit output)	○	○	○	–	○	○	–
0D	PD output latch	PD output port (Digit output)	○	○	○	–	○	○	–
0E	SIO, SLOW operation status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	——	–	–	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	——	–	–	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog timer control	–	○	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	PWM buffer selector	–	○	–	–	–	–	–
18	Undefined	PWM data transfer buffer	–	○	–	–	–	–	–
19	Undefined	Interval timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	VFT drive control(1)	–	○	–	–	–	–	–
1B	Undefined	VFT drive control(2)	–	○	–	–	–	–	–
1C	Undefined	Timer/counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. "——" means the reserved stat. Unavailable for the user program.
Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.
Note 3. In the Key-Scan mode, $IP09_3$ is using as the stats input.

Table 2-1. Port Address Assignments and Available I/O Instructions

2.2 System Clock Controller

The 47C475A has two oscillation circuits with a high-frequency clock and a low-frequency clock. Power consumption can be decreased by switching to low-speed operation using the low-frequency clock when necessary (dual clock operation). The high-frequency clock can be obtained by connecting an oscillator to the XIN and XOUT pins; the low-frequency clock can be obtained by connecting the oscillator to the XTIN and XOUT pins.

2.2.1 Circuit Configuration

Figure 2-4 shows the configuration of system clock controller.

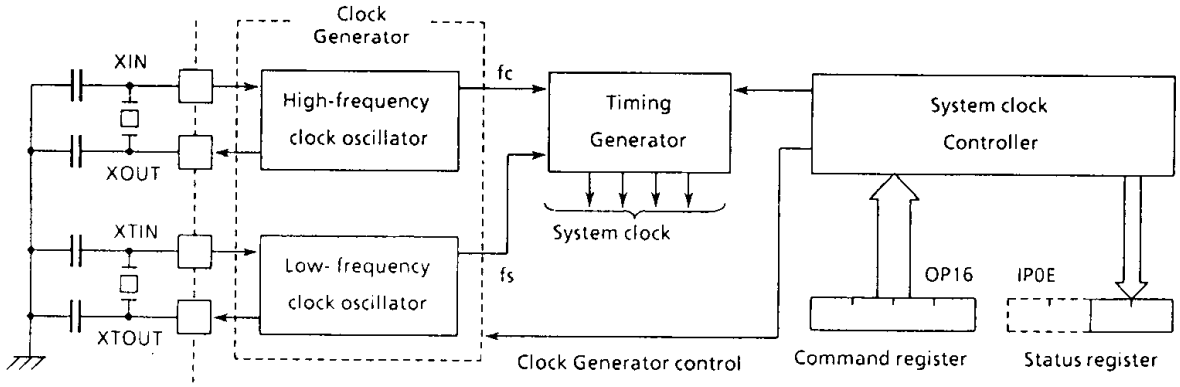


Figure 2-4. System Clock Controller

2.2.2 Dual Clock Operation and Control

Dual clock operation involves two modes : Normal operating mode using the high-frequency clock, and SLOW operating mode using the low-frequency clock. Both oscillators start operating when the power is turned on, after which the Normal operation is selected automatically. The high-frequency clock stops oscillating when a command is issued to switch to the SLOW operation. Operating mode switching is performed using the command register (OP16). The status of the low-frequency clock and the current operating mode can be monitored using the status register (IPOE). Figure 2-5 shows the operating mode transitions, and Figure 2-6 shows the command and status registers.

(1) Operating Mode Transition

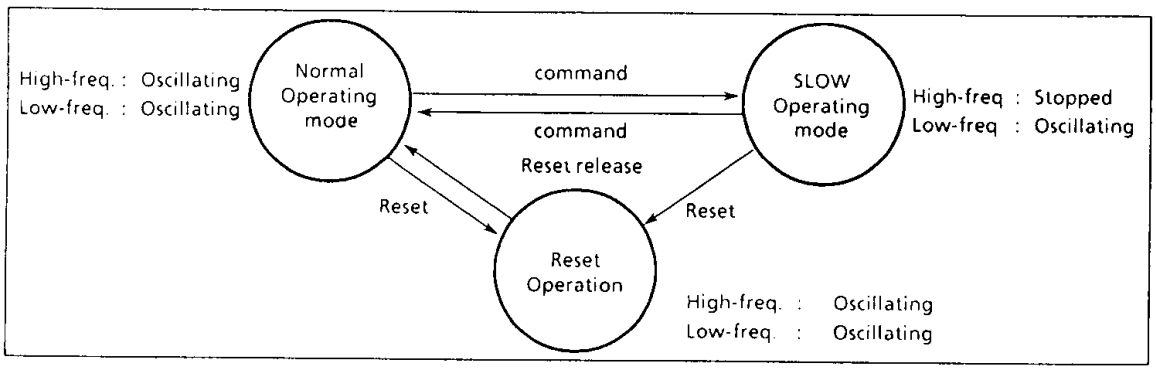


Figure 2-5. Operating Mode Transition Diagram

(2) Operating Mode Control

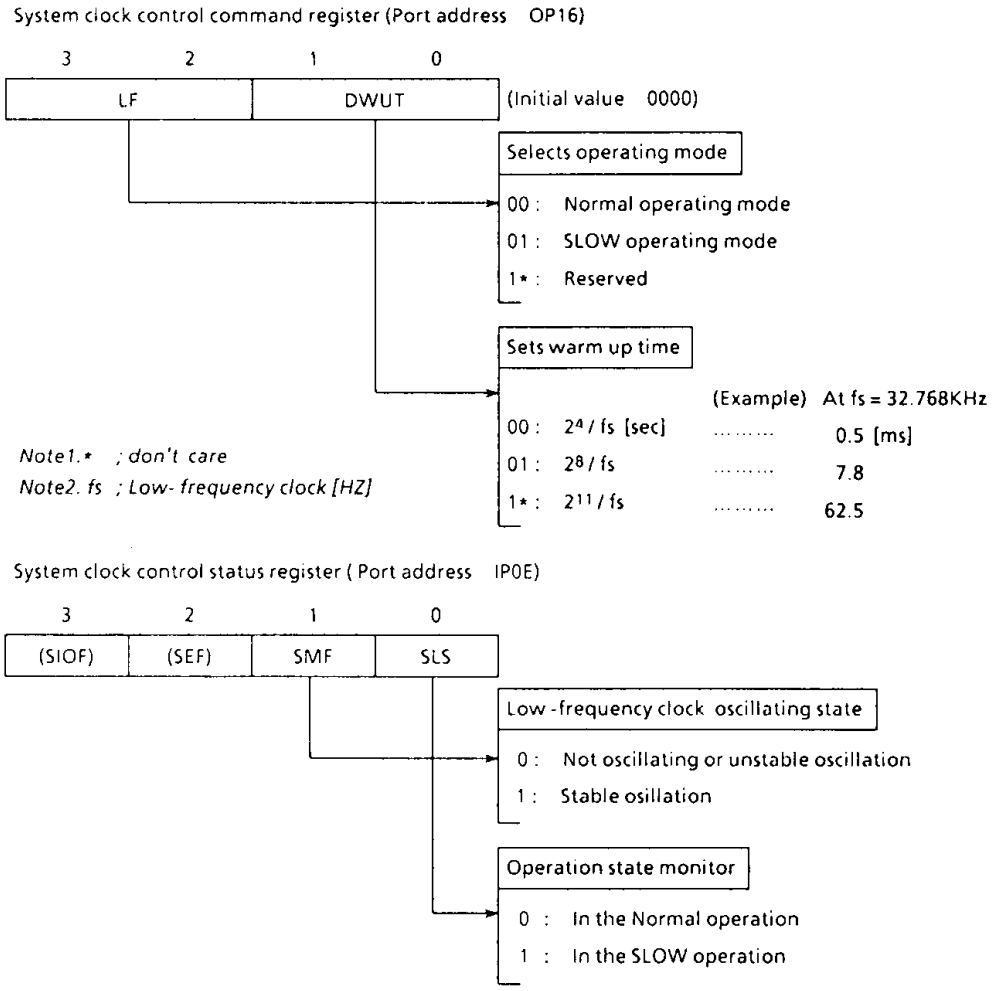


Figure 2-6. Command register and Status register

Note 1. The following operations and functions cannot be used in the SLOW operation ; therefore, this must be taken into consideration in programming.

(1) Timer/Counter 4096Hz (at fs = 32.8kHz) count operation (can be used with other count rates).

(2) Interval timer interrupt 4096Hz (at fs = 32.8kHz) operation (can be used with other timer rates).

(3) Serial Interface

(4) VFT drive circuit

Note 2. The power consumption of the oscillator and internal hardware is decreased in the SLOW operation, but power consumption through pin interfaces (dependent on the external circuitry and program) may prevent overall low power consumption operation ; therefore , caution is necessary during system design and interface circuit design.

(3) Operation mode switching

The following procedure is used to switch between the Normal operation and the SLOW operation. The Normal operation is initialized during reset. Also, the current operating mode can be checked by monitoring SLS (status register bit 0).

a. Switching from Normal operation to SLOW operation

After monitoring SMF (status register bit 1) by program and confirming that the low-frequency clock is stable, set bit 2 of the command register to "1". The high-frequency clock will then stop. Also, after switching from Normal operation to SLOW operation (accessing the command register), execute the NOP (No Operation) instruction.

b. Returning from SLOW operation to Normal operation

When bit 2 of the command register is cleared to "0", the warm-up time must be set in DWUT. When the set warm-up time elapses, operation is switched to the Normal operation.

Example 1 : Normal operation → SLOW operation.

```
SSMF:   TEST    %IP0E, 1        ; To wait until SMF goes to "1"
        B       SSMF
        LD      A, #0100B       ; Selects SLOW operating mode
        OUT     A, %OP16
        NOP                     ; No operation
        :
```

Example 2 : SLOW operation→Normal operation

```
        LD      A,  #0001B      ; Selects Normal operation and sets warm-up
        OUT     A,  %OP16         time (7.8ms)
        :
```

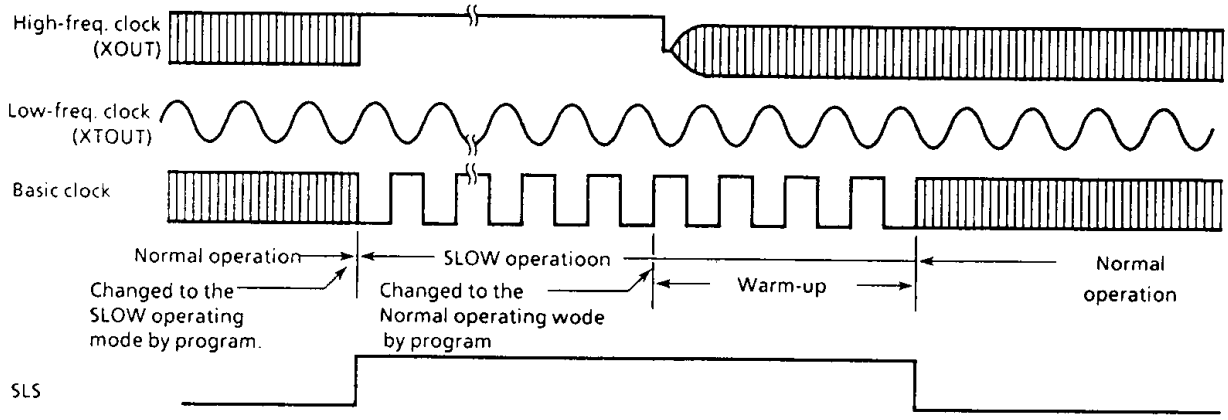


Figure 2-7. System Clock Switching Timing

2.3 Interval Timer

2.3.1 Configuration of interval timer

The interval timer is configured with a 15-stage binary counter and inputs the oscillation circuit output (fs) for the low-frequency clock; therefore, the final stage output is fs/215 [Hz] . This interval timer is cleared to "0" during reset.

Also, "fs" is input directly into the interval timer; therefore, the interval timer interrupts, timer/counter and VFT drive circuit will not operate nomally if the low-frequency oscillation is not stable.

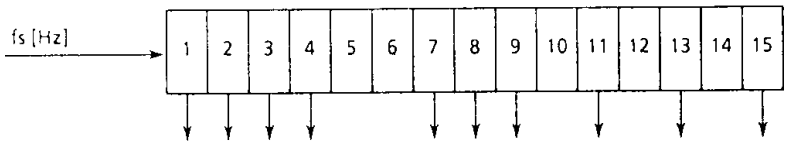


Figure 2-8. Interval timer

2.3.2 Interval Timer Interrupt (ITMR)

Constant-frequency interrupts can be generated using the interval timer, Four different frequencies can be selected for interval timer interrupts using the command register (OP19) . The command register is also initialized to "0" during reset.

An interval timer interrupt is generated at the first rising edge of the binary counters output after the command is set to the command register.

Interval timer interruput control command register (Port address OP19)

3	2	1	0

(Initial value 0000)

Example : At fs = 32.768KHz

00** :	Interrupt disabled				
0100 :	Interruput frequency	fs / 2^3 [Hz]	.....	4096	[Hz]
0101 :	〃	fs / 2^7	.....	256	
0110 :	〃	fs / 2^9	.....	64	
0111 :	〃	fs / 2^{13}	.....	4	
1*** :	Reserved				

Note1. * ; *don't care*

fs ; *Low-frequency clock [Hz]*

Mote2. ; *Operation of fs / 2^3 [HZ] cannot be used in the SLOW operation*

Figure 2-9. Command Register

2.4 Timer/Counter

The Timer/Counter of the 47C475A is operated by a low-frequency clock (fs) ; therefore, the following operating frequencies differ from those of the 47C400A.

① Internal pulse rate.
② Maximum frequency applied in the event counter mode.
③ Drop ratio of instruction execution time when the timer is used.

(1) Internal pulse rate

The internal pulse rates shown in Table 2-2. can be selected by setting the values of the lower 2 bits of the TC1 and TC2 control command registers (OP1C, OP1D) .

Setting value of lower 2 bits (bit 1, 0)	Interval pulse rate	Max. setting time	At fs = 32.768KHz	
			Interval pulse rate	Max. setting time
00	$fs/2^3$ [Hz]	$2^{15}/fs$ [sec]	4096 [Hz]	1 [sec]
01	$fs/2^7$	$2^{19}/fs$	256	16
10	$fs/2^{11}$	$2^{23}/fs$	16	256
11	$fs/2^{15}$	$2^{27}/fs$	1	4096

Table 2-2. Interval Plse Rate

(2) Maximum frequency applied in the event counter mode

		Normal operating mode	SLOW operating mode
a. In 1-channel operation		fc / 32 [Hz]	fs / 32 [Hz]
b. In 2-channel operation	TC1	fc / 32	fs / 32
	TC2	fc / 40	fs / 40

(3) Drop ratio of instruction execution time when the timer is used.

With the 47C475A, count operation is inserted in the ratio of once per {(basic clock frequency) /2^3} / (internal pulse rate) instruction cycle; therefore, execution speed drops as follows :

$$100 \div \left\{ \frac{\text{(basic clock frequency)} / 2^3}{\text{(Internal pulse rate)}} - 1 \right\} \%$$

Example 1 : When fc = 4MHz and fs = 32.8KHz in the Normal operation, and the internal pulse rate $fs/2^3$ is selected, count operation is inserted once per each cycle of 122 instructions, therefore, there is a drop of 100/121 = 0.83% for an instruction execution speed of 2μs.

Example 2: When fs = 32.8KHz in the SLOW operation, and the internal pulse rate $fs2^{11}$ is selected, count operation is inserted once per each cycle of 256 instructions ; therefore, there is a drop of 0.39% for an instruction execution speed of 244 μs. In addition, when the basic clock is obtained from "fs" (SLOW operation) , count operation cannot be used with an internal pulse rate of $fs/2^3$.

2.5 Serial Interface

When operating using the internal clock, $fs/2^2$ [Hz] is used as the serial clock.

Consequentley, when operating at fs = 32.768KHz, the maximum transfer rate is 8192 bit/sec. When the reading and writing of serial data cannot follows this clock rate, the serial clock is automatically stopped and the next shift operation stands by untill the processing is completed.

External clock can be used in the same way as for the 47C400A. The serial interface cannot be used in the SLOW operating mode.

2.6 VFT drive circuit

The 47C475A has built-in circuit whitch can directly drive the vacuume fluorescent tube display (VFT) and its control circuit.

2.6.1 VFT drive circuit functions

(1) There are 24 high breakdown voltage output buffers.
- Digit output 16 pins (G0~G15)
- Segment output 8 pins (S0~S7)

In addition, VKK pin is provided as the drive power pin.

(2) The dynamic lighting system makes it possible to select 8 segments x n digits (n = 1 to 16) by program.

(3) Digit output pins not used for VFT driver can be used as general-I/O ports.

(4) Display data are automatically transferred to the high breakdown voltage output buffer.

(5) A dimmer function enables 4 brightness levels.

(6) A key scan function makes it possible to utilize segment output pins for key strobe output.

2.6.2 Circuit Configuration

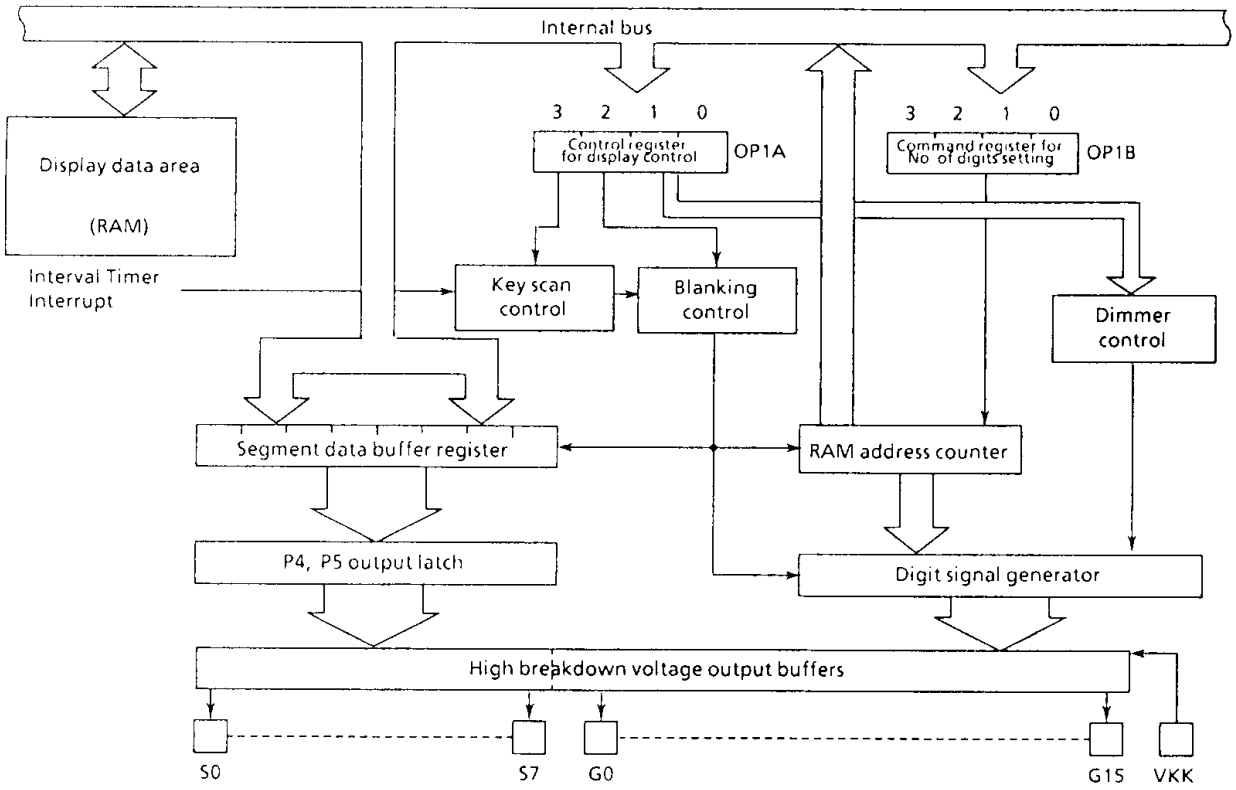


Figure 2-10. VFT driver

2.6.3 Control of VFT drive circuit

VFT drive circuit is controlled by the command register (OP1A and OP1B). The command register is initialized to "4" and "0" during the reset. The operation state of the VFT drive circuit can be known by the status register ($IP09_3$).

Display control command register (Port address OP1A)

3	2	1	0	
EKY	BLK	DIM		(Initial value 0100)

Key scan control

0 : Disables key scan mode
1 : Enables key scan mode

VFT drive control

0 : Release the blanking and enables the display.
1 : Applies or continues the blanking.

Dimmer control

00 :	6 / fs [sec]	(normal display)
01 :	4 / fs	(2/3 dimmer display)
10 :	3 / fs	(1/2dimmer display)
11 :	2 / fs	(1/3dimmer display)

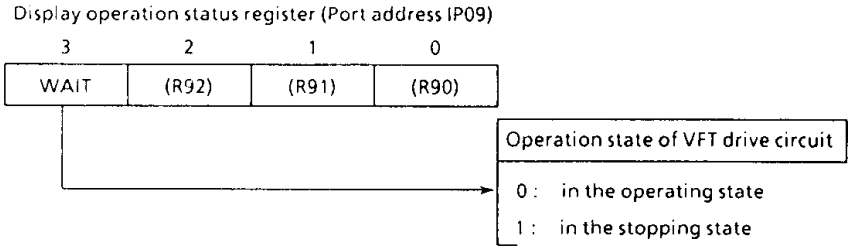
No. of digits setting command register (Port address OP1B)

3	2	1	0	
	DIG			(Initial value 0000)

No. of digits setting

0000 :	1digit display	(Output G0 only)
0001 :	2 digit display	(Output G0, G1)
0010 :	3 digit display	(Output G0~G2)
0011 :	4 digit display	(Output G0~G3)
0100 :	5 digit display	(Output G0~G4)
0101 :	6 digit display	(Output G0~G5)
0110 :	7 digit display	(Output G0~G6)
0111 :	8 digit display	(Output G0~G7)
1000 :	9 digit display	(Output G0~G8)
1001 :	10digit display	(Output G0~G9)
1010 :	11digit display	(Output G0~G10)
1011 :	12digit display	(Output G0~G11)
1100 :	13digit display	(Output G0~G12)
1101 :	14digit display	(Output G0~G13)
1110 :	15digit display	(Output G0~G14)
1111 :	16digit display	(Output G0~G15)

Figure 2-11. Command register



Figeure 2-12. Status register

2.6.4 Display operation

(1) Display data setting

Display data are stored to the display data area (address A0-BFH) in the data memory.

The conversion of data to VFT display data is performed by instruction (mainly using ROM data reference instructions) . Converted display data stored to the display data area are automatically transferred to the VFT drive circuit and output to the high breakdown voltage output buffer, without any program intervention. Consequently, display patterns can be varied by merely changing the data in the display data area.

There is a one-to-one correspondence between the VFT segments (dots) and the bits stored to the display data area of the data memory. A segment lights when the corresponding bit is "1" . Sections of the display data area of the data memory not being used for VFT data are used as normal data memory.

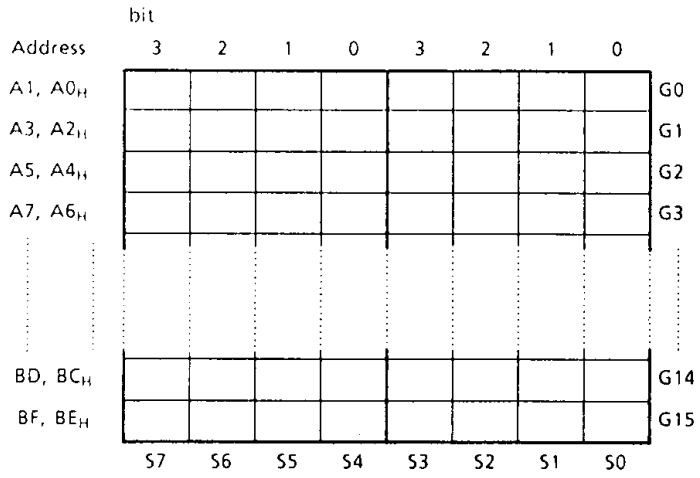


Figure 2-13. Display Data Area (Data Memory)

(2) Display data transfer

Requests for transfer of display data from the VFT drive circuit are sent to the CPU. After execution of an instruction is completed (after completion of timer/counter processing, or receiving of an interrupt) , the CPU sends the segment data in the display data area to the driver, and this operation is performed in one instruction cycle.

The data transfer cycle occurs while the VFT drive circuit is the operating status (BLK = 0) . The data transfer cycle is inserted at a frequency of once per 4/fs [sec.], and once per fc/ (2 × fs) instruction cycle. During operation with fc = 4.19MHz and fs = 32.8MHz, insertion is at the rate of once per cycle of 64 instructions. Figure 2-14. shows the VFT drive waveform.

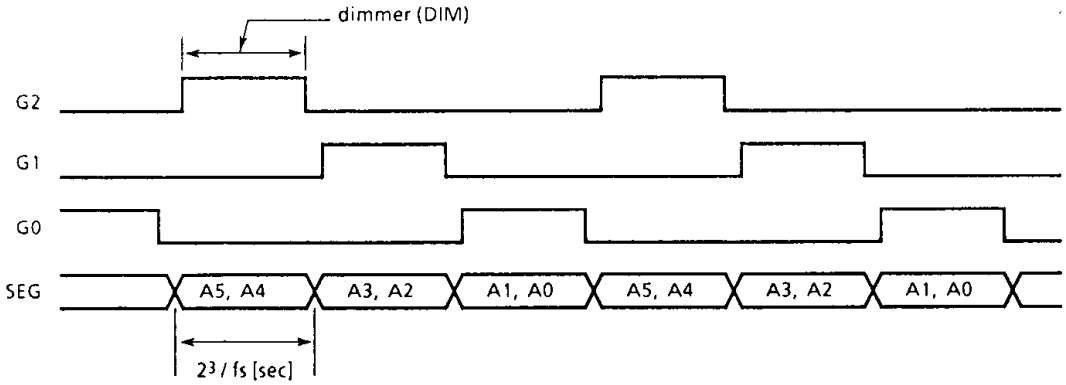


Figure 2-14. Driving Waveform in Normal Display

2.4.5 Key scan function

During display, data output from the segment output pin by instruction is disabled by the hardware but use is possible for the key strobe.

If a program writes "1" to EKY of the display control command register, BLK for that register synchronized with an interval timer interrupt request is automatically set to "1" and the display is blanked. Segment output pins can be accessed by instructions during blanking ; therefore, key scan is possible by entering the key scan program in the interval interrupt service routine.

When EKY is set to "1", however, blanking results when an interval timer interrupt request is generated even when, for example, the receiving of interrupts is disabled by the interrupt enable master F/F (EIF) .

Ports not being used for segment output can be used as normal ports but caution is necessary because the output latch is cleared to "0" by the blanking.

The interval timer interrupt frequency varies depending on the key reading speed required and the display quality but, normally, 256Hz or 64Hz (when fs = 32.8KHz) is appropriate. Blanking continues until BLK is set to "0" by the interrupt service routine and the display restarted with the next data transfer cycle after clearing.

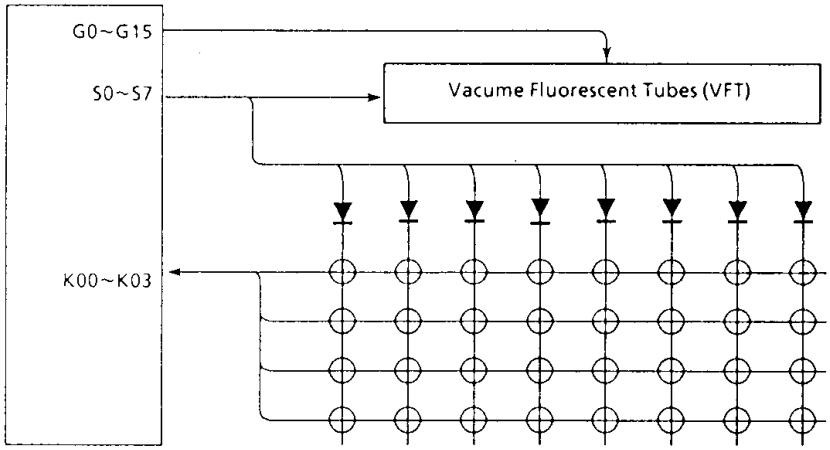
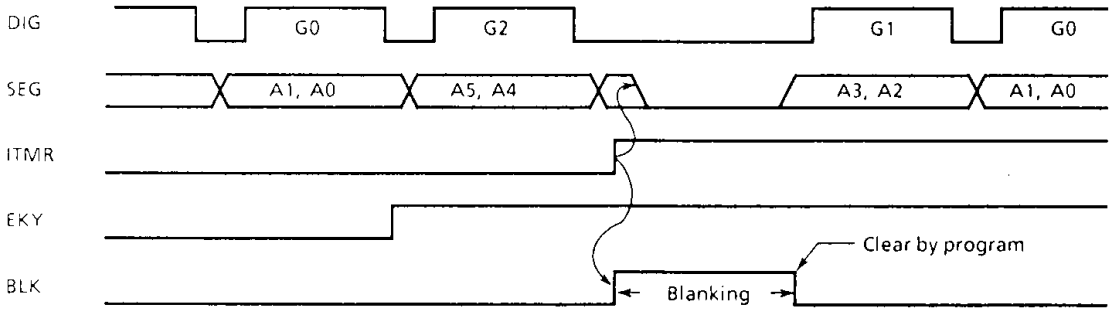


Figure 2-15. Example of 32 Keys Matrix Configuration



Note. In case of blanking time is set as 1-digit, clear BLK under less than (6/fs) ÷ (23/fc) instruction cycle after the ITMR interrupt request.

Figure 2-16. Key Scan Timing

2.5 D/A converter (pulse width modulation) output circuit

The 47C475A has one built-in 14-bit resolution pulse width modulation ($\overline{PWM}$) output channel which can easily be used for D/A converter output by connecting an external low-pass filter.

$\overline{PWM}$ output is from pin R32 ($\overline{PWM}$), which is used for both $\overline{PWM}$ and R32 output. The output latch should be set to "1" when this is used for $\overline{PWM}$ output.

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer can be sent to the PWM data latch by writing "CH" to the buffer selector to switch to $\overline{PWM}$ output. PWM data transferred to the PWM data latch remain intact until overwritten.

The resetting and holding operations clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{PWM}$ output is "H" level).

2.5.1 Circuit Configuration

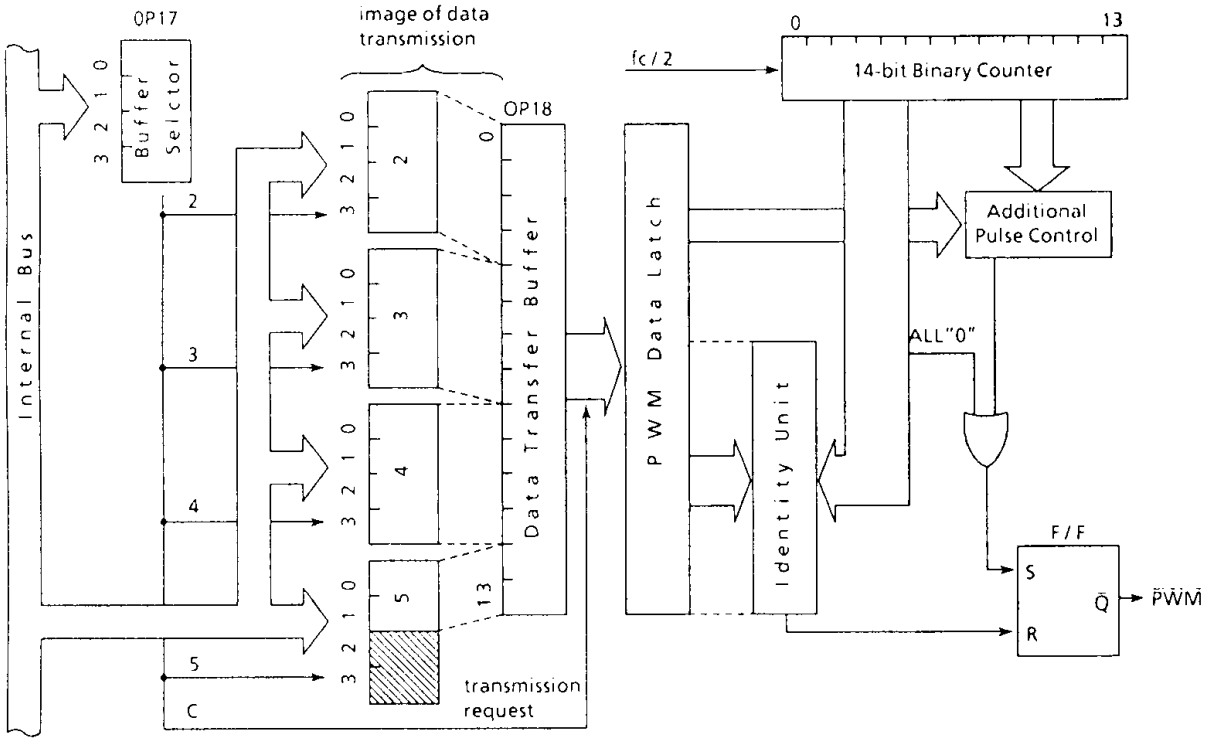


Figure 2-17. Pulse Width Modulation Output

2.5.2 Wave form of PWM output

$\overline{PWM}$ output is a 14-bit resolution pulse output and one cycle is $T_M = 2^{15}/fc$ (8192 μsec. when fc = 4MHz). The upper 8 bits of the PWM data latch control the pulse width of the pulse output with a cycle T_S ($T_S = T_M/64$). The low level pulse has a pulse width of n x to (to = 2/fc) with a cycle T_S when the 8-bit data are n (n = 0 to 255).

The lower 6 bits control the position where the additional pulses with width "to" are output in the 64 intervals T_S (i) (i = 0 to 63) of the T_M cycle. The low level pulse width is (n + 1) to during the interval where the additional pulses are output. The additional pulses are output in the 64 intervals T_S (i) when the 6-bit data are m (m = 0 to 63). Figure 3-20 shows the $\overline{PWM}$ output timing and Table 3-4 shows the relationship between the 6-bit data and the intervals where the additional pulses are output.

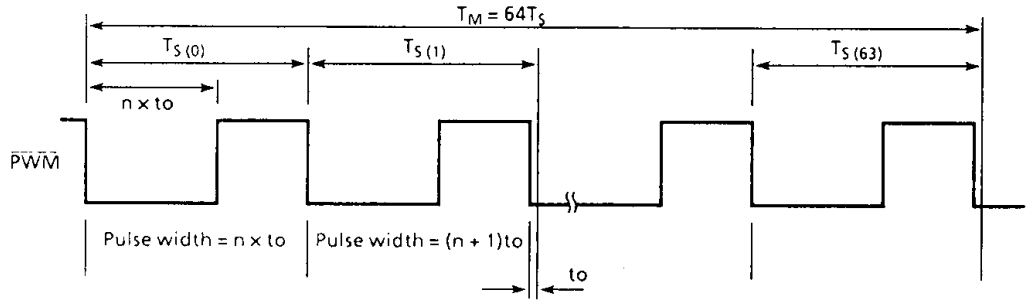


Figure 2-18. $\overline{PWM}$ Output Waveform (With additional pulse at $T_{S(1)}$, $T_{S(63)}$)

Bit position of 6 bits data	Relative position of T_S where the additional pulse is generated (No i of T_{Si} (0<i<63) is listed)
Bit-0	32
Bit-1	16, 48
Bit-2	8, 24, 40, 56
Bit-3	4, 12, 20, 28, 36, 44, 52, 60
Bit-4	2, 6, 10, 14, 18, 22, 26, 30·····, 58, 62
Bit-5	1, 3, 5, 7, 9, 11, 13, 15·····, 59, 61, 63

(Note) PWM output when bit data is "1".

Table 2-3. Correspondence between 6 bits data the addtional pulse generated T_S periods

2.5.3 Control of Pulse Width Modulation (data transfer)

$\overline{PWM}$ output is controlled by writing the output data to the data transfer buffer (OP18). The output data are written is sections using the buffer selector (OP17). In the data transfer buffer, the respective sections of data are assigned buffer numbers and written as indicated in Table 3-5.

① The buffer number of the buffer to which the data are to be written is written to the buffer selector (OP17).

② The corresponding PWM data are written to the selected buffer.

③ The output data are written to the transfer buffer by repeating the operations in items ① and ② above.

④ When writing is completed, "C" is written to the buffer selector by program.

When the output data are being written to the transfer buffer, the previous PWM data are being output. When "C" is written to the buffer selector, the output data are sent to the $\overline{PWM}$ data latch and $\overline{PWM}$ output is enabled, The time from when "C" is written to the buffer selector until PWM output is enable is 2^{15}/fc (8192μsec. at 4MHz) maximum.

Buffer No. (OP17)	Correspond bit (OP18)	Mode	$\overline{PWM}$ output
2	Bit of transfer buffer 0 ~ 3	data write	preceding data
3	Bit of transfer buffer 4 ~ 7	data write	preceding data
4	Bit of transfer buffer 8 ~ 11	data write	preceding data
5	Bit of transfer buffer 12 ~ 13	data write	preceding data
C	——	transfer	present data

Table 2-4. Number of data transmission buffer, bit correspond

2.6 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (runaway) of program due to external noise or other causes and return the operation to thr normal condition. The watchdog timer output is output to R33 ($\overline{WTO}$) pin.

When the watchdog timer is used, the output latch of R33 must be set to "1" . Further, during reset, the output latch of R33 is set to "1" , and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.6.1 Configuration of Watchdog Timer

The watchdog timer consists of 10-stage binary counter, flip-flop (F/F) , and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

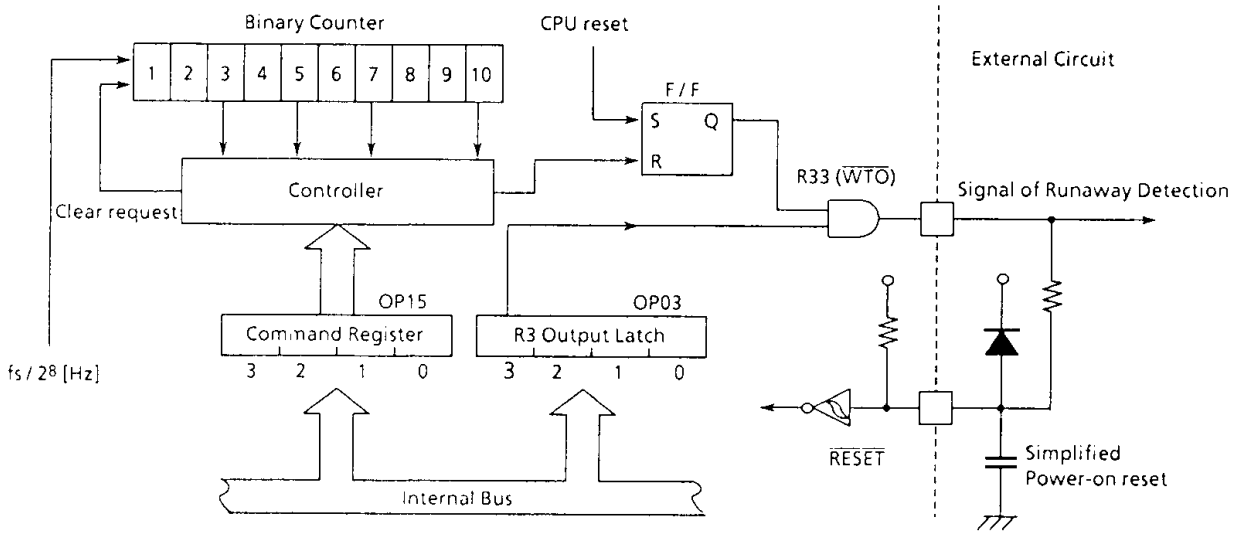


Figure 2-19. Configuration of Watchdog Timer

2.6.2 Control of Watchdog Timer

The watchdog timer is controlled by the command register (OP15) . This command register is initialized to "1000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.

2. The watchdog timer should be become enable

3. Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for same reason and binary counter is not cleared, the F/F is cleared to "0" at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L") .

Note. It is necessary to clear the binary counter prior to enabling watchdog timer. Further, when switching the system clock, the watchdog timer has to halt during the warm-up time at changing from the SLOW mode to the Normal mode.

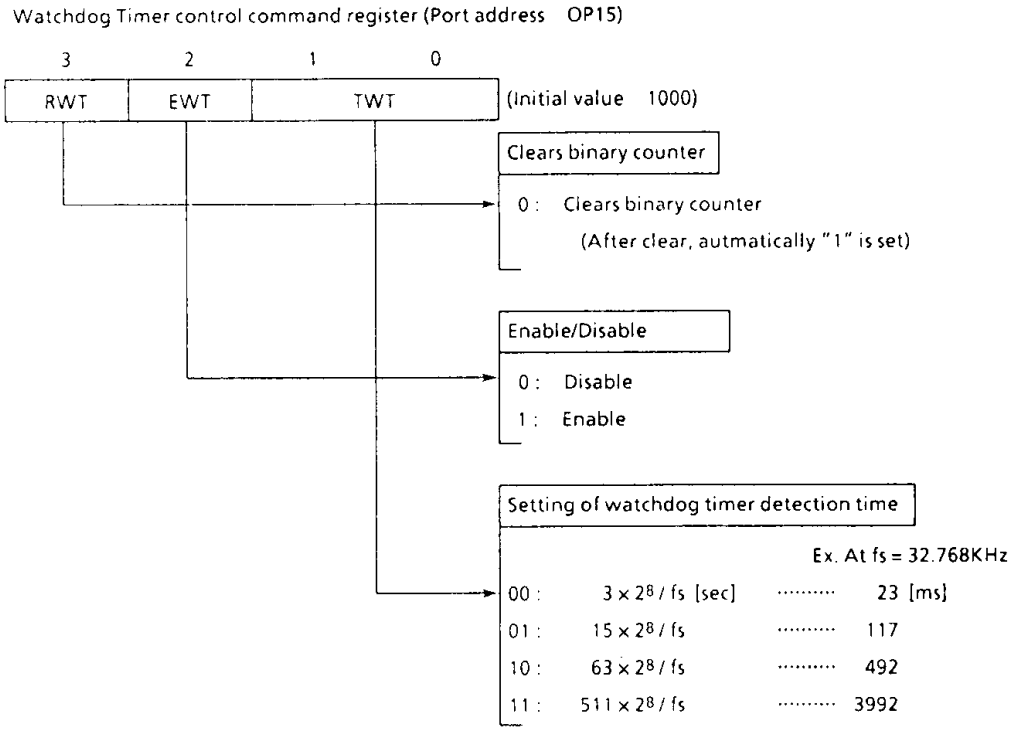


Figure 3-28. Command Register

Example : To set watchdog detection time (63×2^8/fs[sec]). And to enable the watchdog timer.

```
        LD      A, #0010B   ;  OP15 ← 0010B
                               (Sets WDT detection time. Clears binary counter. )
        OUT     A, %OP15
        LD      A, #1110B   ;  OP15 ← 1110B (Enable WDT)
        OUT     A, %OP15
Within WDT
        :
detection time
        :
        :
        LD      A, #0110B
        OUT     A, %OP15    ;  OP15 ← 0110B (Clears binary counter)
        :
        :
```

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5~7	V
Input Voltage	V_{IN}		− 0.5~V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except open drain pin	− 0.5~V_{DD} + 0.5	V
	V_{OUT2}	Sink open drain pin	− 0.5~10	
	V_{OUT3}	Source open drain pin	− 35~V_{DD} + 0.5	
Output Current (per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports R3, R6, R7, R8, R9	3.2	
	I_{OUT3}	Ports P4, P5	− 5	
	I_{OUT4}	Ports PA, PB, PC, PD	− 25	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
	ΣI_{OUT4}	Ports PA, PB, PC, PD	− 100	
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55~125	°C
Operating Temperature	T_{opr}		− 30~70	°C

RECOMMENDED OPERATING COMDITIONS (V_{SS} = 0V, T_{opr} = − 30~70°C)

PARAMETER	SAYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Nomal mode	4.5	6.0	V
			In the SLOW mode	3.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geq$ 4.5V	V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		V_{DD} × 0.75		
	V_{IH3}		V_{DD} < 4.5V	V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geq$ 4.5V	0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.25	
	V_{IL3}		V_{DD} < 4.5V		V_{DD} × 0.1	
Clock Frequency	fc		High frequency clock	0.4	4.2	MHz
	fs		Low frequency clock	30.0	34.0	KHz

Note. Input voltage V_{IH3}, V_{IL3} : in the SLOW mode

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = −30~70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	±2	μA
	I_{IN2}	Ports R (open drain)					
Input Resistance	R_{IN1}	Port K0		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Pull-down Resistance	R_K	Source open drain	V_{DD} = 5.5V, V_{KK} = −30V	−	80	−	
Output Leakage Current	I_{LO1}	Sink open dtrain	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
	I_{LO2}	Source open drain	V_{DD} = 5.5V, V_{OUT} = −32V	−	−	−2	
Output Level High Voltage	V_{OH}	Ports R4, R5	V_{DD} = 4.5V, I_{OH} = −2mA	2.4	−	−	V
Output Level High Voltage	V_{OL}	Ports P3, R7~9 P	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	
High Level Input Current	I_{OH}	Ports RA~RD	V_{DD} = 4.5V, V_{OH} = 2.4V	−	−15	−	mA
Low Level Input Current	I_{OL}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	−	20	−	
Supply Currnt (In the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
Supply Currnt (In the SLOW mode)	I_{DDS}		V_{DD} = 3.0V fs = 32.768KHz	−	30	60	μA

Note 1. Typ. values show those at Topr = 25°C, VDD = 5V

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD} : V_{IN} = 5.3V / 0.2V
The K0 port is open when the input resistor is containd.
The voltage applied to the R port is within the valid range.

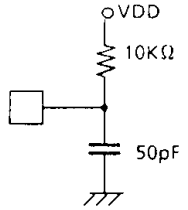
Note 4. Supply Current I_{DDS} : V_{IN} = 2.8V / 0.2V
Only low frequency clock is only osillated (connecting XTIN,TOUT).

A.C. CHARACTERISTICS

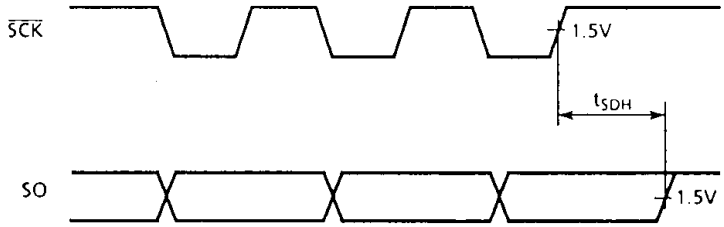
(V_{SS} = 0V, V_{DD} = 4.5~6.0V, T_{opr} = -30~70°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	1.9	–	20	μs
		In the SLOW mode	235	–	267	
High level clock pulse width	t_{WCH}	External clock	80	–	–	ns
Low level clock pulse width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. External circuit for $\overline{SCK}$ Pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5~6.0V, T_{opr} = – 30~70°C)

(1) 4MHz

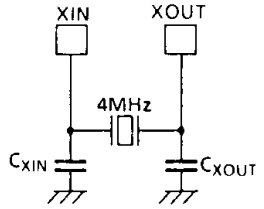
Ceramic Resonator

CSA 4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-4.00MS (KYOCERA) 〃

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

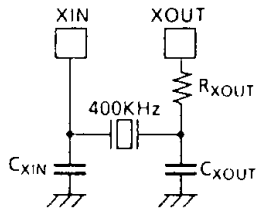


(2) 400KHz

Ceramic Resonator

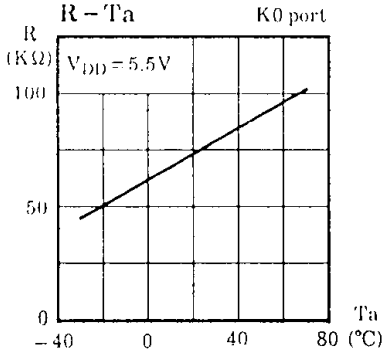
CSB 400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ

KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

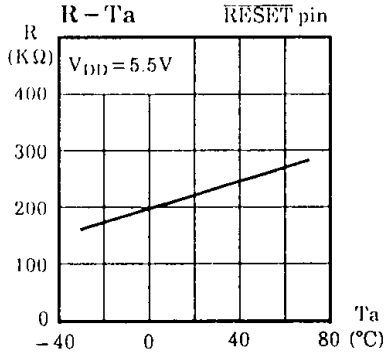


TYPICAL CHARACTERISTICS

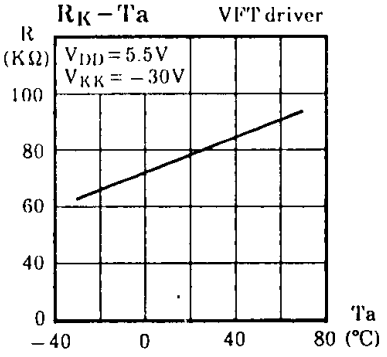
R – Ta K0 port



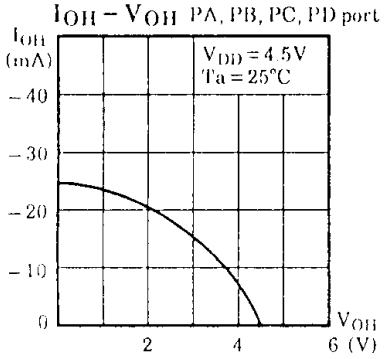
R – Ta $\overline{\text{RESET}}$ pin



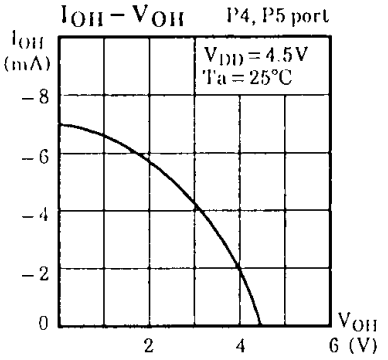
R_K – Ta VFT driver



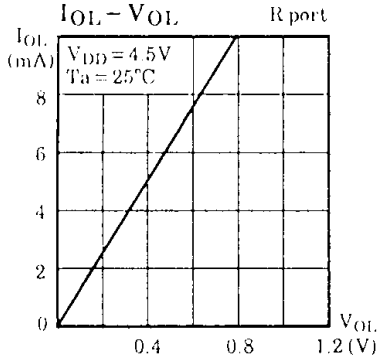
I_{OH} – V_{OH} PA, PB, PC, PD port



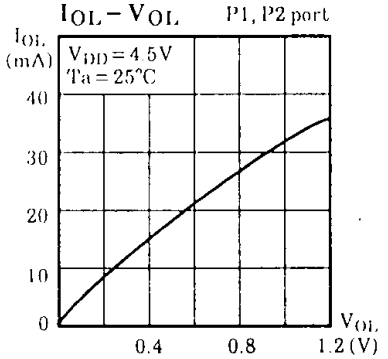
I_{OH} – V_{OH} P4, P5 port



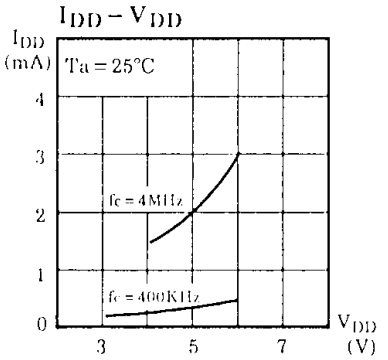
I_{OL} – V_{OL} R port



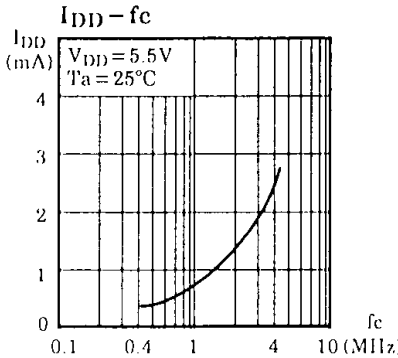
I_{OL} – V_{OL} P1, P2 port



I_{DD} – V_{DD}



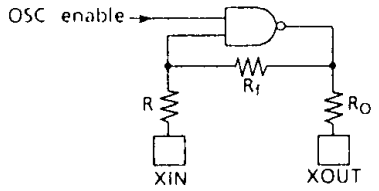
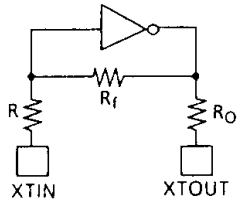
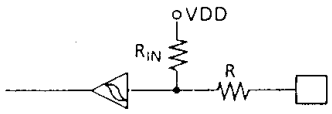
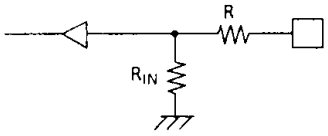
I_{DD} – fc



INPUT/OUTPUT CURCUITRY

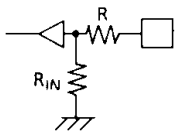
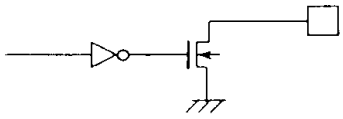
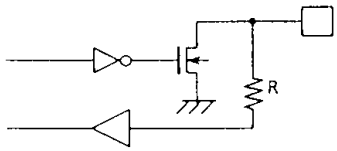
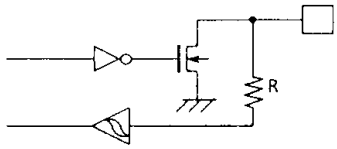
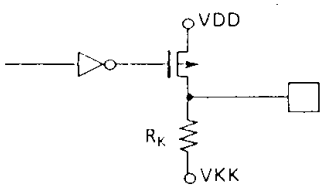
(1) Control pins

Input/Output circuitries of the 47C475A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Osc. connecting pin (High-frequency) R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
XTIN XTOUT	Input Output		Osc. connecting pin (Low-frequency) R = 1KΩ (typ.) Rf = 15MΩ (typ.) RO = 200KΩ (typ.)
RESET	Input		Hysterisis input Contained pull-up resistor RIN = 220KΩ (typ.) R = 1KΩ (typ.)
TEST	Input		Contained pull-down resistor RIN = 70KΩ (typ.) R = 1KΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 47C475A I/O ports are appointed by a code (MC) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUT (CODE : MC)	REMARKS
K0	Input		Pull-down rersistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
P1 P2	Output		Sink open drain output Initial "Hi-Z" High drive current I_{OL} = 20mA (typ.)
R3 R6 R7	I/O		Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)
P4 P5 PA PB PC PD	Output		Source open drain output Initial "Hi-Z" Pull-down resistor R_K = 80KΩ (typ.)

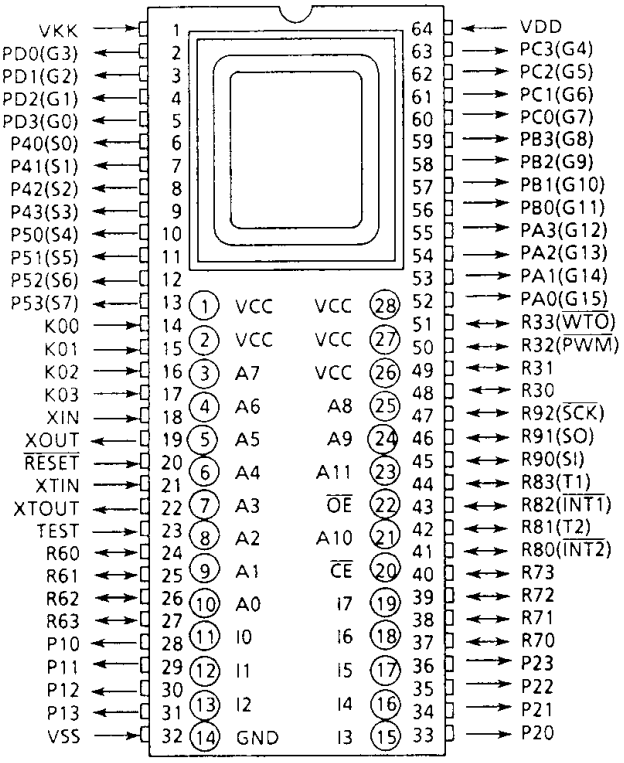
CMOS 4-BIT MICROCONTROLLER

TMP47C975AE

The 47C975A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C475A application systems (programs).
The 47C975A is pin compatible with the 47C475A which are mask-programed ROM devices.

PIN ASSIGNMENT (TOP VIEW)

SDIC64



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V C_L = 100pF Topr = – 30 to 70°C	–	–	150	ns
Data Setup Time	t_{IS}		150	–	–	ns
Data Hold Time	t_{IH}		50	–	–	ns

NOTES FOR USE

(1) Program memory

The program area is shown in Figure1.

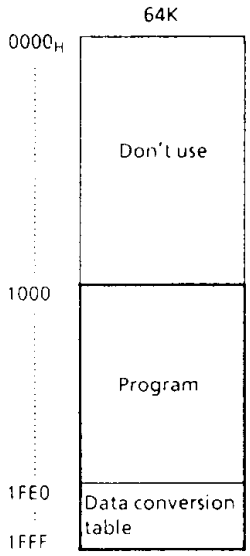


Figure 1. Program area

(2) I/O ports

The input/output circuit for the 47C975A input/output port is the same as that of the 47C475A (code : MC) , except that pulldown resistor is not built into the K0 port.

When this chip is used as evaluator for code MC, it is necessary to provide the external resistors.

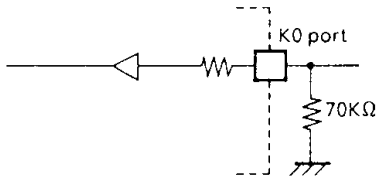


Figure 2. External Circuitry