CMOS 4-BIT MICROCONTROLLER

TMP47C446AF

The 47C446A has LCD driver, 8-bit A/D converter, and watchdog timer based on the TLCS-47 CMOS series. The 47C446A has two oscillation circuit. It is possible to switch the operation mode; high speed operation and low power consumption operation.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C446AF	4096 x 8-bit	256 x 4-bit	QFP64	TMP47C946AG

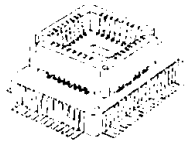
FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆89 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (24 pins)
  - Input 1port 4pins
  - I/O 4ports 20pins
- ◆Interval timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Watchdog Timer
- ◆Serial Interface with 4-bit buffer
  External/internal clock, leading/trailing edge shift mode
- ◆LCD driver (automatic display)
  - LCD direct drive (Max. 12-digit display at 1/4 duty LCD)
  - 1/4, 1/3, 1/2 duty or static drive are programmably selectable.
- ◆8-bit successive approximate type A/D converter
  - With sample and hold
  - 4 analog inputs
  - Converting time : 48μs (4MHz)
- ◆Dual-clock operation
  High-speed/Low-power-comsumption operating mode
- ◆Real Time Emulator : BM47220A

QFP64

TMP47C446AF

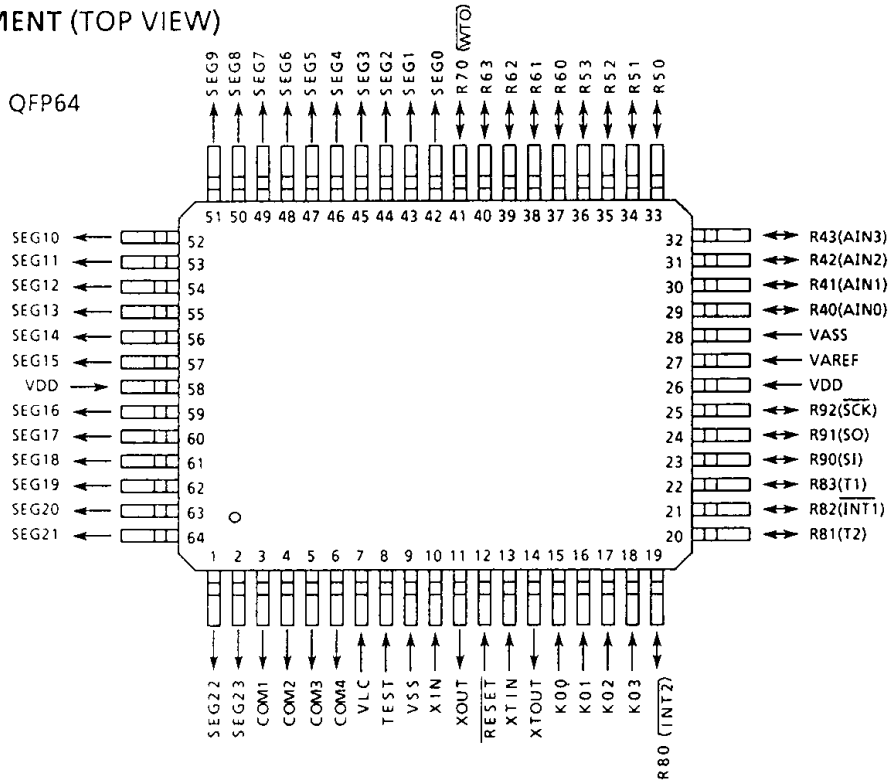
QFC64



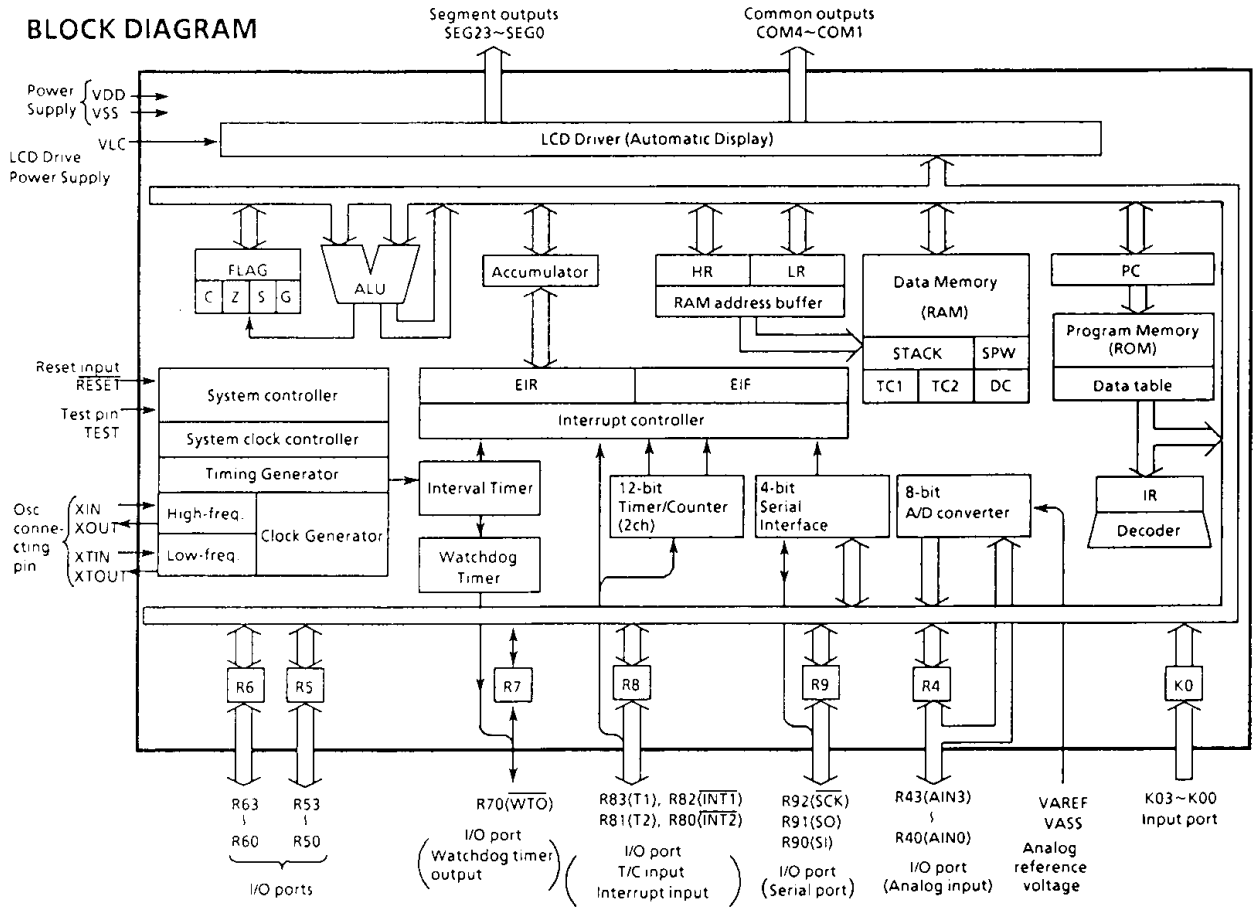
TMP47C946AG

PIN ASSIGNMENT (TOP VIEW)

QFP64



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
R43 (AIN3) - R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	A/D converter analog input
R53 - R50	I/O	1-bit I/O port with latch. When using as input port, the latch must be set to "1".	
R63 - R60			
R70 ($\overline{WTO}$)	I/O (Output)	1-bit I/O port with latch	Watchdog timer output
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When using as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
SEG23 - SEG0	Output	LCD Segment output	
COM4 - COM1		LCD Common output	
XIN	Input	Osc. connecting pins (High-frequency). For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
XTIN	Input	Osc. connecting pins (Low-frequency). For inputting external clock, XTIN is used and XTOUT is opened.	
XTOUT	Output		
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	
VLC		LCD drive power supply	
VAREF		A/D converter analog reference voltage (High)	
VASS		A/D converter analog reference voltage (Low)	

OPERATIONAL DESCRIPTION

Conserning the 47C446A, the hardware configuration and operation are described.
As the description included mainly differences from the 47C400A, refer to thr technical data sheets for the 47C400A. The 47C446A does not have the hold function.

1. SYSTEM CONFIGURATION

(1) I/O Ports
(2) System Clock Controller
(3) Interval Timer
(4) Timer/Counter (TC1, TC2)
(5) Serial Interface
(6) LCD Driver
(7) A / D Converter
(8) Watchdog Timer

2. PERIPHERAL HARDWARE FUNCTION

2.1 Ports

The 47C446A has 7 I/O ports (24 pins) each as follows :

① K0	;	4-bit input
② R4	;	4-bit input/output (shared by the A/D converter analog inputs)
③ R5, R6	;	4-bit input/output
④ R7	;	1-bit input/output (shared by the watchdog timer output)
⑤ R8	;	4-bit input/output(shared by external interrupt request input and timer/counter input)
⑥ R9	;	3-bit input/output (shared by serial port)

This section describes ports of ② and ④ which are changed from the 47C400A.
Ports P1, P2 and KE are eliminated from the 47C400A.
The 5-bit to 8-bit data conversion instruction [OUTB @HL] is not valid.
Table 2-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port R4 (R43-R40)
Port R4 is 4-bit I/O ports with latch shared by the analog inputs for A/D converter. When used as an input port or analog input, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during A/D conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

Port R4 (Port address OP04 / IP04)

3	2	1	0
R43 (AIN3)	R42 (AIN2)	R41 (AIN1)	R40 (AIN0)

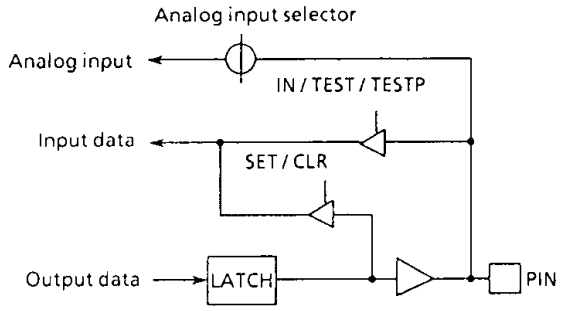


Figure 2-1. Port R4

Port Address (**)	Port		Input/output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port (Analog input)	R4 output port	○	○	○	–	–	–	–
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	○
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	——	——	–	–	–	–	–	–	–
0B	——	——	–	–	–	–	–	–	–
0C	A/D Status input	——	○	–	–	–	–	○	–
0D	A/D converted Value	——	○	–	–	–	–	–	–
0E	SIO, Hold status	——	○	–	–	–	–	○	–
0F	Serial recieve buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	——	–	–	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	A/D analog input selector	–	○	–	–	–	–	–
13	Undefined	A/D start register	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval timer intrrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	LCD Drive control	–	○	–	–	–	–	–
1C	Undefined	Timer/counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note. *"——" means the reserved state. Unavailable for the user programs.*

Table 2-1. Port Address Assignments and Available I/O Instructions

(2) Port R7 (R70)

Port R7 is 1-bits I/O port with latch. R70 pin is shared by the watchdog timer output. To use R70 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R71, R72 and R73 pins do not exist actually but "1" is read when an input instruction is executed.

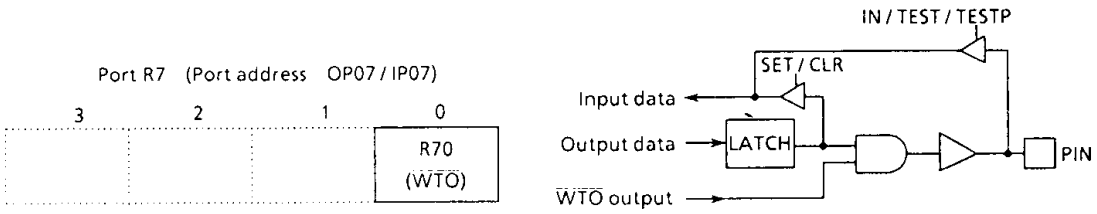


Figure 2-2. Port R7

2.2 System Clock Controller

The 47C446A has two oscillation circuits with a high-frequency clock and a low-frequency clock. Power consumption can be decreased by switching to low-speed operation using the low-frequency clock when necessary (dual clock operation). The high-frequency clock can be obtained by connecting an oscillator to the XIN and XOUT pins; the low-frequency clock can be obtained by connecting the oscillator to the XTIN and XTOUT pins.

2.2.1 Circuit Configuration

Figure 2-3 shows the configuration of system clock controller.

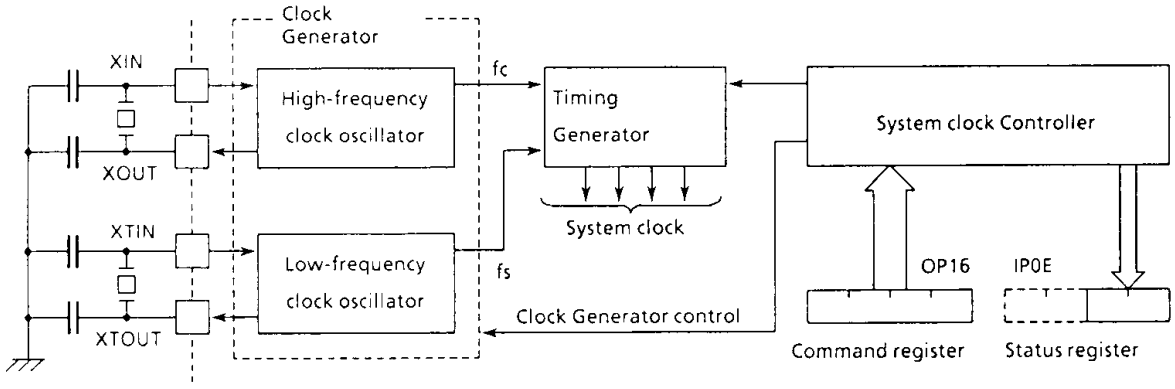


Figure 2-3. System Clock Controller

2.2.2 Dual Clock Operation and Control

Dual clock operation involves two modes : Normal operating mode using the high-frequency clock, and SLOW operating mode using the low-frequency clock. Both oscillators start operating when the power is turned on, after which the Normal operation is selected automatically. The high-frequency clock stops oscillating when a command is issued to switch to the SLOW operation. Operating mode switching is performed using the command register (OP16). The status of the low-frequency clock and the current operating mode can be monitored using the status register (IP0E) . Figure 2-4 shows the operating mode transitions, and Figure 2-5 shows the command and status registers.

(1) Operaiting Mode Transmission

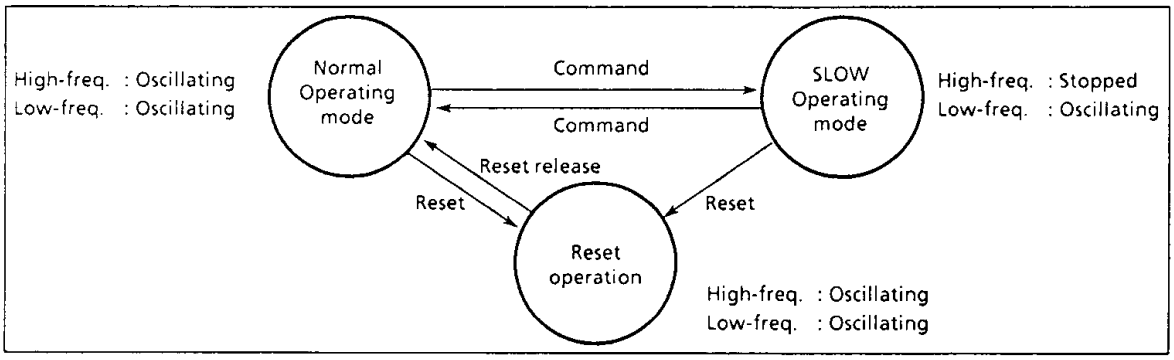


Figure 2-4. Operating Mode Transmission Diagram

(2) Operation Mode Control

System clock control command register (Port address OP16)

3	2	1	0	
LF		DWUT		(Initial value 0000)

Selects operating mode

00 : Normal operating mode
01 : SLOW operating mode
1* : Reserved

Sets warm up time

		Example : At fs = 32.768KHz
00 :	2^4 / fs [sec]	..... 0.5 [ms]
01 :	2^8 / fs	..... 7.8
1* :	2^{11} / fs	..... 62.5

*Note 1. * ; don't care*
Note 2. fs ; Low-frequency clock [Hz]

System clock control status register (Port address IP0E)

3	2	1	0
		SMF	SLS

Low-frequency clock oscillating state

0 : Not oscillating or unstable oscillation
1 : Stable oscillation

Operation state monitor

0 : In Normal operation
1 : In SLOW operation

Figure 2-5. Command register and Status register

Note 1. The following operations and functions cannot be used in the SLOW operation ; therefore, this must be taken into consideration in programming.

① Timer/Counter 4096Hz (at fs = 32.8kHz) count operation (can be used with other count rates).

② Interval timer interrupt 4096Hz (at fs = 32.8kHz) operation (can be used with other timer rates).

③ Serial Interface

Note 2. The power consumption of the oscillator and internal hardware is decreased in the SLOW operation, but power consumption through pin interfaces (dependent on the external circuitry and program) may prevent overall low power consumption operation ; therefore , caution is necessary during system design and interface circuit design.

(3) Operation mode switching

The following procedure is used to switch between the Normal operation and the SLOW operation. The Normal operation is selected during reset. Also, the current operating mode can be checked by monitoring SLS (status register bit 0) .

a. Switching from Normal operation to SLOW operation

After monitoring SMF (status register bit 1) by program and confirming that the low-frequency clock is stable, set bit 2 of the command register to "1" . The high-frequency clock will then stop. Also, after switching from Normal operation to SLOW operation (accessing the command register) , execute the NOP (No Operation) instruction.

b. Returning from SLOW operation to Normal operation

When bit 2 of the command register is cleared to "0" , the warm-up time must be set in DWUT. When the set warm-up time elapses, operation is switched to the Normal operation.

Example 1 : Normal operation → SLOW operation.

```
SSMF:   TEST    %IP0E, 1        ; To wait until SMF goes to "1" .
        B       SSMF
        LD      A, #0100B       ; Selects SLOW operating mode
        OUT     A, %OP16
        NOP                     ; no operation
        :
```

Example 2 : SLOW operation → Normal operation

```
        LD      A,  #0001B      ; Selects Normal operation and sets warm-up
        OUT     A,  %OP16         time (7.8ms)
        :
```

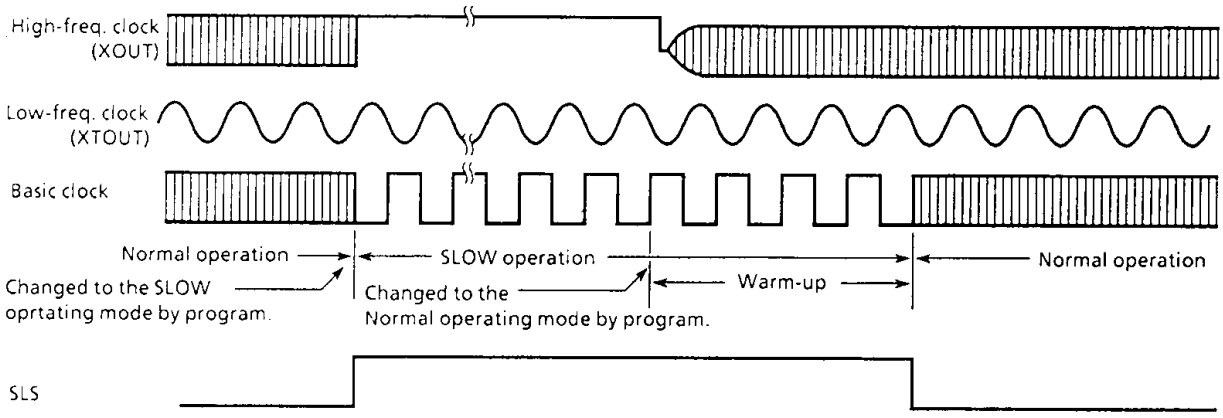


Figure 2-6. System Clock Switching Timing

2.3 Interval Timer

2.3.1 Configuration of Interval Timer

The interval timer is configured with a 15-stage binary counter and inputs the oscillation circuit output (fs) for the low-frequency clock; therefore, the final stage output is fs/2^{15} [Hz]. This interval timer is cleared to "0" during reset.

Also, "fs" is input directly into the interval timer; therefore, the interval timer interrupts, timer/counter and LCD driver will not operate normally if the low-frequency oscillation is not stable.

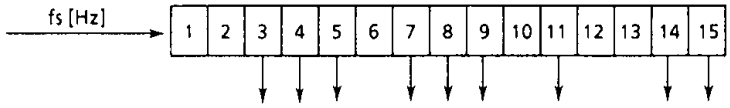


Figure 2-7. Interval Timer

2.3.2 Interval Timer Interrupt (ITMR)

Constant-frequency interrupts can be generated using the interval timer, Four different frequencies can be selected for interval timer interrupts using the command register (OP19). The command register is also initialized to "0" during reset.

An interval timer interrupt is generated at the first rising edge of the binary counters output after the command is set to the command register.

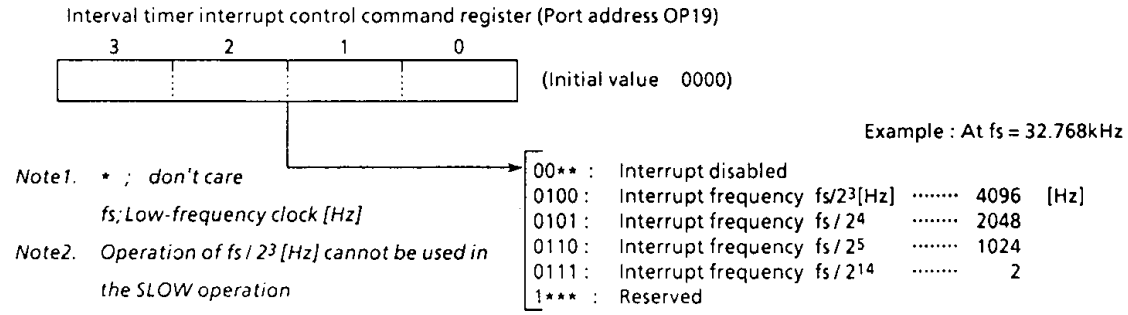


Figure 2-8. Command Register

2.4 Timer/Counter

The timer/counter of the 47C446A is operated by a low-frequency clock (fs); therefore, the following operating frequencies differ from those of the 47C400A.

① Internal pulse rate.
② Maximum frequency applied in the event counter mode.
③ Drop ratio of instruction execution time when the timer is used.

(1) Internal pulse rate

The intrnal pulse rates shown in Table 2-2 can be selected by setting the values of the lower 2 bits of the TC1 and TC2 control command registers (OP1C, OP1D).

The values of lower 2 bits (bit1, 0)	Internal pulse rate	Max. setting time	At fs = 32.768KHz	
			Internal pulse rate	Max. setting time
00	fs / 2^3 [Hz]	2^{15} / fs [sec]	4096 [Hz]	1 [sec]
01	fs / 2^7	2^{19} / fs	265	16
10	fs / 2^{11}	2^{23} / fs	16	256
11	fs / 2^{15}	2^{27} / fs	1	4096

Table 2-2. Internal Pulse Rate

(2) Maximum frequency applied in the event counter mode.

		Nornal operating mode	SLOW operating mode
a. In 1-channel operation		fc / 32 [Hz]	fs / 32 [Hz]
b. In 2-channel operation	TC1	fc / 32	fs / 32
	TC2	fc / 40	fs / 40

(3) Drap ratio of instruction execution time when the timer is used.
With the 47C446A, count operation is inserted in the ratio of once per [(basic clock frequency) /2^3] / (internal pulse rate) instruction cycle; therefore, execution speed drops as follows:

$$100 \div \left\{ \frac{\text{(basic clock frequency)} / 2^3}{\text{(internal pulse rate)}} - 1 \right\} \%$$

Example 1: When fc = 4MHz and fs = 32.8kHz in the Normal operation and the internal pulse rate fs/2^3 is selected, count operation is inserted once per each cycle of 122 instructions; therefore, there is a drop of 100/121 = 0.83% for an instruction execution speed of 2μs.

Example 2: When fs = 32.8kHz in the SLOW operation and the internal pulse rate fs/2^{11} is selected, count operation is inserted once per each cycle of 256 instructions; therefore, there is a drop of 0.39% for an instruction execution speed of 244μs. In addition, when the basic clock is obtained from "fs" (SLOW operation), count operation cannot be used with an internal pulse rate of fs/2^3.

2.5 Serial Interface

When operating using the internal clock, fs/2^2 [Hz] is used as the serial clock. Consequently, when operating at fs = 32.768kHz, the maximum transfer rate is 8192bps. When the reading and writing of serial data cannot follow this clock rate, the serial clock is automatically stopped and the next shift operation stands by untill the processing is completed.
External clock can be used in the same way as for the 47C400A. The serial interface cannot be used in the SLOW operating mode.

2.6 LCD Driver

The 47C446A has the circuit that directly drivers the Liquid Crystal Display (LCD) and its control circuit.
The 47C446A has the following connecting pins with LCD.

① Segment output pins 24 pins (SEG23 - SEG0)
② Common output pins 4pins (COM4 - COM1)

In addition, VLC pin is provided as the driver power.

The devices that can be directly driven is selectable from LCD of following drive methods :

① 1 / 4 duty (1 / 3 bias) LCD ..... Max.96 segments (8 segments × 12 digits)
② 1 / 3 duty (1 / 3 bias) LCD ..... Max.72 segments (8 segments × 9 digits)
③ 1 / 2 duty (1 / 2 bias) LCD ..... Max.48 segments (8 segments × 6 digits)
④ Static LCD ..... Max.24 segments (8 segments × 3 digits)

2.6.1 Configuration of LCD driver

Figure 2-9 shows the configuration of LCD driver.

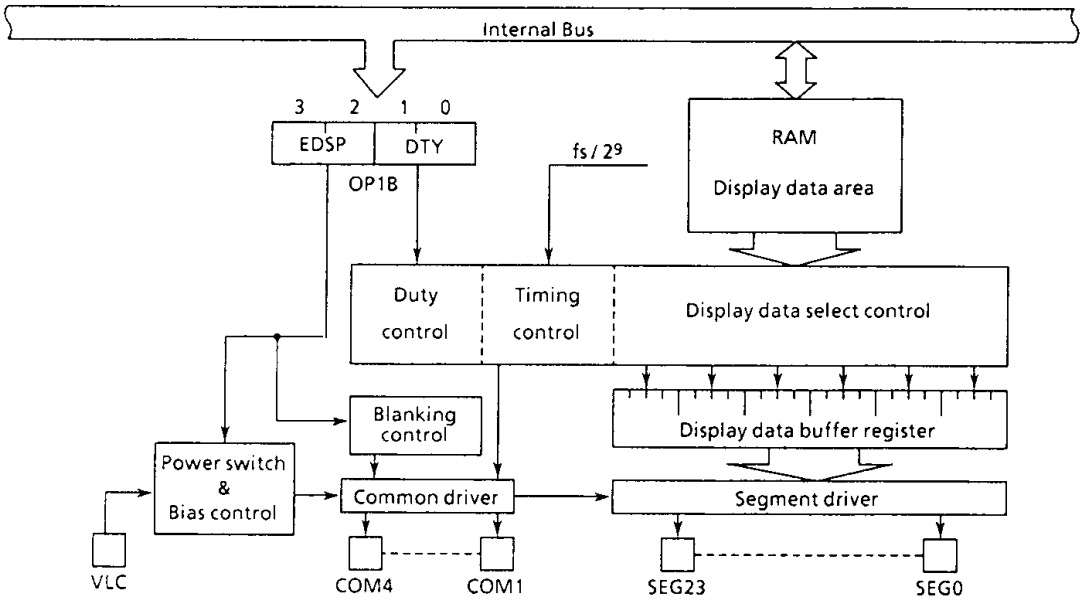


Figure 2-9. Configuration of LCD Driver

2.6.2 Control of LCD Driver

The LCD driver is controlled by the command register (OP1B).

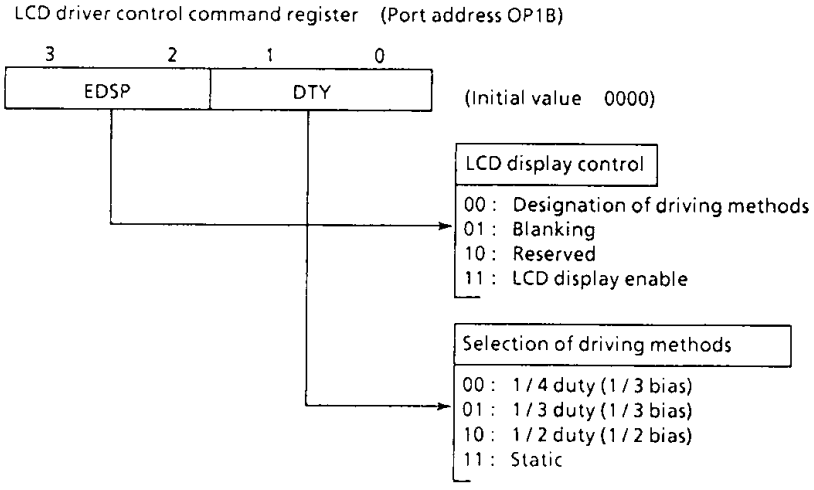
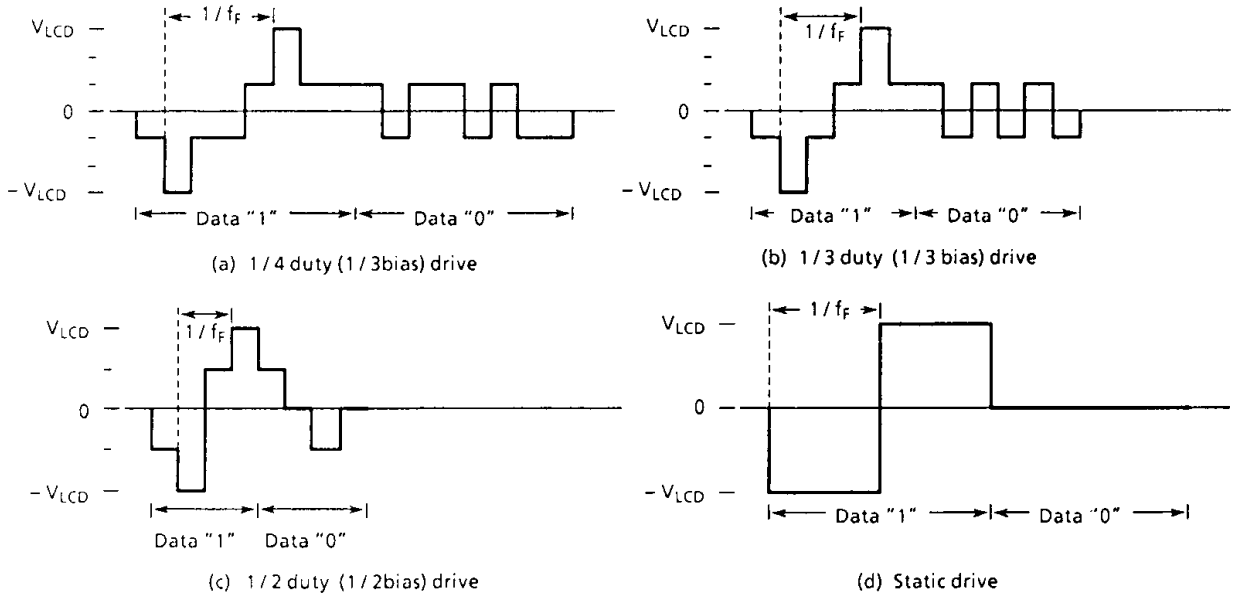


Figure 2-10. LCD Driver Control Command Register

(1) Driving methods of LCD

4 kinds of driving methods can be selected by DTY (bits 1 and 0 of command register).

Figure 2-11 shows driving waveforms for LCD.



Note. : f_F ; LCD Frame frequency V_{LCD} ; LCD drive voltage (= V_{DD}-V_{LC})

Figure 2-11. Driving Waveform for LCD (Voltage COM-SEG Pins)

(2) Frame frequency

The frame frequency is set accoding to the driving method and base frequency as shown in Table 2-3. The base frequency is given by the Interval Timer.

Base Frequency[Hz] \ Driving Method	Frame Frequency [Hz] 1 / 4duty	1 / 3duty	1 / 2duty	static
$\frac{fs}{2^9}$	$\frac{fs}{2^9}$	$\frac{4}{3} \cdot \frac{fs}{2^9}$	$\frac{4}{2} \cdot \frac{fs}{2^9}$	$\frac{fs}{2^9}$
At fs = 32.768KHz	64	85	128	64

fs ; Basic clock frequency [Hz]

Table 2-3. Frame Frequency Setting

(3) LCD drive voltage

The LCD drive voltage (V_{LCD}) is given by the difference in potential (V_{DD}-V_{LC}) between pins VDD and VLC. Therefore, when the CPU operating voltage and LCD drive voltage are the same, the VLC pin is connected to the VSS pin.

The LCD light only when the difference in potential between the segment output and common output is $\pm V_{LCD}$, and turn off at all other times.

During reset, the power switch of the LCD driver is turned off automatically, shutting off the VLC voltage. Both the segment output and common output become V_{DD} level at this time and the LCD turn off.

The power switch is turned on to supply VLC voltage to the LCD driver by setting EDSP (bits 2 and 3 of the command register) to "11_B". After that, the power switch will not turn off even during blanking (setting EDSP to "01_B") and the VLC voltage continues to flow.

2.6.3 LCD Display Operation

(1) Display data setting

Display data are stored to the display data area (Max. 24 words) in the data memory.

The display data stored to the display data area are read automatically and sent to the LCD driver by the hardware.

The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Thus, display patterns can be changed by merely overwriting the contents of the display data area with a program. The table look up instruction is mainly used for this overwriting.

Figure 2-12 shows the correspondence between the display data area and the SEG/COM pins. The LCDs light when the display data is "1" and turn off when "0".

The number of segment which can be driven differs depending on the LCD drive method; therefore, the number of display data area bits used to store the data also differs (Refer to Table 2-4). Consequently, data memory not used to store display data and data memory for which the addresses are not connected to LCDs can be used to store ordinary user's processing data.

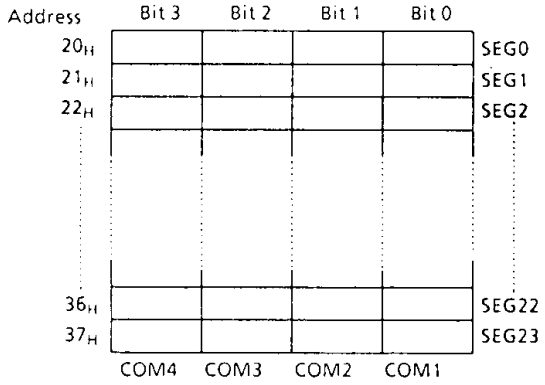


Figure 2-12. Display Data Area and SEG/COM

Driving Method	Bit 3	Bit 2	Bit 1	Bit 0
1/4 duty	COM4	COM3	COM2	COM1
1/3 duty	–	COM3	COM2	COM1
1/2 duty	–	–	COM2	COM1
Static	–	–	–	COM1

Note. – ; This bit is not used for display data.

Table 2-4. Driving Method and Bit for Display Data

(2) Blanking

Blanking is applied by setting EDSP to "01_B" and turns off the LCD by outputting the non light operation level to the COM pin. The SEG pin continuously outputs the signal level in accordance the display data and drive method.

With static drive, no voltage is applied between the COM and SEG pins when the LCD is turned off by data (display data cleared to "0"), but the COM pin output becomes constant at the $V_{LCD}/2$ level when turning off the LCD by blanking, so the COM and SEG pins are then driven by $V_{LCD}/2$.

2.6.4 Control Method of LCD Driver

(1) Initial Setting

Flow chart of initial setting is shown Figure 2-13.

Example : Driving of 1/4duty LCD

```
        LD      A, #0000B   ; Sets 1/4 duty drive
        OUT     A, %OP1B
        :                   ; Initializes display data area
        :
        LD      A, #1100B   ; Display enable (Relese of blanking)
        OUT     A, %OP1B
        :
```

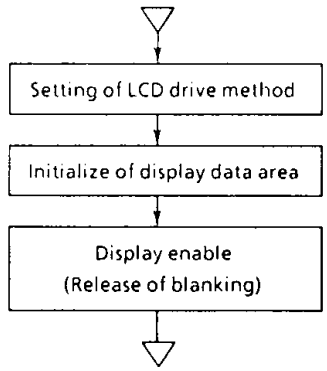


Figure 2-13. Initial Setting of LCD Driver

(2) Display data setting

Normally, display data are kept permanently in the program memory and are then stored to the display data area by the table look-up instruction. This can be explained using numerical display with 1/4 duty LCD as an example. The COM and SEG connections to the LCD are the same as those shown in Figure 2-14 and the display, data are as shown in Table 2-5.

Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20_H and 21_H.

```
        LD      HL, #0FCH           ; To set the DC
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16 ,@HL+
        ST      #DTBL/256,@HL+
        LD      HL,#20H             ; Display of data corresponding
        LDL     A, @DC
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        :
DTBL : DATA     11011111B, 00000110B, 11100011B, 10100111B, 00110110B,
                10110101B, 11110101B, 00010111B, 11110111B, 10110111B
```

Numeral	Display	Display data		Numeral	Display	Display data	
		Upper	Lower			Upper	Lower
0	0.	1101	1111	5	5	1011	0101
1	1	0000	0110	6	6	1111	0101
2	2	1110	0011	7	7	0001	0111
3	3	1010	0111	8	8	1111	0111
4	4	0011	0110	9	9	1011	0111

Table 2-5. Examples of Display Data (1/4 Duty LCD)

Table 2-6 shows the same numerical display used in Table 2-5, but using 1/2 duty LCD are the same as those shown in Figure 2-16.
Programming example for displaying numerals corresponding to BCD data stored at address 10_H in the data memory is shown below. The display data area is at addresses 20 through 23_H.

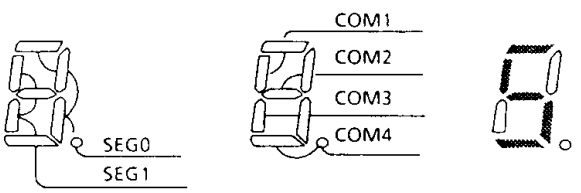
```
        LD      HL, #0FCH           ; To set the DC
        LD      A, 10H
        ST      A, @HL+
        ST      #DTBL/16, @HL+
        ST      #DTBL/256, @HL+
        LD      HL, #20H            ; Display of data corresponding
        LDL     A, @DC
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
        LDH     A, @DC+
        ST      A, @HL+
        RORC    A
        RORC    A
        ST      A, @HL+
         :
DTBL :  DATA    01110111B, 00100010B, 10010111B, 10100111B, 11100010B,
                11100101B, 11110101B, 01100011B, 11110111B, 11100111B
```

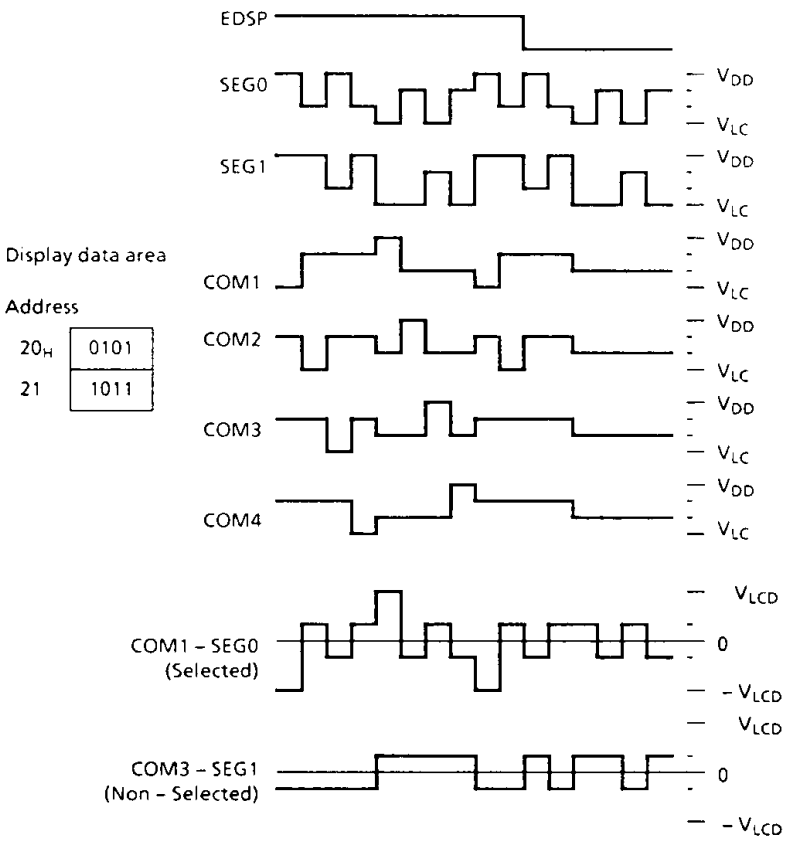
Numeral	Display data				Numeral	Display data			
	Upper			Lower		Upper			Lower
0	**01	**11	**01	**11	5	**11	**10	**01	**01
1	**00	**10	**00	**10	6	**11	**11	**01	**01
2	**10	**01	**01	**11	7	**01	**10	**00	**11
3	**10	**10	**01	**11	8	**11	**11	**01	**11
4	**11	**10	**00	**10	9	**11	**10	**01	**11

*Note. * ; don't care*

Table 2-6. Examples of Display Data (1/2 Duty LCD)

(3) Driving Example



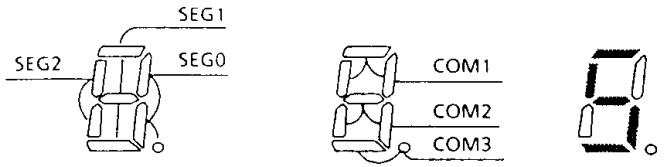


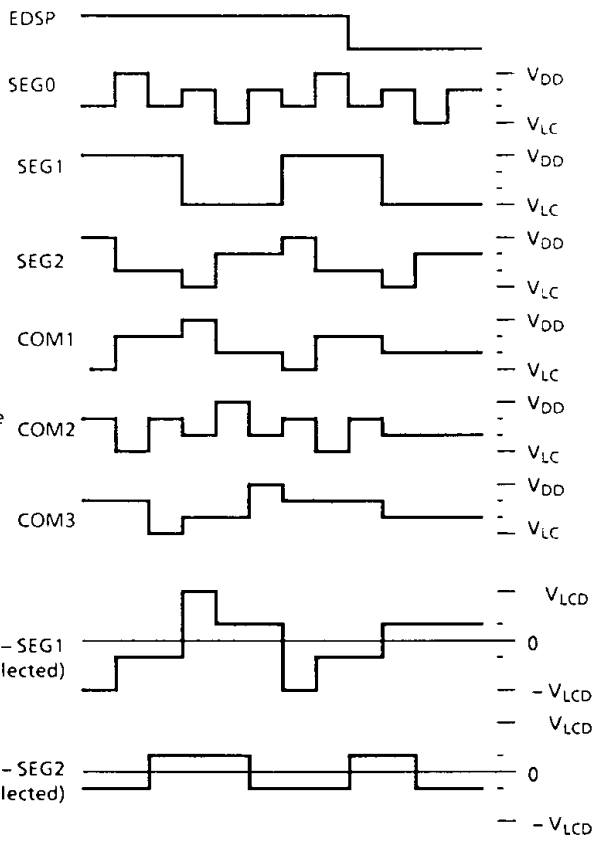
Display data area

Address

20_H	0101
21	1011

Figure 2-14. 1/4 Duty (1/3 Bias) Drive





Display data area

Address

20_H	*010
21	*111
22	**01

Note. ★; *don't* care

Figure 2-15. 1/3 Duty (1/3 Bias) Drive

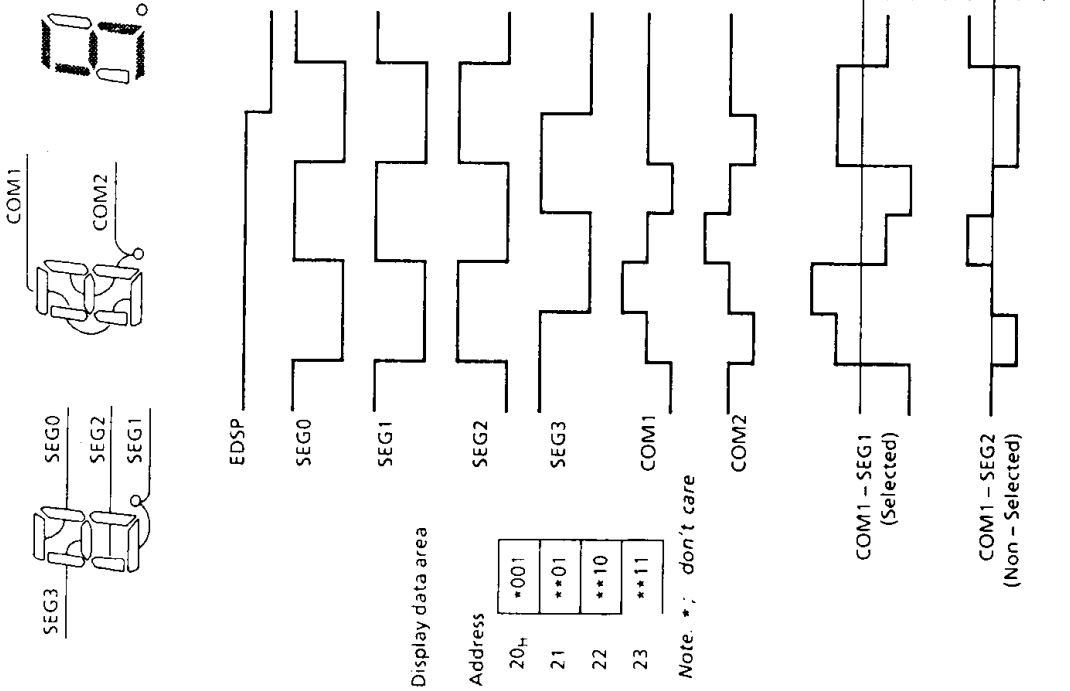


Figure 2-16. 1/2 Duty (1/2 Bias) Drive

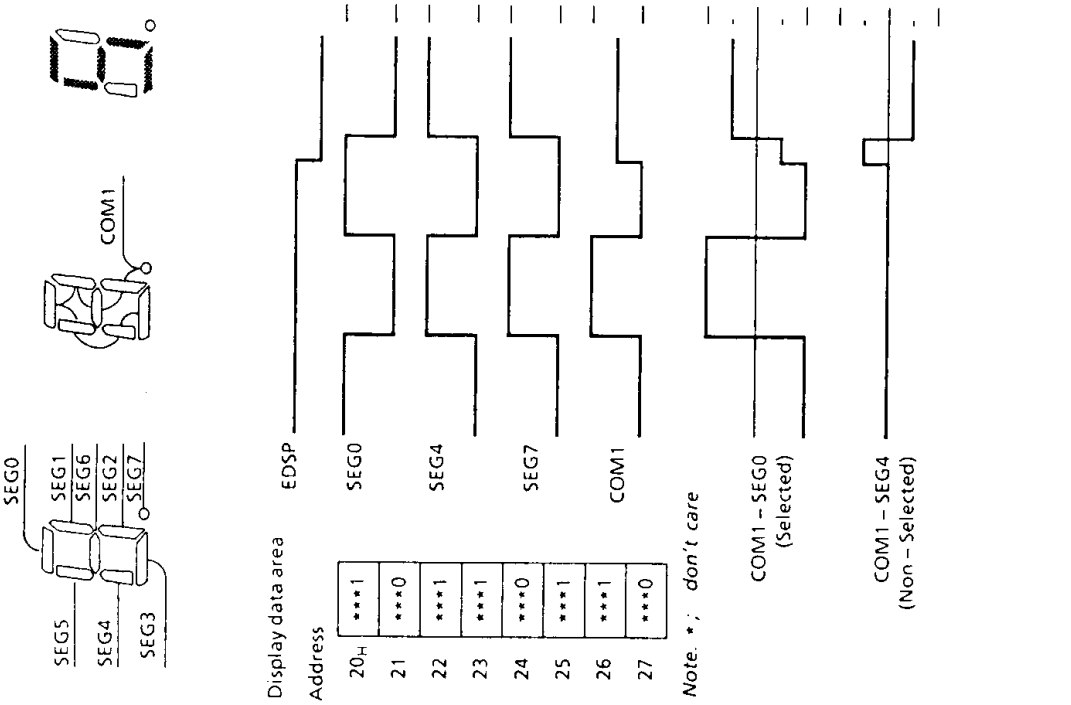


Figure 2-17. Static Drive

2.7 A/D Converter

The 47C446A has a 8-bit successive approximate type A/D converter and is capable of processing 4 analog inputs.

2.7.1 Circuit configuration

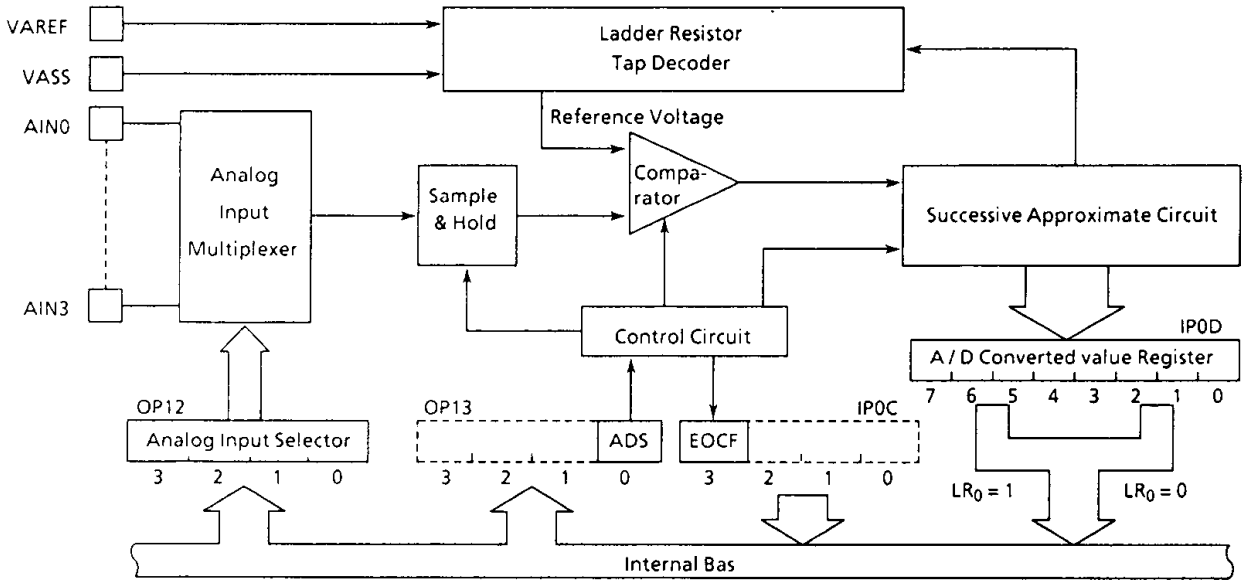


Figure 2-18. Block Diagram of A/D Converter

2.7.2 Control of A/D converter

The operation of A/D converter is controlled by a command. The command register is accessed as port adderesses OP12 and OP13. A/D converted value and end of conversion flag (EOCF) can be known by accessing port addresses IP0D and IP0C.

(1) Analog input selector

Analog inputs (AIN0 through AIN7) are selected by values of this register.

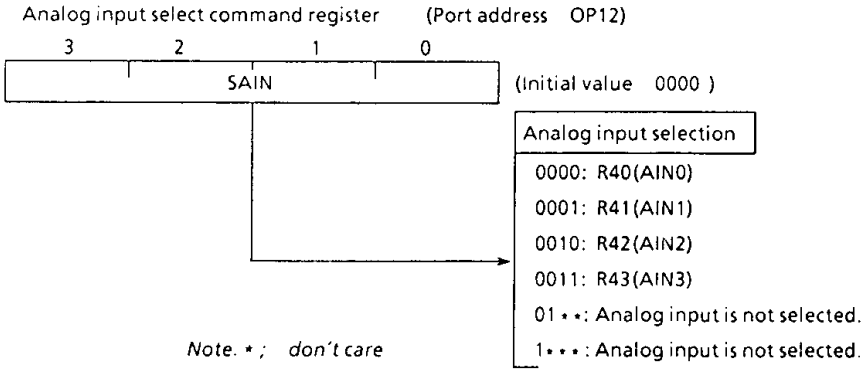


Figure 2-19. Analog input selector

(2) Start of A/D conversion

A/D conversion is started when ADS is set to "1" . After the conversion is started, ADS is cleared by hardware. If the restart is requested during the conversion, the conversion is started again at the time.

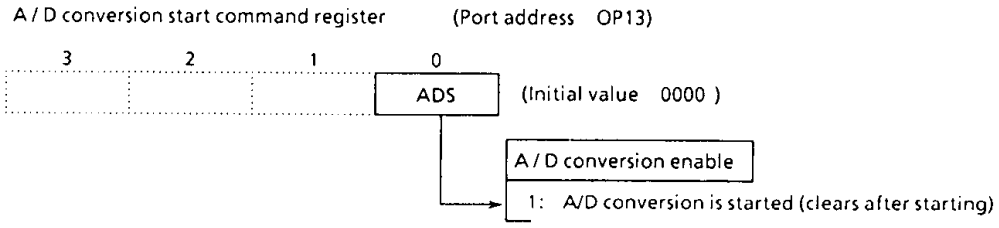


Figure 2-20. A/D conversion start register

(3) A/D converted value register

An A/D converted value is read by accessing port address IP0D. An A/D converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L-registers).

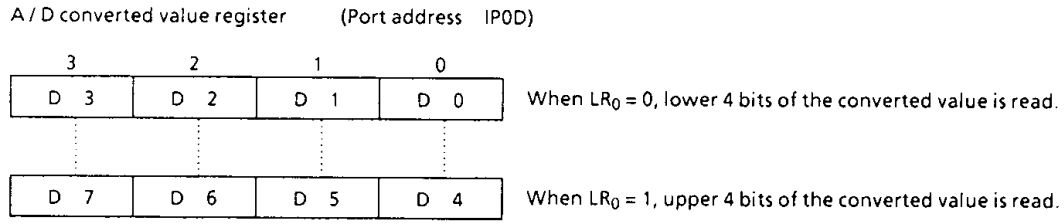


Figure 2-21. A/D converted value register

(4) A/D converter status register

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or A/D conversion is started, EOCF is cleared to "0".

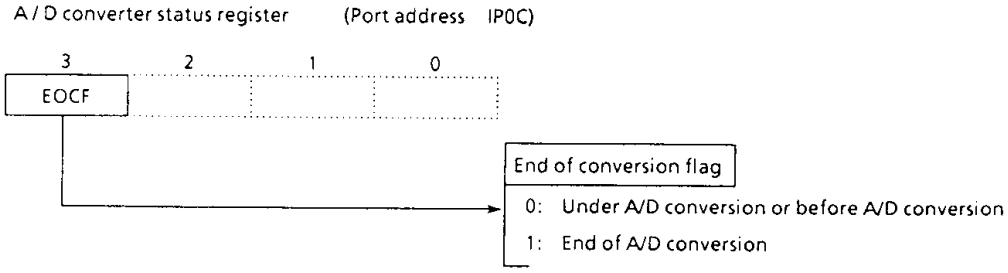


Figure 2-22. A/D converter status register

2.7.3 How to use A/D converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VASS pin. The A/D conversion is carried out by splitting reference voltage between VAREF and VASS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.

(1) Start of A / D conversion

Prior to conversion, select one of the analog input AIN0 through AIN3 by the analog input selector. Place output of the analog input, which is to be A/D converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.

A/D conversion is started by setting ADS (bit 1 of the A/D conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".

(2) Reading of an A/D converted value

After the end of conversion, read an A/D converted value is read by splitting into lower 4 bits and upper 4 bits by the A/D converted value register (IP0D).

Lower 4 bits of the A/D converted value can be read when $LR_0 = 0$ and upper 4 bits when $LR_0 = 1$. Usually an A/D converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an A/D converted value is read during the conversion, it becomes an indefinite value.

Example: Selecting analog input (AIN3), starting A/D conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
        LD      A, #3           ; Selecting analog input (AIN3)
        OUT     A, %OP12
        LD      A, #1           ; Start of A/D conversion
        OUT     A, %OP13
SLOOP : TEST    %IP0C, 3        ; To wait until EOCF goes to "1"
        B       SLOOP
        LD      HL, #10H        ; HL ← 10H
        IN      %IP0D, @HL      ; RAM [10H] ← Lower 4 bits
        INC     L               ; Increment of L registers
        IN      %IP0D, @HL      ; RAM [11H] ← Upper 4 bits
```

2.8 Watchdog timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (ranaway) of program due to external noise or other causes and return the operation to the normal condition. The watchdog timer output is output to R70 ($\overline{WTO}$) pin.

When the watchdog timer is used, the output latch of R70 must be set to "1". Further, during reset, the output latch of R70 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.8.1 Configuration of Watchdog Timer

The watchdog timer consists of 10-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

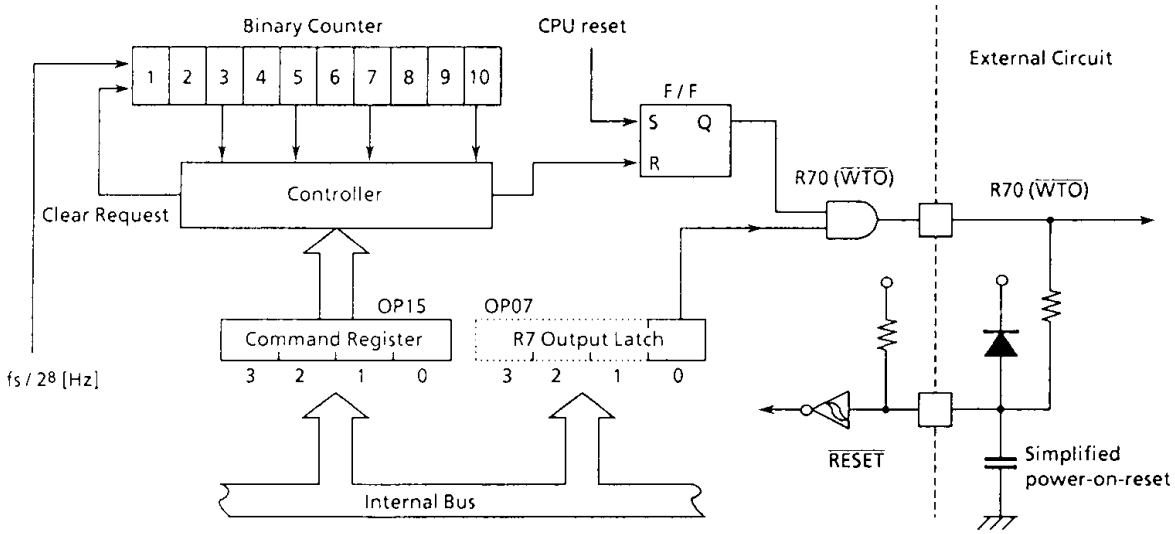


Figure 2-23. Watchdog Timer

2.8.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "1000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.

② The watchdog timer should be become enable.

③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0" at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

Watchdog Timer control command register (Port address OP15)

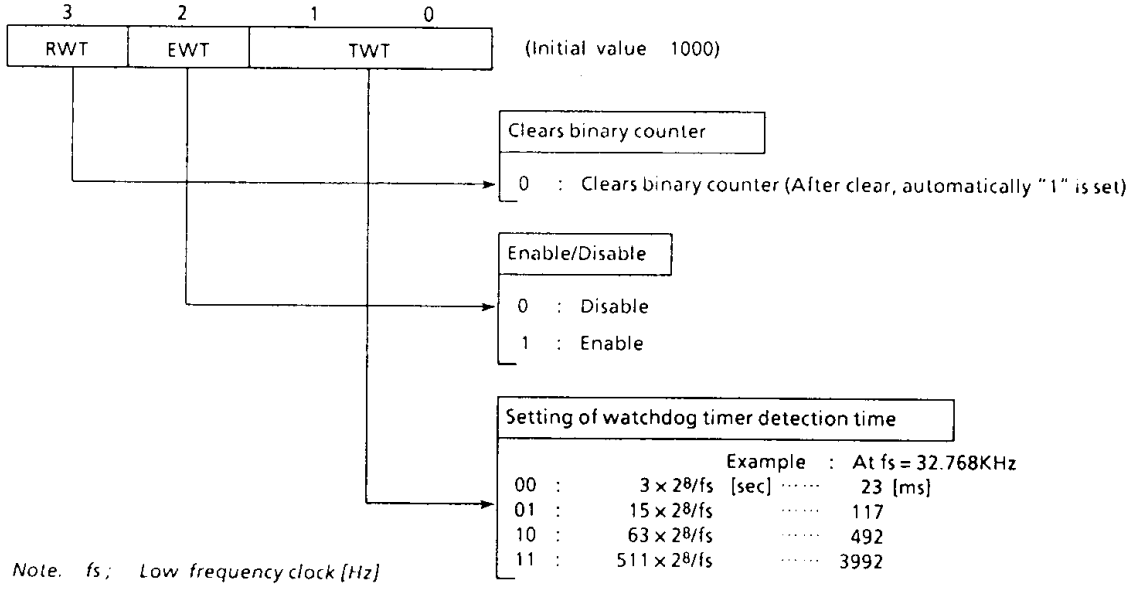


Figure 2-24. Command Register

Example : To set the watchdog detection time (63×2^8/fs [sec]). And to enable the watchdog timer.

```
        LD      A, #0010B       ; OP15 ← 0010B
                                  (Sets WDT detection time. Clears binary counter)
        OUT     A, %OP15
        LD      A, #1110B       ; OP15 ← 1110B (Enables WDT)
        OUT     A, %OP15
Within WDT
        :
detection time
        :
        :
        LD      A, #0110B       ; OP15 ← 0110B (Clears binary counter)
        OUT     A, %OP15
        :
```

Note . It is necessary to clear the binary counter prior to enabling watchdog timer. Further, when switching the system clock, the watchdog timer has to halt during the warm-up time at changing from the SLOW operating mode to the Normal operating mode.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.5 to 7	V
Supply Voltage (LCD drive)	V_{LC}		− 0.5 to V_{DD} + 0.5	V
Input Voltage	V_{IN}		− 0.5 to V_{DD} + 0.5	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include R4	− 0.5 to V_{DD} + 0.5	V
	V_{OUT2}	Ports R5-R9	− 0.5 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency (High freq.)	fc	XIN, XOUT		0.4	4.2	MHz
Clock Frequency (Low freq.)	fs	XTIN, XTOUT		30.0	34.0	KHz

Note 1. Input Voltage V_{IH3}, V_{IL3} : in the SLOW mode

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	–	–	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Level Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	–	–	– 2	mA
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	–	–	2	μA
Output High Voltage	V_{OH}	Ports R (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	–	–	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
Segment Output Resistance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} – V_{LC} = 3V	–	20	–	KΩ
Common Output Resistance	R_{OC}	COM pin					
Segment/Common Output Voltage	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5V, V_{LC} = V_{SS} fc = 4MHz	–	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3V, V_{LC} = V_{SS} fs = 32.768KHz	–	15	30	μA

Note 1. Typ. values shows those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Output Resistance Ros, Roc : Shows on-resistance at the level switching.

Note 4. $V_{O2/3}$: Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
$V_{O1/2}$: Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
$V_{O1/3}$: Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. Supply Current I_{DD} : V_{IN} = 5.3V/0.2V
The Port K0 is open when the input resistor is contained.
The voltage applied to the Port R is within the valid range.

Note 6. Supply Current I_{DDS} : V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).

A / D CONVERSION CHARACTERISTICS (T_{opr} = – 30 to 70°C)

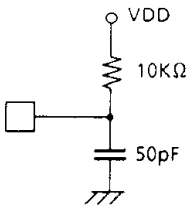
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{ASS}	2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}		–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = 5.000V V_{ASS} = 0.000V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

A. C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

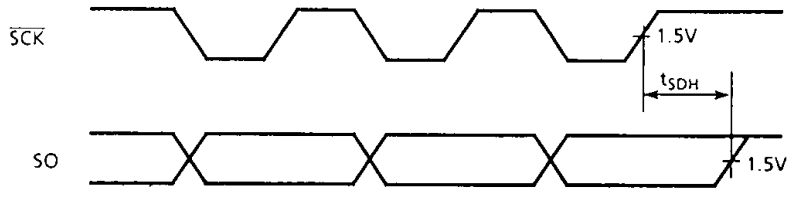
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	1.9	–	20	μs
		In the SLOW mode	235	–	267	
High level Clock pulse Width	t_{WCH}	External clock mode	80	–	–	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}	fc = 4MHz	–	4	–	μs
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 30 to 70°C)

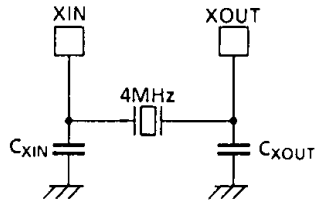
(1) 4MHz

Ceramic Resonator

CSA4. 00MG (MURATA)	$C_{XIN} = C_{XOUT} = 30pF$
KBR-4. 00MS (KYOCERA)	$C_{XIN} = C_{XOUT} = 30pF$

Crystal Oscillator

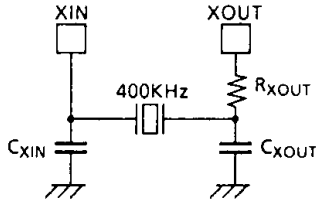
204B-6F 4. 0000 (TOYOCOM)	$C_{XIN} = C_{XOUT} = 20pF$



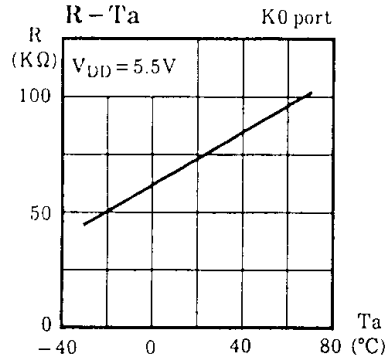
(2) 400KHz

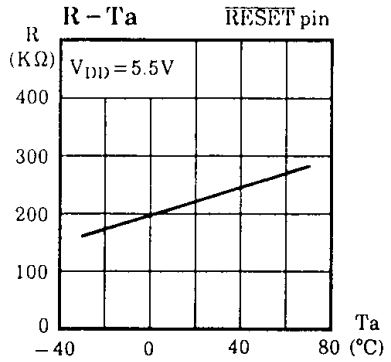
Ceramic Resonator

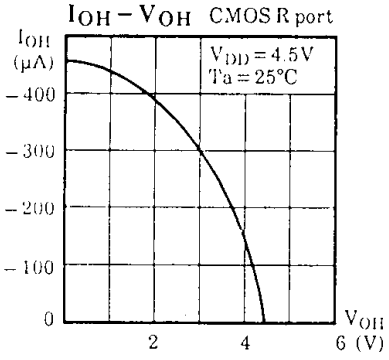
CSB400B (MURATA)	$C_{XIN} = C_{XOUT} = 220pF$, $R_{XOUT} = 6.8K\Omega$
KBR-400B (KYOCERA)	$C_{XIN} = C_{XOUT} = 100pF$, $R_{XOUT} = 10K\Omega$

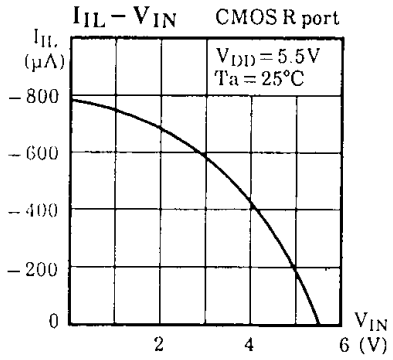


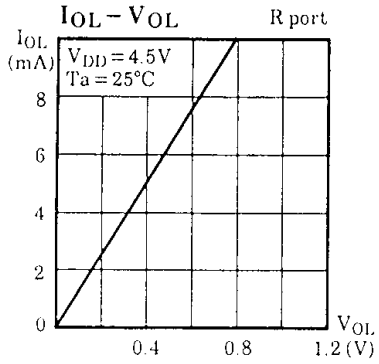
TYPICAL CHARACTERISTICS

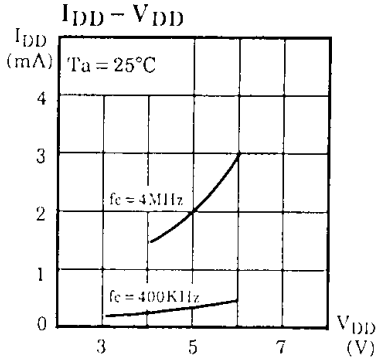


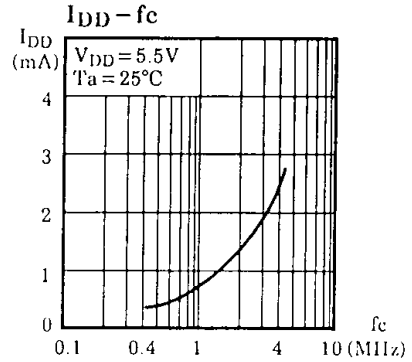








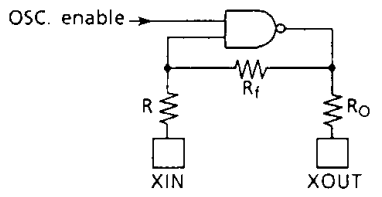
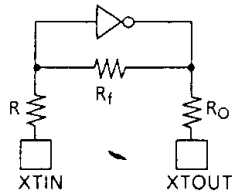
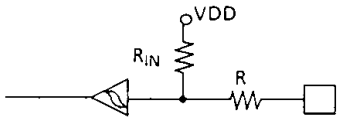
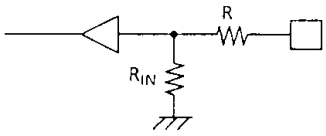




INPUT/OUTPUT CIRCUITRY

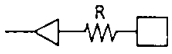
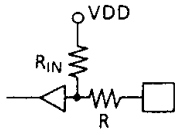
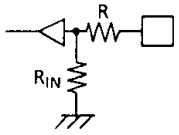
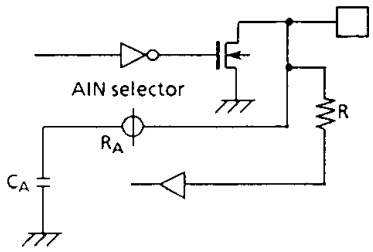
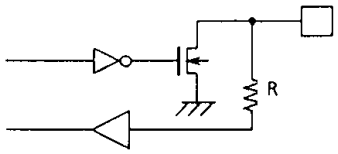
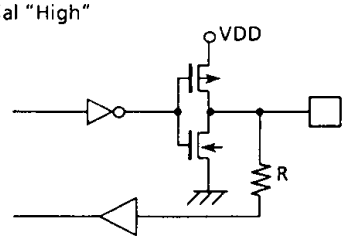
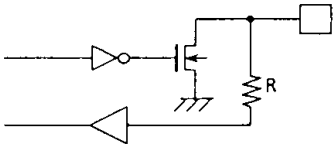
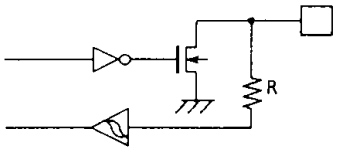
(1) Control pins

Input/Output circuitries of the 47C446A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	INPUT OUTPUT		Resonator connecting pins (High frequency) R = 1KΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2KΩ (typ.)
XTIN XTOUT	INPUT OUTPUT		Resonator connecting pins (Low frequency) R = 1KΩ (typ.) R_f = 15MΩ (typ.) R_O = 200KΩ (typ.)
$\overline{RESET}$	INPUT		Hysteresis input Pull-up resistor R_{IN} = 220KΩ (typ.) R = 1KΩ (typ.)
TEST	INPUT		Contained pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)

(2) I/O Ports

The input/output circuitries of the 47C446A I/O ports are shown as below, any one of the circuitries can be chosen by a code (SA-SF) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	SA, SD:  SB, SE:  SC, SF: 	Pull-up / pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
R4	I/O		Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.) Analog input R_A = 5KΩ (typ.) C_A = 12pF (typ.)
R5 R6	I/O	SA, SB, SC: Initial "Hi-Z"  SD, SE, SF: Initial "High" 	Sink open drain output or push-pull output R = 1KΩ (typ.)
R7	I/O		Sink open drain output Initial "Hi-Z" R = 1KΩ (typ.)
R8 R9	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1KΩ (typ.)

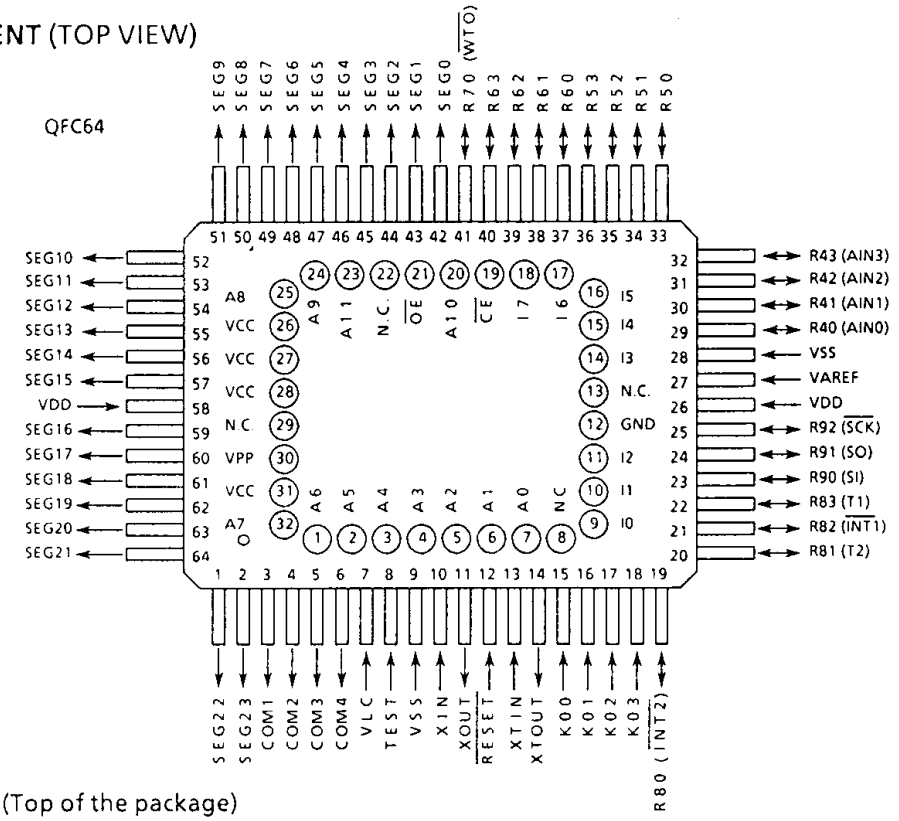
CMOS 4-BIT MICROCONTROLLER

TMP47C946AG

The 47C946A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C446A application systems (programs).
The 47C946A is pin compatible with the 47C446A which are mask-programed ROM devices.

PIN ASSIGNMENT (TOP VIEW)

QFC64



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A11 ~ A0	Output	Program memory address output
I7 ~ I0	Input	Program memory data input
$\overline{CE}$	Output	Chip enable signal output
$\overline{OE}$		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	V_{SS} = 0V, V_{DD} = 4.5 to 6.0V C_L = 100pF Topr = - 30 to 70°C	–	–	150	ns
Data Setup Time	t_{IS}		150	–	–	ns
Data Hold Time	t_{IH}		50	–	–	ns

NOTES FOR USE

(1) Program memory

The program area is as shown in Figure 1.

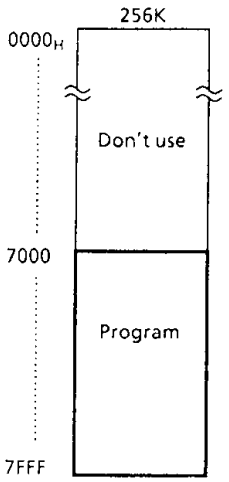


Figure 1. Program area

(2) I/O ports

Input/Output circuitries of I/O ports in the 47C946A are similar to the code SA of the 47C446A.

When this chip is used as evaluator with other I/O code, it is nacessary to provide the external resistors.

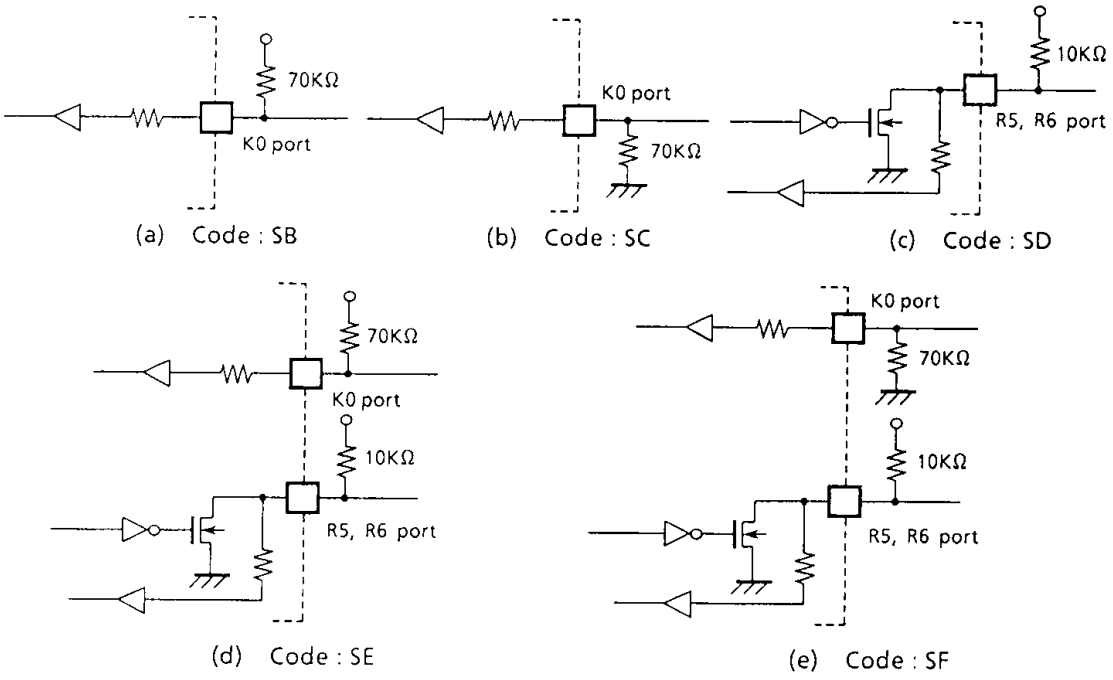


Figure 2. I/O code and external circuitry