NMOS 4-BIT MICROCONTROLLER

TMP4700AC

The 4700A is the system development evaluator chip used for developmental and operational check of the TLCS-47 application systems (programs).

PART No.	ROM	RAM	PACKAGE
TMP4700AC	4096 x 8-bit (external)	256 x 4-bit	QIC80

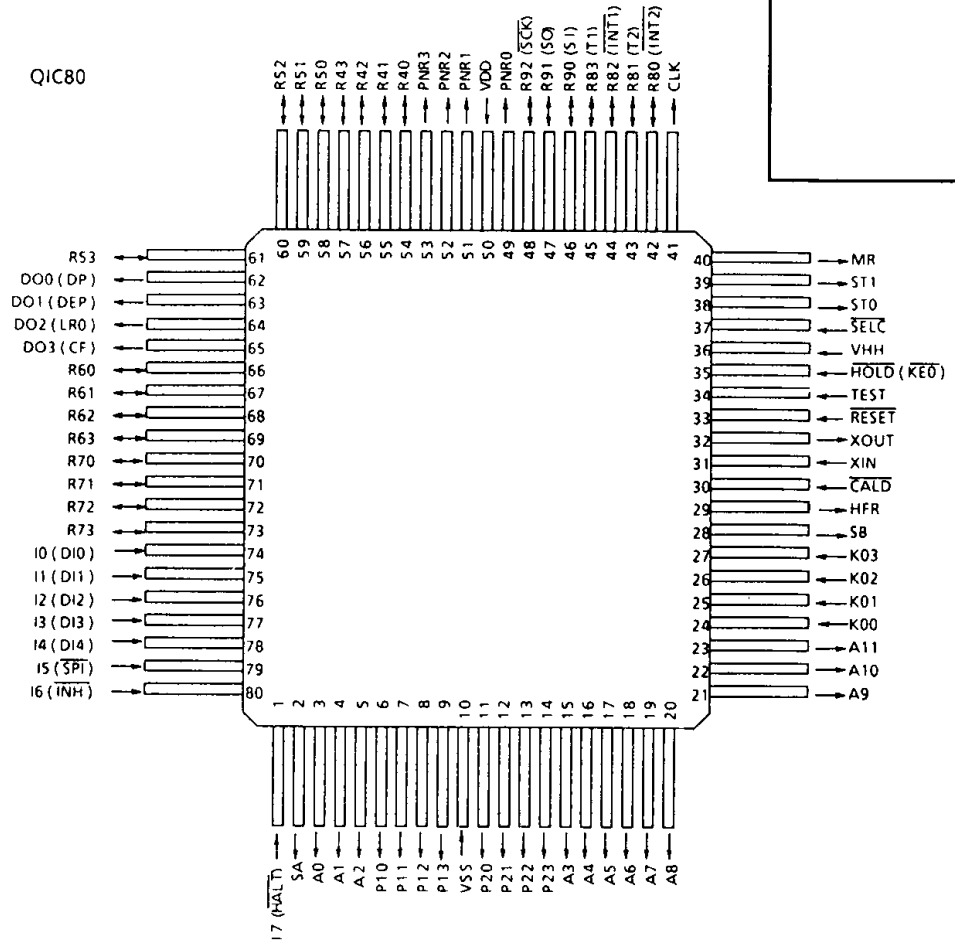
FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆90 basic instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
- ◆Serial Interface with 4-bit buffer.
- ◆Memory holding function and Hold function

QIC80

TMP4700AC

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch	
P23 - P20			
R43 - R40	I/O	4-bit I/O port with latch	
R53 - R50			
R62 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pins	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
A11 - A0	Output	Program memory address output	
I7 ($\overline{HALT}$)	Input (Input)	Program memory data input	Halt request signal input
I6 ($\overline{INH}$)			Inhibit timer and interrupt signal input
I5 ($\overline{SPI}$)			Port control signal input
I4 (DI4) - I0 (DI0)			Port data input
DO3 (CF)	Output (Output)	Port data output	Carry flag monitor output
DO2 (LR0)			Bit 0 of L register monitor output
DO1 (DEP)			Port control signal output
DO0 (DP)			
PNR3 - PNR0	Output	Port address output	
CLK		Strobe signal output	

PIN NAME	Input/Output	FUNCTIONS
ST, ST1	Output	State signal output
SA, SB		Cycle status signal output
MR		Master reset signal output
HFR		Hold operation monitor output
$\overline{CALD}$	Input	Data fetch cycle request signal input
$\overline{SELC}$		Clock division select signal input
VDD	Power Supply	+ 5V
VHH		+ 5V (Power supply for RAM)
VSS		0V (GND)