8-Port IEEE 802.3af/at PSE Controller for Power-over-Ethernet

Features

- IEEE 802.3af/at compliant
- Single DC power supply voltage input (44~57V)
- Supplies 8 independent power ports
- Supports DC Load-Removal Detections
- Built-in power FETs
- 0.1Ω Sense embedded
- Up to 50W per Port for PSE Applications
- Wide temperature range: -40°C ~+85°C
- 9-Bit Port Current and Voltage Monitoring
- I ^{2}C Bus to access up to 8 x TMI7608S devices
- Independent system parameters setting for every port
- Thermal monitoring and protection
- Built-in 3.3V regulators for external devices
- Built-in Power on Reset
- Configurations: 30W x 8ports
- Built-in LEDs control for multi-port use
- Built-in EEPROM interface for dumb application
- Overload LED
- Pin Selectable Detection Backoff Timer for ALT_A/B
- 2-Event Pin-Select
- Support 24V low voltage application
- Pin Programmable Maximum Total current limit for Smart power management.
- Robust Short-Circuit Protection
- Space-Saving,56-Pin QFN (8mm x 8mm) Power Package

Application

- PSE-ICM
- Power-Sourcing Equipment (PSE)
- Switches/Routers
- ALT_A/B Power Injectors

Description

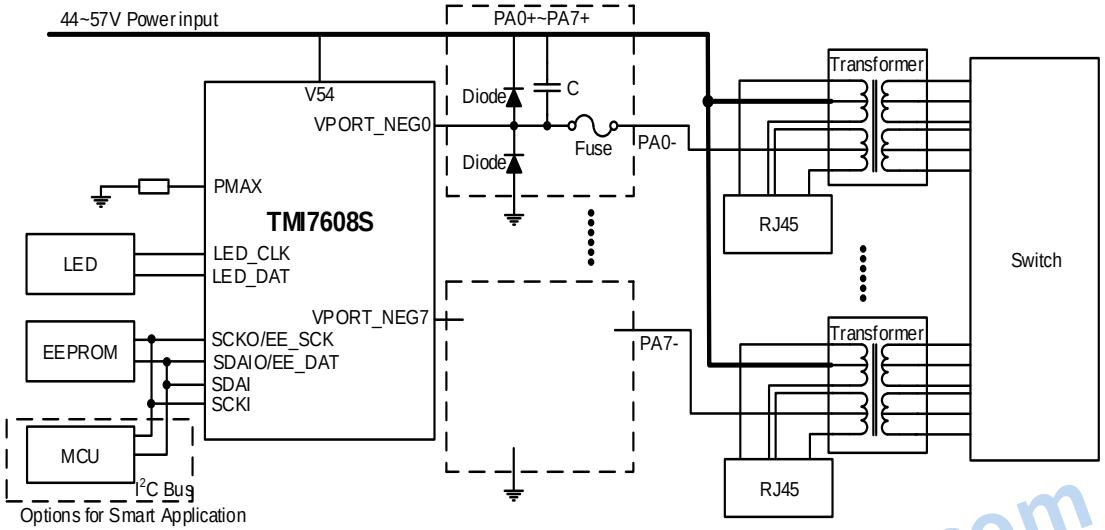
TMI7608S is an 8-port PSE (Power Sourcing Equipment) controller IC for PoE (Power over Ethernet) systems. It integrates power, analog and logic circuits into a single chip, and can be used for Midspans and Endpoint PSE applications. TMI7608S meets all IEEE 802.3AF-2003 requirements, such as multi-point resistor detection, PD classification, DC Disconnect, and Back-off for Midspans. It also meets all IEEE 802.3AT-2009 requirements, such as two-event classification and supply maximum 36W per port. The device also supports Class4+ for detection and classification of high-power PDs. The device supports single-supply operation, provides up to 50W to each port (Class4+ enabled).

TMI7608S comprises internal temperature monitoring and thermal protection to protect against junction overheating.

TMI7608S has a maximum power setting pin. Connect a resistor from this pin to AGND to set the total power capability on all 8 output ports. TMI7608S will limit the total power on 8 ports below this power limit.

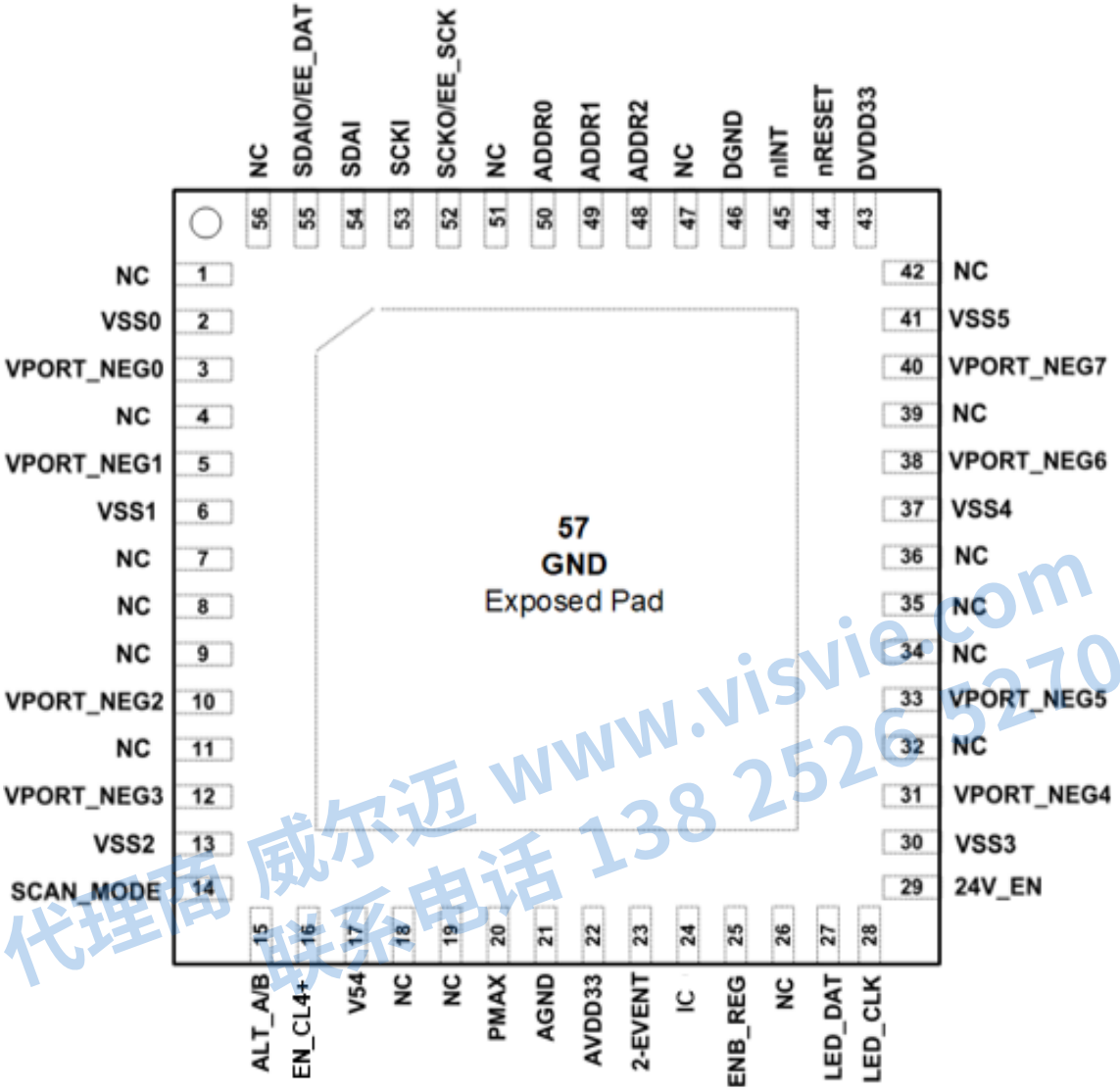
The 3.3V regulator is built-in to support external devices. Multiple TMI7608Ss can integrate to build an 8 x N ports PSE system, and I^{2}C bus uses to collect PD power status from each TMI7608S to support global power managements. Management switch host has options to communicate TMI7608S via I^{2}C bus for PSE management activities. Optocouplers can be implemented to provide electrical isolations between the host and TMI7608S for signal communication.

Typical Application



TMI7608S Typical Application Diagram

Package



Top View

QFN8x8-56

Top Marking: T7608S/XXXXX (T7608S: Device Code, XXXXX: Inside Code)

Order Information

Part Number	Package	Top Marking	Quantity/Reel
TMI7608S	QFN8x8-56	T7608S XXXXX	3000

TMI7608S devices are Pb-free and RoHS compliant.

Pin Functions

Pin	Name	Function
1	NC	No internal connection.
2	VSS0	Analog ground.
3	VPORT_NEG0	PortN0 negative feeding voltage input.
4	NC	No internal connection.
5	VPORT_NEG1	PortN1 negative feeding voltage input.
6	VSS1	Analog ground.
7	NC	No internal connection.
8	NC	No internal connection.
9	NC	No internal connection.
10	VPORT_NEG2	PortN2 negative feeding voltage input.
11	NC	No internal connection.
12	VPORT_NEG3	PortN3 negative feeding voltage input.
13	VSS2	Analog ground.
14	SCAN_MODE	SCAN_MODE is internally pulled down to AGND. It should be connected to AGND for normal operation.
15	ALT_A/B	This pin is latched upon power-on reset to define the ALT_A/B Type and is internally pulled downed to DGND. 0: ALT_A(Default) 1: ALT_B
16	EN_CL4+	Class4+ Enable Input. Referenced to DGND. EN_CL4+ is internally pulled down to DGND. Leave unconnected to disable the classification for Class4+ devices (IEEE 802.3at-compliant mode). Connect EN_CL4+ to V3P3 to enable the classification of Class4+ devices. EN_CL4+ is latched in after the device is powered up or after a reset condition.
17	V54	Main power supply input for chip the 1uF capacitor should be added between V54 and AGND.
18	NC	No internal connection.
19	NC	No internal connection.
20	PMAX	Maximum loading power setting pin. Connect a 75kΩ resistor from this pin to AGND to set the total power capability on all 8 output ports. TMI7608S will limit the total power on 8 ports below this power limit. The PMAX setting signal is latched in IC during IC is powered up or after a reset condition. $P_{max}=R_{max}*78uA*V54$
21	AGND	Analog ground.
22	AVDD33	Analog 3.3V Power. When EnB_Reg is connected to AGND, the built-in 3.3V regulator is active, and besides TMI7608S itself, AVDD33 can provide 3.3V (6mA) for external device. When EnB_Reg is connected to 3.3V, AVDD33 should be connected to an external power 3.3V (6mA minimum) for TMI7608S. A 4.7uF capacitor should be added between AVDD33 and AGND.

Pin	Name	Function
23	2-EVENT	2-Event Classification Select. Referenced to AGND. 2-EVENT is internally pulled up to the digital supply. Leave unconnected to enable 2-Event classification. Force low to disable the 2-Event classification.
24	IC	eFuse power: Internally Connected. Leave unconnected.
25	EnB_Reg	Enable/Disable the internal 3.3V regulator Please refer to pin description of AVDD33.EnB_Reg is internally pulled up to AVDD33.
26	NC	No internal connection.
27	LED_DAT	Serial LED data output. This pin is internally pulled up to the DVDD33.
28	LED_CLK	Serial LED clock output.
29	24V_EN	This pin is latched upon power-on reset to define the 24V_En and is internally pulled downed to DGND. 0: Disable (Default) 1 : Enable
30	VSS3	Analog ground.
31	VPORT_NEG4	PortN4 negative feeding voltage input.
32	NC	No internal connection.
33	VPORT_NEG5	PortN5 negative feeding voltage input.
34	NC	No internal connection.
35	NC	No internal connection.
36	NC	No internal connection.
37	VSS4	Analog ground.
38	VPORT_NEG6	PortN6 negative feeding voltage input.
39	NC	No internal connection.
40	VPORT_NEG7	PortN7 negative feeding voltage input.
41	VSS5	Analog ground.
42	NC	No internal connection.
43	DVDD33	Digital power 3.3V. Internally connected to AVDD33.
44	nRESET	It is a low active signal to reset TMI7608S.
45	nINT	Interrupt output and low active
46	DGND	Digital ground, it should be connected to AGND.
47	NC	No internal connection.
48	ADDR2	I^2C device address bus AD2.
49	ADDR1	I^2C device address bus AD1.
50	ADDR0	I^2C device address bus AD0.
51	NC	No internal connection.
52	SCKO/EE_SCK	This pin is I2C clock output.
53	SCKI	I^2C serial clock input.
54	SDAI	I^2C serial data output.
55	SDAIO/EE_DAT	This pin is I2C serial data input and output.
56	NC	No internal connection.

57	EPAD	Exposed pad, it should be connected to AGND.

Absolute Maximum Ratings (Note 1)

Items	Description	Min	Typ	Max	Unit
Supply Voltage	V54-AGND	-0.3		90	V
PortN0~PortN3	PortNn– AGND @n=0~7	-0.3		90	V
All other Pins	All other Pin – (AGND, or DGND)	-0.3		6	V
DGND	DGND – AGND	-0.3		0.3	V
Maximum Junction Temperature				150	°C
Storage Temperature Range		-65		150	°C
Lead Temperature	30s, reflow			260	°C
T_A	Operating Ambient Temperature	-40		85	°C

ESD Rating (Note2)

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2017 Classification, Class: 2	±2000	V
V_{ESD_CDM}	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2018 Classification, Class: C3	±1000	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±200	mA

JEDEC specification JS-001

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Devices are ESD sensitive. Handling precaution is recommended.

Electrical Characteristics

(V54 = 32V to 60V, AGND = DGND = 0V, TA = -40°C to +85°C. All voltages are referenced to AGND, unless otherwise noted. Typical values are at V54 = 54V, TA = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.)

Symbol	Description	Conditions		Min	Typ	Max	Units
POWER SUPPLIES							
V54	Power Supply voltage	45V~57V @IEEE802.3af		32		60	V
		51V~57V @IEEE802.3at		50		60	V
I54	V54 operating current	All ports on @w/o peripheral load current & port load current			8	10	mA
V_{3P3}	AVDD33 voltage	IV3P3=0~10mA		3	3.30	3.6	V
V_{3P3_UVLO}	AVDD33 Undervoltage Lockout				2		V
V_{FLBK_ST}	Foldback Initial Voltage	VPortN_ - AGND above which the current-limit trip voltage starts folding back	IEEE802.3af		32		V
			IEEE802.3at		18		V
V_{FLBK_END}	Foldback Final Voltage	V54 - VPortN_ above which the current limit reaches VTH_FB			46		V
I_{LIM-TH_FB}	Minimum Foldback Current-Limit Threshold	VPortN_= V54 = 57V			120		mA
	RS_ Input Bias Current	VRS_= AGND				-2	μA
I_{Inrush}	Output current in POWER_UP State			400		450	mA
I_{LIM}	Short Circuit Current Limit Threshold(Note 3)	Class0~3		400		500	mA
		Class4		750		1000	
		Class4+				2000	
I_{CUT}	Overcurrent Threshold after Startup	Class0		350	375	400	mA
		Class1		91	112	133	
		Class2		160	206	252	
		Class3		350	375	400	
		Class4		600	640	680	
		Class4+		1200	1280	1360	

Electrical Characteristics

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SUPPLY MONITORS						
V_{UVLO}	V54 Undervoltage Lockout	V54-AGND, V54-AGND increasing		30		V
V_{UVLO_H}	V54 Undervoltage Lockout Hysteresis	Ports shut down if: V54 - AGND < AGND_UVLO - AGND_UVLOH		3		V
T_{SHD}	Thermal-Shutdown Threshold	Port is shut down and device resets if the junction temperature exceeds this limit, temperature increasing (test mode) (Note 4)		150		°C
T_{SHDN}	Thermal-Shutdown Hysteresis	Temperature decreasing (Note 4)		20		°C
PortN MONITOR						
I_{BPortN}	PortN_ Input Current	VPortN_ = V54, during idle			2	μA
		V54 - AGND = 48V, VPortN_ = AGND, during idle			-70	μA
R_{DIS}	Idle Pullup Resistance at PortN_	Detection and classification off, port shut down	0.7	1	1.25	MΩ
P_{GTH}	PGOOD High Threshold	VPortN_ - AGND, PortN_ decreasing	1.5	2	2.5	V
P_{GHYS}	PGOOD Hysteresis			220		mV
t_{PGOOD}	PGOOD Low-to-High Glitch Filter	Time VPortN_ - AGND has to exceed PGTH to set the PGOOD_ bit in register 1Dh	2		4	ms
Total Load Power Limit						
P_{max}	Load Power Limit on All 8 Ports	RMAX = 19kΩ (18kΩ+1kΩ) (Imax=78μA*Rmax, V54=54V)		80		W
		RMAX = 28.5kΩ (27kΩ+1.5kΩ)		120		
		RMAX = 38kΩ (36kΩ+2kΩ)		160		
		RMAX =47.5kΩ		200		
		RMAX =57kΩ (56kΩ+1kΩ)		240		
P_{MAX_LIMIT}	Maximum Load Capability on all 8 Ports	Float PMAX pin (V54=54V)		430		W
$T_{MAX-DLY}$	Maximum Load Power Protection Delay	TPMAX bit=10 100% x PMAX <Load <150% x PMAX		60		ms
		Load >150% x PMAX		1.024		ms
LOAD DISCONNECT						
I_{MPSTH}	DC Load Disconnect Threshold	Minimum Iport allowed before disconnect (DC disconnect active), VPortN_ = 0V	5	7.5	10	mA
t_{DISC}	Load Disconnect Time	Time from VRS_ < VDCTH to gate shutdown	300	350	400	ms

Electrical Characteristics

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DETECTION							
V_{DPH1}	Detection Probe Voltage (First Phase)	V54 - VDET during the first detection phase		3.8	4	4.2	V
V_{DPH2}	Detection Probe Voltage (Second Phase)	V54 - VDET during the second detection phase		8.6	9	9.4	V
I_{DLIM}	Current-Limit Protection	VPortN_ = V54, current measured through PortN_ during detection		1.5		2	mA
V_{DCP}	Short-Circuit Threshold	If V54 - VPortN_ < VDCP after the first detection phase, a short circuit to AGND is detected			1.5		V
I_{D_OPEN}	Open-Circuit Threshold	First point measurement current threshold for open condition			12.5		µA
R_{DOK}	Resistor Detection Window	(Note 5)		19		26.5	kΩ
R_{DBAD}	Resistor Rejection Window	Detection rejects lower values				15.2	kΩ
		Detection rejects higher values		32			
CLASSIFICATION							
V_{CL}	Classification Probe Voltage	V54 - VPortN_ during classification		15.5		20	V
I_{CL_LIM}	Current-Limit Protection	VPortN_ = V54, current measured through PortN		60	70	80	mA
t_{CL_E}	Classification Event Timing			14	18	22	ms
V_{MARK}	Mark Event Voltage	V54 - VDET during mark event		8		9.6	V
I_{MARK_LIM}	Mark Event Current Limit	VDET = V54, during mark event measure current through DET		34	40	46	mA
t_{MARK_E}	Mark Event Timing			7	9	11	ms
I_{CL}	Classification Current Thresholds	Classification current thresholds between classes	Class 0, Class 1	5	6.5	8	mA
			Class 1, Class 2	13	14.5	16	
			Class 2, Class 3	21	23	25	
			Class 3, Class 4	31	33	35	
			Class 4 upper limit (Note 6)	45	48	51	

Electrical Characteristics

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DIGITAL INPUTS/OUTPUTS (Voltages Referenced to AGND)						
V_{IL}	Digital Input Low				0.8	V
V_{IH}	Digital Input High		2			V
R_{DIN}	Internal Input Pullup/Pulldown Resistor	Pullup (pulldown) resistor to V3P3 (DGND) to set default level	25	50	75	kΩ
V_{OL}	Open-Drain output Low Voltage	ISINK = 10mA			0.4	V
I_{OL}	Open-Drain Leakage	Open-drain high impedance, VPortN_ = 3.3V			1	μA
I_{DL}	SCL, SDAIN Input Leakage	Input connected to the pull voltage			1	μA
	Hardware Reset Pulse Width	Minimum low pulse duration on nRESET to lead to a hardware reset event	120			μs
TIMING						
t_{START}	Startup Time	Time during which a current limit set by VSU_LIM is allowed, starts when the GATE_ is turned on	50	60	70	ms
t_{FAULT}	Fault Time	Time allowed for an overcurrent fault set by VFLT_LIM after startup	50	60	70	ms
t_{LIM}	Current Limit	Time during after startup (Note 7)	50	60	70	ms
t_{OFF}	Port_ Turn-Off Time	Minimum delay between any port turn-off, does not apply in a reset case		0.1		ms
Ron	Port on resistance	Iport ≦ 640mA, & Ta=25℃		0.15		Ω
	Detection Reset Time	Time allowed for the port voltage to reset before detection starts		800		ms
t_{DET}	Detection Time	Maximum time allowed before detection is completed			330	ms
t_{DMID}	ALT_A/B Mode Detection Delay		2			s
t_{CLASS}	Classification Time	Time allowed for classification		19	25	ms
t_{DLY}	V54_UVLO Turn-On Delay	Time V54 must be above the V54_UVLO threshold before the device operates	2		4	ms
$t_{RESTART}$	Restart Timer	Time the device waits before turning on after an overcurrent fault, ALT_A/B disabled	1.6	2	2.4	s

Electrical Characteristics

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ADC PERFORMANCE (Power-On Mode)							
	Resolution				9		Bits
	Offset Error	Voltage reading	TA = -40°C to +85°C			3	LSB
		Current reading	TA = -40°C to +85°C			3	
	Gain Error	Gain error voltage	TA = -40°C to +85°C	-2.5		2.5	%
		Gain error current					
	V54 Voltage Accuracy	V54-AGND=48V	TA = -40°C to +85°C	-2.5		2.5	%
I_{NL}	Integral Nonlinearity					1	LSB
D_{NL}	Differential Nonlinearity					1	LSB
	Current Reading Range	Classes 0-4			1		A
		Class4+			2		
	Current LSB Step Size	Classes 0-4			1.956		mA
		Class4+			3.912		
	Voltage Reading Range	All Classes			63.6		V
	Voltage LSB Step Size	All Classes			124.5		mv
TIMING CHARACTERISTICS							
f_{SCL}	Serial Clock Frequency			1		1000	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition			0.125			µs
$t_{HD, STA}$	Hold Time for a START Condition			0.125			µs
t_{LOW}	Low Period of the SCL Clock			0.25			µs
t_{HIGH}	High Period of the SCL Clock			0.25			µs
		START and STOP conditions		0.125			
$t_{HD, DAT}$	Data in Hold Time	Receive		0			ns
		Transmit		250		375	
$t_{SU, DA}$	Data in Setup Time			125			ns
t_{LOW_EXT}	Cumulative Clock Low Extend Time					10	ms
t_F	Fall Time of SDAO Transmitting	(Note 8)				250	ns
$t_{SU, STO}$	Setup Time for STOP Condition			0			µs
t_{SP}	Pulse Width of Spike Suppressed	(Note 8)			30		ns

Production testing done at +25°C. Overtemperature limits are guaranteed by design and not production tested.

Note 3: The current-limit thresholds are programmed through the I^2C interface.

Note 4: Functional test is performed over thermal shutdown entering test mode.

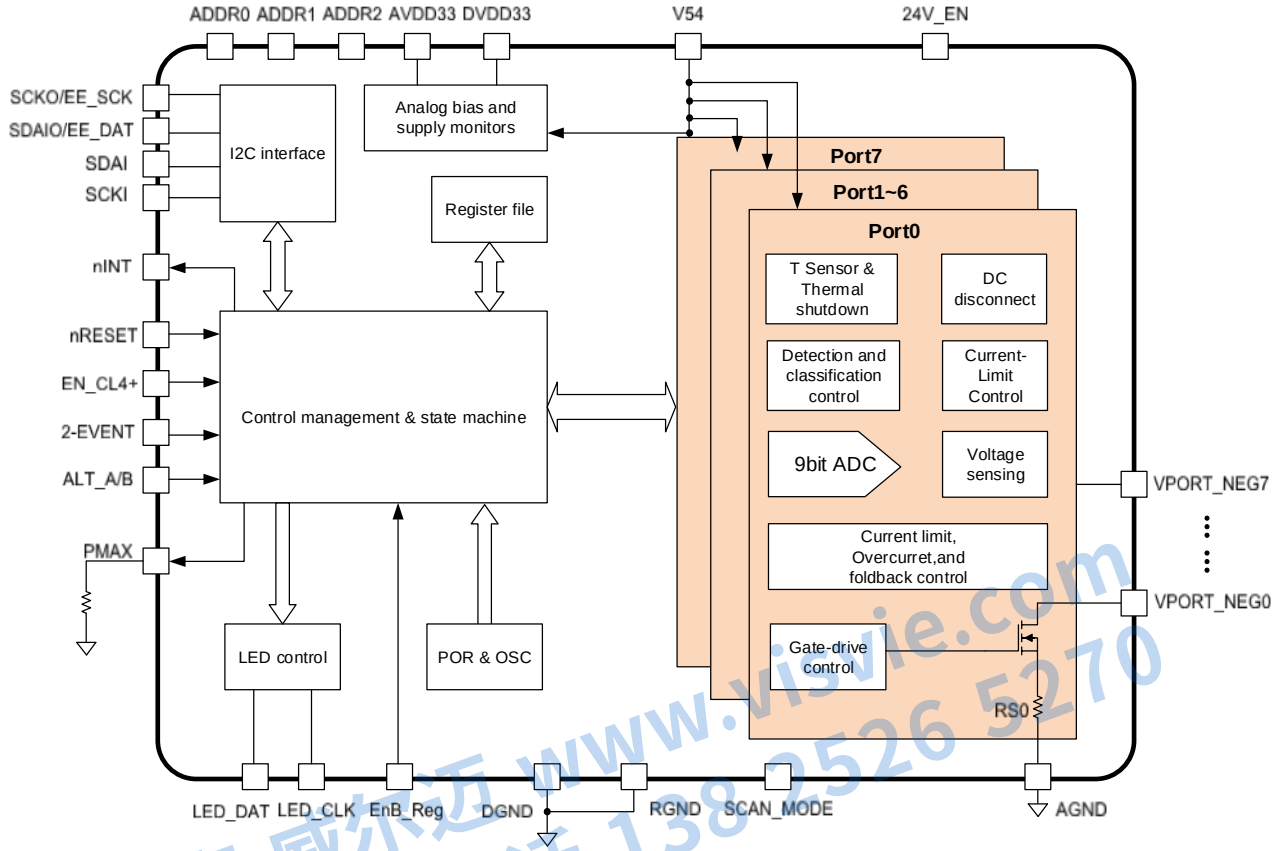
Note 5: RDOK = (VPortN2 - VPortN1) / (IPortN2 - IPortN1). VPortN1, VPortN2, IPortN1, and IPortN2 represent the voltage at PortN_ and the current into PortN_ during phase 1 and 2 of the detection, respectively.

Note 6: If Class4+ is enabled, this value is the classification current threshold from Class 4 to Class4+, and classification currents between 51mA and ICL_LIM will be classified as Class4+.

Note 7: Default value. The fault timer can be reprogrammed through the I^2C interface (TLIM_[3:0]).

Note 8: Guaranteed by design. Not subject to production testing.

Block Diagram



TMI7608S Block Diagram

Functions Description

Detailed Description

The TMI7608S is an 8-port PSE power controller designed for use in IEEE 802.3at/af-compliant PSE. This device provides PD discovery, classification, current limit, and load disconnect detections. The device supports both fully automatic operation and software programmability. The device also supports 2-event classification and Class4+ for detection and classification of high-power PDs. The device supports single-supply operation, pro- vides up to 50W to each port (Class4+ enabled), and still provides high-capacitance detection for legacy PDs. The device features an I^2C -compatible is fully software configurable and programmable. The device provides instantaneous readout of port current and voltage through the I^2C interface. The device provides input under-voltage lockout (UVLO), over-temperature protection, and output voltage slew-rate limit during startup.

Reset

The device is reset by any of the following conditions:
1) Power-up/down. Reset condition is asserted once V54 falls below the UVLO threshold.
2) Hardware reset. To initiate a hardware reset, pull nRESET low to DGND for at least 100μs. Hardware reset clears once, nRESET returns high to AVDD33, and all registers are set to their default states.
3) Software reset. To initiate a software reset, write a logical 1 to the RESET_IC register (R2Bh[4]) any time after power-up. Reset clears automatically.
4) Thermal shutdown. The device enters thermal shut- down at +150°C. The device exits thermal shutdown and is reset once the temperature drops below 130°C.
During normal operation, changes to the address inputs, ALT_A/B, EN_CL4+, 2-EVENT and PMAX are ignored, and they can be changed at any time prior to a reset state. At the end of a reset event, the device latches in the state of these inputs.

Port Reset

Set RESET_P_ (R2Ah[7:0]) high anytime during normal powered operation to turn off port, disable detection and classification, and clear the Port Event and Status registers. If a port is not powered, setting RESET_P_ high for that port has no effect. Individual port reset does not initiate a global device reset.

ALT_B Mode

In ALT_B mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the ports wait at least 2s before attempting to detect again. ALT_B mode is activated by setting ALT_A/B high and then powering or resetting the device. Alternatively, ALT_B mode can be software programmed individually for each port by setting ALT_B_ (R24h[7:0]) to a logical 1. By default, the ALT_A/B input is internally pulled downed to AGND to disable this function.

Operation Modes

The device provides four operating modes to suit different system requirements. By default, auto mode allows the device to operate automatically at its default settings without any software. Semiautomatic mode automatically detects and classifies devices connected to the ports but does not power a port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.
Switching between auto, semiautomatic, and manual mode does not interfere with the operation of an out- put port. When a port is set into shutdown mode, all port operations are immediately stopped and the port remains idle until shutdown mode is exited.

Auto (Automatic) Mode

By default, The device enters auto mode after power-up or when the reset condition is cleared. To manually place a port into auto mode from any other mode, set the corresponding port mode bits (R1Fh[7:0]/R20h[7:0) to [11]. In auto mode, the device performs detection, classification, and powers up the port automatically if a valid PD is connected to the port. If a valid PD is not connected at the port, the device repeats the detection routine continuously until a valid PD is connected. When entering auto mode after a reset condition, the DET_EN_(R22h[7:0]) and CLASS_EN_ bits (R23h[7:0]) are set to high and stay high, unless changed by software. When entering auto mode from any other mode due to a software command (programmed with R1Fh[7:0]/R20h[7:0]), the DET_EN_ and CLASS_EN_ bits retain their previous state.

Semiautomatic (Semi) Mode

Enter semiautomatic mode by setting the port operating mode (R1Fh/R20h) to [10]. When entering semi mode, the DET_EN_ and CLASS_EN_ bits retain their previous states. When the DET_EN_ and/or CLASS_EN_ bits are set to 1, the TMI7608S performs detection and/or classification repeatedly, but do not power up the port(s) automatically. Setting R28h[7:0] (PWR_ON_) high turns on power to the port(s) if detection and classification has successfully completed. If a port is powered down while in semiautomatic mode, the corresponding DET_EN_ and CLASS_EN_ bits are reset to 0.

Manual Mode

Enter manual mode by setting the port operating mode (R1Fh/R20h) to [01]. Manual mode allows the software to dictate any sequence of operation. In manual mode, the Detection/Classification register (R22h) is set to 00h, and DET_EN_/CLASS_EN_ become push-button bits. A port will only perform a single detection/classification cycle when DET_EN_/ CLASS_EN_ are set high, and they are reset low after execution.
PWR_ON_ (R28h[7:0]) has the highest priority, and setting PWR_ON_ high at any time causes the device to immediately enter the powered mode. Setting DET_EN_ and CLASS_EN_ high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN_ and CLASS_EN_ commands.

Shutdown Mode

To put a port into shutdown mode, set the corresponding port mode bits (R1Fh/R20h) to [00]. Putting a port into shutdown mode immediately turns off port power, clears the event and status bits, and halts all port operations. In shutdown mode the serial interface is still fully active; however, all DET_EN_, CLASS_EN_, and PWR_ON_ commands are ignored.

PD Detection

During normal operation, the device probes the output for a valid PD. A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3at/af standard. Table 1 shows the IEEE 802.3at specification for a PSE detecting a valid PD signature. After each detection cycle, the device sets DET_ (R06h[7:0] and R07h[7:0]) to 1 and reports the detection results in the detection status bits. The DET_ bits are reset to 0 when read through the CoR (clear on read) register (R07h), or after a reset event.
During detection, the device keeps the internal MOSFET off and forces two probe voltages through PortN_. The current through PortN_ is measured, as well as the voltage difference from AGND to PortN_. A two point slope measurement is used, as specified by the IEEE 802.3at/ af standard, to verify the device connected to the port. The device implements appropriate settling times to reject 50Hz/60Hz power-line noise coupling. To prevent damage to non-PD devices, and to protect itself from an output short circuit, the device limits the current into PortN_ to less than 2mA (max) during PD detection. In ALT_B mode, after every failed detection cycle, the device waits at least 2.0s before attempting another detection cycle.

Table 1. PSE PI Detection Modes Electrical Requirements (IEEE 802.3at)

PARAMETER	SYMBOL	MIN	MAX	UNIT	ADDITIONAL INFORMATION
Open-Circuit Voltage	VOC	—	30	V	In detection mode only
Short-Circuit Current	ISC	—	5	mA	In detection mode only
Valid Test Voltage	VVALID	2.8	10	V	—
Voltage Difference Between Test Points	△VTEST	1	—	V	—
Time Between Any Two Test Points	tBP	2	—	ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	VSLEW	—	0.1	V/μs	—
Accept Signature Resistance	RGOOD	19	26.5	kΩ	—
Reject Signature Resistance	RBAD	＜15	＞33	kΩ	—
Open-Circuit Resistance	ROPEN	500		kΩ	—
Accept Signature Capacitance	CGOOD		150	nF	—
Reject Signature Capacitance	CBAD	10		μF	—
Signature Offset Voltage Tolerance	VOS	0	2.0	V	—
Signature Offset Current Tolerance	IOS	0	12	μA	—

Power Device Classification

During PD classification, the device forces a probe voltage between 15V and 20V at PortN_ and measures the current into PortN_. The measured current determines the class of the PD.
After each classification cycle, the device sets CLS_ (R08h[7:0] and R09h[7:0]) to 1 and reports the classification results in the classification status bits . The CLS_ bits are reset to 0 when read through the CoR (clear on read) register (R09h) or after a reset event.
If EN_CL4+ is left unconnected, the device will classify the PD based on IEEE 802.3at standard. If the measured current exceeds 51mA, the device will not power the PD, but will report an over- current classification result and will return to IDLE state before attempting a new detection cycle.

Class4+ PD Classification

The device supports high power beyond the IEEE802.3at standard by providing an additional classification (Class4+) if needed. To enable Class4+, connect EN_CL4+ to V3P3 and initiate a global reset or use the soft- ware to individually enable Class4+ classification for each port (R2Dh[3:0]). Once Class4+ is enabled, during classification, if the device detects currents in excess of the Class 4 upper-limit threshold, the PD will be classified as a Class4+ powered device. The PD is guaranteed to be classified as a Class4+ device for any classification current from 51mA up to the classification current-limit threshold. The Class4+ overcurrent threshold and current limit will be set automatically with ICUT [5:0] and ILIM_. Leave EN_CL4+ unconnected to disable Class4+ detection and to be fully compliant to IEEE 802.3at standard classification.

2-Event PD Classification

If the result of the first classification event is Class 0 to 3, then only a single classification event occurs as shown in Figure 1. However, if the result is Class 4 (or Class4+), the device will perform a second classification event as shown in Figure 2. Between the classification cycles, the device performs a first and the second mark event as required by the IEEE 802.3at standard, forcing a 9.1V probing voltage at PortN_.

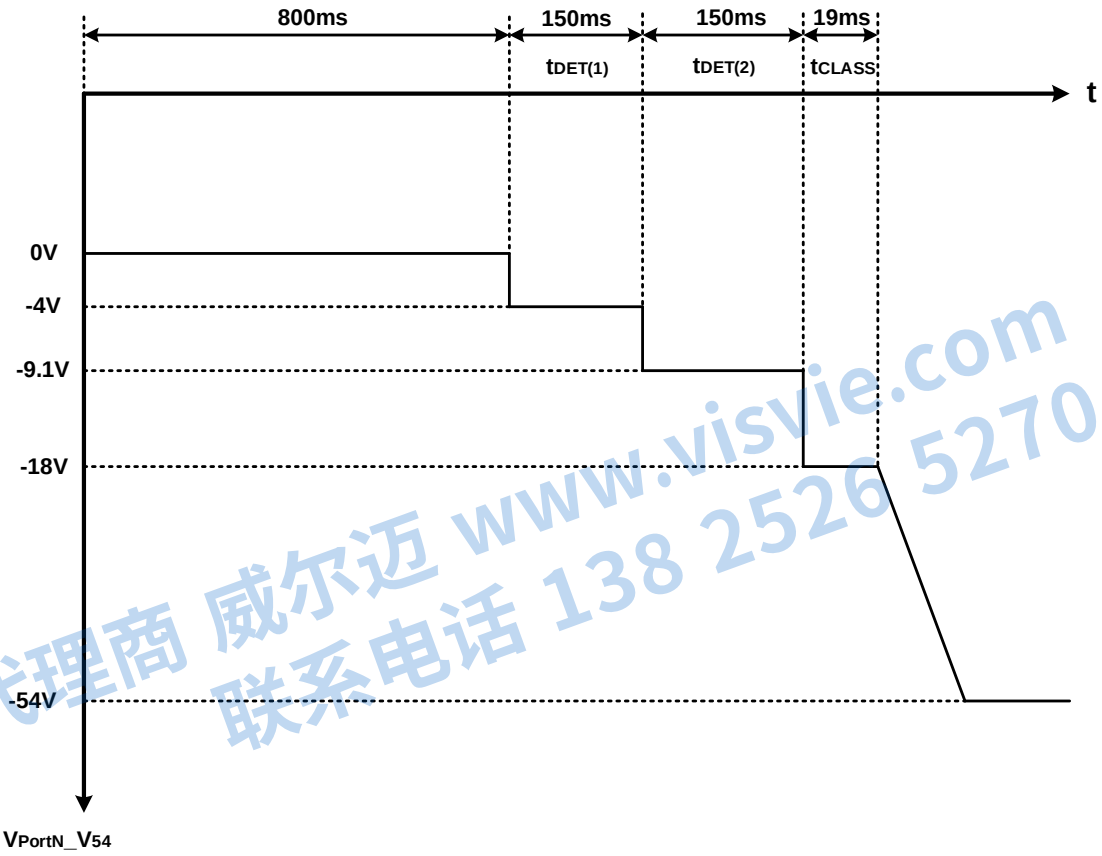


Figure 1. Detection, Classification, and Port Power-Up Sequence

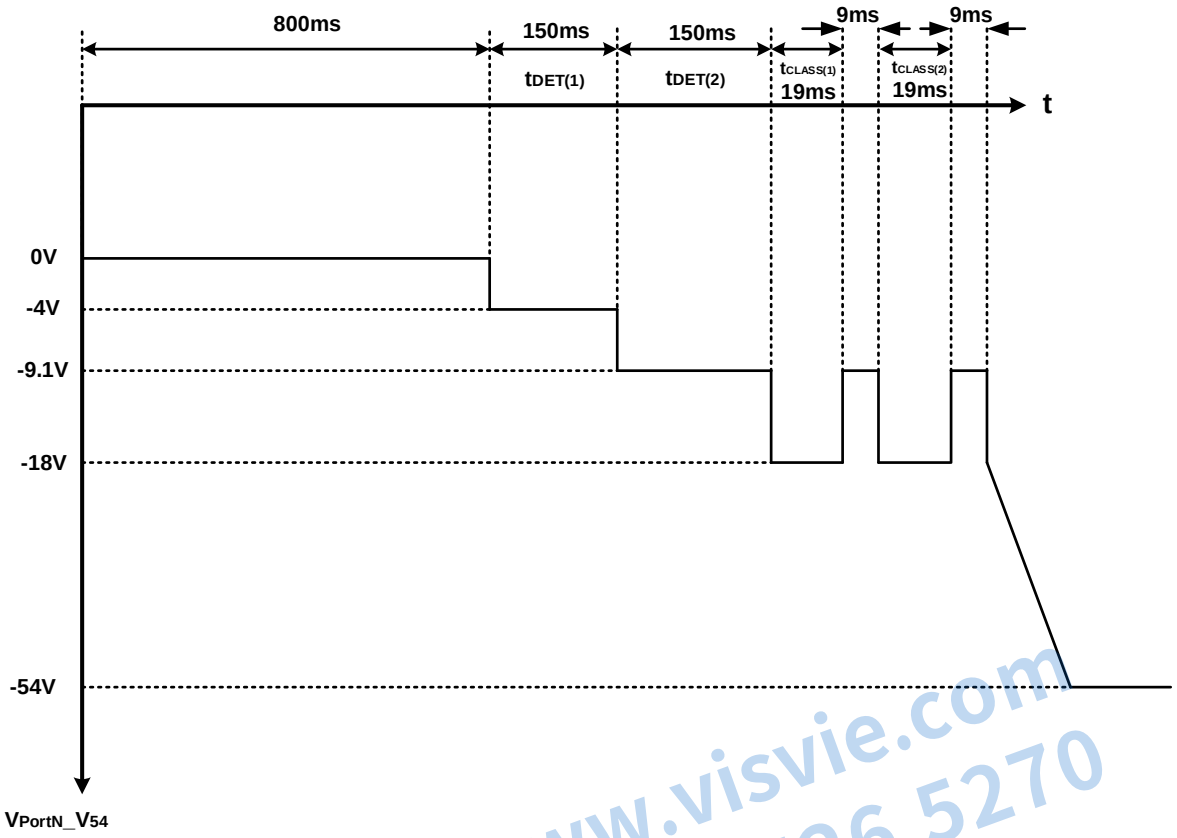


Figure 2. Detection, 2-Event Classification, and Port Power-Up Sequence

Powered State

When the device enters a powered state, the tFAULT timer is reset and power is delivered to the PD. PGOOD_ (R1Dh[7:0]) is set to 1 when the device enters the normal power condition. PGOOD_ immediately resets to 0 whenever the power to the port is turned off. The power-good change bits, PG_CHG_ (R02h[7:0]) are set both when the port powers up and when it powers down.

Over current Protection

During startup, if the current-limit condition persists, when the startup timer, tSTART, times out, the port shuts off, and the TSTART_ bit is set (R0Eh[7:0] and R0Fh[7:0]). In the normal powered state, the device checks for overcurrent conditions as determined by VCUT. The tFAULT counter sets the maximum allowed continuous current period.

When the counter reaches the tFAULT limit, the device powers the port down and asserts the corresponding TCUT_ bit (R0Ah[7:0] and R0Bh[7:0]). For a continuous overstress, a fault latches exactly after a period of tFAULT. VCUT is programmable through the ICUT_ registers. If a port is powered down due to a current-limit condition, during normal operation, the device asserts the corresponding ICV_ bit (R10h[7:0] and R11h[7:0]) After power-off due to an overcurrent fault, the tFAULT timer is not immediately reset but starts decrementing at the same slower pace. The device allows a port to be powered on only when the tFAULT counter is at zero. This feature sets an automatic duty-cycle protection to the internal MOSFET to avoid overheating.

Table 2. PSE Classification of a PD (Table 33-9 of the IEEE 802.3at Standard)

MEASURED ICLASS (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 or 1
8 to 13	Class 1
> 13 and < 16	Either Class 1 or 2
16 to 21	Class 2
> 21 and < 25	Either Class 2 or 3
25 to 31	Class 3
> 31 and < 35	Either Class 3 or 4
35 to 45	Class 4
> 45 and < 51	Either Class 4 or Invalid

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at PortN_ and when necessary reduces the current-limit clamp voltage (VSU_LIM) to help reduce the power dissipation through the internal FET. When ILIM_ = (Class 0–3), foldback begins when VPortN_ - AGND > 32V; and when ILIM_ = (Class 4 and 4+), foldback begins when VPortN_ - AGND > 18V. The VSU_LIM eventually reduces down to the minimum current-limit threshold VTH_FB when VPortN_ - AGND > 46V (Figure 3).

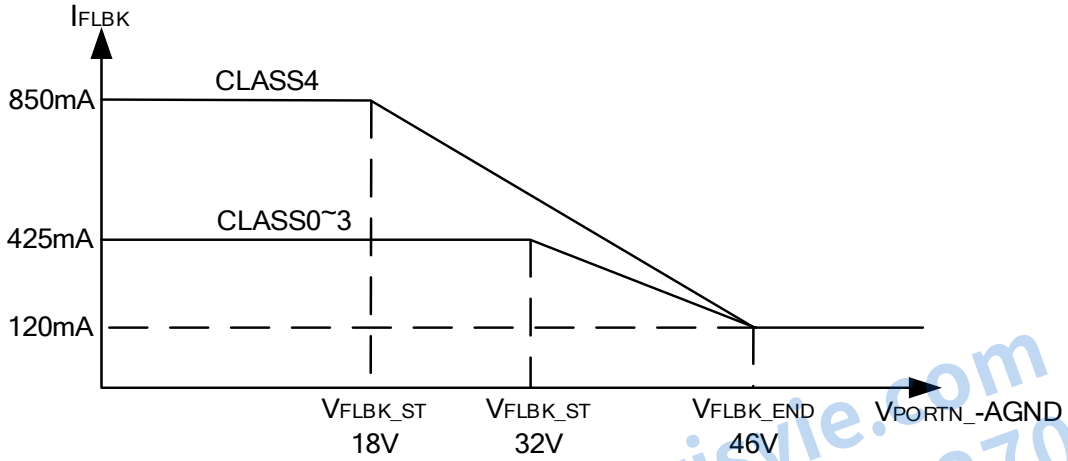


Figure 3. Foldback Current Characteristics

Interrupt

The device contains an open-drain logic output (nINT)that goes low when an interrupt condition exists. The Interrupt register (R00h) contains the interrupt flag bits and the Interrupt Mask register (R01h) determines which events can trigger an interrupt. When an event occurs, the appropriate Interrupt Event register bits (in R02h to R13h) and the corresponding interrupt (in R00h) are set to 1 and nINT is asserted low (unless masked). If the master device on the I2C bus sends out an Alert Response Address, any TMI7608S device on the bus that has nINT asserted will respond. As a response to an interrupt, the controller can read the status of the event register(s) to determine the cause of the interrupt and take appropriate action. Each interrupt event register is paired with a Clear-on-Read (CoR) register. When an interrupt event register is read through the corresponding CoR register, the corresponding event register is reset to 0 (clearing interrupt event). nINT remains low and the interrupt is not reset when the Interrupt Event register is read through the read-only address. For example, to clear a supply event fault read R13h (CoR) not R12h (readonly). Use the INT_CLR bit (R2Bh[7]) to clear an interrupt, or the RESET_IC bit (R2Bh[4]) to initiate software resets.

AVDD33 Power Supply

The device has an internally regulator generates 3.3V power for internal use and 3.3V power also can supply typical 10mA current on V3P3 pin for external devices. V3P3 has an under-voltage lockout (V3P3_UVLO) of 2V, and an under- voltage condition on V3P3 keeps the device in reset and the ports shut off. When V3P3 has recovered and the Reset condition clears, the V3P3_UVLO bit in the Supply Event registers is set to 1 (R0Ah[12] and R0Bh[13]). The digital address inputs, and ALT_A/B are internally pulled up to AVDD33, and all digital inputs are referenced to DGND. AVDD33 can also be used to source up to 6mA for external circuitry. For internal regulator stability, connect a 1uF capacitor in parallel with a 33nF capacitor at the AVDD33 output (Figure 4). If an external load is to be shared among multiple TMI7608S devices, isolate the external supply bus with a series resistor (50Ω for 3 devices, 75Ω for 4 devices), and place a single 1uF capacitor on the bus.

In addition, the TMI7608S can also be powered by an external 3.3V connection to the AVDD33, and the EnB_Reg must also be pulled up to 3.3V, which can reduce the power consumption and temperature rise of the device.

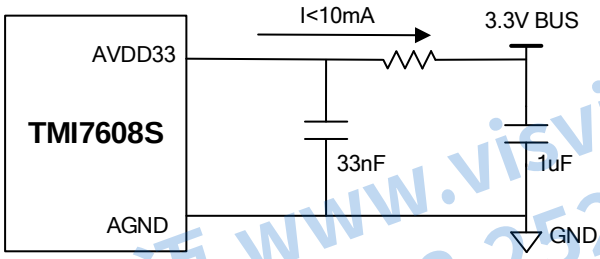


Figure 4 AVDD33 External Power Sourcing

Undervoltage Protection

The device contains undervoltage protection features, and the flag bits can be found in the Supply Event register (R12h and R13h) . An internal AGND undervoltage lockout circuit keeps the MOSFET off and the device in reset until V54 exceeds 30V for more than 3ms. An internal overvoltage circuit shuts down the ports. The digital supply also contains an undervoltage lockout that triggers when V3P3 - AGND ≤ 2V.

DC Disconnect Monitoring

The DC disconnect monitoring settings are found in the Disconnect Enable register (R21h). To enable DC disconnect, set either the DCD_EN_ bit for the corresponding port to 1. To disable the DC disconnect monitoring, DCD_EN_ bit for that port must be set to 0. When enabled, if VRSENSE_ (the voltage across RSENSE_) falls below the DC load disconnect threshold, VDCTH, for more than tDISC, the device turns off power and asserts the DIS_ bit for the corresponding port (R0Ch[7:0] and R0Dh[7:0]).

Hardware Power-Down

The nRESET digital input is referenced to DGND and is used for hardware level control of device power management. During normal operation, nRESET should be externally pulled directly up to V3P3, the 3.3V internal regulator output. To initiate a hardware reset and port power-down, pull nRESET to DGND for at least 100µs. While nRESET is held low, the device remains in reset and the ports remain securely powered down. Normal device operation resumes once nRESET is pulled up to the V3P3.

LED Interface

In auto mode or manual mode, the LED interface can hook up with an IP403 (Serial-to-Parallel LED driver) to display the port status. A port status LED is lit up when TMI7608S allocates power to the port. LED interface is enabled by pulling up LED_DAT pin with a resister. One TMI7608S can handle 8 LEDs and up to five TMI7608Ss can share one IP403, where one TMI7608S serves as the master to drive LED_CLK and the others are slaves. AD2 pin defines TMI7608S to be a master or a slave. The index counter in all TMI7608Ss counts from 0 to 55 repeatedly with LED_CLK after reset and the value of index counter in all TMI7608S are identical. An TMI7608S will send out 8-bit LED information on LED_DAT when its index counter reaches start index defined in start index register (0x8C). The detail is illustrated in the LED start index register (0x8C) and Figure 9. If there is only one TMI7608S, user can replace IP403 with a 74LS164 to display port status for cost saving. TMI7608S should be configured as a master.

Total Load Power Limit

TMI7608S has the classification capability to allocate power to each port based on IEEE802.3at, except this, TMI7608S can monitor the total loading power and automatically shut down the lower priority port if total load power is higher than expected power rating. Set the ‘PMAXEN’ bit high can enable this function, and TMI7608S will compare total load power with the reference power set by PMAX pin. If the total loading is higher the programmed power level and TPMAX over load timer is out, TMI7608S will shut down the lowest priority port among the powered ports. If the total loading power is higher than 150% of programmed limit, the lowest priority port will be shut down at once with about 1ms delay.

EEPROM controller

When TMI7608S operates in auto mode, the register file can be loaded with some initial value from external EEPROM (24xx series EEPROM, Maximum support to 24C16). TMI7608S reads the EEPROM starting from address 0, parses the contents of the EEPROM command blocks, checks for integrity of the contents, and then writes the designated registers. This process continues until there is either no more data or the integrity check fails. EEPROM is necessary only if user wants to modify the default value of registers in auto mode.

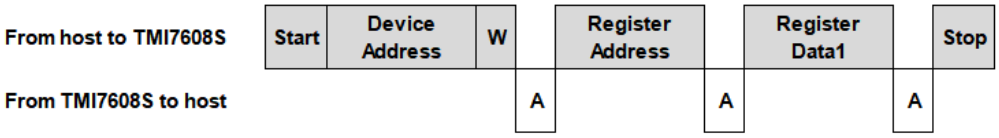
Thermal Shutdown

If the device's die temperature reaches 150°C (typ), an overtemperature fault is generated and the device shuts down. The die temperature must cool down below 130°C (typ) to remove the overtemperature fault con- dition. After a thermal shutdown condition clears, the device is reset and the TSD event bit is set to a logical 1 (R12h[7]/R13h[7]).

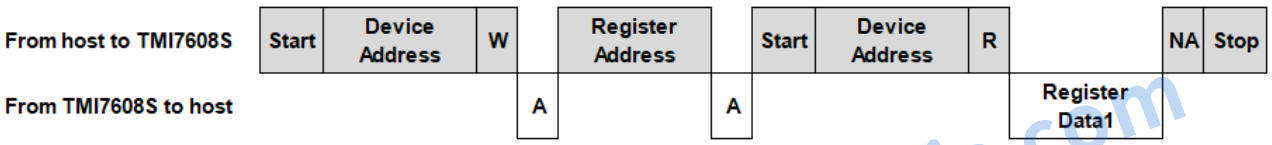
I2C Slave Interface

Through the I²C slave interface of TMI7608S, host CPU can access the register file in TMI7608S. It consists of SCL, SDAO and SDAI pins, where SCL is Clock, SDAO is Serial Data Output and SDAI is Serial Data Input. This I²C interface supports the 7-bit addressing mode of the I²C standard. The clock speed can be up to 1 Mbit/sec. There can be up to eight TMI7608S chips on one I²C bus, the LSB 3 bits of the I²C address can be assigned with the address pin AD2~AD0. The MSB 4 bits of the I²C address are fixed at 1110b. The following diagram is the register read/write cycles of the I²C bus.

I²C Register Write 1 Byte Cycle:



I²C Register Read 1 Byte Cycle:



Start Bit = 1→0, Stop Bit = 0→1

W = write Bit = 0, R = Read Bit = 1

A = ACK Bit = 0, NA = NO ACK Bit = 1

I2C bus read/write cycles diagram

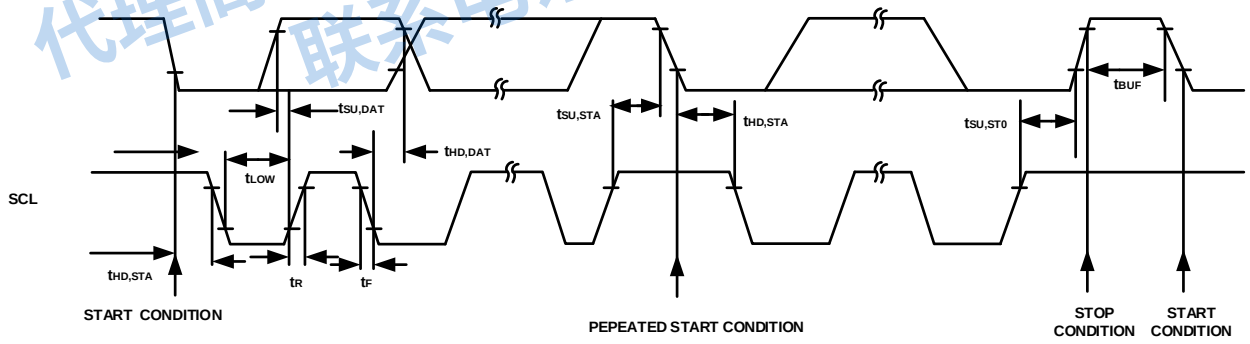


Figure 5 Serial Interface Timing Details

Table 3. Programmable Device Address Settings

DEVICE ADDRESS						
B7	B6	B5	B4	B3	B2	B1
1	1	1	0	AD2	AD1	AD0

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission (see Figure 6).

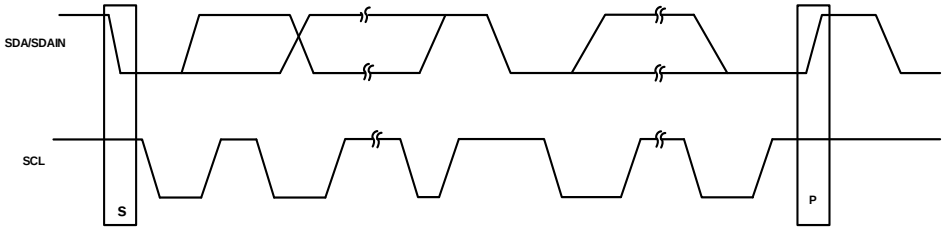


Figure 6 START and STOP Conditions

Bit Transfer

Each clock pulse transfers one data bit (Figure 7). The data on SDA must remain stable while SCL is high.

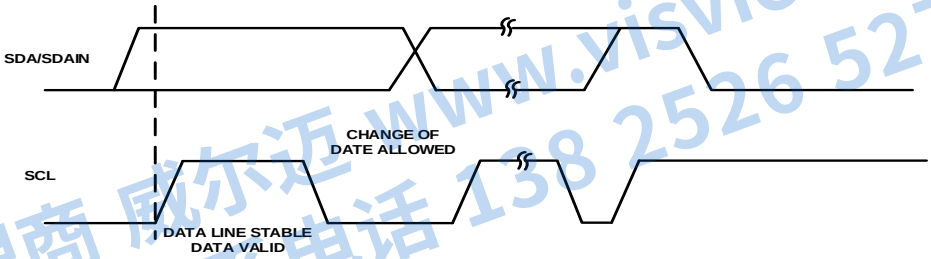


Figure 7 Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8) that the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master transmits to the TMI7608S, the device generates the acknowledge bit. When the device transmits to the master, the master generates the acknowledge bit.

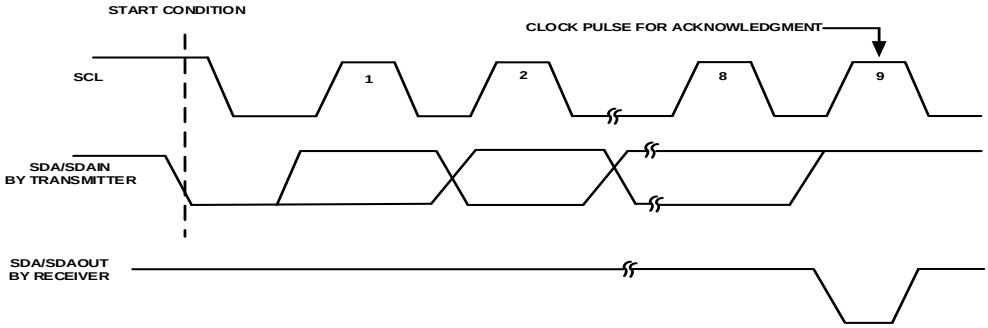


Figure 8 Acknowledge

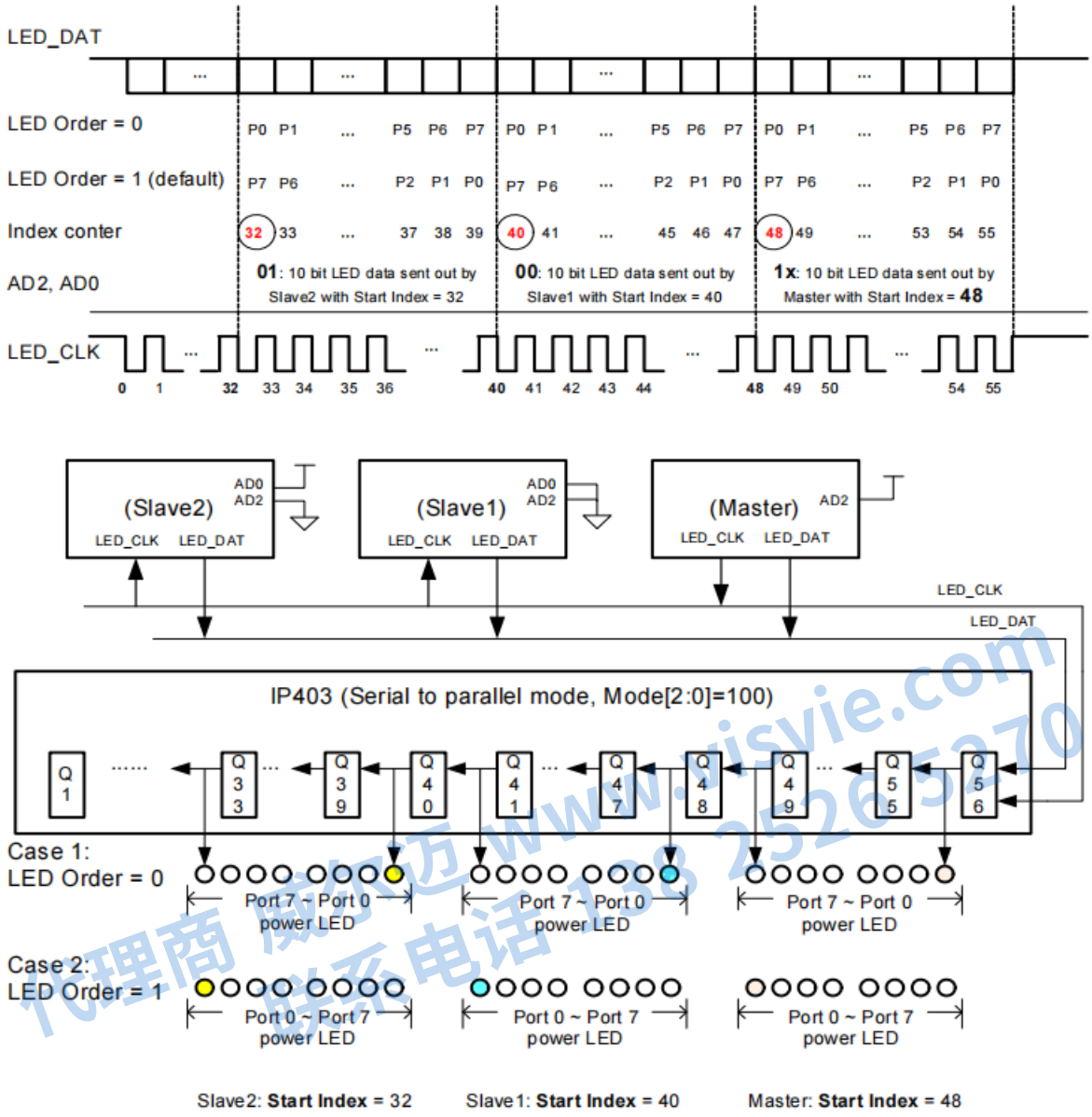
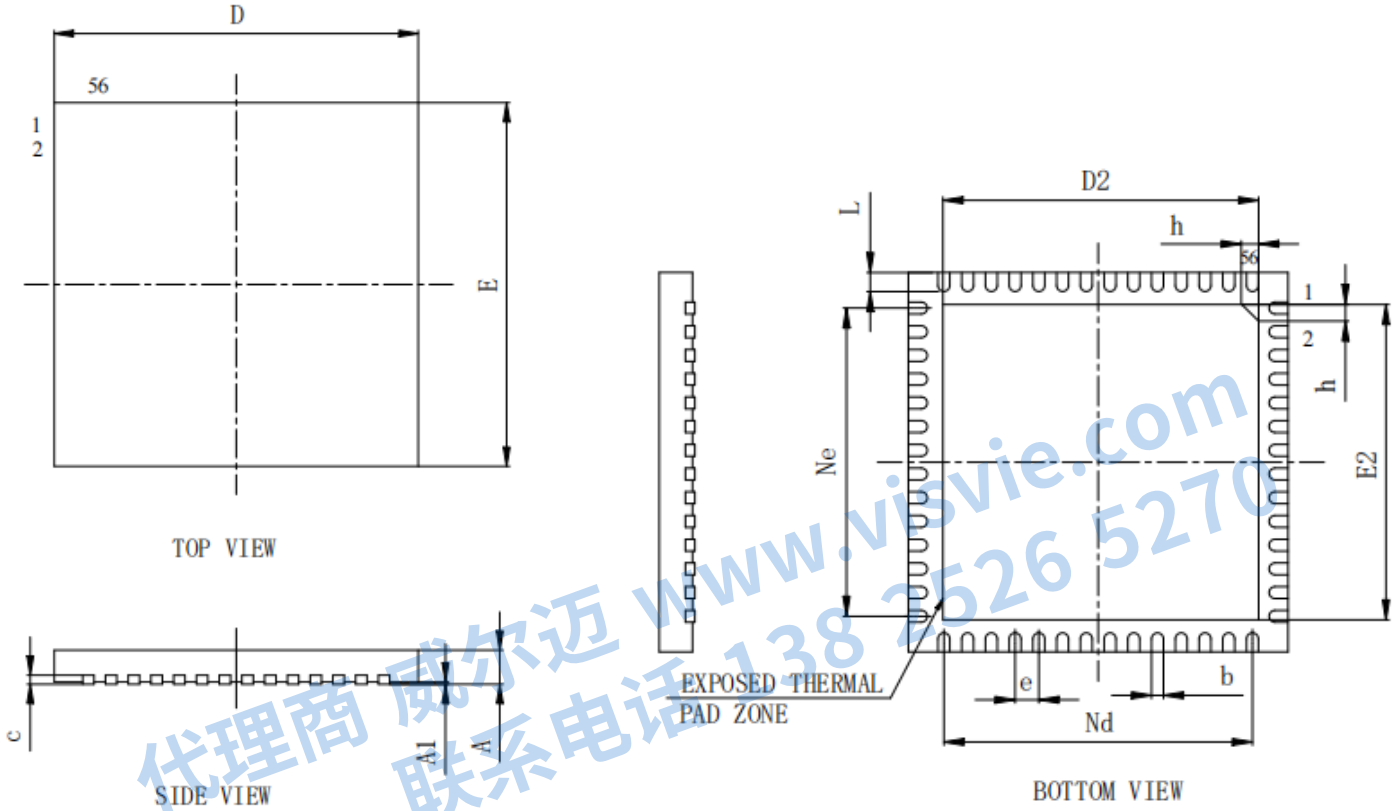


Figure 9 LED behavior and system diagram of multiple TMI7608S application

Package Information

QFN8X8-56



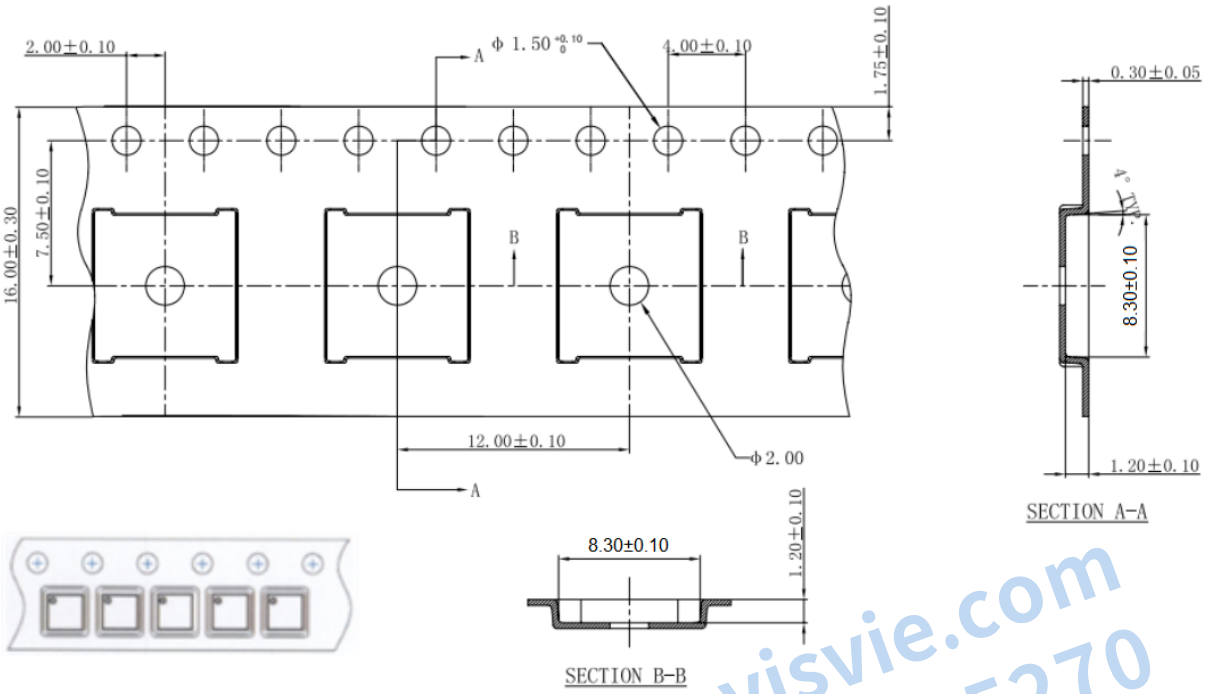
Unit: mm

Symbol	Dimensions In Millimeters			Symbol	Dimensions In Millimeters		
	Min	Nom	Max		Min	Nom	Max
A	0.7	0.75	0.8	D2	6.55	6.65	6.75
A1	-	0.02	0.05	E2	6.55	6.65	6.75
b	0.18	0.25	0.30	e	0.50BSC		
c	0.18	0.25	0.30	Nd	6.50BSC		
D	7.90	8.00	8.10	L	0.35	0.40	0.45
E	7.90	8.00	8.10	h	0.30	0.35	0.40
Ne	6.50BSC						

Note 1: All dimensions are in millimeters.

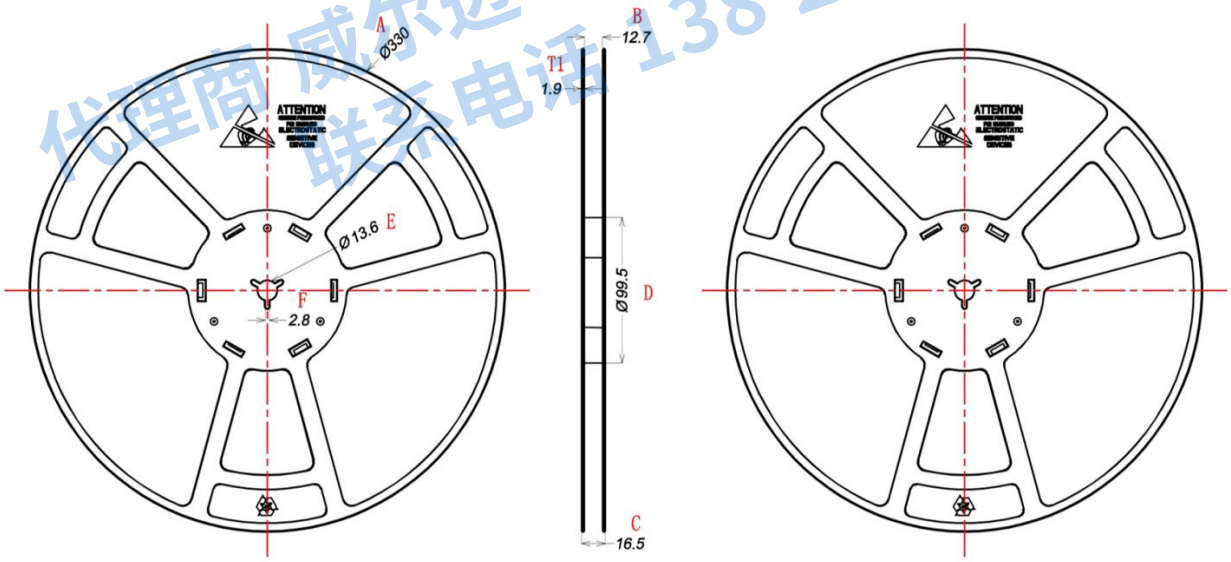
Tape And Reel Information

TAPE DIMENSIONS:QFN8X8-56



Unit: mm

REEL DIMENSIONS:



Unit: mm

A	B	C	D	E	F	T1
Ø 330±1	12.7±0.5	16.5±0.3	Ø 99.5±0.5	Ø 13.6±0.2	2.8±0.2	1.9±0.2

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 3

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