

TMC1420-LA DATASHEET

Dual N & P-Channel 40V Power MOSFET with extremely low on-resistance.

High energy efficiency and good thermal performance.

+



+

+

+

PRODUCT SUMMARY

	N-CH	P-CH
BV_{DSS}	40V	-40V
$R_{DS(ON)}$	26.5m Ω	42m Ω
I_D	8.8A	-7.3A

FEATURES AND BENEFITS

N & P-Channel MOSFET Half Bridge Device

Simple Drive Requirement

Good Thermal Performance

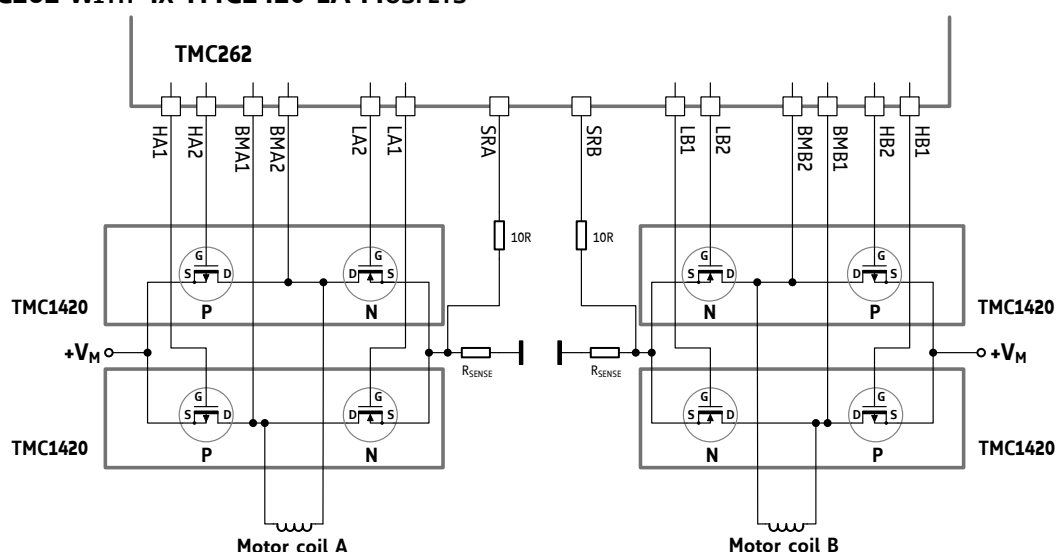
IR-reflow and backside heat sink

Fast Switching Performance for quick motor reaction

PQFN package, 5x6 mm

RoHS Compliant and Halogen-Free

TMC262 WITH 4X TMC1420-LA MOSFETS



APPLICATIONS

TMC1420 MOSFETs fit best with TRINAMIC 2-phase bipolar stepper motor drivers:

TMC262: up to 4A RMS motor current with 4xTMC1420-LA

TMC248: up to 3.5A RMS motor current with 4xTMC1420-LA

TMC249: up to 3.5A RMS motor current with 4xTMC1420-LA

DESCRIPTION

The TMC 1420-LA is highly energy efficient. Employing silicon process technology, the TMC1420 achieves an extremely low on-state resistance and fastest switching performance. The TMC1420-LA is intended for power conversion and power management applications that require high efficiency and power density. The PQFN 5x6 package uses standard infrared reflow technique with the backside heat sink and has a very good thermal performance. The package is similar to other enhanced SO-8 packages in the market, such as LFPak and PowerSO-8.

Order code	Description	Size
TMC1420-LA	N and P-channel enhancement mode power MOSFET	5 x 6 mm ²

Table of Contents

1	PIN ASSIGNMENTS	3
2	ABSOLUTE MAXIMUM RATINGS	3
3	THERMAL DATA	3
4	ELECTRICAL CHARACTERISTICS	4
4.1	N-CH @T _J =25°C (UNLESS OTHERWISE SPECIFIED)	4
4.1.1	Source-Drain Diode	4
4.2	P-CH @T _J =25°C (UNLESS OTHERWISE SPECIFIED)	4
4.2.1	Source-Drain Diode	5
5	N-CHANNEL DIAGRAMS	6
6	P-CHANNEL DIAGRAMS	8
7	PACKAGE MECHANICAL DATA	10
7.1	DIMENSIONAL DRAWINGS	10
7.2	PACKAGE MARKING INFORMATION	10
7.3	PACKAGE CODE	10
8	DISCLAIMER	11
9	ESD SENSITIVE DEVICE	11
10	TABLE OF FIGURES	12
11	REVISION HISTORY	12

1 Pin Assignments

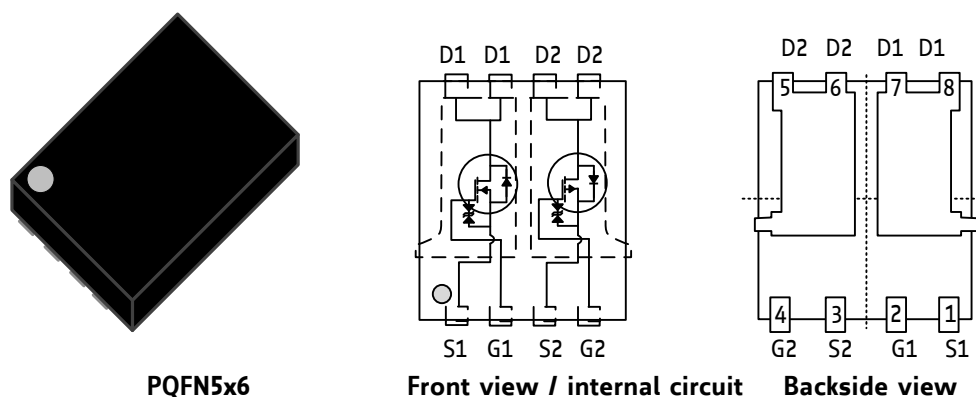


Figure 1.1 TMC1420-LA pin assignments

2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances. Operating the circuit at or near more than one maximum rating at a time for extended periods shall be avoided by application design.

Parameter	Symbol	N-channel	P-channel	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current* ²	$I_D @ T_A = 25^\circ\text{C}$	8.8	-7.3	A
Continuous Drain Current* ²	$I_D @ T_A = 70^\circ\text{C}$	7	-5.8	A
Pulsed Drain Current* ¹	I_{DM}	30	-30	A
Total Power Dissipation	$P_D @ T_A = 25^\circ\text{C}$	3.57		W
Storage Temperature Range	T_{STG}	-55 to 150		$^\circ\text{C}$
Operating Junction Temperature Range	T_J	-55 to 150		$^\circ\text{C}$

*¹ Pulse width is limited by maximum junction temperature.

*² Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 85 $^\circ\text{C}/\text{W}$ at steady state.

3 Thermal Data

Parameter	Symbol	N-channel	P-channel	Unit
Max. Thermal Resistance, Junction-case	R_{thj-c}	6	6	$^\circ\text{C}/\text{W}$
Max. Thermal Resistance, Junction-ambient*	R_{thj-a}	35	35	$^\circ\text{C}/\text{W}$

* Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 85 $^\circ\text{C}/\text{W}$ at steady state.

4 Electrical Characteristics

4.1 N-CH @T_j=25°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Static Drain-Source On-Resistance*	$R_{DS(ON)}$	$V_{GS}=10V, I_D=7A$ $V_{GS}=4.5V, I_D=5A$		21.2 32.7	26.5 45	mΩ mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.7	3	V
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=7A$		14		S
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$			10	mA
Gate-Source Leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			±30	mA
Total Gate Charge	Q_g	$I_D=7A$		7	11.2	nC
Gate-Source Charge	Q_{gs}	$V_{DS}=20V$		2.2		nC
Gate-Drain ("Miller") Charge	Q_{gd}	$V_{GS}=4.5V$		3.7		nC
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=20V$		6		ns
Rise Time	t_r	$I_D=1A$		18		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G=3.3\Omega$		17		ns
Fall Time	t_f	$V_{GS}=5V$		19		ns
Input Capacitance	C_{iss}	$V_{GS}=0V$		660	1050	pF
Output Capacitance	C_{oss}	$V_{DS}=15V$		120		pF
Reverse Transfer Capacitance	C_{rss}	$f=1.0MHz$		75		pF
Gate Resistance	R_g	$f=1.0MHz$		2.2	4.4	Ω

* Pulse test

4.1.1 Source-Drain Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward On Voltage*	V_{SD}	$V_{GS}=0V, I_S=2.9A$			1.2	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_S=7A$		24		ns
Reverse Recovery Charge	Q_{rr}	$dI/dt=100A/\mu s$		21		nC

* Pulse test

4.2 P-CH @T_j=25°C (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40			V
Static Drain-Source On-Resistance*	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5A$ $V_{GS}=-4.5V, I_D=-3A$		33.3 53.3	42 70	mΩ mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.7	-3	V
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-5A$		11		S
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-32V, V_{GS}=0V$			-10	mA
Gate-Source Leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			±30	mA
Total Gate Charge	Q_g	$I_D=-5A$		11.5	18.4	nC
Gate-Source Charge	Q_{gs}	$V_{DS}=-20V$		2.3		nC
Gate-Drain ("Miller") Charge	Q_{gd}	$V_{GS}=-4.5V$		7		nC
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=-20V$		7		ns
Rise Time	t_r	$I_D=-1A$		20		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G=3.3\Omega$		34		ns
Fall Time	t_f	$V_{GS}=-5V$		29		ns
Input Capacitance	C_{iss}	$V_{GS}=0V$		720	1150	pF
Output Capacitance	C_{oss}	$V_{DS}=-15V$		205		pF
Reverse Transfer Capacitance	C_{rss}	$f=1.0MHz$		165		pF
Gate Resistance	R_g	$f=1.0MHz$		6	12	Ω

* Pulse test

4.2.1 Source-Drain Diode

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward On Voltage*	V_{SD}	$V_{GS}=0V$, $I_S=-2.9A$			-1.2	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0V$, $I_S=-5A$ $dI/dt=100A/\mu s$		32		ns
Reverse Recovery Charge	Q_{rr}			34		nC

* Pulse test

5 N-Channel Diagrams

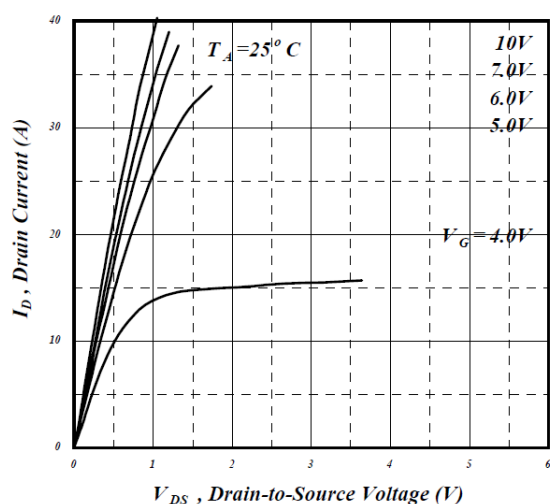


Figure 5.1 Typical output characteristics

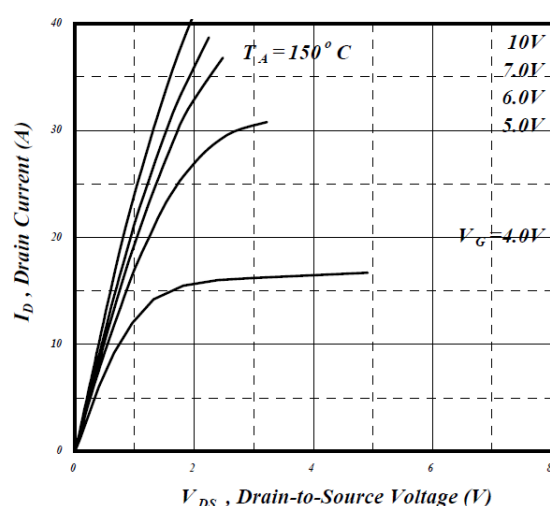


Figure 5.2 Typical output characteristics

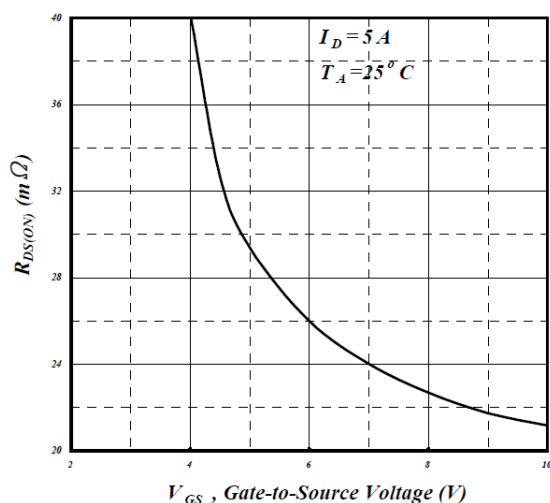


Figure 5.3 On-resistance v.s. gate voltage

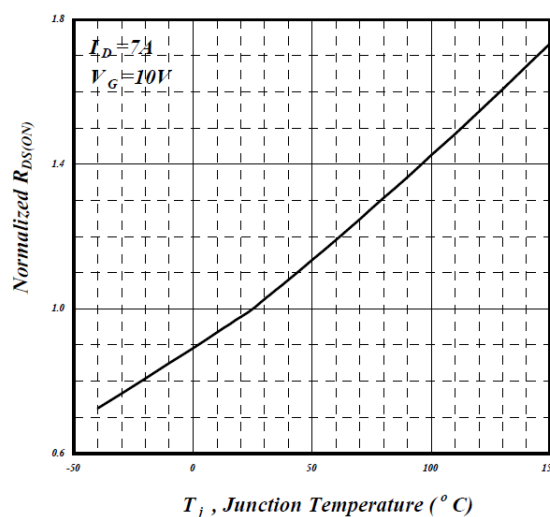


Figure 5.4 Normalized on-resistance v.s. junction temperature

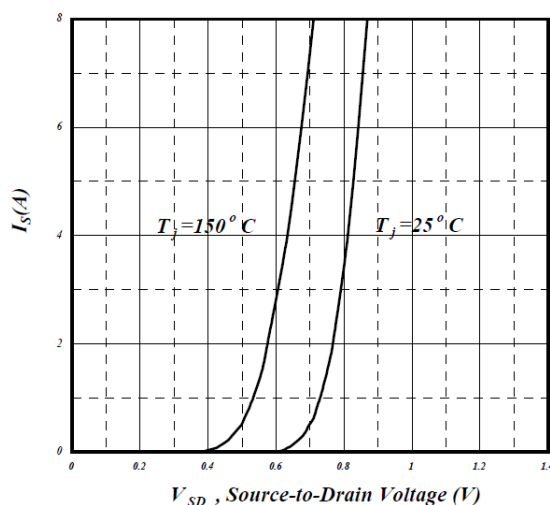


Figure 5.5 Forward characteristic of reverse diode

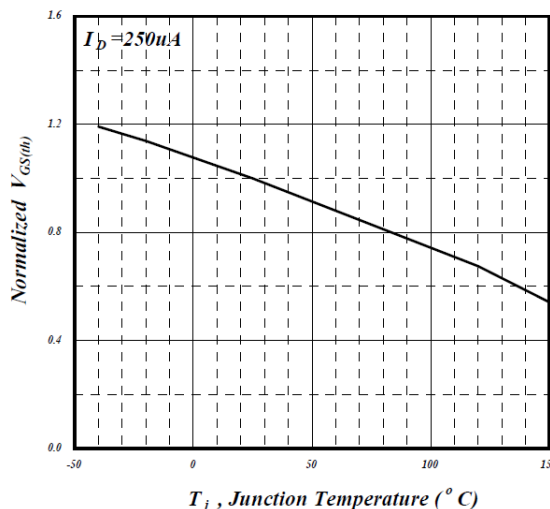


Figure 5.6 Gate threshold voltage v.s. junction temperature

N-Channel Diagrams

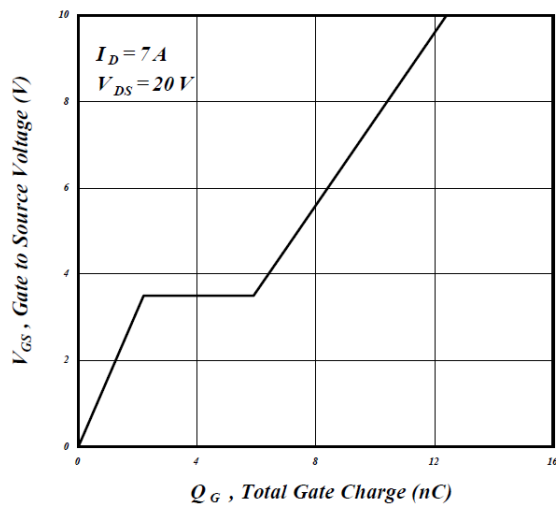


Figure 5.7 Gate charge characteristics

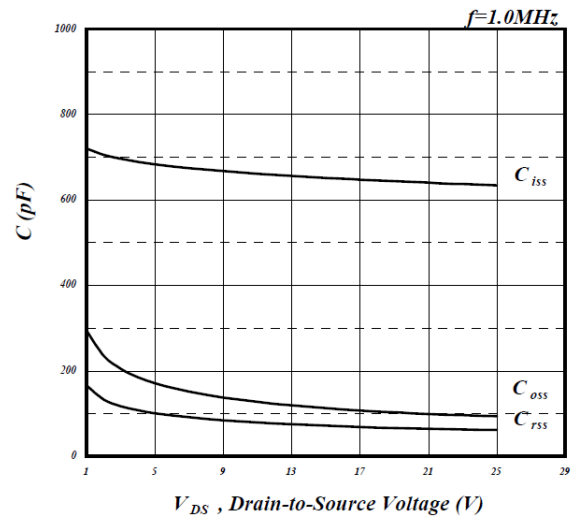


Figure 5.8 Typical capacitance characteristics

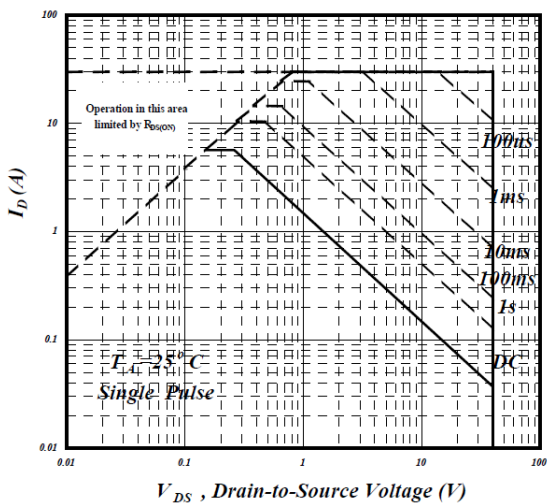


Figure 5.9 Maximum safe operating area

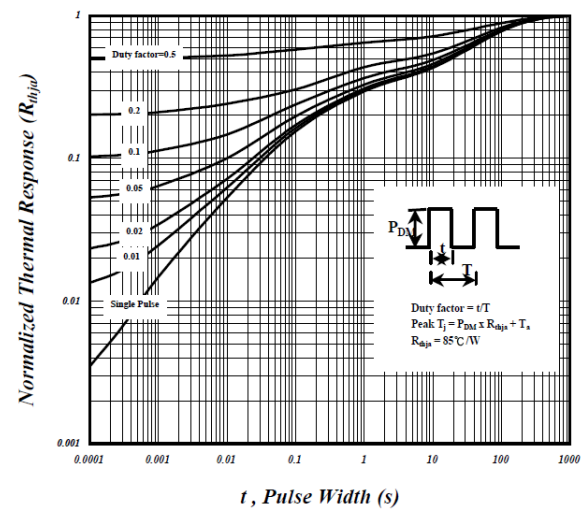


Figure 5.10 Effective transient thermal impedance

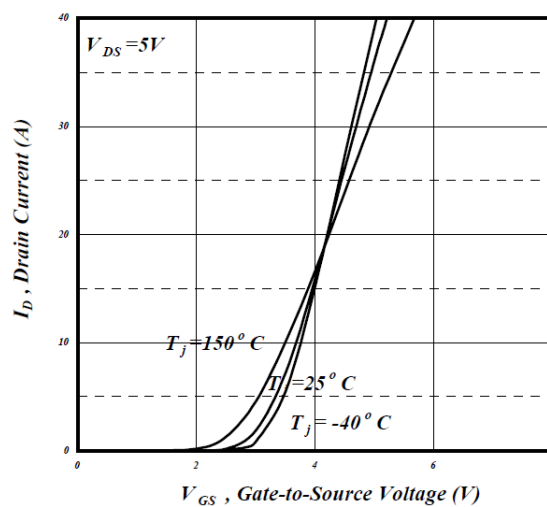


Figure 5.11 Transfer characteristics

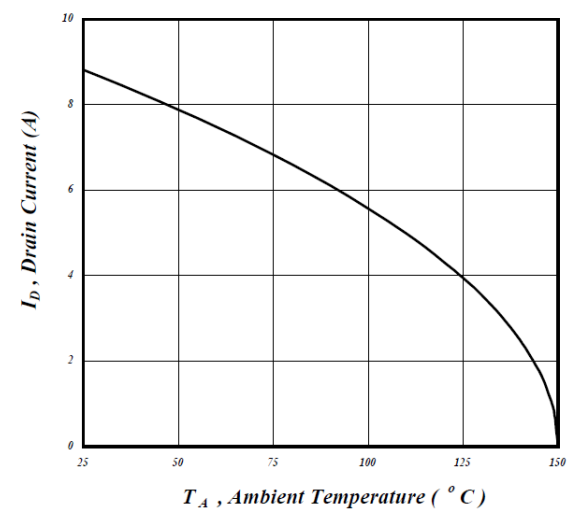


Figure 5.12 Maximum continuous drain current v.s. ambient temperature

6 P-Channel Diagrams

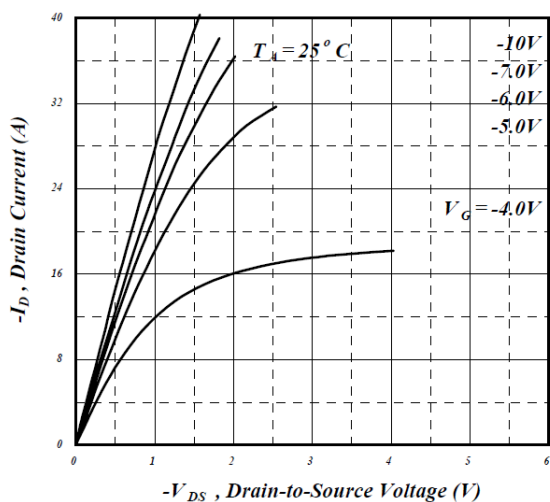


Figure 6.1 Typical output characteristics

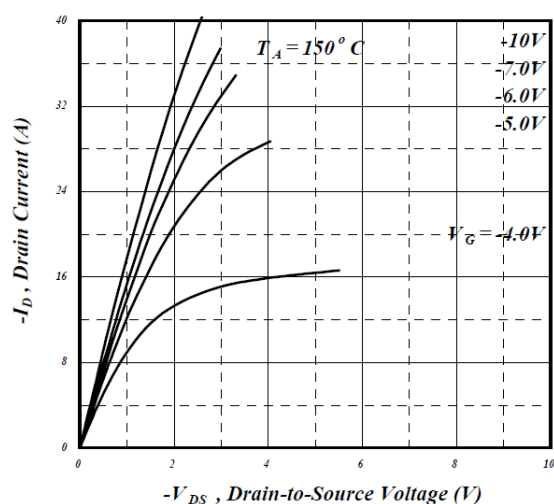


Figure 6.2 Typical output characteristics

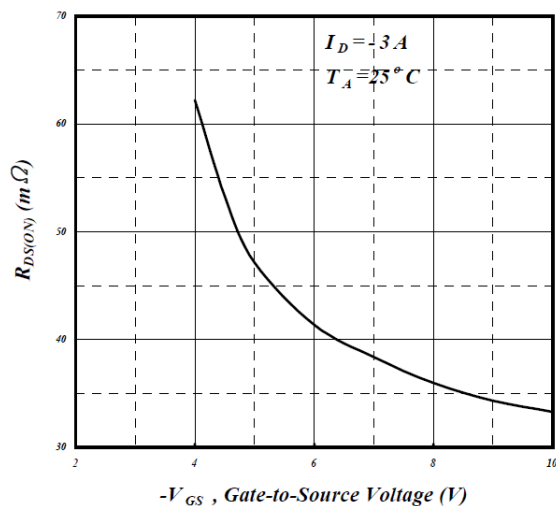


Figure 6.3 On-resistance v.s. gate voltage

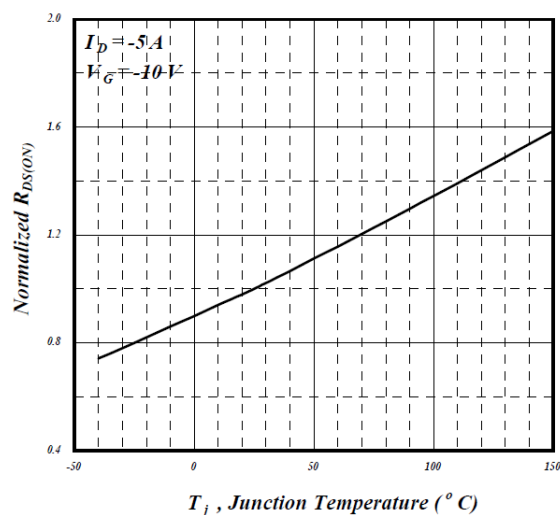


Figure 6.4 Normalized on-resistance v.s. junction temperature

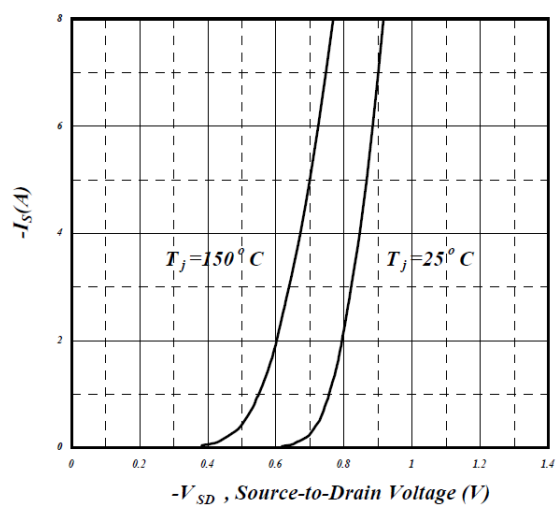


Figure 6.5 Forward characteristic of reverse diode

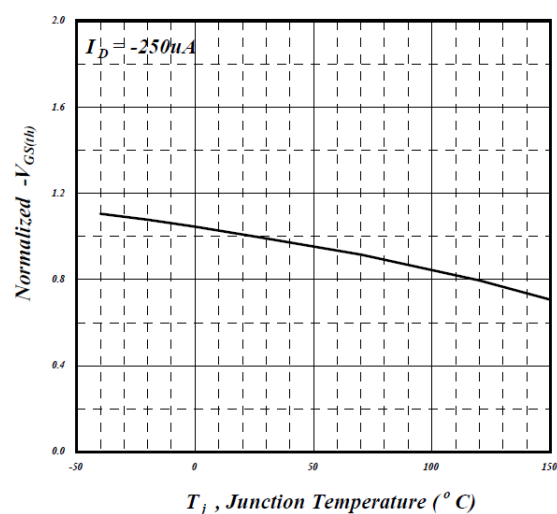


Figure 6.6 Gate Threshold voltage v.s. junction temperature

P-Channel Diagrams

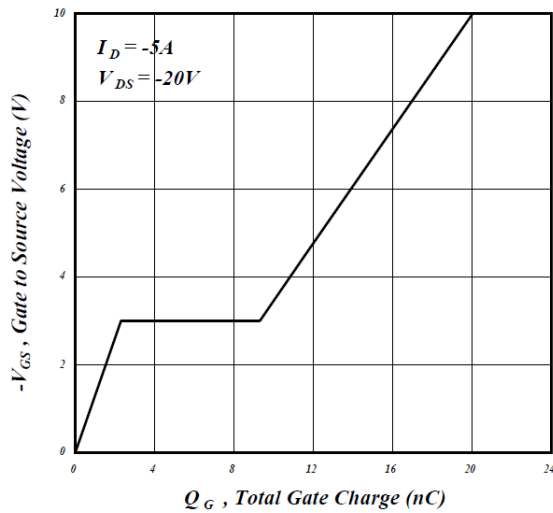


Figure 6.7 Gate charge characteristics

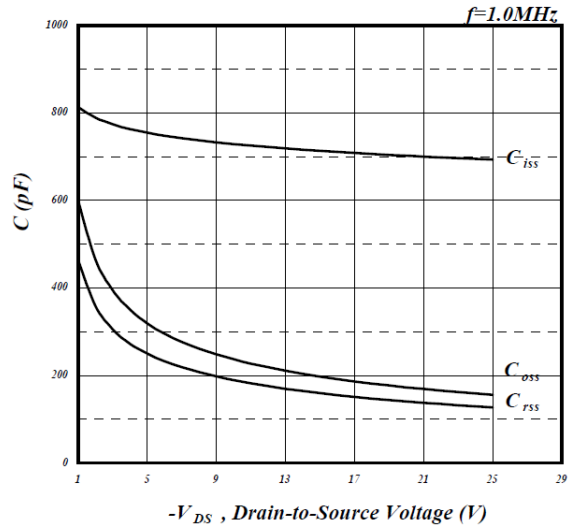


Figure 6.8 Typical capacitance characteristics

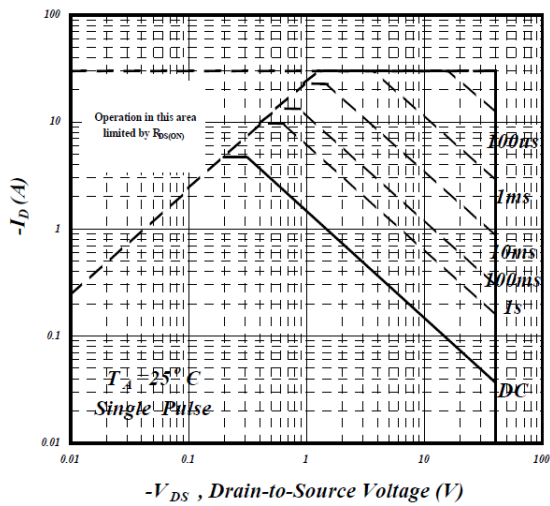


Figure 6.9 Maximum safe operating area

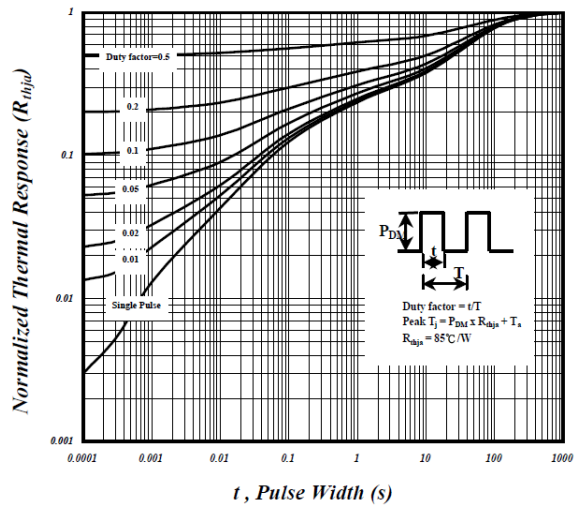


Figure 6.10 Effective transient thermal impedance

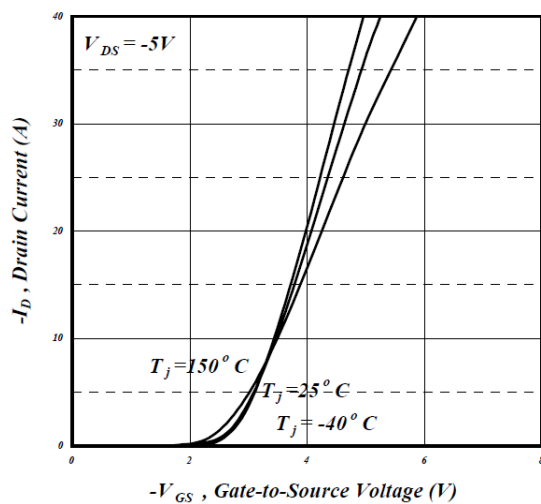


Figure 6.11 Transfer characteristics

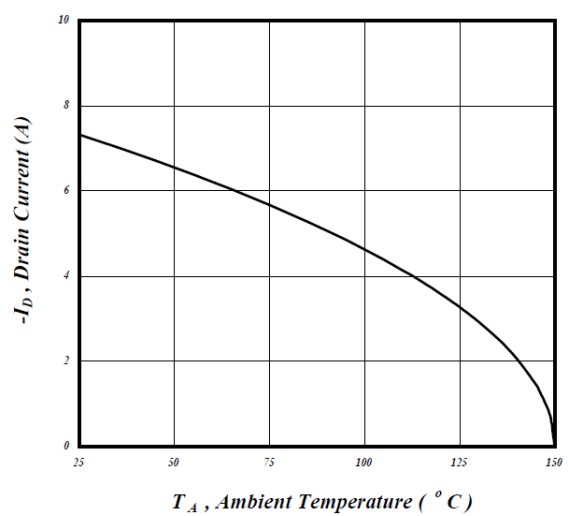


Figure 6.12 Maximum continuous drain current v.s. ambient temperature

7 Package Mechanical Data

7.1 PQFN 5x6 Dimensional Drawings

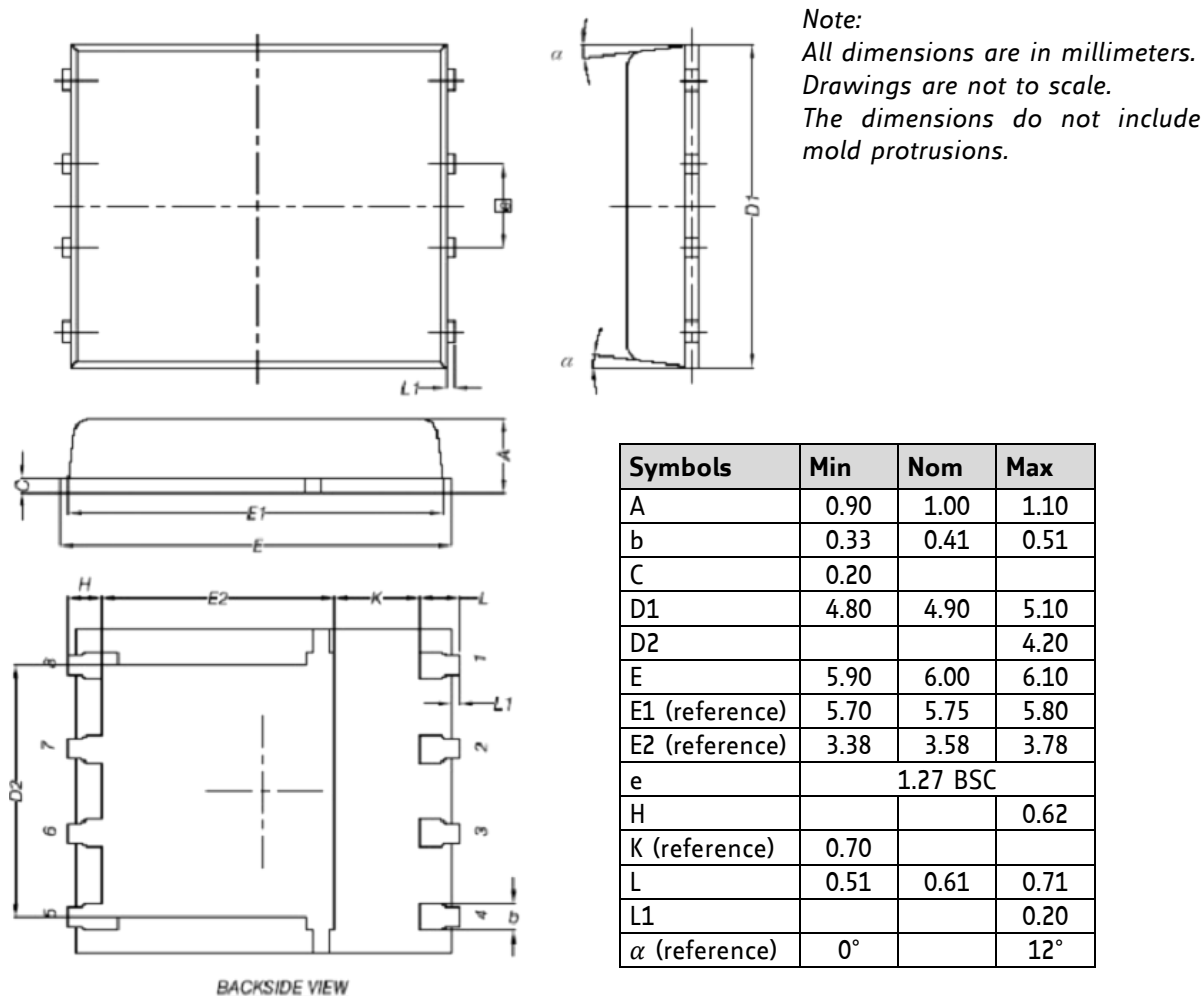


Figure 7.1 Dimensional drawings

7.2 Package Marking Information

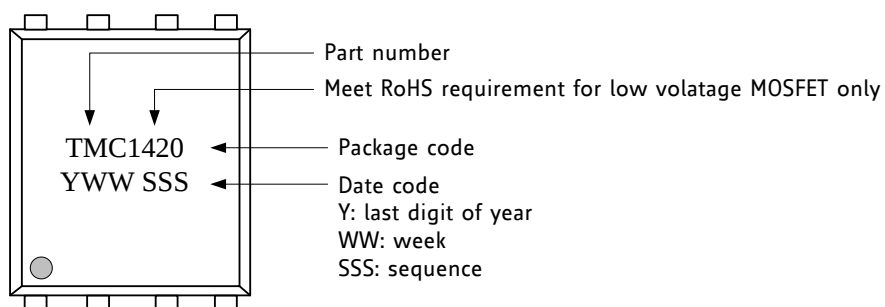


Figure 7.2 Package marking information

7.3 Package Code

Device	Package	Temperature range	Code/ Marking
TMC1420	PQFN 5x6	-55° to +150°C	TMC1420-LA

8 Disclaimer

TRINAMIC Motion Control GmbH & Co. KG does not authorize or warrant any of its products for use in life support systems, without the specific written consent of TRINAMIC Motion Control GmbH & Co. KG. Life support systems are equipment intended to support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

Information given in this data sheet is believed to be accurate and reliable. However no responsibility is assumed for the consequences of its use nor for any infringement of patents or other rights of third parties which may result from its use.

Specifications are subject to change without notice.

All trademarks used are property of their respective owners.

9 ESD Sensitive Device

The TMC1420-LA is an ESD sensitive CMOS device sensitive to electrostatic discharge. Take special care to use adequate grounding of personnel and machines in manual handling. After soldering the devices to the board, ESD requirements are more relaxed. Failure to do so can result in defect or decreased reliability.



10 Table of Figures

Figure 1.1 TMC1420 pin assignments.....	3
Figure 5.1 Typical output characteristics.....	6
Figure 5.2 Typical output characteristics.....	6
Figure 5.3 On-resistance v.s. gate voltage.....	6
Figure 5.4 Normalized on-resistance v.s. junction temperature	6
Figure 5.5 Forward characteristic of reverse diode	6
Figure 5.6 Gate threshold voltage v.s. junction temperature.....	6
Figure 5.7 Gate charge characteristics	7
Figure 5.8 Typical capacitance characteristics.....	7
Figure 5.9 Maximum safe operating area	7
Figure 5.10 Effective transient thermal impedance	7
Figure 5.11 Transfer characteristics	7
Figure 5.12 Maximum continuous drain current v.s. ambient temperature	7
Figure 6.1 Typical output characteristics.....	8
Figure 6.2 Typical output characteristics.....	8
Figure 6.3 On-resistance v.s. gate voltage.....	8
Figure 6.4 Normalized on-resistance v.s. junction temperature	8
Figure 6.5 Forward characteristic of reverse diode	8
Figure 6.6 Gate Threshold voltage v.s. junction temperature	8
Figure 6.7 Gate charge characteristics	9
Figure 6.8 Typical capacitance characteristics.....	9
Figure 6.9 Maximum safe operating area	9
Figure 6.10 Effective transient thermal impedance	9
Figure 6.11 Transfer characteristics	9
Figure 6.12 Maximum continuous drain current v.s. ambient temperature	9
Figure 7.1 Dimensional drawings	10
Figure 7.2 Package marking information	10

11 Revision History

Version	Date	Author SD – Sonja Dwersteg	Description
1.00	2013-MAR-18	SD	Initial version
1.01	2014-MAY-12	SD	RMS motor current values in combination with TMC262, TMC248, and TMC249 updated.

Table 11.1 Documentation revisions