GENERAL DESCRIPTION

TM87A12 is CMOS 12-bit SAR A/D converter, comparator and 4 individual operation amplifiers (input Rail to Rail). A serial control interface is easy to communicate with MCU.

FEATURE

- 3-pins Serial control interface is easy to communicate with MCU.
- Operates ratio metrically or with 5 Vdc or analog span adjusted voltage reference.
- 8-channel multiplexer with address logic.
- 0V to VDD input range with single 2.2V ~ 5V power supply.
- 4 independent input Rail to Rail operation amplifier.

KEY SPECIFICATION

- Resolution 12 Bits
- Total Unadjusted Error ±6 LSB
- Single Supply 2.2V ~ 5V
- A/D Conversion Time 48.5μs
- Comparison Time 26.5μs

PIN DESCRIPTION

Name	I/O	Description
VDD	P	Positive power supply.
VR	I	Reference voltage for analog input signal.
CE	I	Chip enable control signal.
OSCIN	I	RC oscillator input pin.
OSCOUT	O	RC oscillator output pin.
PADEOC	O	A pulse signal of EOC(end of conversion).
CLK	I	Clock for serial interface.
DIN	I	Data input for serial interface.
DOUT	O	Data output for serial interface, tri-state output.
GND	P	Negative supply voltage.
CH1 ~ CH8	I	Analog input channels.
VP1~4	I	OP positive input.
VN1~4	I	OP negative input.
OUT1~4	O	OP output.
AGND	P	Analog GND.

ABSOLOUTE MAXIMUM RATINGS

- Supply Voltage (VDD) -0.3 ~ +5.7V
- Voltage at Any Pin -0.3V to (VDD+0.3V)
- Operating Temperature -20 ~ +70 °C
- Storage Temperature Range -55 ~ +150°C

ALLOWABLE OPERATING CONDITIONS

at Ta=0 to 70℃,GND= 0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD		2.2		5	V
Analog Input Voltage	Vsin		0		5	V
Analog Input Voltage	Vsin		0		5	V
Oscillator Frequency	Fosc	RC oscillator	-	2000	-	kHz

ELECTRICAL CHARACTERISTICS

1. A/D Converter Digital Levels and DC Specification

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
Operating current	Ivdd	VDD = 5V		0.72		mA
		VDD = 3V		0.35		mA
	Isb	VDD = 2.2~5.5, A/D inactive			1	uA
	Ivr	VDD = 5V, A/D Active		220		uA
		VDD = 3V, A/D active		140		uA
		OSC. Active, A/D inactive		50		uA
OFF Channel Leakage Current	Ioff(+)	Analog Multiplexer VDD=5V, Vin=5V		0		uA
	Ioff(-)	Analog Multiplexer VDD=5V, Vin=0V		0		uA

2. Digital Levels and DC Specification

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
Logical “1” Input Voltage	Vih	VDD=5V	4.2		5	V
Logical “0” Input Voltage	Vil	VDD=5V	0		0.7	V
Logical “1” Output Voltage	Voh	VDD=5V	4.2		5	V
Logical “0” Output Voltage	Vol	VDD=5V	0		0.7	V

3. A/D Converter and Comparator Timing Specification

Name	Symb.	Condition	Min.	Typ.	Max.	Unit.
Conversion Time	Tadc	For A/D conversion Fosc=2MHz		44.5		μs
Conversion Time	Tcomp	Comparison mode Fosc=2MHz		26.5		μs

4. A/D Conversion Specification

Name	Symb.	Condition	Min.	Typ.	Max.	Unit.
A/D conversion	Resolution			10		bit
	Differential linearity	Fosc=2MHz, VDD=VR=5V		±2.5	±4	LSB
	Linearity	Fosc=2MHz, VDD=VR=5V		±3.2	±5	
	Total error	Fosc=2MHz, VDD=VR=5V		±4	±6	

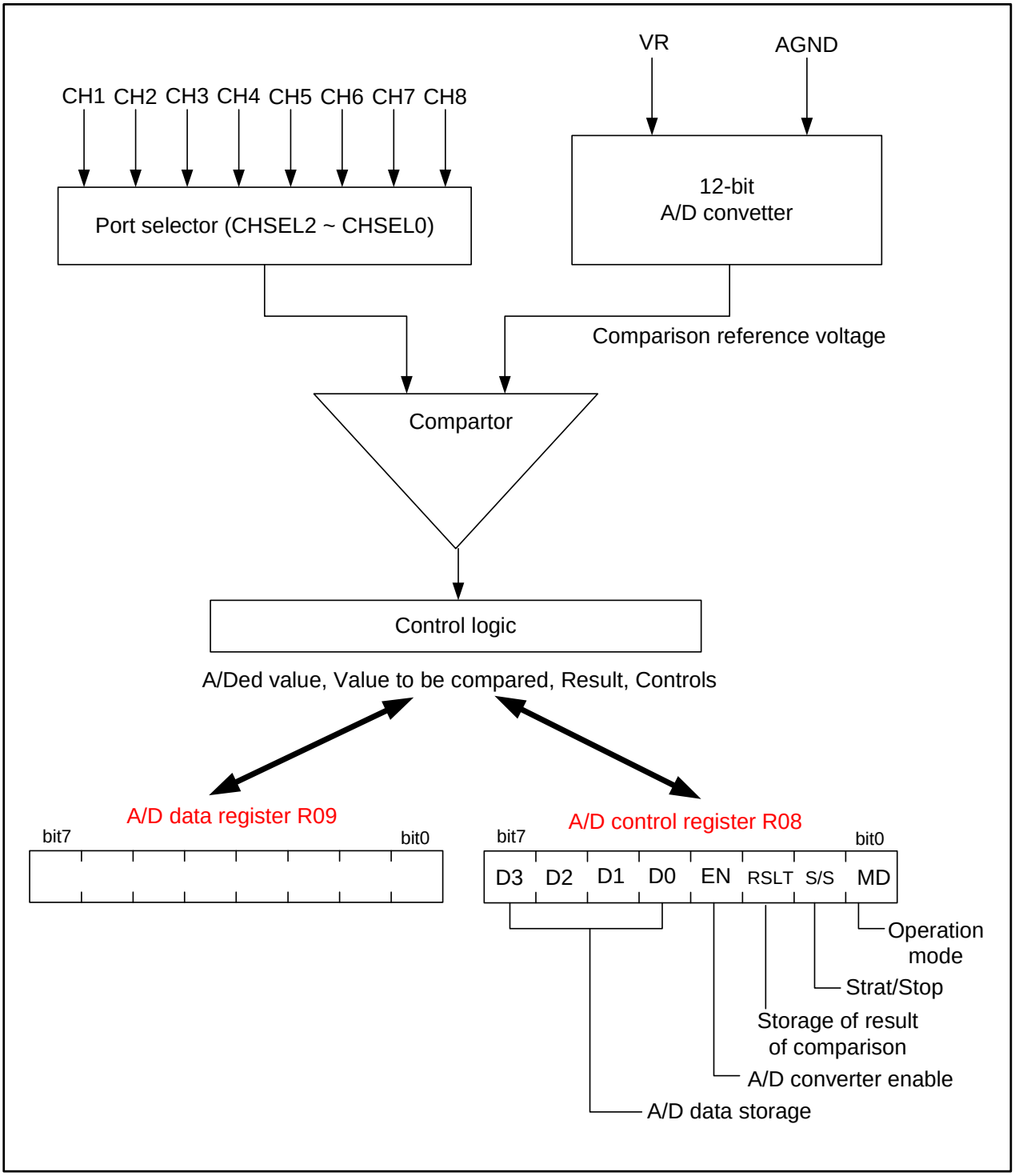
5. OPAMP Specification

Vdd=3.6V，Ta=25℃ unless otherwise specified

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OS}	Input Offset Voltage	Vo=1.8V	—	±7	±15	mV
dV_{OS}/dT	Average Temperature Coefficient of Input Offset Voltage			±15		μV／℃
I_{OS}	Input Offset Current		—	1	—	pA
I_{BIAS}	Input Bias Current			1		pA
V_{ICOM}	Input Common Mode Voltage		0	—	V_+—1	V
V_{OUT+}	Positive Output Voltage Swing	R_L=1MΩ； R_L connect with GND $V_{IN+}-V_{IN-}\geqq$10mV	3.4	3.58	—	V

V_{OUT-}	Negative Output Voltage Swing	R_L=1MΩ； R_L connect with VDD $V_{IN-} - V_{IN+} \geqq 10mV$	—	0.022	0.03	V
R_L	OP amplifier driving R_L	Vo=1.8V； The V_O change under 2%	140			kΩ
R_O	Output Impedance		3			kΩ
GBM	Gain Band Width	R_L=1MΩ；C_L=100pF	—	0.1	—	MHz
CMRR	Common Mode Rejection Ratio		50	70	—	dB
PSRR	Power Supple Rejection Ratio		50	70	—	dB
I_{SUPPLY}	Supple Current Per Single amplifier		—	80	—	μA
S.R+	Slew Rate	Vdd=3.6V , C_L=100pf OP input voltage=3.1±0.5v	—	1	—	v/μsec
S.R-			—	0.13	—	
S.R+		Vdd=3.6V , C_L=100pf OP input voltage = 1.8±0.5v	—	0.26	—	
S.R-			—	0.08	—	
S.R+		Vdd=3.6V , C_L=100pf OP input voltage = 0.5±0.5v	—	0.2	—	
S.R-			—	0.4	—	
S.R+		Vdd=3.6V , C_L=100pf OP input voltage = Rail to Rail	—	1	—	
S.R-			—	0.4	—	
Φm	Phase Margin at Unity Gain	R_L=1MΩ；C_L=100pF	—	65	—	Degree
A_{VOL}	Large Signal Voltage Gain	Vo=1 to 4 V，Vi=1.4V R_L=1MΩ	20	100		V/mV

Block Diagram of A/D Comparator



Function Description

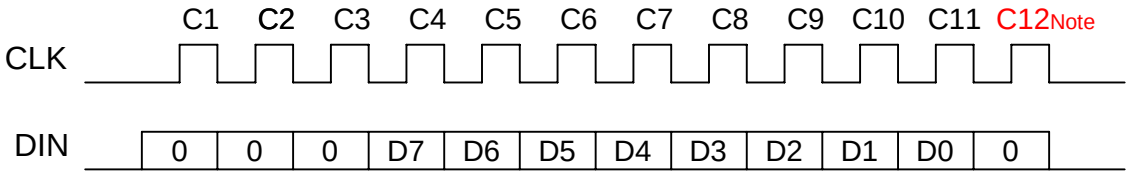
1. Serial Interface Command

There are 5 commands for serial interface, STCH, WR8, WR9, RR8 and RR9.

- *STCH*: enable oscillator for A/D (comparator) & OP enable control & select A/D (comparator) signal input channel,
  Command code: 000
- *WR8*: write data into Register 08,
  Command code: 100
- *WR9*: Write data into Register 09,
  Command code: 110
- *RR8*: Read data from Register 08,
  Command code: 101
- *RR9*: Read data from Register 09,
  Command code: 111

1-1. Select A/D (comparator) signal input channel, enable oscillator for A/D (comparator) and OP enable control

The following diagram shows the timing diagram of sending STCH command.



DOUT Don't care

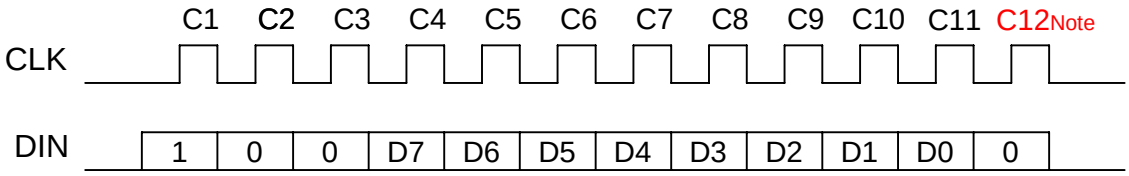
The DIN data in C1~C3 cycle is STCH command, C1 is MSB, C3 is LSB. The DIN data in C4 cycle is Oscillator enable bit, D7=ENOSC. The DIN data in C5~C8 cycle is OPAMP selection information, D6 = EB4, D5 =EB3, D4=EB2, D3=EB1. The DIN data in C8~C10 cycle is A/D converter (comparator) channel selection information, D2 = CHSEL2, D1 = CHSEL1, D0 = CHSEL0.

Note:

- C12 cycle indicated the end of bit.
- It is important to deliver this bit while the command is completed.

1-2. Write data into Register 08 (WR8)

The following diagram shows the timing diagram of writing data into Register 08.



DOUT Don't care

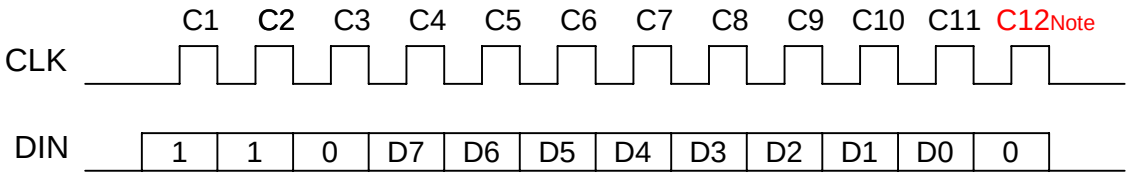
The DIN data in C1~C3 cycle is WR8 command, C1 is MSB, C3 is LSB. The DIN data in C4~C11 cycles are input data for Register 08, D7 = $R08_7$, D6 = $R08_6$,…. D0 = $R08_0$.

Note:

- C12 cycle indicated the end of bit.
- It is important to deliver this bit while the command is completed.

1-3. Write data into Register 09 (WR9)

The following diagram shows the timing diagram of writing data into Register 09.



DOUT Don't care

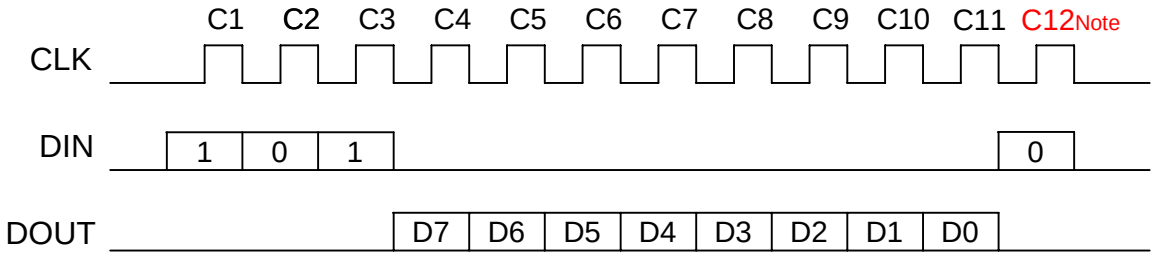
The DIN data in C1~C3 cycle is WR9 command, C1 is MSB, C3 is LSB. The DIN data in C4~C11 cycles are the input data for Register 09, D7 = $R09_7$, D6 = $R09_6$,…. D0 = $R09_0$.

Note:

- C12 cycle indicated the end of bit.
- It is important to deliver this bit while the command is completed.

1-4. Read data from Register 08 (RR8)

The following diagram shows the timing diagram of reading data from Register 08.



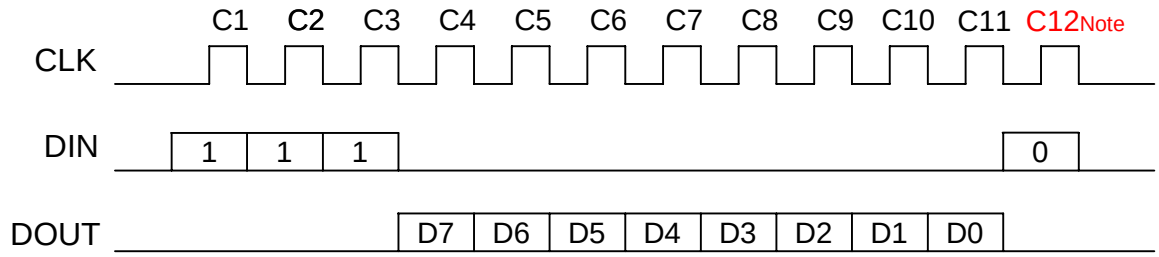
The DIN data in C1~C3 cycle is R08 command, C1 is MSB, C3 is LSB. The DOUT data in C4~C11 cycles are the output data from Register 08, D7 = $R08_7$, D6 = $R08_6$,…. D0 = $R08_0$.

Note:

- C12 cycle indicated the end of bit.
- It is important to deliver this bit while the command is completed.

1-5. Read data from Register 09 (RR9)

The following diagram shows the timing diagram of reading data from Register 09.



The DIN data in C1~C3 cycle is RR9 command, C1 is MSB, C3 is LSB. The DOUT data in C4~C11 cycles are the output data from Register 09, D7 = $R09_7$, D6 = $R09_6$,…. D0 = $R09_0$.

Note:

- C12 cycle indicated the end of bit.
- It is important to deliver this bit while the command is completed.

2. Chip Enable and Chip Reset

The CE input pin is an input for chip enabled controlled and chip reset controlled. When CE=0, the chip will enter reset condition. In this time all function stops operating and the DOUT pin becomes tri-state output. For reducing the power consumption, it is recommended to reset CE pin as 0 when ADC (DAC) function is inactive.

When CE=1, the chip will wake up from reset condition. All function have ready to operate and the DOUT pin becomes output data. The chip will get into waiting state to receive the command from serial interface.

Since no power on reset circuitry is built in this chip, it is necessary to set CE pin to 0 after power on state to initiate this chip.

3. A/D conversion mode

The A/D conversion mode converts the analog voltage on A/D pin into the digital value. The input analog voltage is successively compared with weighted voltages form the capacitor array. Digitized conversion data (12-bit) are stored into upper 4 bit places of the control register R08 and the remaining bit into the data register R09.

The time required for the converter to complete conversion is as follows:

Conversion duration = Oscillator clock period x 2 x 44.5

Example:

(a). 48.5us (oscillator clock at 2MHz)

(b). 485us (oscillator clock at 200KHz)

Caution:

While in the A/D conversion mode, do not use registers (upper 4 bits of R08 register and the R09 register) reserved for storage of A/D data to store other data.

3-1. Selecting A/D input pin & selecting OPAMP & A/D enable control

Executing STCH command to enable Oscillator and then select one of A/D pins (CH1~CH8) as the A/D input pin.

- *Setting of Oscillator enable pins*

  Before using A/D conversion function, ENOSC bit must be set to 1 to start-up the oscillator in order to provide the clock for A/D conversion mode.

ENOSC= ' 1' => Oscillator turn on	ENOSC= ' 0' => Oscillator turn off

It is recommended to turn off the oscillator when A/D conversion mode is completed in order to reduce the power consumption.

- *Setting of A/D select pins (selection of A/D pin)*

Bits of CHSEL0 ~ 2			A/D pin
CHSEL2	CHSEL1	CHSEL0	
0	0	0	CH1
0	0	1	CH2
0	1	0	CH3
0	1	1	CH4
1	0	0	CH5
1	0	1	CH6
1	1	0	CH7
1	1	1	CH8

When executing STCH command to enable A/D conversion or comparison mode, the OPAMP selection information bits (EB4~EB1) have to be kept in the state they are, or the OPAMP will be malfunction.

3-2. Starting A/D conversion

A/D conversion starts according to the bit setting of the A/D control register R08. Other operations are set up 0 on setting the start of A/D conversion. All settings specified by the contents of the control register R08 are set at the same time when A/D conversion starts. Execute WR8 command and delivers the desired value into R08 register. Refer to **1-2. Write data into Register 08 (WR8)** for the execution of WR8 command.

- *Settings to start A/D conversion*

Setting of register R08	Operation
R083, R081 = 1	Start A/D conversion
R080 = 0	Set operation mode to A/D conversion

When setting A/D control register R08 for A/D conversion start, the bits of R08 other than bits shown in the table above can be any value. These bits will not affect A/D conversion. In contrast, do not modify contents of the control register R08 and data register R09 while the A/D converter is running.

3-3. Indication of end of A/D conversion

At the end of A/D conversion the bit-S/S (bit 1 of control register R08) and bit EN (bit 3 of control register R08) are cleared. Monitoring one of these bits detects the end of A/D conversion. There is an external pin (PADEOC) to indicate the end of conversion. When the conversion is completed, an “H” pulse signal will outputted to this pin.

3-4. Storing digitized data

The digital equivalent of analog input voltage (ADed data) consisting of 12 bits is stored into registers: LSB 4 bits into the control register R08(bits R084、R085、R086 and R087) and the remaining 8 bits into the data register R09.

- *[ADed data stored in registers]*

Bit-11	Bit-10	Bit-9	Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R097	R096	R095	R094	R093	R092	R091	R090	R087	R086	R085	R084

R097 ~ R090: A/D data register R09

R087 ~ R084: Upper 4 bits of control register R08

- *[Input voltage and ADed data]*

Input voltage = [ADed data (12 bits) / 4096] * VR (V)

Note: ADed data (12 bits) = Converts into decimal value

Executing RR8 and RR9 command could read out the contents of register R08 and R09 to DOUT pin. Refer to **1-4. Read data from Register 08 (RR8)** and **1-5. Read data from Register 09 (RR9)** for the operation of RR8 and RR9 command.

4. Comparison mode

The comparison mode compares the level of analog voltage coming from one of pins of CH1 ~ CH8 with the internal voltage set by the control registers R08 and R09, storing the result into the bit 4 (R084) of the mode register R08.

The time required to complete conversion is as follows:

Conversion duration = Oscillator clock period x 2 x 26.5

Example:

(a). 26.5us (Oscillator clock at 2MHz)

(b). 265us (Oscillator clock at 200KHz)

4-1. Selecting A/D input pin

Executing STCH command to enable Oscillator and then select one of A/D pins (CH1~CH8) as the A/D input pin.

- *Setting of Oscillator enable pins*

  Before using comparator function, ENOSC bit must be set to 1 to start-up the oscillator in order to provide the clock for comparison mode.

ENOSC= ' 1' => Oscillator turn on	ENOSC= ' 0' => Oscillator turn off

  It is recommended to turn off the oscillator when A/D conversion mode is completed in order to reduce the power consumption.

- *Setting of A/D select pins (selection of A/D pin)*

Bits of CHSEL0 ~ 2			A/D pin
CHSEL2	CHSEL1	CHSEL0	
0	0	0	CH1
0	0	1	CH2
0	1	0	CH3
0	1	1	CH4
1	0	0	CH5
1	0	1	CH6
1	1	0	CH7
1	1	1	CH8

When executing STCH command to enable comparison mode, the operational amplifier selection information bits (EB4~EB1) have to be kept in the state they are, or the operational amplifier will be malfunction.

4-2. Setting internal comparison voltage

The internal voltage data to be compared with the analog A/D input is stored into the data register R09 and upper 4 bit positions of the control register R08, the same location as for storing ADed data. The same registers are used for storing ADed data and internal voltage data.

Executing WR8 and WR9 command to deliver the internal voltage data and store the data into register R08 (R09).

- *[Internal reference voltage data set in registers]*

Bit-11	Bit-10	Bit-9	Bit-8	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
R097	R096	R095	R094	R093	R092	R091	R090	R087	R086	R085	R084

R097 ~ R090: A/D data register R09

R087 ~ R084: Upper 4 bits of control register R08

- *[Internal reference voltage]*

Comparison reference voltage = [Register value (12 bits) / 4096] * VR (V)

Note: Register value (12 bits) = Convert register value into decimal number

4-3. Starting comparison

The comparison starts when the bit of the A/D control register is set. The operation mode should be set upon starting of the comparison. All A/D control register settings are made at the same time.

Executing WR8 command to deliver the desired value and store the data into register R08. Settings are shown below:

- *Settings to start comparison*

Setting of register R08	Settings
R087, R086, R085, R084 = * , *	Lower 4 comparison bits
R081, R083 = 1	Start comparison
R080 = 1	Set mode to comparison

Settings of bits other than those necessary to start comparison will not affect the comparison operation. Do not modify mode registers R08 and R09 while the A/D converter is running.

4-4. Indication of end of comparison

At the end of comparison, the bit-S/S (bit 1 of control register R08) and bit EN (bit 3 of control register R08) are cleared. Monitoring one of these bits detects the end of comparison.

There is an external pin (PADEOC) to indicate the end of conversion. When the conversion is completed, an “H” pulse signal will outputted to this pin.

4-5. Storing comparison result

The result of comparison sets the bit RSLT (bit 2 of control register R08) or the control register to either [1] or [0] depending on the level of the input voltages as shown below.

Bit 2 of register R08	Result
R082 = 0	Input voltage < internal reference voltage
R082 = 1	Input voltage > internal reference voltage

When the input voltage is equal to the internal reference voltage, the level of bit RSLT (R082) is undefined.

5. Setting OPAMP mode

When CE pin is set to 1, all of the OPAMPs are in disable condition. Executing STCH command to enable the OPAMP you needed. Each of these OPAMPs could be enabled or disable individually.

- *Setting of OPAMP select pins*

Bits of EB1 ~ 4				OP
EB4	EB3	EB2	EB1	
0	0	0	1	OP1 turn on
0	0	1	0	OP2 turn on
0	1	0	0	OP3 turn on
1	0	0	0	OP4 turn on
1	1	1	1	OP1~4 turn on

- *Setting of Oscillator enable pins*

When A/D conversion mode and comparison mode don't be used in this period, ENOSC bit could be set to 0 to reduce the power consumption. If these functions are still operating in this period, ENOSC bit must be set to 1 to keep in operation.

ENOSC= ' 1' => Oscillator turn on	ENOSC= ' 0' => Oscillator turn off

- *Setting of A/D select pins (selection of A/D pin)*

When A/D conversion mode and comparison mode don't be used in this period, CHSEL0~2 could be any data. If these functions are still operating in this period, these bits must be kept in their previous state, or A/D conversion mode and comparison mode will be malfunction.

Bits of CHSEL0 ~ 2			A/D pin
CHSEL2	CHSEL1	CHSEL0	
0	0	0	CH1
0	0	1	CH2
0	1	0	CH3
0	1	1	CH4
1	0	0	CH5
1	0	1	CH6
1	1	0	CH7
1	1	1	CH8

6. Summary of A/D converter operations

Typical operation procedure of A/D converter is summarized as below. The bit represented by [X] is user settable.

6-1. General procedure of using A/D conversion mode

The procedure is to use the A/D converter in the A/D conversion mode.
Steps below are to convert the analog voltage on pin CH1 to the digital value.

1). Start-up oscillator ← (ENOSC) = 1
2). Select analog input pin ← (CHSEL2, CHSEL1, CHSEL0) = 000
3). Control register R08 ← 0000 1010B (specify operation mode and start A/D converter)

This procedure starts the A/D converter. When A/D conversion time has elapsed, the A/D converter stops and stores the result in register R08 (upper 4 bit places) and the register R09. End of the operation can be verified by reading bits 1 or 3 of control register R08 that should be [0].

6-2. General procedure of using comparison mode

This operation is to compare the analog voltage from pin CH3 with the internal reference digital value.

1). Start-up oscillator ← (ENOSC) = 1

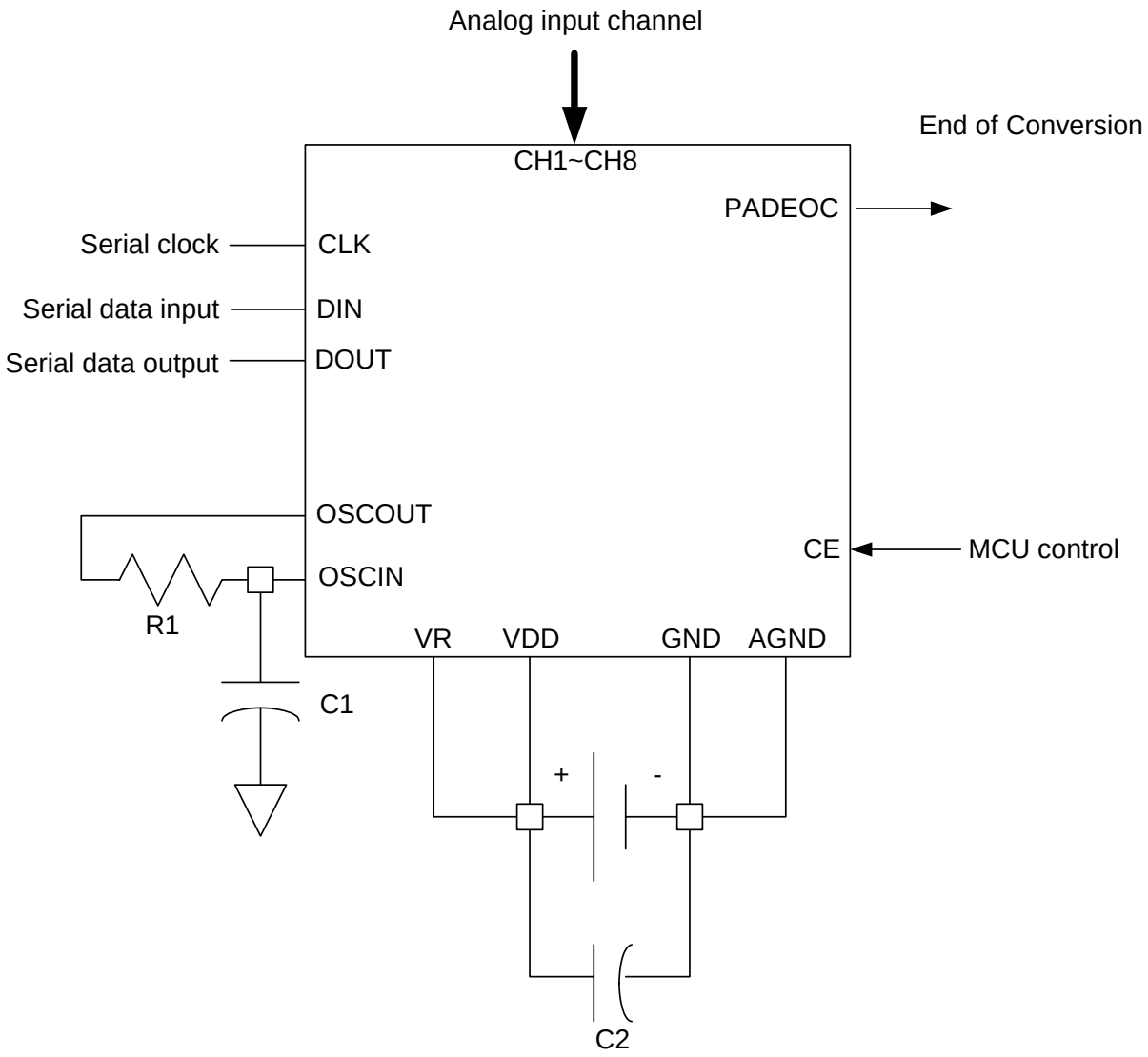
2). Select analog input pin ← (CHSEL2, CHSEL1, CHSEL0) = 011

3). Data register R09 ← XXH (sore upper 8 bits of comparison data)

4). Control register R08 ← XXXX 1011B (store lower 4 bits, specify operation mode, start A/D converter)

The above procedure starts the A/D converter. When the conversion time has elapsed, the converter stops and stores the results of comparison into bit 2 of the register R08:[1] when the analog input is higher than the reference voltage, [0] when lower.

Typical Application Circuit of A/D converter and comparator



Note:

- R1 and C1 are the external components of the RC oscillator.
- RC Oscillator output frequency on OSCOUT pin: 2MHz (the loading of probe (10pf) is included)
- Condition:
  R1 = 4.99k C1 = 30p(Xin), @ VDD=2.4V
  R1 = 5.62k C1 = 30p(Xin), @ VDD=3V
  R1 = 6.81k C1 = 30p(Xin), @ VDD=5V