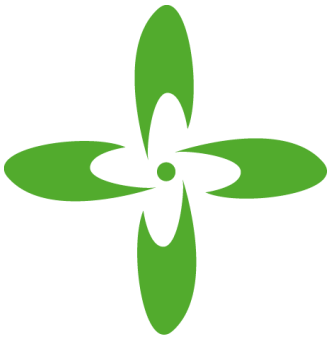

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TM56F1543

DATA SHEET

Rev 0.94

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AMENDMENT HISTORY

Version	Date	Description
0.90	Sep, 2022	New Release
0.91	Oct, 2022	Page 5,8, 13~15: Add Lib Protect function description Page 5, 122: update DC current description
0.92	Dec, 2022	Page 10: Add Pin Assignment Page 12: Add Pin Summary
0.93	Mar, 2023	Page 11: Add Pin Assignment for SOP8 Page 13: Add Pin Summary for SOP8 Page 25: Add HWAUTO only work for ASM Page 34: Add TK INT can't wakeup from IDLE mode description Page 125: modify EEPROM write endurance condition Page 130: Add Ordering information for SOP8
0.94	May, 2023	Page 5: Modify System Oscillation Sources can be divided by 1/2/4/8 Page 7: Add Note for Operating Voltage Page 7: Modify Operating Temperature Range: : -40℃ to + 105℃ Page 8: Modify Lib Protect function description Page 18, 107: add forbid reading TABR in interrupt Page 130: Add Ordering information for TSSOP20

CONTENTS

FEATURES

1. **ROM: 8K x 16 bits Flash Program Memory with Page Locker function.**
2. **EEPROM: 128 x 8 bits**
3. **RAM: 496 x 8 bits**
4. **STACK: 8 Levels**
5. **System Oscillation Sources (Fsys) :**
   - Fast-clock
     - ✧ FIRC (Fast Internal RC) : Max. 18.432 MHz (can be trimmed)
     - ✧ FXT (Fast Crystal): 1M~18MHz
   - Slow-clock
     - ✧ SIRC (Slow Internal RC) : 50 KHz @VCC=5V
     - ✧ SXT (Slow Crystal): 32.768KHz
6. **System Clock Prescaler:**
   - System Oscillation Sources can be divided by 1/2/4/8 as System Clock (Fsys)
7. **Dual System Clock:**
   - FIRC+SIRC
   - FIRC+SXT
   - FXT+SIRC
8. **I/O ports: Maximum 26 programmable I/O pins**
   - Open-Drain Output
   - CMOS Push-Pull Output
   - Schmitt Trigger Input with pull-up resistor option
   - Support High sink mode: 70mA @VCC=5V, V_{OL}=0.5V; 140mA@VCC=5V, V_{OL}=1.2V
   - Support constant current Drive mode: 19mA@VCC=5V,V_{OH}=2.5V~3.8V
9. **Power Saving Operation Mode**
   - FAST Mode: Slow-clock can be disabled or enabled, Fast-clock keeps CPU running
   - SLOW Mode: Fast-clock can be disabled or enabled, Slow-clock keeps CPU running
   - IDLE Mode: Fast-clock and CPU stop. Slow-clock, T2, or Wake-up Timer keep running
   - STOP Mode: All clocks stop, T2 and Wake-up Timer stop
10. **3 Independent Timers**
    - Timer0
      - ✧ 8-bit timer divided by 1~256 pre-scaler option, Reload/Interrupt/Stop function

- Timer1
  - ✧ 8-bit timer divided by 1~256 pre-scaler option, Reload/Interrupt/Stop function
  - ✧ Overflow and Toggle out
- T2
  - ✧ 15-bit timer with 4 interrupt interval time options
  - ✧ IDLE mode wake-up timer or used as one simple 15-bit time base
  - ✧ Clock source: Slow-clock (SIRC), Fsys/128

11. Interrupt

- Three External Interrupt pins
  - ✧ 1 pin is falling edge wake-up triggered & interrupts
  - ✧ 2 pins are rising or falling edge wake-up triggered & interrupt
- Timer0/Timer1/T2/WKT (wake-up) Interrupts
- ADC Interrupt
- TK (3 Touch Key module)
- I2C Interrupt
- UART Interrupt
- Pin Change Interrupt
- LVD Interrupt

12. Wake-up (WKT) Timer

- Clocked by built-in RC oscillator with 4 adjustable interrupt times
  20.5 ms/41 ms/82 ms/164 ms

13. Watchdog Timer

- Clocked by built-in RC oscillator with 4 adjustable reset times
  164ms/328ms/655ms/1311ms
- Watchdog timer can be disabled/enabled in STOP mode

14. PWM

- PWM0 :
  - ✧ 16 bits, duty-adjustable, period-adjustable controlled PWM
  - ✧ PWM0 Clock source: System clock or FIRC (18.432MHz) or FIRC*2 (36.864MHz)
  - ✧ PWM0 with 4 output modes
  - ✧ Complementary PWM0 output (PWM0P, PWM0N)
  - ✧ Non overlap time durations adjustable. (0~15 PWM CLK)
- PWM1~5:
  - ✧ 16 bits, duty-adjustable (Independent) , period-adjustable controlled (shared with PWM0)
  - ✧ Clock source (Shared with PWM0)

15. 24-Channel Touch Key with 3 TK-module (TKM0/TKM1/TKM2)

- Each TK module with 8-channel touch key
- Each module include:
  - ✧ 3-bit TK reference clock capacitor adjustment
  - ✧ 8-bit touch key clock frequency select(can be fixed frequency or auto change)
  - ✧ 14-bit TK scan length adjustment
- Interrupt/Wake-up CPU while key is pressed.

16. I2C Interface

- Specific purpose slave I2C interface with interrupt function

17. UART Interface

- 7/8/9 bits mode TX/RX selectable
- Supported Baud-Rate range from 9600bps to 115200 bps with proper selected oscillation frequency and baud rate clock divide
- Automatic parity generation and detection
- Detects Overrun, Frame Error and Parity Error

18. 12-bit ADC Converter with 14 input channels and 1 internal reference voltage

- Internal Reference Voltage: VBG 1.20V±1% @VCC=5V~2.5V, 25℃
- Internal reference voltage: 1/4VCC
- ADC reference voltage: VCC, 2.5V

19. All pin change wake up (negedge and posedge trigger)

20. Reset Sources

- Power On Reset/Watchdog Reset/Low Voltage Reset/External Pin Reset

21. Low Voltage Reset (LVR) /Low Voltage Detection Flag (LVD) Option:

- 16-Level Low Voltage Reset: 2.05 ~ 4.15 V
- 16-Level Low Voltage Detection Flag (Disable, 2.28V ~ 4.15V)

22.Operating Voltage :

- Fsys= 1 MHz, LVR ~5.5V
- Fsys=18.432 MHz, 2.5~5.5V

Note: Power-up VCC must exceed POR 1.95V and user selected LVR level, refer to the "Electrical Characteristics Graphs" to avoid entering ROM dead zone

23. Operating Temperature Range : -40°C to + 105°C

24. Integrated 16-bit Cyclic Redundancy Check (CRC)

25. Table Read Instruction: 16-bit ROM data lookup table

26. Instruction set: 39 Instructions

27. Instruction Execution Time

- 2 system clocks (Fsys) per instruction except branch

28. Built-in 1/2 bias for software LCD display (4 COM)

29. Programming connectivity support 4-wire (ICP) or 5-wire program

30. Page Locker Size: 512W/640W/768W …./2304W by 128 words step

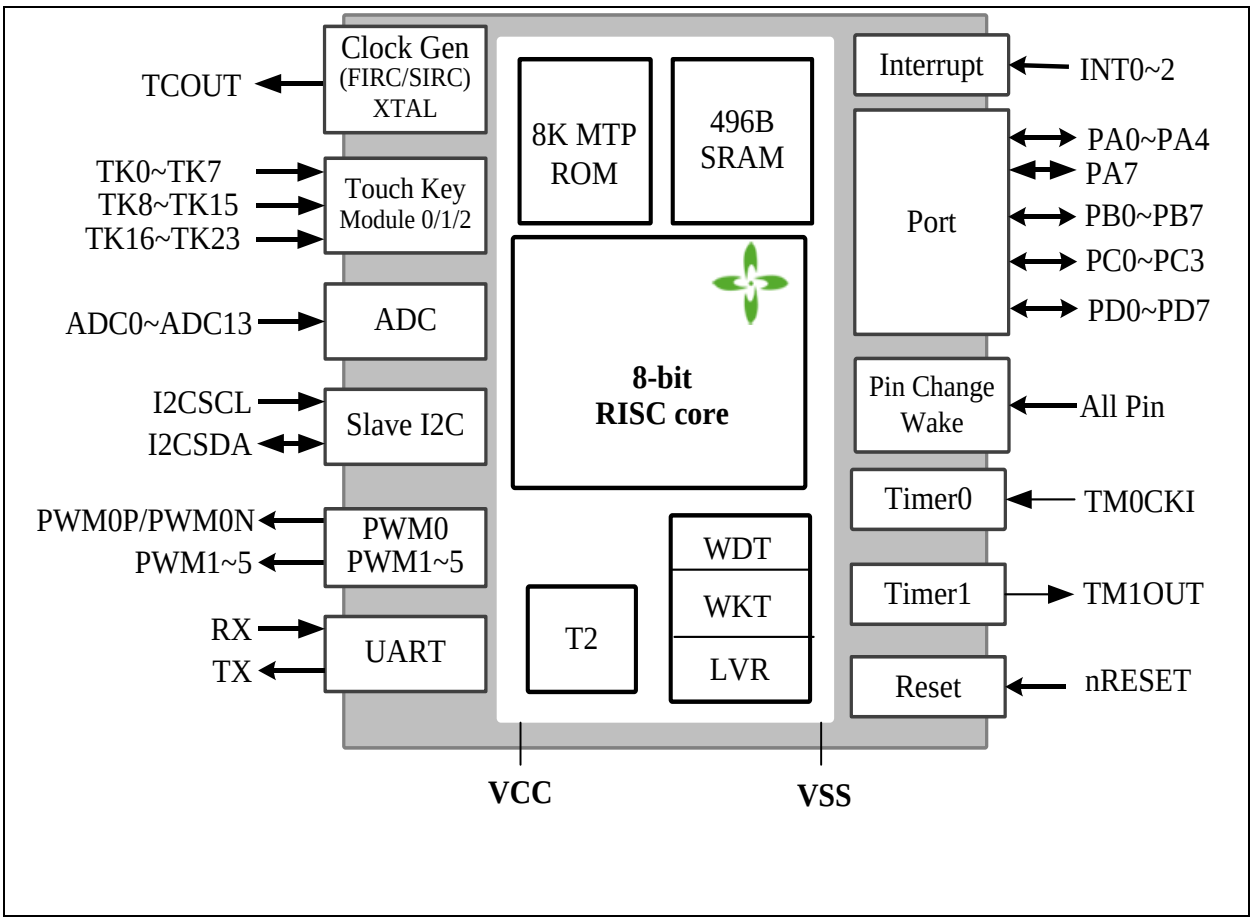
31. Package Types:

- SOP-28

32. Supported EV board (ICE) on Real Chip Debug

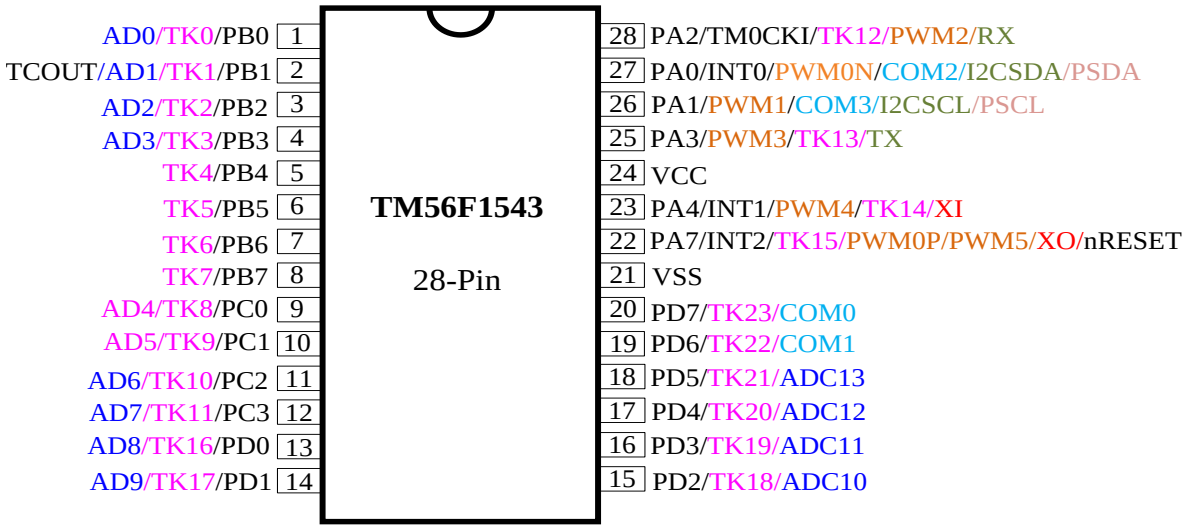
- Use PA0/PA1 pin or PC0/PC1 pin
- Share with ICP programming pin

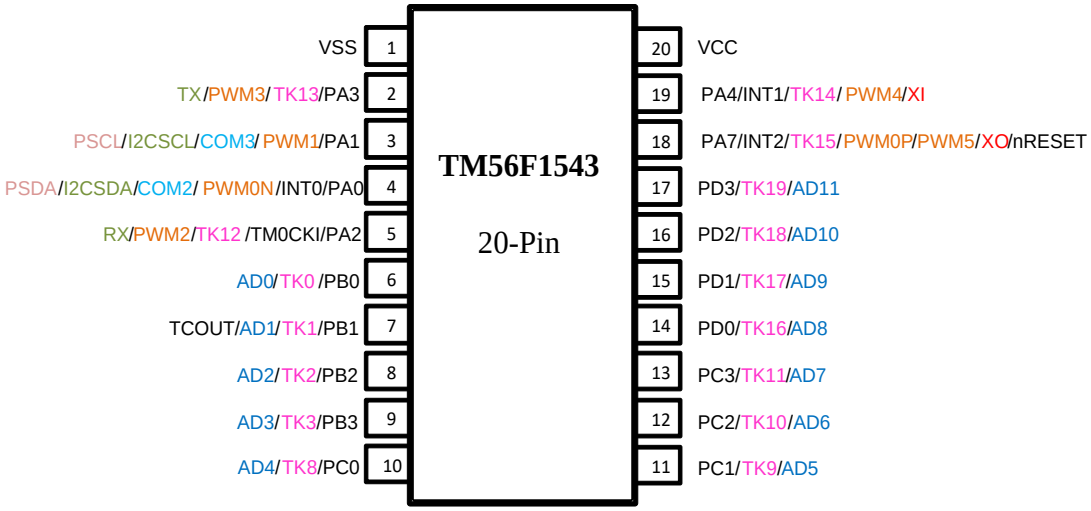
SYSTEM BLOCK DIAGRAM

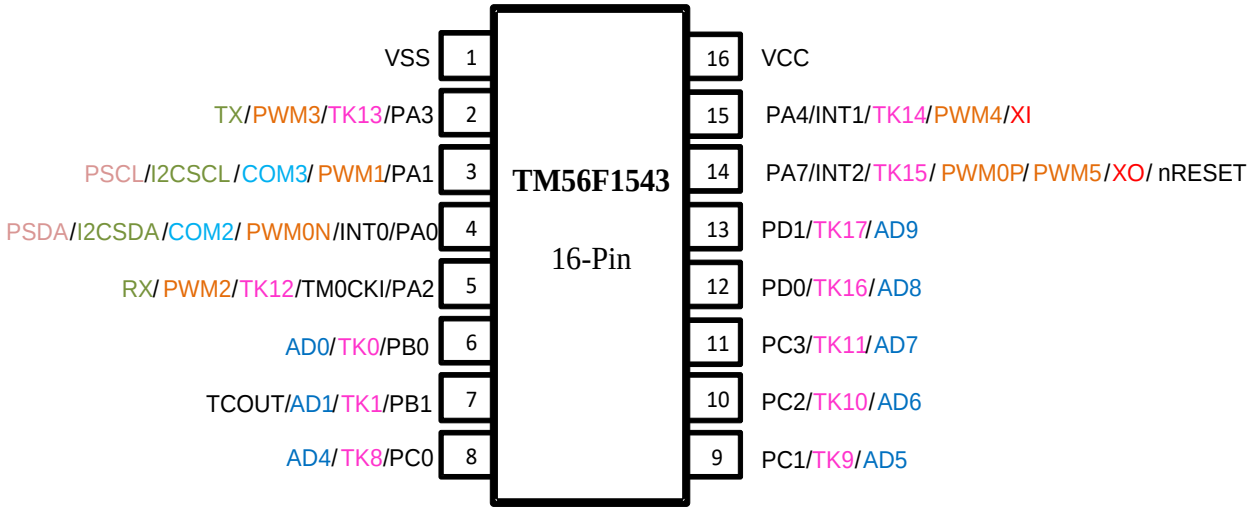


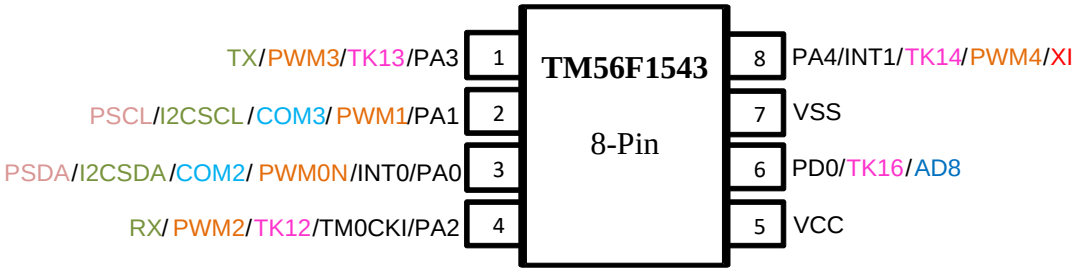
TM56F1543 Block Diagram

PIN ASSIGNMENT DIAGRAM






TM56F1543
16-Pin
VSS 1
TX/PWM3/TK13/PA3 2
PSCL/I2CSCL/COM3/PWM1/PA1 3
PSDA/I2CSDA/COM2/PWM0N/INT0/PA0 4
RX/PWM2/TK12/TM0CKI/PA2 5
AD0/TK0/PB0 6
TCOUT/AD1/TK1/PB1 7
AD4/TK8/PC0 8
16 VCC
15 PA4/INT1/TK14/PWM4/XI
14 PA7/INT2/TK15/PWM0P/PWM5/XO/nRESET
13 PD1/TK17/AD9
12 PD0/TK16/AD8
11 PC3/TK11/AD7
10 PC2/TK10/AD6
9 PC1/TK9/AD5


TM56F1543
8-Pin
TX/PWM3/TK13/PA3 1
PSCL/I2CSCL/COM3/PWM1/PA1 2
PSDA/I2CSDA/COM2/PWM0N/INT0/PA0 3
RX/PWM2/TK12/TM0CKI/PA2 4
8 PA4/INT1/TK14/PWM4/XI
7 VSS
6 PD0/TK16/AD8
5 VCC

PIN DESCRIPTIONS

Name	In/Out	Pin Description
PA7, PA4–PA0	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or open-drain output. Pull-up resistor are assignable by software.
nRESET	I	External active low reset/ Schmitt-trigger input
VCC, VSS	P	Power input pin and ground
INT0~INT2	I	External interrupt input
PB7-PB0	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or open-drain output. Pull-up resistor are assignable by software.
PC3-PC0	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or open-drain output. Pull-up resistor are assignable by software.
PD7-PD0	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or open-drain output. Pull-up resistor are assignable by software.
PWM0P/PWM0N PWM1 PWM2 PWM3 PWM4 PWM5	O	PWM0/PWM1/PWM2/PWM3/PWM4/PWM5 outputs
ADC13~ADC0	I	Analog to Digital Convert input pin
TK7~TK0	I	Touch Key Module 0 input
TK15~TK8	I	Touch Key Module 1 input
TM23~TK16	I	Touch Key Module 2 input
TM0CKI	I	Timer0’s input pin in counter mode
TCOUT	O	Fsys/2 clock output
TM1OUT	O	Timer1 overflow toggle output
I2CSCL	I	I2C Serial clock input
I2CSDA	I/O	I2C serial data pin
PSCL	I	I2C Serial clock input for program/ICE
PSDA	I/O	I2C serial data pin for program/ICE
XI, XO	-	Crystal/Resonator oscillator connection for System clock (FXT or SXT)
RX	I	UART receive pin
TX	O	UART transmit pin

Programming pins:

Normal mode (5-wire): VCC / VSS / PA0 / PA1 / PA2

ICP mode (4-wire): VCC / VSS / PA0 / PA1 -When using ICP (In-circuit Program) mode, the PCB needs to remove all components of PA0, PA1.

Pin Summary

Pin number				Pin Name	Type	GPIO				Function after reset	Alternate Function					
						Input		Output								
SOP28	SOP20	SOP16	SOP8			Weak Pull-up	Ext. Interrupt	O.D.	P.P.		PWM	ADC	Touch Key	I2C	UART	MISC
1	6	6		PB0/TM1OUT/TK0/ADC0	I/O	✓		✓	✓	PB0		✓	✓			TM1OU
2	7	7		PB1/TCOUT/TK1/ADC1	I/O	✓		✓	✓	PB1		✓	✓			TCOUT
3	8			PB2/TK2/ADC2	I/O	✓		✓	✓	PB2		✓	✓			
4	9			PB3/TK3/ADC3	I/O	✓		✓	✓	PB3		✓	✓			
5				PB4/TK4	I/O	✓		✓	✓	PB4			✓			
6				PB5/TK5	I/O	✓		✓	✓	PB5			✓			
7				PB6/TK6	I/O	✓		✓	✓	PB6			✓			
8				PB7/TK7	I/O	✓		✓	✓	PB7			✓			
9	10	8		PC0/TK8/ADC4/PSDA	I/O	✓		✓	✓	PC0		✓	✓			
10	11	9		PC1/TK9/ADC5/PSCL	I/O	✓		✓	✓	PC1		✓	✓			
11	12	10		PC2/TK10/ADC6	I/O	✓		✓	✓	PC2		✓	✓			
12	13	11		PC3/TK11/ADC7	I/O	✓		✓	✓	PC3		✓	✓			
13	14	12		PD0/TK16/ADC8	I/O	✓		✓	✓	PD0		✓	✓			
14	15	13		PD1/TK17/ADC9	I/O	✓		✓	✓	PD1		✓	✓			
15	16			PD2/TK18/ADC10	I/O	✓		✓	✓	PD2		✓	✓			
16	17			PD3/TK19/ADC11	I/O	✓		✓	✓	PD3		✓	✓			
17				PD4/TK20/ADC12	I/O	✓		✓	✓	PD4		✓	✓			
18				PD5/TK21/ADC13	I/O	✓		✓	✓	PD5		✓	✓			
19				PD6/TK22/COM1	I/O	✓		✓	✓	PD6			✓			
20				PD7/TK23/COM0	I/O	✓		✓	✓	PD7			✓			
21	1	1	7	VSS	P											
22	18	14		PA7/ TK15/PWM0P/INT2/XO	I/O	✓	✓	✓	✓	PA7	✓		✓			nRESET
23	19	15	8	PA4/TK14/PWM4/INT1/XI	I/O	✓	✓	✓	✓	PA4	✓		✓			
24	20	16	5	VCC	P											
25	2	2	1	PA3/TK13/PWM3/TX	I/O	✓		✓	✓	PA3	✓		✓		✓	
26	3	3	2	PA1/PWM1/COM3/I2CSCL/PSCL	I/O	✓		✓	✓	PA1	✓			✓		
27	4	4	3	PA0/PWM0N/INT0/COM2/I2CSDA/PSDA	I/O	✓	✓	✓	✓	PA0	✓			✓		
28	5	5	4	PA2/TK12/TM0CKI/PWM2/RX	I/O	✓		✓	✓	PA2	✓		✓		✓	TM0CKI

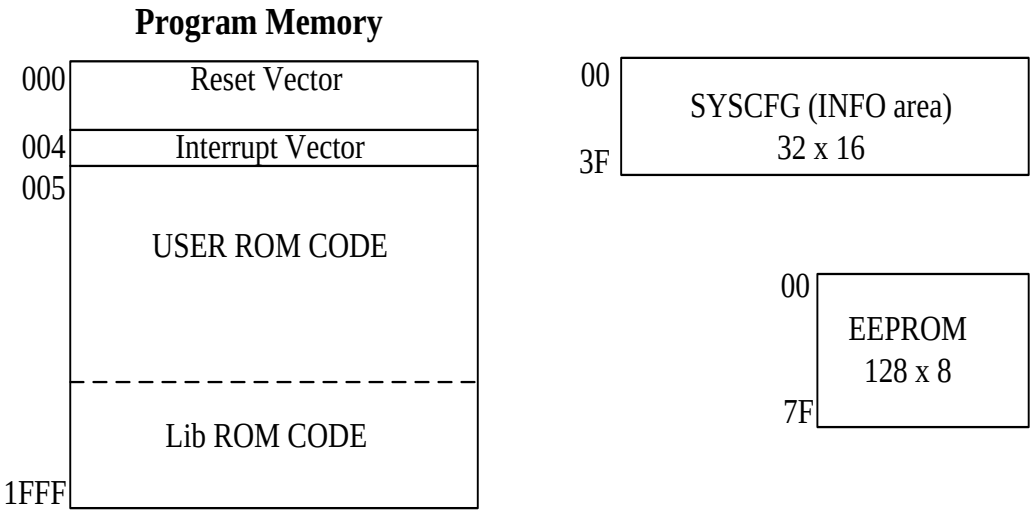
Symbol：O.D. = Open Drain
P.P. = Push-Pull Output

FUNCTION DESCRIPTION

1. CPU Core

1.1 Program ROM (PROM)

The 8Kx16 bits Flash Program ROM of this device is 8K words, with an extra 32-Word INFO area to store the SYSCFG and another extra 128-Byte EEPROM. The ROM can be written multi-times and can be read as long as the PROTECT and LPROT bits of SYSCFG are not set. The SYSCFG can be read no matter PROTECT or LPROT is set or cleared, but PROTECT bit can be cleared only when User ROM Code area is erased, and LPROT bit can be cleared only when the Lib ROM Code area is erased. That is, unprotect the PROTECT or LPROT bit needs to erase the corresponding ROM area. If LPROT bit is set, the ROM can still be written multi-times in the User ROM Code area to update user ROM code again by writer, but the Lib ROM Code area will not be read or written again by writer until the LPROT bit is cleared. On the other hand, if PROTECT bit is set, the user ROM code area will not be read by writer, and the user ROM code can't be updated until the PROTECT bit is cleared.



1.1.1 Reset Vector (000H)

After reset, system will restart the program counter (PC) at the address 000h, all registers will revert to the default value.

1.1.2 Interrupt Vector (004H)

When an interrupt occurs, the program counter (PC) will be pushed onto the stack and jumps to address 004H.

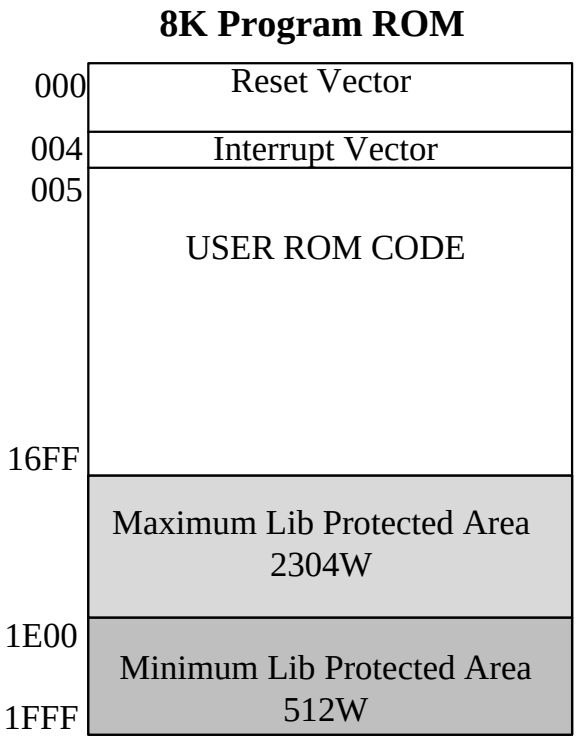
1.2 System Configuration Register (SYSCFG)

The System Configuration Register (SYSCFG) is located at Flash INFO area; it contains two 16bits registers (CFGWL/CFGWH). The SYSCFG determines the option for initial condition of CPU. It is written by PROM Writer only. User can select LVR operation Mode and chip operation mode by SYSCFG register. The 15th bit of CFGWH is code protect selection bit. If this bit is 1, the data in PROM will be protected, when user reads PROM.

Bit		**15~0**	
Default Value		**0000000000000000**	
Bit		**Description**	
CFGWL (INFO area Address 00)	15~14	Reserved	
	13	**LPROT**: Lib Code protection selection	
		1	Enable
		0	Disable
	12~9	**LSIZE**: Lib Size selection	
		1111	2304W
		……	……
		0001	512W
		0000	No use Page locker function
	8~0	Reserved	
CFGWH (INFO area Address 01)	15	**PROTECT**: Code protection selection	
		1	Enable
		0	Disable
	14	**XRSTE**: External Pin (PA7) Reset Enable	
		1	Enable
		0	Disable
	13~10	**LVR**: Low Voltage Reset Mode	
		1111	LV Reset 4.15V
		1110	LV Reset 4.01V
		….	….
		0001	LV Reset 2.19V
		0000	LV Reset 2.05V
	9~8	**WDTE**: WDT Reset Enable	
		11	Always Enable
		10	Enable in FAST/SLOW mode, Disable in IDLE/STOP mode
		0X	Disable
	7~0	Reserved	

1.3 Page Lock Function

TM56F1543 support Page locker function. By setting LPROT (CFGWL.13), user can choose whether to turn it on. If the user A (library code provider) turns this function on, the user A (library code provider) can select different size (512~2304W) of lib protected area by LSZIE (CFGWL 12~9). In lib protected area, the user B (firmware developer) can't read ROM code by TABRL/TABRH instruction or in any other way. By using the TICE99IDE tool, the user A can provide a protected lib for the user B to use, but the user B does not know its details, and the user B still can continue to complete the main code in the unprotected area.



LSIZE	Lib Protected Area
2304	(1700H~1FFFH)
2176	(1780H~1FFFH)
2048	(1800H~1FFFH)
1920	(1880H~1FFFH)
1792	(1900H~1FFFH)
1664	(1980H~1FFFH)
1536	(1A00H~1FFFH)
1408	(1A80H~1FFFH)
1280	(1B00H~1FFFH)
1152	(1B80H~1FFFH)
1024	(1C00H~1FFFH)
896	(1C80H~1FFFH)
768	(1D00H~1FFFH)
640	(1D80H~1FFFH)
512	(1E00H~1FFFH)

1.4 EEPROM

The TM56F1543 contains 128 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. According the physical characteristic the EEPROM need more long access time than Program ROM. The EEPROM has an endurance of at least 10K write/erase cycle.

The EEPROM Read usage is same as use Table Read instruction except EEPROM enable bit must be set to high and DPH is always set to zero. By writing 0xE2 to register EEPEN (192h) can set the EEPROM enable bit, writing other value to EEPEN (192h) will clear the EEPROM enable bit.

◇Example: read EEPROM data @address 23h

```
MOVLW     E2h       ;
MOVWX     EEPEN     ; set EEPROM enable bit
CLRX      DPH       ; set DPH=0 for EEPROM write/read
MOVLW     00h
MOVWX     DPH
MOVLW     23h
MOVWX     DPL       ; set DPTR=0023h
; read EEPROM @Address 23h data into W by using opcode TABRL
TABRL
….
; another way to read EEPROM data into W
MOVLW     01h       ;
MOVWX     TABR      ; TABR=01h=opcode TABRL
MOVXW     TABR      ; Read EEPROM data to W
…
```

The EEPROM Write usage is similar to read EEPROM except stop the Interrupt service. When F/W writes data to the register EEPDT (193h), the data will also be written to EEPROM. When the supply power (VCC) is bellow 3V, F/W must set **CPUPSC**=2 to lower the system clock to avoid the EEP write error. Besides, F/W must clear WDT before EEPROM write if WDT is enabled.

◇Example: write EEPROM data A5h to address 23h

```
CLRX      INTIE     ; disable INTIE
CLRX      INTIE1    ; disable INTIE1
CLRWDT
MOVLW     E2h       ;
MOVWX     EEPEN     ; set EEPROM enable bit
CLRX      DPH       ; set DPH=0 for EEPROM write/read
MOVLW     23h
MOVWX     DPL       ; set DPTR=0023h(set EEPROM Address)
MOVLW     00000010b
MOVWX     EEPCTL    ; set EEPROM write with 10mS time out
MOVLW     A5h
MOVWX     EEPDT     ; write data A5h EEPDT (193h)
                    ; the data also save to EEPROM @Address 23h
BTXSC     EEPTO     ; check EEPROM write time-out flag
LGOTO     TIMEOUT
MOVXW     CLKCTL
ANDLW     FCh
IORLW     02h       ; If VCC is lower than 3V, F/W must set CPUPSC=2
MOVXW     CLKCTL    ; Fsys=FIRC/2 before write EEPROM
MOVLW     35h       ; write next EEPROM address 0x35
MOVWX     DPL       ; set DPTR=0035h
LCALL     WAIT100us ; If VCC is dropping and near LVR, it's necessary to wait
                    ; 100us before continue to write next EEPROM address
```

```
MOVLW     A5h
MOVWX     EEPDT     ; write data A5h EEPDT (193h)
                    ; the data also save to EEPROM @Address 35h
…..
CLRX      EEPEN     ; protect EEPROM from abnormal write
```

191h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPCTL	EEPTO	–	–	–	–	–	EEPTE	
R/W	R	–	–	–	–	–	R/W	R/W
Reset	0	–	–	–	–	–	0	0

191h.7 **EEPTO:** EEPROM Write Time-Out flag
191h.1~0 **EEPTE:** Write Time-Out enable (Busy wait time)
00:Disable 01: 2.5ms 10:10ms 11:20ms

192h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPEN	EEPEN							
R/W	W							
Reset	0							

192h.7~0 **EEPEN:** EEPROM Access Enable
write 0xE2 to this register will enable EEPROM access
write others value to this register will disable EEPROM access

193h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPDT	EEPDT							
R/W	W							
Reset	0							

193h.7~0 **EEPDT:** EEPROM Data to write
write data to this register will let H/W write the data to EEPROM when EEPROM access is enable

107h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRPD	LVRPD						PORPDF	LVRPDF
R/W	W						R/W	R/W
Reset	0							

107.7~0 **LVRPD:** LVR/POR power down register
Write 0x37 to force LVR+POR be disabled (when read PORPDF=LVRPDF=1).
Write 0x38 to force LVR be disabled, POR still enable (when read PORPDF=0, LVRPDF=1).
Write 0x39 to force POR be disabled, LVR still enable (when read PORPDF=1, LVRPDF=0)
Write other value to enable LVR+POR (when read PORPDF=LVRPDF=0)

18Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TABR	TABR							
R/W	R/W							
Reset	0							

18C.7~0
1. TABR write 01h = opcode TABRL
2. TABR write 02h = opcode TABRH
3. After setp1 or step2, read TABR to get main ROM table read value
   After step1, read TABR to get EEPROM value (When EEPEN=E2h)

Table Read for ASM: instruction TABRL/TABRH or register TABR
Table Read for C : using register TABR ***and it is forbidden to use in interrupt***

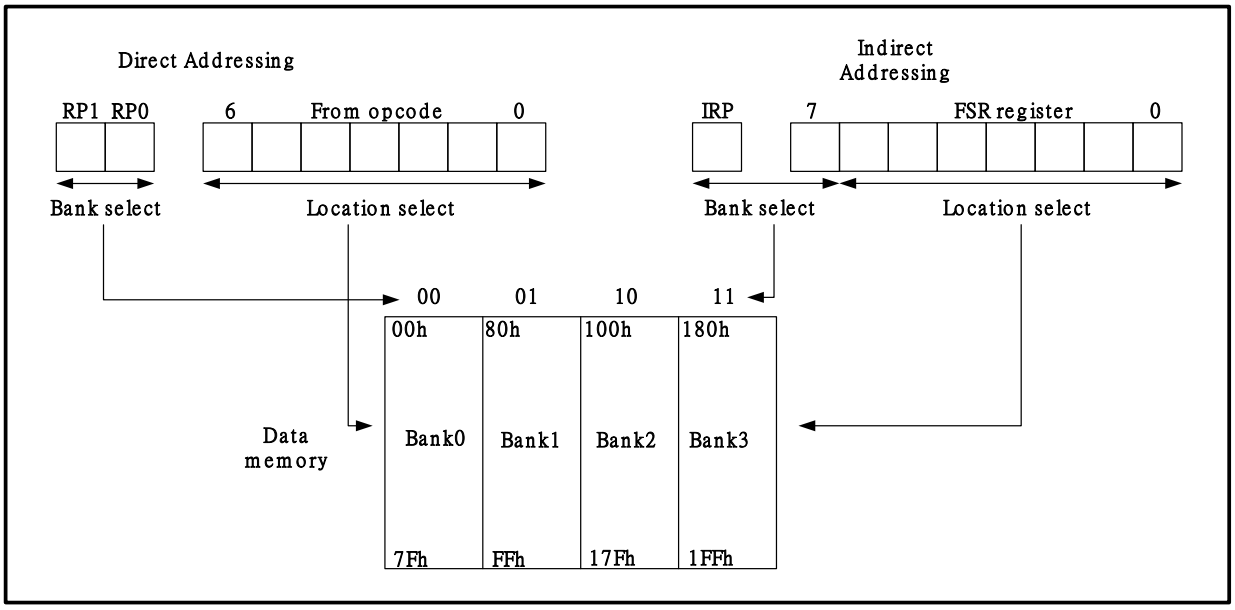
1.5 RAM Addressing Mode

The TM56F1543 has a 336-Byte Data Memory space and an additional 160-Byte Data Memory in CPU. The 336-Byte memory is partitioned into four banks memory plane. Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for Special Function Register (SFR). Above the SFR are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

Bit RP1 and RP0 (STATUS[6:5]) are the bank select bit for BANK 0/1/2/3

RP1 : RP0	BANK
00	0
01	1
10	2
11	3

The 336-Byte memory plane can be addressed directly or indirectly for BANK 0/1/2/3. The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing. Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself, indirectly (FSR = '0') will read 00h. Writing to the NDF register indirectly results in a no operation (although status bit may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>). Refer to the figure below.



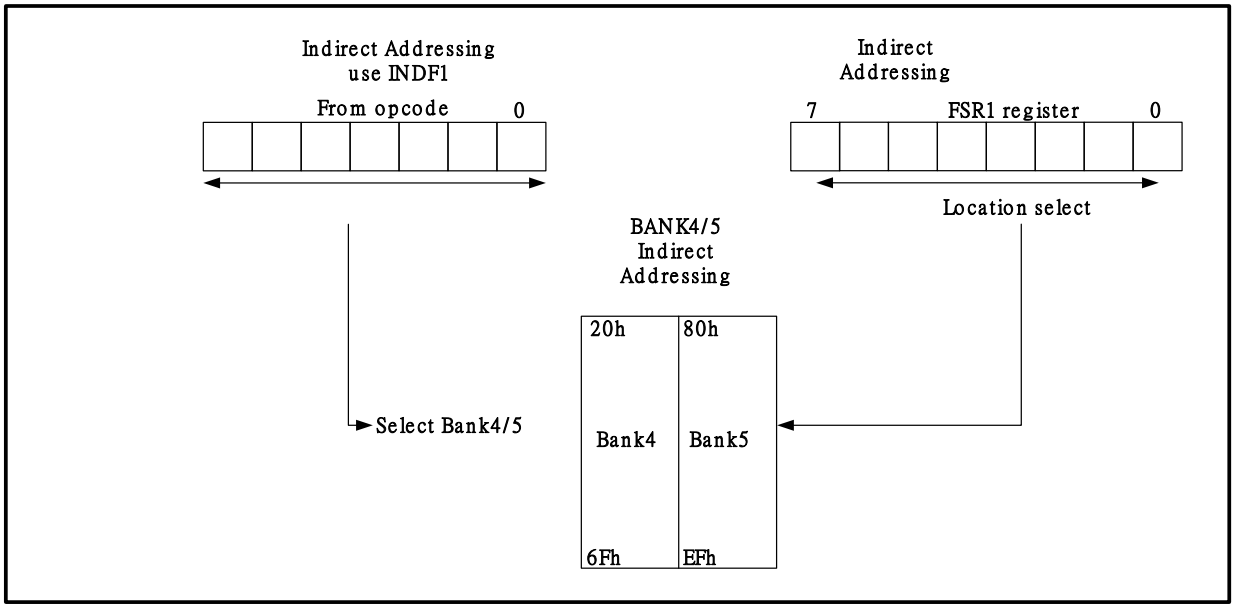
Direct / Indirect Addressing for BANK 0/1/2/3

Keeping RP0=RP1=0 in the beginning of the F/W code and using the new instruction set. The advantage of using new instruction is user can ignore the bank location of registers and the code size can be saved. The new instruction is almost same as the old instruction. By replacing the "F" to "X" in the instruction set can easily use the new instruction without switching the bank.

For example:

BC**F**	TM0IE	➔	BC**X**	TM0IE
DEC**F**	CNT, 1	➔	DEC**X**	CNT,1
INC**F**SZ	RAM25, 0	➔	INC**X**SZ	RAM25, 0
MOVW**F**	PAMODL	➔	MOVW**X**	PAMODL
RL**F**	RAMA0, 0	➔	RL**X**	RAMA0, 0
SWAP**F**	ADCTL, 0	➔	SWAP**X**	ADCTL, 0

There is an additional 160-Byte memory plane (BANK 4/5) which can only be accessed by using indirect addressing (using INDF1 and FSR1) to access this RAM space. INDF1 is used to select BANK 4/5 and FSR1 is used as the address pointer. For BANK4 the memory address is from 20H to 6FH and for BANK5 the memory address is from 80H to EFH.



Indirect Addressing for BANK 4/5

	BANK0 00~7Fh		BANK1 80h~FFh		BANK2 100h~17Fh		BANK3 180h~1FFh		BANK4 20~6Fh		BANK5 A0~EFh
00h	INDF0	80h	INDF0	100h	INDF0	180h	INDF0				
01h	TM0	81h	OPTION	101h	TM0	181h	OPTION				
02h	PCL	82h	PCL	102h	PCL	182h	PCL				
03h	STATUS	83h	STATUS	103h	STATUS	183h	STATUS				
04h	FSR	84h	FSR	104h	FSR	184h	FSR				
05h	PAD	85h	PAMODH	105h	TSTREG	185h	DPL				
06h	PBD	86h	PAMODL	106h	ChgRdMode	186h	DPH				
07h	PCD	87h	PBMODH	107h	LVRPD	187h	UARTCTL				
08h	PDD	88h	PBMODL	108h	LOE	188h	UARTSTA				
09h	INDF1	89h	INDF1	109h	INDF1	189h	INDF1				
0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH				
0Bh	INTIE	8Bh	INTIE	10Bh	INTIE	18Bh	INTIE				
0Ch	INTIF	8Ch	PCMODL	10Ch	PCH	18Ch	TABR				
0Dh	FSR1	8Dh	PDMODH	10Dh	UBAUD	18Dh	URDATA				
0Eh	INTIE1	8Eh	PDMODL	10Eh	BGTRIM	18Eh	CRCDL				
0Fh	CLKCTL	8Fh	OPTION2	10Fh	IRCF	18Fh	CRCDH				
10h	TM0RLD	90h	PWMOE	110h	I2CTXD0	190H	CRCIN				
11h	TM0CTL	91h	PWMCTL	111h	I2CTXD1	191h	EEPCTL				
12h	TM1	92h	PWMPRDH	112h	I2CCTL	192h	EEPEN				
13h	TM1RLD	93h	PWMPRDL	113h	I2CFLG	193h	EEPDT				
14h	TM1CTL	94h	PWM0DH	114h	I2CRCD0	194h	TKM0TMRL				
15h	T2CTL	95h	PWM0DL	115h	I2CRCD1	195h	TKM0TMRH				
16h	LVCTL	96h	PWM1DH	116h	TKM0DL	196h	TKM1TMRL				
17h	ADCDH	97h	PWM1DL	117h	TKM0DH	197h	TKM1TMRH				
18h	ADCTL	98h	PWM2DH	118h	TKM1DL	198h	TKM2TMRL				
19h	ADCTL2	99h	PWM2DL	119h	TKM1DH	199h	TKM2TMRH				
1Ah	INTIF1	9Ah	PWM3DH	11Ah	TKM2DL	19Ah	TKM0REFC				
1Bh	IOCCTL	9Bh	PWM3DL	11Bh	TKM2DH	19Bh	TKM1REFC				
1Ch	PAWKE	9Ch	PWM4DH	11Ch	TKMCON0	19Ch	TKM2REFC				
1Dh	PBWKE	9Dh	PWM4DL	11Dh	TKMCON1	19Dh	TKMCHS0				
1Eh	PCWKE	9Eh	PWM5DH	11Eh	TKMCTL0	19Eh	TKMCHS1				
1Fh	PDWKE	9Fh	PWM5DL	11Fh	TKMCTL1	19Fh	CTRLRFK				
20h ~ 6Fh	General Purpose SRAM 80 Bytes	A0h ~ EFh	General Purpose SRAM 80 Bytes	120h ~ 16Fh	General Purpose SRAM 80 Bytes	1A0h ~ 1EFh	General Purpose SRAM 80 Bytes	20h ~ 6Fh	Indirect Addressing SRAM 80 Bytes BANK4	A0h ~ EFh	Indirect Addressing SRAM 80 Byte BANK5
70h ~ 7Fh	Common Area 16 Bytes	F0h ~ FFh	accesses 70h~7Fh	170h ~ 17Fh	accesses 70h~7Fh	1F0h ~ 1FFh	accesses 70h~7Fh	70h ~ 7Fh	accesses 70h~7Fh	F0h ~ FFh	accesses 70h~7Fh

◇Example: read/write register by using direct addressing (RP0=RP1=0) for BANK 0/1/2/3

```
TM1             equ     12h     ;SFR in Bank0
PWM1DH          equ     96h     ;SFR in Bank1
I2CTXD0         equ     110h    ;SFR in Bank2
TKM0TMRL        equ     194h    ;SFR in Bank3
RAM20           equ     20h     ;RAM in Bank0
RAMA0           equ     A0h     ;RAM in Bank1
RAM120          equ     120h    ;RAM in Bank2
RAM1A0          equ     1A0h    ;RAM in Bank3

MOVXW   TM1             ; read TM1 (Bank0) to W
MOVXW   PWM1DH          ; read PWM1PRD (Bank1) to W
MOVXW   I2CTXD0         ; read I2CTXD0 (Bank2) to W
MOVXW   TKM0TMRL        ; read TKM0TMRL (Bank4) to W

MOVLW   16h
MOVWX   RAM20           ; W=16h write to RAM[0x20]
MOVWX   RAMA0           ; W=16h write to RAM[0xA0]
MOVWX   RAM120          ; W=16h write to RAM[0x120]
MOVWX   RAM1A0          ; W=16h write to RAM[0x1A0]
.
MOVLW   037H            ; W=37H
MOVWX    LVRPD          ; LVRPD  = W = 037H , force LVR+POR disable
```

◇Example: read/write register by using indirect addressing (RP0=RP1=0, IRP=1) for BANK 0/1/2/3

```
BSX     IRP             ; IRP=1  =>Bank2/3
MOVLW   10h             ; W=10H
MOVWX   FSR             ; FSR = W =10H
MOVXW   INDF            ; read SFR I2CTXD0 (110h) to W
.
BSX     IRP             ; IRP=1 =>Bank2/3
MOVLW   10H             ; W=10H
MOVWX   FSR             ; FSR = W =10H
MOVLW   37H             ; W=37H
MOVWX    INDF           ; I2CTXD0 (110H) = W = 037H
```

◇Example: read/write register by using indirect addressing (RP0=RP1=0, IRP=0) for BANK 0/1/2/3

```
BCX     IRP             ; IRP=0  =>Bank0/1
MOVLW   10h             ; W=10H
MOVWX   FSR             ; FSR = W =10H
MOVXW   INDF            ; read SFR TM0RLD (10h) to W
.
BCX     IRP             ; IRP=0 =>Bank0/1
MOVLW   10H             ; W=10H
MOVWX   FSR             ; FSR = W =10H
MOVLW   37H             ; W=37H
MOVWX    INDF           ; TM0RLD (10H) = W = 037H
```

◇Example: read/write register by using indirect addressing for BANK 4/5

```
; Write data to BANK4 memory
MOVLW   20h             ; W=20H
MOVWX   FSR1            ; FSR1 = W =20H
```

```
MOVLW   5Ah             ; W=5AH
MOVWX   INDF1           ; write data 5AH to BANK4 memory   @20h

; Write data to BANK5memory
MOVLW   A7h             ; W=A0H
MOVWX   FSR1            ; FSR1 = W =A7H
MOVLW   69h             ; W=69H
MOVWX   INDF1           ; write data 69H to BANK5 memory   @A7h

; Read data from BANK4 memory
MOVLW   20h             ; W=20H
MOVWX   FSR1            ; FSR1 = W =20H
MOVXW   INDF1           ; read memory BANK4 data @20h to W

; Read data from BANK5 memory
MOVLW   A0h             ; W=A0H
MOVWX   FSR1            ; FSR1 = W =A0H
MOVXW   INDF1           ; read memory BANK5 data @A0h to W
```

0h/80h/100h/180h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF	INDF							
R/W	R/W							
Reset	0							

INDF : addressing INDF actually point to the register whose address is contained in the FSR register

04h/84h/104h/184h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSR	FSR							
R/W	R/W							
Reset	0							

FSR : **File Select Register**, indirect address mode pointer

09h/89h/109h/189h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF1	INDF1							
R/W	R/W							
Reset	0							

INDF1 : addressing INDF1 actually point to the register whose address is contained in the FSR1 register
Used for BANK4/BANK5 memory only

0Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSR1	FSR1							
R/W	R/W							
Reset	0							

FSR1 : **File Select Register1**, indirect address mode pointer
Used for BANK4/BANK5 memory only

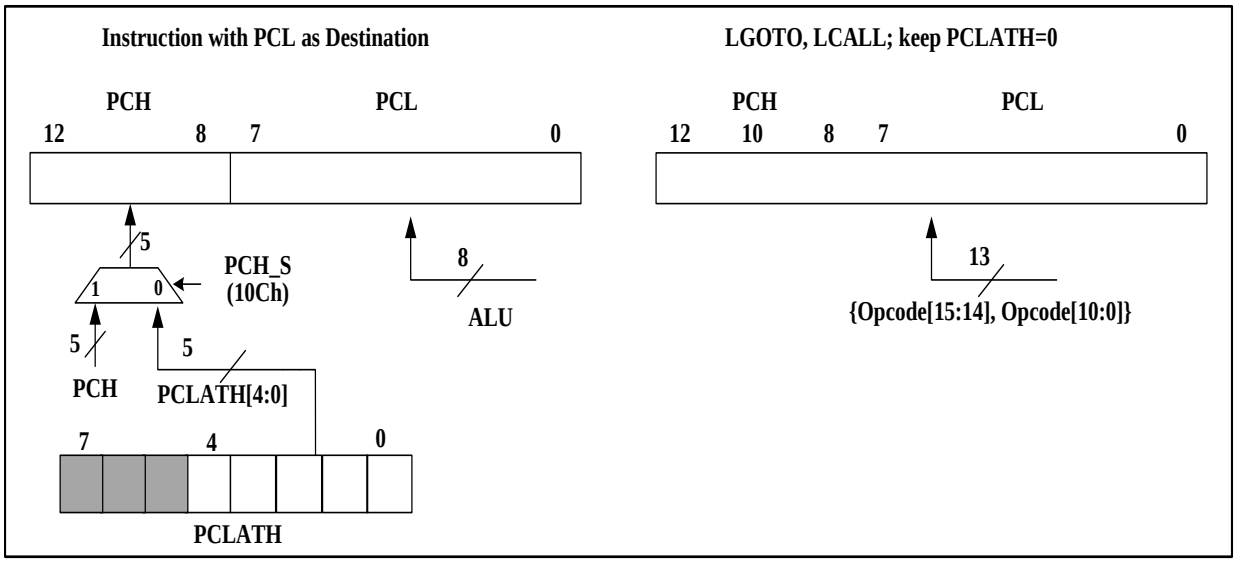
1.6 Programming Counter (PC) and Stack

The Programming Counter is 13-bit wide capable of addressing an 8K x 16 Flash ROM. The low byte comes from PCL register, which is readable and writable register. The upper bits (PC[12:8]) are not readable, but are indirectly writable through the PCLATH register or keeps unchanged when PCH_S is setting to "1"(by writing 1Ch to PCH_S register). On any RESET, the upper bits of the PC will be cleared. As a program instruction is executed, the PC will contain the address of the next program instruction to be executed. The PC value is normally increased by one except the followings. The Reset Vector (000h) and the Interrupt Vector (004h) are provided for PC initialization and Interrupt. For LCALL/LGOTO instruction, PC loads 13 bit address from instruction word. For RET/RETI/RETLW instruction, PC retrieves its content from the top level STACK.

When PCH_S is cleared to '0' (by writing 0h to PCH_S register), executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC[12:8] bits (PCH) to be replaced by the contents of the PCLATH register . This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

When PCH_S is setting to '1', executing any instruction with the PCL register as the destination the lower 8 bits are written to the PCL register and will not change the Program Counter PC[12:8] bits (PCH).

For assembly code, **Setting PCH_S to "1" in the beginning of the F/W code and using new instruction LGOTO/LCALL (Hi-tech C doesn't support the coding).** The advantage of using new instruction is user can ignore setting PCLATH register, system will auto-read INST [15:14] directly from 8K ROM. The new instruction can easily use the new instruction without setting PCLATH



10Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCH_S	PCH_S							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

10Ch PCH_S**:** Program Counter Upper bits selection when instruction with PCL as destination is executed
write 0x1C to set PCH_S= 1: PCH keep the original value
write others to clear PCH_S=0: PCH is from PCLATH[4:0]

81h/181h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	HWAUTO	INT0EDG	INT1EGE	-	WDTPSC		WKTPSC	
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset	0	0	0	-	1	1	1	1

81h.7 HWAUTO**:** Enter interrupt vector, HW auto save/restore WREG and STATUS w/o TO, PD (only work for ASM, not for C)
0: disable
1: enable; (only work for ASM not for C)

The STACK is 13-bit wide and 8-level in-depth. The LCALL instruction and hardware interrupt will push STACK level in order. While the RET/RETI/RETLW instruction pops STACK level in order.

For table lookup, the device offer the powerful table read instructions TABRL, TABRH to return the 16-bit ROM data into W register by setting DPTR={DPH, DPL} registers. It also offers another way to read the 16-bit ROM data into W register by setting TABR (18Ch) for C language.

◇ Example: To look up the PROM data located “TABLE1” and “TABLE2”.

```
        ORG         00h             ; Reset Vector
        LGOTO       START
        ORG         04h             ; Interrupt Entry Address
        MOVWX       W_TMP           ; if HWAUTO =1, can omit this line
        MOVXW       STATUS          ; if HWAUTO =1, can omit this line
        MOVWX       STATUS_TMP      ; if HWAUTO =1, can omit this line
        MOVXW       PCLATH
        MOVWX       PCLATH_TMP

        BTXSC       TM0IF
        LCALL       TM0INT_TASK
        …….
        MOVXW       PCLATH_TMP
        MOVWX       PCLATH
        MOVXW       STATUS_TMP      ; if HWAUTO =1, can omit this line
        MOVWX       STATUS          ; if HWAUTO =1, can omit this line
        SWAPX       W_TMP, f        ; if HWAUTO =1, can omit this line
        SWAPX       W_TMP           ; if HWAUTO =1, can omit this line
        MOVXW       W_TMP           ; if HWAUTO =1, can omit this line
        RETI

START:
        MOVLW       00h
        MOVWX       INDEX           ; Set lookup table’s address
        MOVLW       1Ch
        MOVWX       PCH_S
        MOVLW       00h
        MOVWX       RAM20           ; RAM20 as PCL counter
LOOP:
        MOVXW       RAM20
        LCALL       TABLE1          ; To lookup data, W=55h
        ……
        INCX        RAM20, 1
        ……
        LGOTO       LOOP            ; Go to LOOP label
```

```
        ……
        MOVLW       (TABLE2>>8) & 0xff
        MOVWX       DPH             ; DPH register (F186.4~0)
        MOVLW       (TABLE2) & 0xff
        MOVWX       DPL             ; DPL register (F185.7~0)
; Table Read by opcode TABRL / TABRH
        TABRL                       ; read PROM low byte data to W (W=86h)
        TABRH                       ; read PROM high byte data to W (W=19h)
        ……
; Table Read by SFR TABR
        MOVLW       01h             ; TABR=01h=opcode TABRL
        MOVWX       TABR
        MOVXW       TABR            ; read PROM low byte data to W (W=86h)

        MOVLW       02h             ; TABR=02h=opcode TABRH
        MOVWX       TABR
        MOVXW       TABR            ; read PROM high byte data to W (W=19h)

        ORG         F68h
TABLE1:
        ADDWX       PCL, 1          ; Add the W with PCL, the result back in PCL
        RETLW       55h             ; W=55h when return
        RETLW       56h             ; W=56h when return
        RETLW       57h             ; W=57h when return
        RETLW       58h             ; W=58h when return

        ……
        ORG         368h
TABLE2:
        .DT 0x1986, 0x3719, 0x2983  ; 16-bit ROM data
        ….
        ORG         100h
TM0INT_TASK:
        MOVLW       11101111B
        MOVWX       INTIF
        …….
        RET
```

1.7 ALU and Working (W) Register

The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. In two-operand instructions, typically one operand is the W register, which is an 8-bit non-addressable register used for ALU operations. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either W register or a file register. Depending on the instruction executed, the ALU may affect the values of Carry (C), Digit Carry (DC), and Zero (Z) Flags in the STATUS register. The C and DC flags operate as a /Borrow and /Digit Borrow, respectively, in subtraction.

Note: /Borrow represents inverted of Borrow register.
/Digit Borrow represents inverted of Digit Borrow register

1.8 STATUS Register (03H/83H/103H/183H)

This register contains the arithmetic status of ALU and the Reset status. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. It is recommended, therefore, that only BCX, BSX and MOVWX instructions are used to alter the STATUS Register because these instructions do not affect those bits.

STATUS	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Bit	Description							
7	**IRP**: Register Bank Select bit (used for indirect addressing) 0 = Bank 0,1 (00h - FFh) 1 = Bank 2,3 (100h - 1FFh)							
6:5	**RP1:RP0**: Register Bank Select bits (used for direct addressing) 00 = Bank 0 (00h - 7Fh) 01 = Bank 1 (80h - FFh) 10 = Bank 2 (100h - 17Fh) 11 = Bank 3 (180h - 1FFh) Each bank is 128 bytes							
4	**TO**: Time Out Flag 0: after Power On Reset, LVR Reset or CLRWDT/SLEEP instruction 1: WDT time out occurs							
3	**PD**: Power Down Flag 0: after Power On Reset, LVR Reset or CLRWDT instruction 1: after SLEEP instruction							
2	**Z**: Zero Flag 0: the result of a logic operation is not zero 1: the result of a logic operation is zero							
1	**DC**: Decimal Carry Flag or Decimal / Borrow Flag							
	ADD instruction				SUB instruction			
	0: no carry 1: a carry from the low nibble bits of the result occurs				0: a borrow from the low nibble bits of the result occurs 1: no borrow			
0	**C**: Carry Flag or /Borrow Flag							
	ADD instruction				SUB instruction			
	0: no carry 1: a carry occurs from the MSB				0: a borrow occurs from the MSB 1: no borrow			

◇ Example: Write immediate data into STATUS register.

```
MOVLW   00h
MOVWX   STATUS      ; Clear STATUS register
```

◇ Example: Bit addressing set and clear STATUS register.

```
BSX     STATUS, 0   ; Set C=1.
BCX     STATUS, 0   ; Clear C=0.
```

◇ Example: Determine the C flag by BTXSS instruction.

```
BTXSS   STATUS, 0   ; Check the carry flag
LGOTO   LABEL_1     ; If C=0, goto label_1
LGOTO   LABEL_2     ; If C=1, goto label_2
```

2. Reset

This device can be RESET in four ways.

- Power-On-Reset (POR)
- Low Voltage Reset (LVR)
- External Pin Reset (PA7)
- Watchdog Reset (WDT)

Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Watchdog Timer Reset (WDTR) , or Low Voltage Reset (LVR) . The CFGWH controls the Reset functionality. After Reset, the SFRs are returned to their default value, the program counter (PC) is cleared, and the system starts running from the reset vector 000H place. The TO and PD flags at status register (STATUS) are indicate system reset status.

2.1 Power on Reset

After Power-On-Reset, all system and peripheral control registers are then set to their default hardware Reset values. The clock source, LVR level and chip operation mode are selected by the SYSCFG register value.

2.2 Low Voltage Reset

The chip provides Low Voltage Reset (LVR) and Low Voltage Detection (LVD) functions. There are 16-level LVR can be selected by CFGWH and 16-level LVD can be selected by SFR LVDS

SYSCFG 01h	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CFGWH	PROT	XRSTE	LVRE				WDTE	

CFGWH.13~10 **LVRE:** Low Voltage Reset function select
0000: Set LVR at 2.05V
0001: Set LVR at 2.19V
0010: Set LVR at 2.33V
0011: Set LVR at 2.47V
0100: Set LVR at 2.62V
0101: Set LVR at 2.75V
0110: Set LVR at 2.89V
0111: Set LVR at 3.03V
1000: Set LVR at 3.17V
1001: Set LVR at 3.31V
1010: Set LVR at 3.45V
1011: Set LVR at 3.59V
1100: Set LVR at 3.73V
1101: Set LVR at 3.87V
1110: Set LVR at 4.01V
1111: Set LVR at 4.15V

16h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVCTL	LVDF	-	LVRSAV	LVDSAV	LVDS			
R/W	R	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	1	1	0	0	0	1

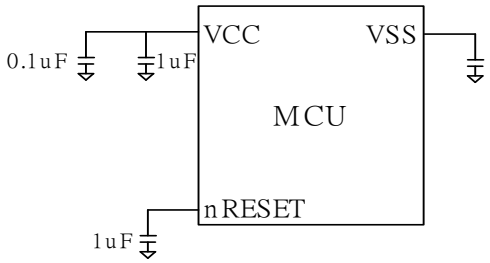
16h.7 **LVDF:** Low Voltage Detect output Flag
16h.5 **LVRSAV:** when set to 1, LVR auto power off in STOP/IDLE mode
16h.4 **LVDSAV:** when set to 1, LVD auto power off in STOP/IDLE mode
16h.3~0 **LVDS:** Low Voltage Detect select
0000: Disable LVD
0001: Set LVD at 2.19V
0010: Set LVD at 2.33V
0011: Set LVD at 2.47V
0100: Set LVD at 2.62V
0101: Set LVD at 2.75V
0110: Set LVD at 2.89V
0111: Set LVD at 3.03V
1000: Set LVD at 3.17V
1001: Set LVD at 3.31V
1010: Set LVD at 3.45V
1011: Set LVD at 3.59V
1100: Set LVD at 3.73V
1101: Set LVD at 3.87V
1110: Set LVD at 4.01V
1111: Set LVD at 4.15V

Different Fsys have different system minimum operating voltage, reference to Operating Voltage of DC characteristics, if current system voltage is low than minimum operating voltage and lower LVR is selected, then the system maybe enters dead-band and error occurs.

2.3 External Pin Reset

The External Pin Reset can be disabled or enabled by the SYSCFG register (XRSTE). It needs to keep at least 2 SIRC clock cycle long to be seen by the chip. External Pin Reset also set all the control registers to their default reset value. The TO/PD flags are not affected by these resets.

External reset pin is low level active. The system is running when reset pin is high level voltage input. The reset pin receives the low voltage and the system is reset. The external reset can reset the system during power on duration and good external reset circuit can protect the system to avoid operating at inappropriate power condition.



SYSCFG 01h	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CFGWH	PROT	XRSTE	LVRE				WDTE	

CFGWH.14 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

2.4 Watchdog Timer Reset

WDT overflow Reset can be disabled or enabled by the SYSCFG register. It runs in Fast/Slow mode and runs or stops in IDLE/STOP mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit WDT overflow Reset also set all the control registers to their default reset value. The TO/PD flags are not affected by these resets.

SYSCFG 01h	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CFGWH	PROT	XRSTE	LVRE				WDTE	

CFGWH.9~8 **WDTE:** WDT overflow flow Reset control
0x: Disable WDT Reset
10: Enable WDT Reset in Fast/Slow Mode, Disable in IDLE/STOP Mode
11: Always Enable WDT Reset

81h/181h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	HWAUTO	INT0EDG	INT1EGE	-	WDTPSC		WKTPSC	
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset	0	0	0	-	1	1	1	1

81h.3~2 **WDTPSC:** WDT period (@VCC=5V)
00: 164ms WDT overflow rate
01: 328ms WDT overflow rate
10: 655ms WDT overflow rate
11: 1311ms WDT overflow rate

◇ Example: Defining Reset Vector

```
        ORG     000H
        LGOTO   START       ; Jump to user program address.

        ORG     010H

START:
        …                   ; 010H, The head of user program
        …
        LGOTO   START
```

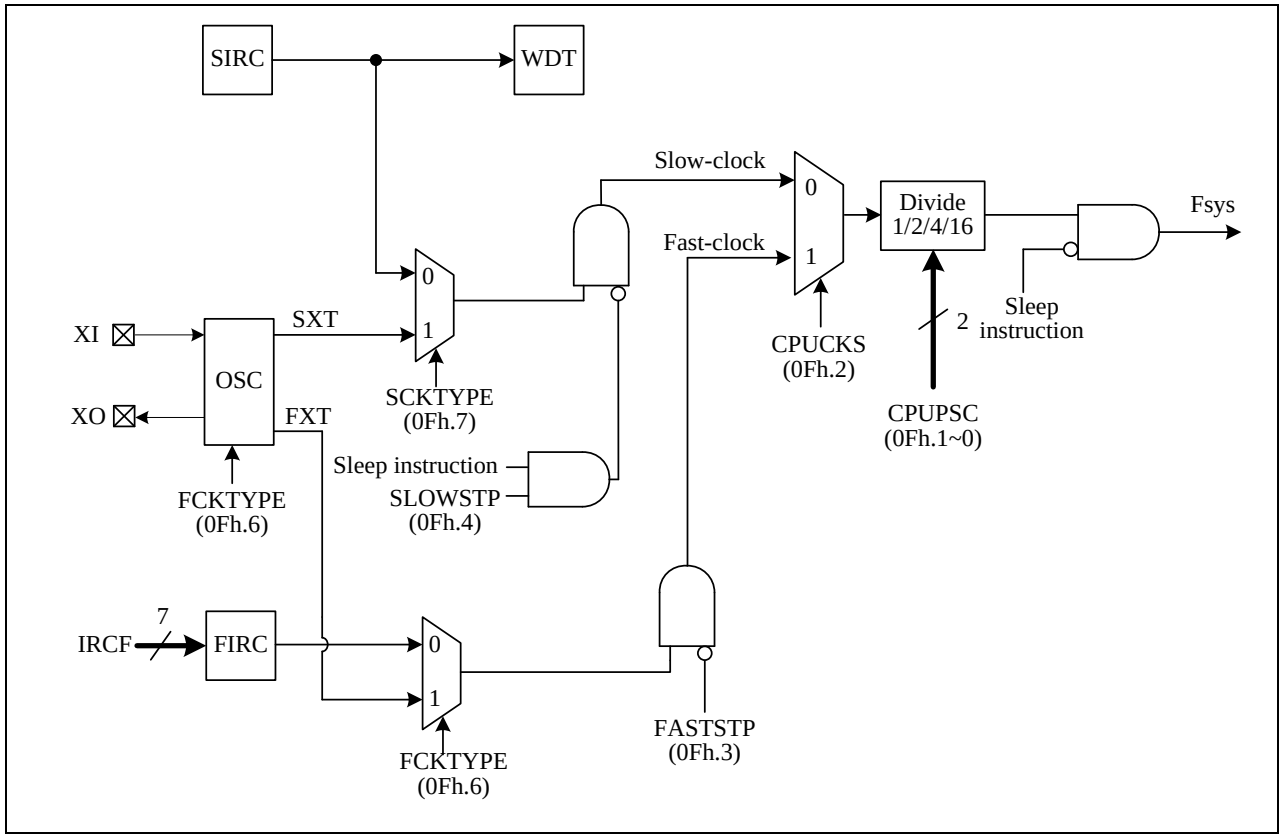
3. Clock Circuitry and Operation Mode

3.1 System Clock

The device is designed with dual-clock system. There are two kinds of clock source, i.e. Slow clock or fast clock. The Slow clock can be selected as SIRC (Slow Internal RC) or SXT (Slow Crystal, 32KHz). The Fast clock can be selected as FIRC (Fast Internal RC) or FXT (Fast Crystal 18MHz). Each clock source can be applied to CPU kernel as system clock. When in IDLE mode, only Slow-clock can be configured to keep oscillating to provide clock source to T2 block. Refer to the figure below.

After Reset, the device is running at Slow mode with 50 KHz SIRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, an 18.432 MHz System clock rate requires V_{CC} > 2.8V.

The CLKCTL SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow-clock type in Fast mode and change the Fast-clock type in Slow mode. Never to write both FASTSTP=1 & CPUCKS=1. It is recommended to write this SFR bit by bit.



Clock Scheme Block Diagram

The frequency of FIRC (Fast Internal RC) can be adjusted by IRCF and IRCF is trimmed to FIRC=18.432 MHz in chip manufacturing

0Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCTL	SCKTYPE	FCKTYPE	–	SLOWSTP	FASTSTP	CPUCKS	CPUPSC	
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	1	0	1	1

0Fh.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode(CPUCKS=1)
0: SIRC
1: SXT, PA7 and PA4 are crystal pins

0Fh.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode(CPUCKS=0)
0: FIRC
1: FXT, PA7 and PA4 are crystal pins, oscillator gain is high for FXT

0Fh.4 **SLOWSTP:** Stop Slow-clock in Stop Mode
0: no Stop
1: Stop Slow-clock

0Fh.3 **FASTSTP:** Stop Fast Clock
0: Fast Clock Running
1: Fast Clock Stop

0Fh.2 **CPUCKS:** System Clock selection
0: Slow Clock as system clock
1: Fast Clock as system clock

0Fh.1~0 **CPUPSC:** System clock Prescaler
0: div 8
1: div 4
2: div 2
3: div 1

FAST Mode:
In this mode, the program is executed using Fast-clock as CPU clock (Fsys). The Timer0 block is driven by Fast-clock or SXT/16. The Timer1 block is also driven by Fast-clock; The PWMx blocks can be driven by FIRC, FIRC*2 or Fsys. T2 can be driven by Slow-clock or Fsys/128 by setting T2CKS (15h.2).

SLOW Mode:
After power-on or reset, device enters SLOW mode, the default Slow-clock is SIRC. In this mode, the Fast-clock can stopped (by FASTSTP=1, for power saving) or running (by FASTSTP=0), and Slow-clock is enabled. All peripheral blocks (Timer0, Timer1etc...) clock sources are Slow-clock in the SLOW mode.

IDLE Mode:
If Slow-clock is enabled (SLOWSTP=0) and T2CKS=0 before executing the SLEEP instruction, the CPU enters the IDLE mode. In this mode, the Slow-clock source keeps T2 block running. CPU stop fetching code and all blocks are stop except T2 related circuits. Idle mode is terminated by Reset or enabled Interrupts (exclude TK interrupt) wake up.

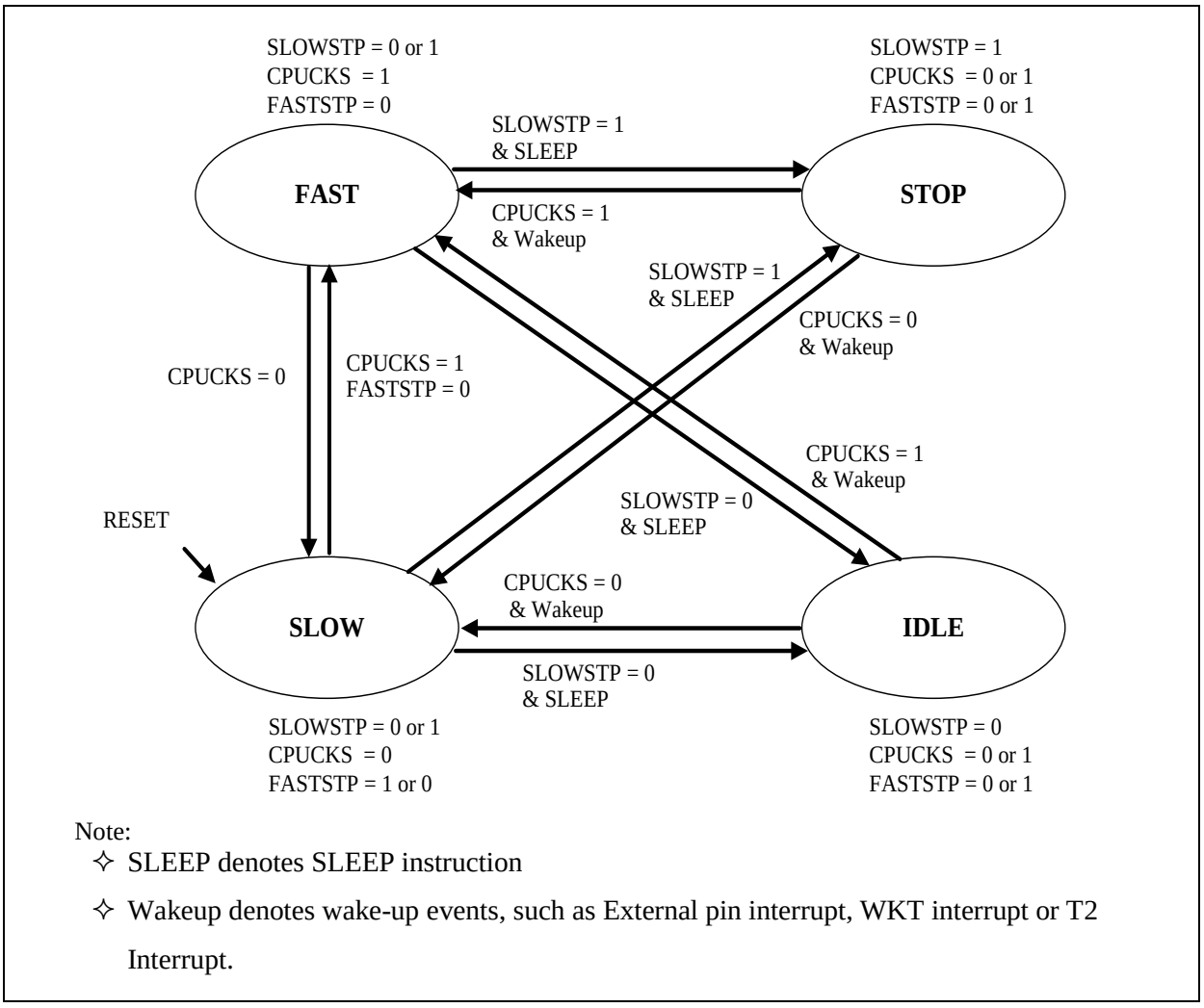
Another way to keep clock oscillation in IDLE mode is setting WKTIE=1 before executing the SLEEP instruction. In such condition, the WKT keeps working and wake up CPU periodically.

T2 and WKT/WDT are independent and have their own control registers. It is possible to keep both T2 and WKT working and wake-up in the IDLE mode.

STOP Mode:
If Slow-clock and WKT/WDT are disabled before executing the SLEEP instruction, every block is turned off and the device enters the STOP mode. STOP mode is similar to IDLE mode. The difference is all clock oscillators either Fast-clock or Slow-clock is power down and no clock is generated.

3.2 Dual System Clock Modes Transition

The device is operated in one of four modes: FAST mode, SLOW mode, IDLE mode, and STOP mode.



Note:

- ✧ SLEEP denotes SLEEP instruction
- ✧ Wakeup denotes wake-up events, such as External pin interrupt, WKT interrupt or T2 Interrupt.

CPU Operation Block Diagram

CPU Mode & Clock Functions Table:

Mode	Oscillator	Fsys	Fast-clock	Slow-clock	TM0/TM1	T2	Wakeup event
FAST	FIRC, FXT	Fast-clock	Run	Set by SLOWSTP	Run	Run	X
SLOW	SIRC, SXT	Slow-clock	Set by FASTSTP	Run	Run	Run	X
IDLE	SIRC, SXT	Stop	Stop	Run	Stop	Run	WKT/IO/T2
STOP	Stop	Stop	Stop	Stop	Stop	Stop	IO

- **FAST mode switches to SLOW mode**

The following steps are suggested to be executed by order when FAST mode switches to SLOW mode:

(1) Enable Slow-clock (SLOWSTP=0)

(2) Switch to Slow-clock (CPUCKS=0)

(3) Stop Fast-clock (FASTSTP=1)

◇ Example: Switch FAST mode to SLOW mode.

```
BCX     SLOWSTP     ; Enable Slow-clock.
NOP
BCX     CPUCKS      ; Fsys=Slow-clock.
BSX     FASTSTP     ; Disable Fast-clock.
```

- **SLOW mode switches to FAST mode**

SLOW mode can be enabled by CPUCKS=0 in CLKCTL register. The following steps are suggested to be executed by order when SLOW mode switches to FAST mode:

(1) Enable Fast-clock (FASTSTP=0)

(2) Switch to Fast-clock (CPUCKS=1)

◇ Example: Switch SLOW mode to FAST mode (The Fast-clock stop).

```
BCX     FASTSTP     ; Enable Fast-clock.
NOP
BSX     CPUCKS      ; Fsys=Fast-clock
```

- **IDLE mode Setting**

The IDLE mode can be configured by following setting in order:

(1) Enable Slow-clock (SLOWSTP=0) or WKT(WKTIE=1)

(2) Switch T2 clock source to Slow-clock (T2CKS=0)

(3) Execute SLEEP instruction

IDLE mode can be wakened up by External interrupt, WKT interrupt and T2 interrupt.

◇ Example: Switch FAST/SLOW mode to IDLE mode.

```
BCX     SLOWSTP     ; Enable Slow-clock.
MOVLW   00000000B
MOVWX   T2CTL       ; T2 Clock source=Slow-clock. T2PSC=div 32768
SLEEP               ; Enter IDLE mode.
```

STOP Mode Setting

The STOP mode can be configured by following setting in order:

(1) Stop Slow-clock (SLOWSTP=1)

(2) Stop WKT/WDT (WKTIE=0, WDTE=10 or 0X)

(3) Execute SLEEP instruction

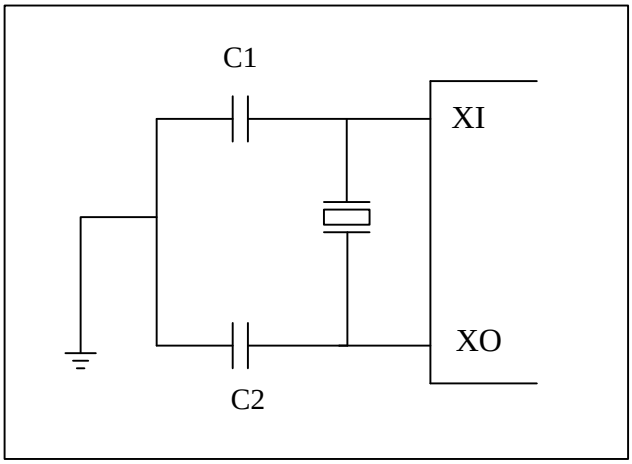
STOP mode can be wakened up only by External pin interrupt or Pin Change.

◇ Example: Switch FAST/SLOW mode to STOP mode.

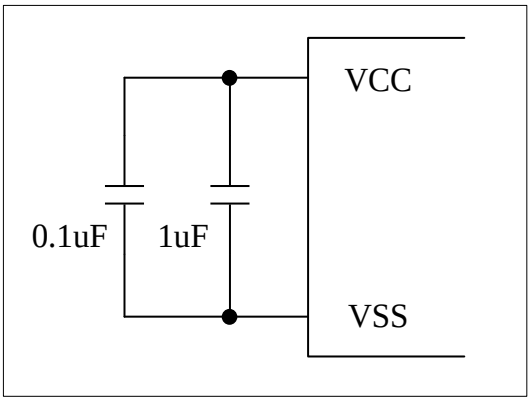
```
BSX     SLOWSTP     ; Disable Slow-clock.
MOVLW   00000000B   ; Disable WKT counting
MOVWX   INTIE
SLEEP               ; Enter STOP mode.
```

3.3 System Clock Oscillator

System clock can be operated in four different oscillation modes. Four oscillation modes are FIRC, FXT, SIRC and SXT respectively. In the Fast Internal RC (FIRC) mode, the on-chip oscillator generates 18.432 MHz system clock. In Slow/Fast Crystal (SXT/FXT) mode, a crystal or ceramic resonator is connected to XI and XO pins to establish oscillation. Since power noise degrades the performance of Internal Clock Oscillator, placing power supply bypass capacitors 1uF and 0.1uF very close to VCC/VSS pins improves the stability of clock and the overall system.



External Oscillator Circuit
(Crystal or Ceramic)



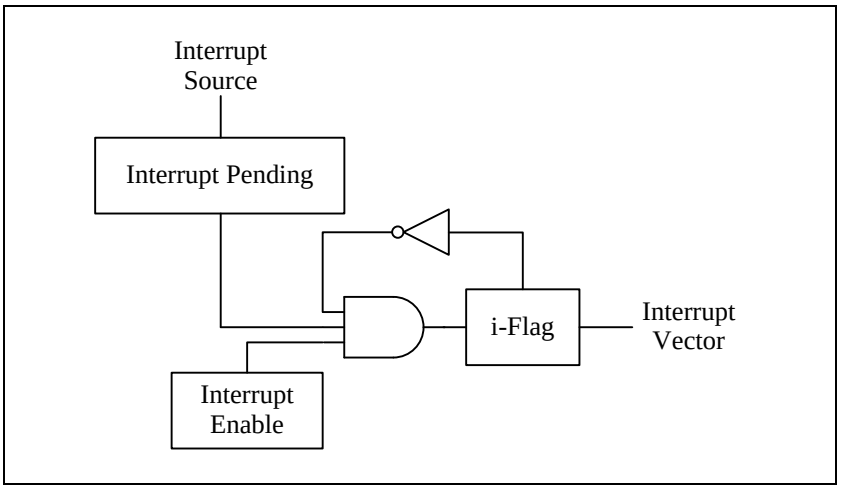
Internal RC Mode

4. Interrupt

TM56F1543 has 1 level, 1 vector and 13 interrupt sources. Each interrupt source has its own enable control bit. An interrupt event will set its individual pending flag; no matter its enable control bit is 0 or 1.

If the corresponding interrupt enable bit (INTIE[7:0] or INTIE1[7:0]) has been set, it would trigger CPU to service the interrupt. CPU accepts interrupt in the end of current executed instruction cycle. In the mean while, a "LCALL 004" instruction is inserted to CPU, and i-Flag is set to prevent recursive interrupt nesting.

The i-Flag is cleared in the instruction after the "RETI" instruction. That is, at least one instruction in main program is executed before service the pending interrupt. The interrupt event is level triggered. F/W must clear the interrupt event register while serving the interrupt routine.



◇ Example: Setup INT1 (PA4) interrupt request with rising edge trigger.

```
        ORG     00h         ; Reset Vector
        LGOTO   START       ; Goto user program address

        ORG     004h        ; All interrupt vector
        LGOTO   INT         ; If INT1 (PA4) input occurred rising edge

        ORG     100h
START:
        MOVLW   xxxxxx00B
        MOVWX   PAMODH      ; select INT1 Pin Mode as Mode0

        MOVLW   xxx1xxxxB
        MOVWX   PAD         ; Release INT1, it becomes Schmitt-trigger
                            ; input with pull-up resistor
        MOVLW   xx1xxxxxB
        MOVWX   OPTION      ; Set INT1 interrupt trigger as rising edge
        MOVLW   111111 01B
        MOVWX   INTIF       ; Clear INT1 interrupt request flag
        MOVLW   000000 10B
        MOVWX   INTIE       ; Enable INT1 interrupt
MAIN:
```

```
        ….
        LGOTO       MAIN
INT:
        MOVWX       RAM20h      ; Store W data to RAM 20h
        MOVXW       STATUS      ; Get STATUS data
        MOVWX       RAM21h      ; Store SATAUS data to RAM 21h
CHKI1:
        BTXSC       INT1IE      ;
        BTXSS       INT1IF      ;
        LGOTO       END_CHK     ; if INT1IE=0 or INT1IE=1 & INT1IF=0
        LCALL       INT1INT     ; if INT1IE=1 & INT1IF=1
        ….                      ; CALL INT1 interrupt service routine

END_CHK:
        MOVXW       RAM21h      ; Get RAM 21h data
        MOVWX       STATUS      ; Restore STATUS data
        MOVXW       RAM20h      ; Restore W data
        RETI                    ; Return from interrupt

INT1INT:
        MOVLW       11111101B
        MOVWX       INTIF       ; clear INT1IF
        …..
        RET
```

0Bh/8Bh/10Bh/18Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	ADCIE	T2IE	TM1IE	TM0IE	WKTIE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

INTIE.7 **ADCIE:** ADC interrupt enable
0: disable
1: enable

INTIE.6 **T2IE:** T2 interrupt enable
0: disable
1: enable

INTIE.5 **TM1IE:** Timer1 interrupt enable
0: disable
1: enable

INTIE.4 **TM0IE:** Timer0 interrupt enable
0: disable
1: enable

INTIE.3 **WKTIE:** Wakeup Timer interrupt enable
0: disable
1: enable

INTIE.2 **INT2IE:** INT2 (PA7) interrupt enable
0: disable
1: enable

INTIE.1 **INT1IE:** INT1 (PA4) interrupt enable
0: disable
1: enable

INTIE.0 **INT0IE:** INT0 (PA0) interrupt enable
0: disable
1: enable

0Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	ADCIF	T2IF	TM1IF	TM0IF	WKTIF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Ch.7 **ADCIF:** ADC interrupt event pending flag
This bit is set by H/W after end of ADC conversion , write 0 to this bit will clear this flag

0Ch.6 **T2IF:** T2 interrupt event pending flag
This bit is set by H/W while T2 overflows, write 0 to this bit will clear this flag

0Ch.5 **TM1IF:** Timer1 interrupt event pending flag
This bit is set by H/W while Timer1 overflows, write 0 to this bit will clear this flag

0Ch.4 **TM0IF:** Timer0 interrupt event pending flag
This bit is set by H/W while Timer0 overflows, write 0 to this bit will clear this flag

0Ch.3 **WKTIF:** Wakeup Timer interrupt event pending flag
This bit is set by H/W while Wakeup Timer is timeout, write 0 to this bit will clear this flag

0Ch.2 **INT2IF:** INT2 (PA7) pin falling interrupt pending flag
This bit is set by H/W at INT2 pin's falling edge, write 0 to this bit will clear this flag

0Ch.1 **INT1IF:** INT1 (PA4) pin falling/rising interrupt pending flag
This bit is set by H/W at INT1 pin's falling/rising edge, write 0 to this bit will clear this flag

0Ch.0 **INT0IF:** INT0 (PA0) pin falling/rising interrupt pending flag
This bit is set by H/W at INT0 pin's falling/rising edge, write 0 to this bit will clear this flag

81h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTON	HWAUTO	INT0EDG	INT1EGE	-	WDTPSC		WKTPSC	
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset	0	0	0	-	1	1	1	1

81h.6 INT0EDG**:** INT0 interrupt trigger edge
0: falling edge trigger, 1: rising edge trigger

81h.5 INT1EDG**:** INT1 interrupt trigger edge
0: falling edge trigger, 1: rising edge trigger

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE1	LVDIE				TKIE	I2CIE	UARTIE	PXIE
R/W	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

INTIE1.7 **LVDIE:** LVD interrupt enable
0: disable
1: enable

INTIE1.3 **TKIE:** Touch Key interrupt enable
0: disable
1: enable

INTIE1.2 **I2CIE:** Slave I2C interrupt enable
0: disable
1: enable

INTIE1.1 **UARTIE:** UART TX/RX complete interrupt enable
0: disable
1: enable

INTIE1.0 **PXIE:** Pin Change Wakeup interrupt enable
0: disable
1: enable

1Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF1	LVDIF	TKM2IF	TKM1IF	TKM0IF	TKIF	I2CIF	UARTIF	PXIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1Ah.7 **LVDIF:** Low Voltage Detect interrupt pending flag
This bit is set by H/W , write 0 to this bit will clear this flag

1Ah.6 **TKM2IF:** Touch Key module2 interrupt pending flag
This bit is set by H/W after end of TK2 conversion, write 0 to clear this bit or write 1 to TKM2SOC will clear this flag

1Ah.5 **TKM1IF:** Touch Key module1 interrupt pending flag
This bit is set by H/W after end of TK1 conversion, write 0 to clear this bit or write 1 to TKM1SOC will clear this flag

1Ah.4 **TKM0IF:** Touch Key module0 interrupt pending flag
This bit is set by H/W after end of TK0 conversion, write 0 to clear this bit or write 1 to TKM0SOC will clear this flag

1Ah.3 **TKIF:** Touch Key interrupt pending flag,
set by H/W while TKM0 or TKM1 or TKM2 are end of conversion, write 0 to this bit will clear all of Touch Key interrupt flag

1Ah.2 **I2CIF:** Slave I2C interrupt pending flag
This bit is set by H/W while

- ✧ I2CRCD0 or I2CRCD1 receive data finished
- ✧ I2CRCD0 or I2CRCD1 data overflow occurred
- ✧ I2CTXD0 or I2CTXD1 data transmit finished

Write 0 to this bit will clear this flag and slave I2C related flags.

1Ah.1 **UARTIF:** UART interrupt pending flag
This bit is set by H/W while TX/RX transfer is completed, write 0 to this bit will clear this flag.

1Ah.0 **PXIF:** Pin Change interrupt pending flag
This bit is set by H/W while the corresponding pin change, write 0 to this bit will clear this flag

113h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CFLG	-	-	TXD1F	TXD0F	RCD1OVF	RCD1F	RCD0OVF	RCD0F
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	0	0	0	0	0	0

113h.5 **TXD1F:** Slave I2C transmitting data register 1 flag
This bit is set by H/W while I2CTXD1 data transmitting finished, write 0 to this bit will clear this flag

113h.4 **TXD0F:** Slave I2C transmitting data register 0 flag
This bit is set by H/W while I2CTXD0 data transmitting finished, write 0 to this bit will clear this flag

113h.3 **RCD1OVF:** Slave I2C receiving data register 1 overflow
This bit is set by H/W while receiving I2CRCD1 overflow, write 0 to this bit will clear this flag

113h.2 **RCD1F:** Slave I2C receiving data register 1 flag
This bit is set by H/W while data receiving to I2CRCD1 finished, write 0 to this bit will clear this flag

113h.1 **RCD0OVF:** Slave I2C receiving data register 0 overflow
This bit is set by H/W while receiving I2CRCD0 overflow, write 0 to this bit will clear this flag

113h.0 **RCD0F:** Slave I2C receiving data register 0 flag
This bit is set by H/W while data receiving to I2CRCD0 finished, write 0 to this bit will clear this flag

5. I/O Port

5.1 PA0-4, PA7, PB0-7, PC0-3 and PD0-7

These pins can be used as Schmitt-trigger input, CMOS push-pull output. The pull-up resistor is assignable to each pin by S/W setting. To use the pin in Schmitt-trigger input mode, S/W needs to set the I/O pin to Mode0 or Mode1 and PxD=1 (x=A, B, C or D). Reading the pin data (PxD) has different meaning. In "Read-Modify-Write" instruction, CPU actually reads the output data register. In the others instructions, CPU reads the pin state. The so-called "Read-Modify-Write" instruction includes BSX, BCX and all instructions.

These pins can operate in four different modes as below.

Mode	PA0~PA4, PB, PC, PD pin function	PxD SFR data	Pin State	Resistor Pull-up	Digital Input
Mode 0	Open Drain	0	Drive Low	N	N
	Input	1	Pull-up	Y	Y
Mode 1	Open Drain	0	Drive Low	N	N
		1	Hi-Z	N	Y
Mode 2	CMOS Output	0	Drive Low	N	N
		1	Drive High	N	N
	Touch Key	0	TK	N	N
Mode 3	ADC	X (don't care)	–	N	N

I/O Pin Function Table

The chip support I/O Pin Current control (High-Sink/LED Current Control). For efficient control, we divided the High-sink pin or LED Pins into four groups (PA, PB, PC and PD group) independently. It is enable by setting IOCCTRL register.

1Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOCCTRL	LED				HSNK			
R/W	R/W				R/W			
Reset	0	0	0	0	0	0	0	0

1Bh.7~4 **LED:** IO Pin Current Control for LED application
LED[0]: 1: enable PA as LED application
LED[1]: 1: enable PB as LED application
LED[2]: 1: enable PC as LED application
LED[3]: 1: enable PD as LED application

1Bh.3~0 **HSNK:** IO Pin Current for High Sink Control
HSNK[0]: 1: enable PA as High Sink application
HSNK[1]: 1: enable PB as High Sink application
HSNK[2]: 1: enable PC as High Sink application
HSNK[3]: 1: enable PD as High Sink application

Beside I/O port function, each pin has one or more alternative functions, such as LCD, ADC and Touch Key.

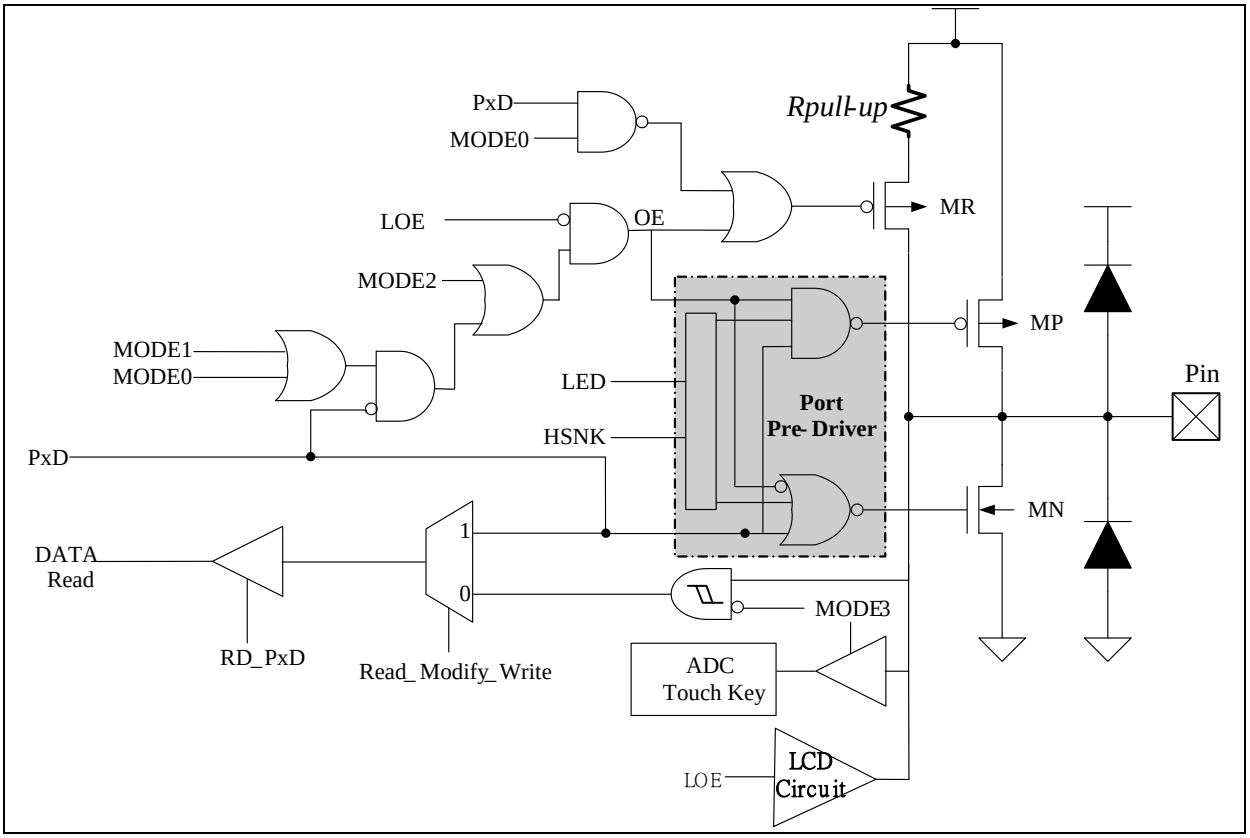
Pin Name	Wake-up	CKO	ADC/TK	LCD	PWM	others	Mode3
PA0	Wakeup / INT0			COM2	PWM0N	I2CSDA	
PA1	Wakeup			COM3	PWM1	I2CSCL	
PA2	Wakeup		TK12		PWM2	TM0CKI	
PA3	Wakeup		TK13		PWM3		
PA4	Wakeup / INT1		TK14		PWM4	XI	
PA7	Wakeup / INT2		TK15		PWM0P/ PWM5	XO	
PB0	Wakeup	TM1OUT	AD0/TK0				AD0
PB1	Wakeup	TCOUT	AD1/TK1				AD1
PB2	Wakeup		AD2/TK2				AD2
PB3	Wakeup		Ad3/TK3				AD3
PB4	Wakeup		TK4				
PB5	Wakeup		TK5				
PB6	Wakeup		TK6				
PB7	Wakeup		TK7				
PC0	Wakeup		AD4/TK8				AD4
PC1	Wakeup		AD5/TK9				AD5
PC2	Wakeup		AD6/TK10				AD6
PC3	Wakeup		AD7/TK11				AD7
PD0	Wakeup		AD8/TK16				AD8
PD1	Wakeup		AD9/TK17				AD9
PD2	Wakeup		AD10/TK18				AD10
PD3	Wakeup		ADC11/TK19				AD11
PD4	Wakeup		AD12/TK20				AD12
PD5	Wakeup		AD13/TK21				AD13
PD6	Wakeup		TK22	COM1			
PD7	Wakeup		TK23(TKREF)	COM0			

PortA/B/C/D multi-function Table

The necessary SFR setting for pin's alternative function is list below.

Alternative Function	Mode	PxD SFR data	Pin State	Other necessary SFR setting
INT0, INT1 TM0CKI	**0**	1	Input with Pull-up	INTxIE TM0CTL
	1	1	Input	
TK0~TK23	**2**	0	Touch Key Idling, CMOS output Low	
			Touch Key Scanning	TKMxCHS
AD0~AD13	**3**	X	ADC Channel	ADCHS
LCD0~LCD3	**X**	X	1/2 Vcc Bias Output	LOE
UART RX	**1**	X	UART input	UART
UART TX	**2**	X	UART output	UART
PWM0N, PWM0P, PWM1/2/3/4/5	**1**	X	PWM Output (Open Drain)	PWM0N PWM0P PWM1/2/3/4/5
	2	X	PWM Output (COMS Output)	
I2CSCL	**0**	1	Input with Pull-up	I2CCTL
	1	1	Input	
I2CSDA	**0**	X	Input with Pull-up/ Open Drain Output	
	1	X	Input / Open Drain Output	
XI, XO	**0**	1	Crystal oscillation	CLKCTL

Mode Setting for Port Alternative Function



PA0 Pin Structure

05h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAD	PAD7			PAD4	PAD3	PAD2	PAD1	PAD0
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	1			1	1	1	1	1

05h.7~0 **PAD:** PA7~PA0 data

06h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBD	PBD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

06h.7~0 **PBD:** PB7~PB0 data

07h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCD					PCD			
R/W					R/W			
Reset					1	1	1	1

07h.3~0 **PCD:** PC3~PC0 data

08h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDD	PDD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

08h.7~0 **PDD:** PD7~PD0 data

85h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODH	PA7MOD						PA4MOD	
R/W	R/W						R/W	
Reset	0	1					0	1

85h.7~6 **PA7MOD:** PA7 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

85h.1~0 **PA4MOD:** PA4 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

86h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODL	PA3MOD		PA2MOD		PA1MOD		PA0MOD	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

86h.7~6 **PA3MOD:** PA3 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

86h.5~4 **PA2MOD:** PA2 Pin Mode Control

00: Mode0
01: Mode1
10: Mode2
11: Mode3

86h.3~2 **PA1MOD:** PA1 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

86h.1~0 **PA0MOD:** PA0 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

87h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODH	PB7MOD		PB6MOD		PB5MOD		PB4MOD	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

87h.7~6 **PB7MOD:** PB7 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

87h.5~4 **PB6MOD:** PB6 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

87h.3~2 **PB5MOD:** PB5 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

87h.1~0 **PB4MOD:** PB4 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

88h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODL	PB3MOD		PB2MOD		PB1MOD		PB0MOD	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

88h.7~6 **PB3MOD:** PB3 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PB3 as ADC3 channel input

88h.5~4 **PB2MOD:** PB2 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PB2 as ADC2 channel input

88h.3~2 **PB1MOD:** PB1 Pin Mode Control

00: Mode0
01: Mode1
10: Mode2
11: Mode3, PB1 as ADC1 channel input

88h.1~0 **PB0MOD:** PB0 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PB0 as ADC0 channel input

8Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCMODL	PC3MOD		PC2MOD		PC1MOD		PC0MOD	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

8Ch.7~6 **PC3MOD:** PC3 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PC3 as ADC7 channel input

8Ch.5~4 **PC2MOD:** PC2 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PC2 as ADC6 channel input

8Ch.3~2 **PC1MOD:** PC1 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PC1 as ADC5 channel input

8Ch.1~0 **PC0MOD:** PC0 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PC0 as ADC4 channel input

8Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDMODH	PD7MOD		PD6MOD		PD5MOD		PD4MOD	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

8Dh.7~6 **PD7MOD:** PD7 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

8Dh.5~4 **PD6MOD:** PD6 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3

8Dh.3~2 **PD5MOD:** PD5 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PD5 as ADC13 channel input

8Dh.1~0 **PD4MOD:** PD4 Pin Mode Control

00: Mode0
01: Mode1
10: Mode2
11: Mode3, PD4 as ADC12 channel input

8Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDMODL	PD3MOD		PD2MOD		PD1MOD		PD0MOD	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

8Eh.7~6 **PD3MOD:** PD3 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PD3 as ADC11 channel input

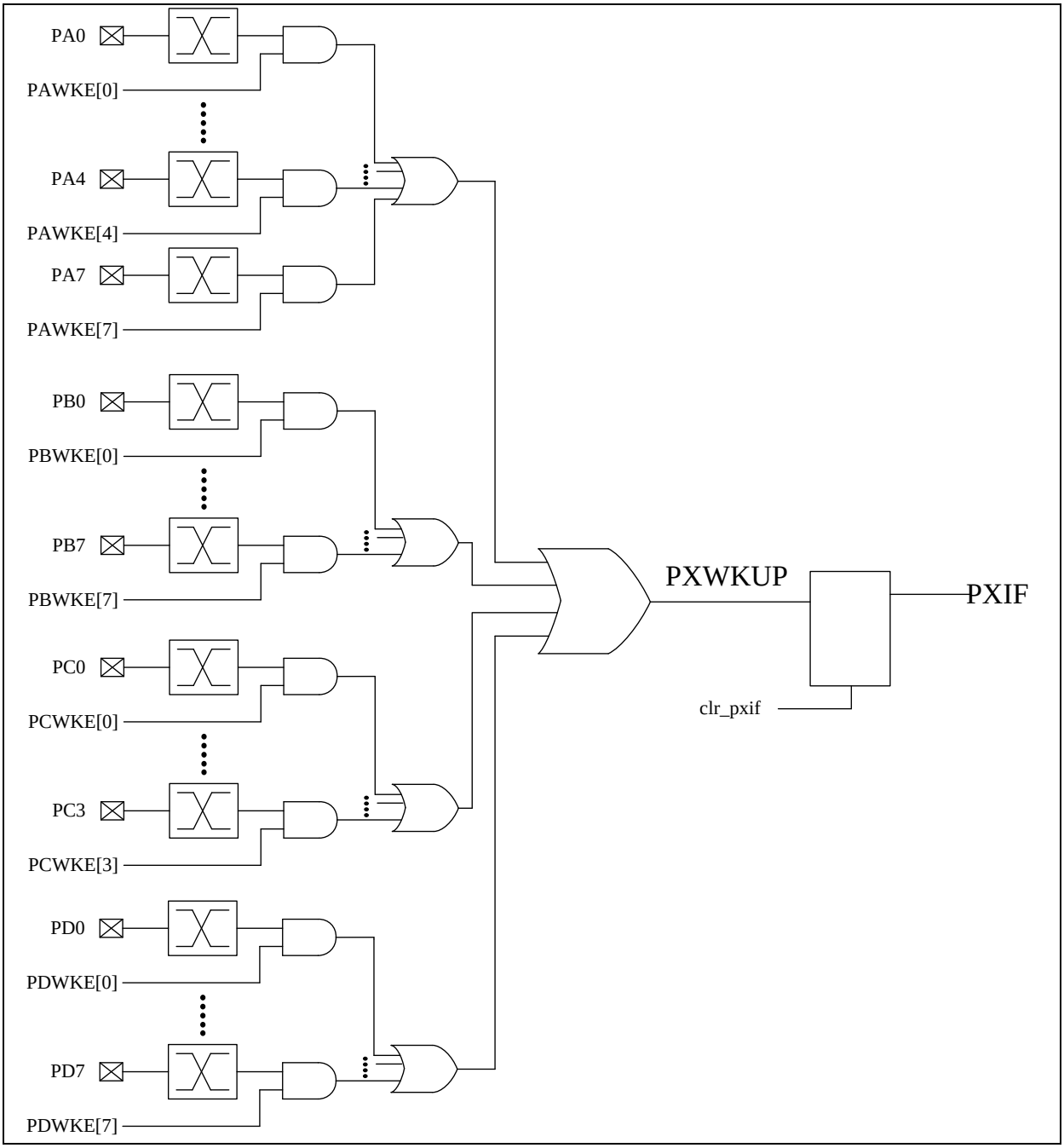
8Eh.5~4 **PD2MOD:** PD2 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PD2 as ADC10 channel input

8Eh.3~2 **PD1MOD:** PD1 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PD1 as ADC9 channel input

8Eh.1~0 **PD0MOD:** PD0 Pin Mode Control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, PD0 as ADC8 channel input

5.2 Pin Interrupt

Pin interrupts include INT0, INT1,INT2 and PA0-4, PA7, PB0-7, PC0-3 and PD0-7 Change Interrupt. These pins also have the STOP mode wake up capability. INT0 and INT1 are falling edge or rising edge triggered, INT2 is falling edge triggered. All of the IO pins Change Interrupt is triggered by any pin state change when the pin wakeup register PxWKE (x=A, B, C or D) and Pin Change Interrupt Enable bit (PXIE) is set to enable the function.



◇ Example: Setup Port B as Pin Change interrupts.

```
ORG     00h     ; Reset Vector
LGOTO   START   ; Goto user program address
```

```
        ORG         004h        ; All interrupt vector
        LGOTO       INT         ; If PXINT (PB) pin change occurred

        ORG         100h
START:
        MOVLW       00000000B
        MOVWX       PBMODH      ; set PB Pin Mode as Mode0
        MOVWX       PBMODL

        MOVLW       11111111B
        MOVWX       PBWKE       ; set PB as Pin Change wakeup
                                ; input with pull-up resistor
        BSX         PXIE        ; Enable PXIE (Pin Change Interrupt Enable)

MAIN:
        ….
        SLEEP
        ….
        LGOTO       MAIN
INT:
        MOVWX       RAM20h      ; Store W data to RAM 20h
        MOVXW       STATUS      ; Get STATUS data
        MOVWX       RAM21h      ; Store SATAUS data to RAM 21h
        …
CHKPX:
        BTXSC       PXIE
        BTXSS       PXIF
        LGOTO       END_CHK     ; if PXIE=0 or PXIE=1 & PXIF=0
        LCALL       PXINT       ; if PXIE=1 & PXIF=1

END_CHK:
        MOVXW       RAM21h      ; Get RAM 21h data
        MOVWX       STATUS      ; Restore STATUS data
        MOVXW       RAM20h      ; Restore W data
        RETI                    ; Return from interrupt

PXINT:
        MOVLW       11111110B
        MOVWX       INTIF1      ; clear PXIF
        …..
        RET
```

1Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAWKE	PAWKE7			PAWKE 4	PAWKE 3	PAWKE 2	PAWKE 1	PAWKE 0
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

1Ch.7~0 **PAWKE:** PA7~PA0 individual wakeup enable

1Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBWKE	PBWKE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

1Dh.7~0 **PBWKE:** PB7~PB0 individual wakeup enable

1Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCWKE					PCWKE			
R/W					R/W			
Reset					0	0	0	0

1Eh.3~0 **PCWKE:** PC3~PC0 individual wakeup enable

1Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDWKE	PDWKE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

1Fh.7~0 **PDWKE:** PD7~PD0 individual wakeup enable

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE1	LVDIE				TKIE	I2CIE	UARTIE	PXIE
R/W	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

INTIE1.0 **PXIE:** Pin Change Wakeup interrupt enable
0: disable
1: enable

1Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF1	LVDIF	TKM2IF	TKM1IF	TKM0IF	TKIF	I2CIF	UARTIF	PXIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1Ah.0 **PXIF:** Pin Change interrupt pending flag
This bit is set by H/W while the corresponding pin change, write 0 to this bit will clear this flag

108h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOE					LOE			
R/W					R/W			
Reset					0	0	0	0

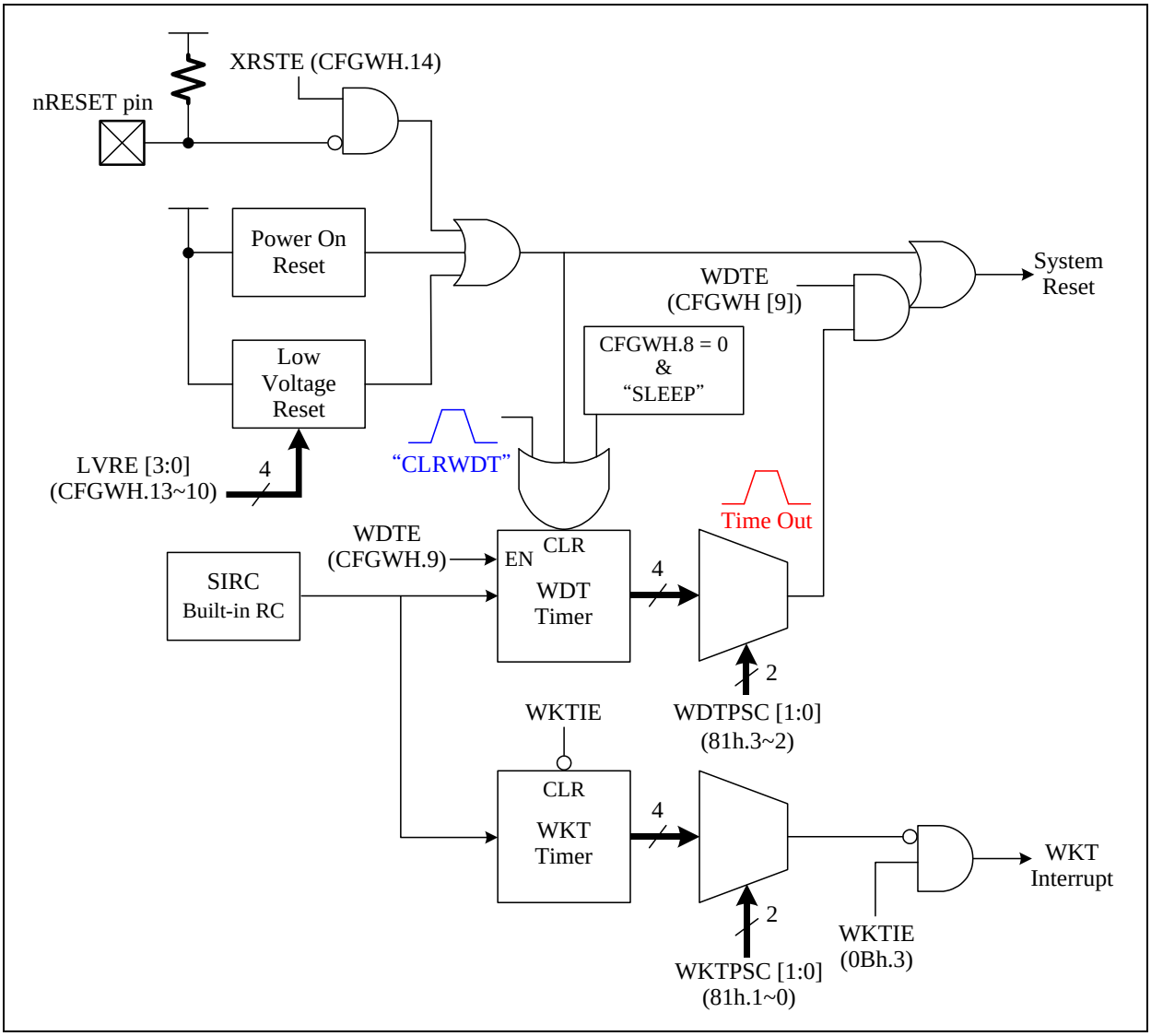
108h.3~0 **LOE:** COM0~COM3 LCD 1/2 bias output enable control
0001: COM0 (PD7) Enable
0010: COM1 (PD6) Enable
0100: COM2 (PA0) Enable
1000: COM3 (PA1) Enable

6. Peripheral Functional Block

6.1 Watchdog (WDT) /Wakeup (WKT) Timer

The WDT and WKT share the same built-in internal RC Oscillator and have individual own counters. The overflow period of WDT, WKT can be selected by individual prescaler (WDTPSC [1:0] , WKTPSC [1:0]) . The WDT timer is cleared by the CLRWDT instruction. If the Watchdog is enabled (CFGWH.9=WDTE=1) , the WDT generates the chip reset signal. Set CFGWH.8 to '0' can let WDT timer stop counting after executing SLEEP instruction, i.e. CFGWH.8=1 WDT timer is always keep counting even if the SLEEP instruction is executed.

The WKT timer is an interval timer, WKT time out will generate WKT Interrupt Flag (WKTIF). The WKT timer is cleared/stopped by WKTIE=0. Set WKTIE=1, the WKT timer will always count regardless at any CPU operating mode.



WDT/WKT Block Diagram

Watchdog clear is controlled by CLRWDT instruction and moving any value into WDTCLR is to clear watchdog timer.

◇ Example: Clear watchdog timer by CLRWDT instruction.

```
MAIN:
        …                       ; Execute program.
        CLRWDT                  ; Execute CLRWDT instruction.
        …
        GOTO    MAIN
```

◇ Example: Setup WDT time and disable after executing SLEEP instruction.

```
        MOVLW   0000011B
        MOVWX   OPTION          ; Select WDT Time out=328 ms @5V

        SLEEP
```

◇ Example: Set WKT period and interrupt function.

```
        MOVLW   00000110B
        MOVWX   OPTION          ; Select WKT period=82 ms @5V.

        MOVLW   11110111B       ; Clear WKT interrupt request flag by using byte operation
                                ; Don't use bit operation "BCX WKTIF" clear interrupt flag
        MOVWX   INTIF           ;

        MOVLW   00001000B       ; Enable WKT interrupt function
        MOVWX   INTIE
```

0Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	ADCIF	T2IF	TM1IF	TM0IF	WKTIF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Ch.3 **WKTIF:** Wakeup Timer interrupt event pending flag
This bit is set by H/W while Wakeup Timer is timeout, write 0 to this bit will clear this flag

0Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	ADCIE	T2IE	TM1IE	TM0IE	WKTIE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Bh.3 **WKTIE:** Wakeup Timer interrupt enable
0: disable
1: enable

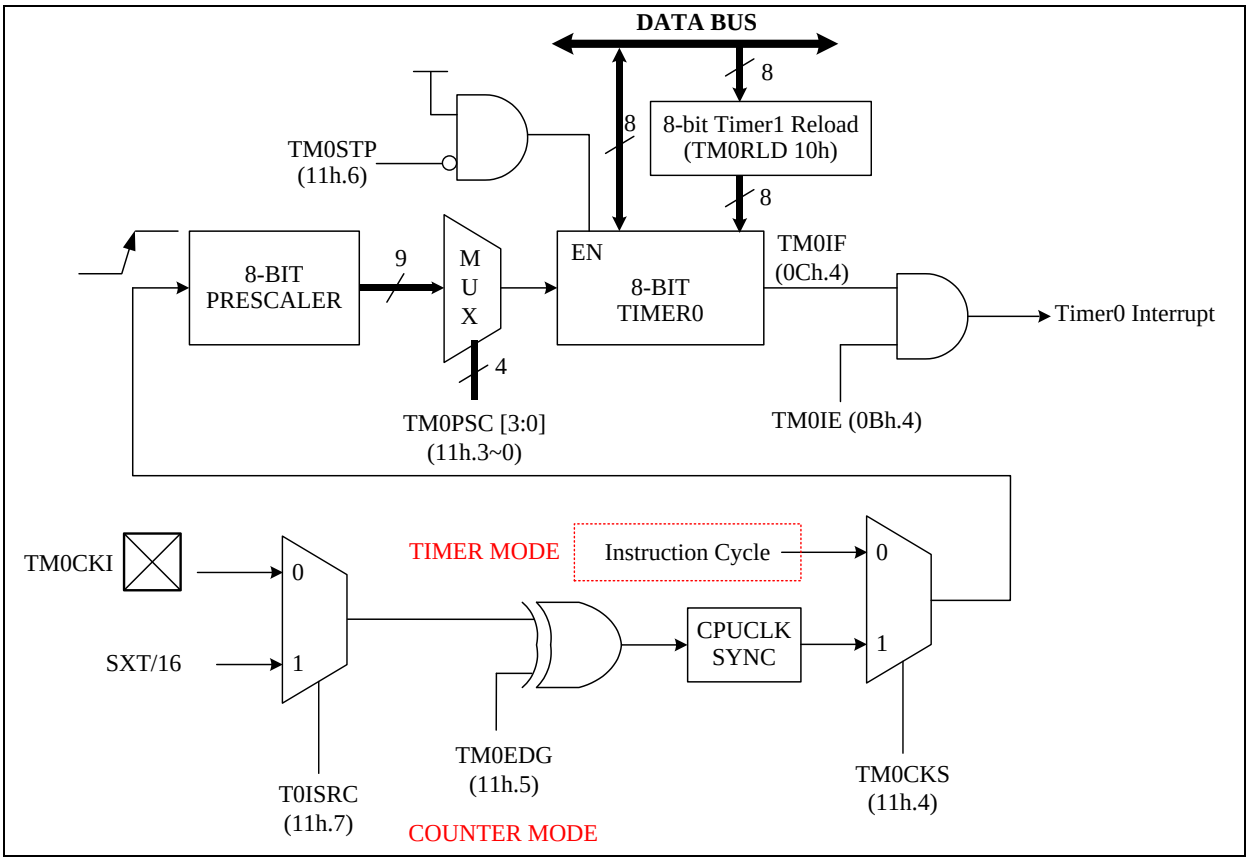
81h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTON	HWAUTO	INT0EDG	INT1EGE	-	WDTPSC		WKTPSC	
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset	0	0	0	-	1	1	1	1

81h.3~2 **WDTPSC:** WDT period (@VCC=5V)
00: 164 ms 01: 328 ms 10: 655 ms 11: 1311 ms

81h.1~0 **WKTPSC:** WKT period (@VCC=5V)
00: 21ms 01: 41 ms 10: 82 ms 11: 164 ms

6.2 Timer0

The Timer0 is an 8-bit wide register 01h (TM0). It can be read or written as any other register. Besides, Timer0 increases itself periodically and automatically rolls over a new "offset value" (TM0RLD) while it rolls over based on the pre-scaled clock source, which can be Fsys/2 when TM0CKS=0 or TM0CKI (PA2) rising/falling input when TM0CKS=1 and T0ISRC=0 or SXT/16 when TM0CKS=1 and T0ISRC=1. The Timer0 increase rate is determined by “Timer0 Pre-Scale” (TM0PSC) register. The Timer0 always generates TM0IF when its count rolls over. It generates Timer0 Interrupt if (TM0IE) is set. Timer0 can be stopped counting if the TM0STP bit is set.



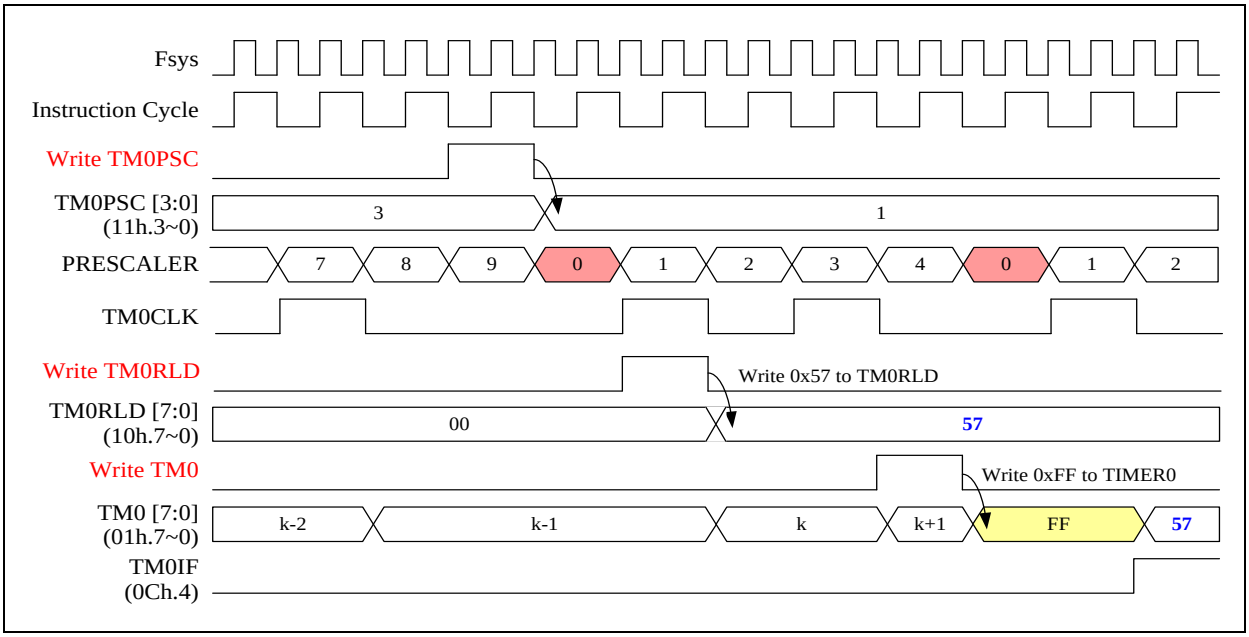
Timer0 Block Diagram

	Timer Mode	Counter Mode TM0CKI(PA2)	Counter Mode SXT/16
TM0CKS	0	1	1
T0ISRC	x	0	1

Timer0 Mode Control Signal Table

The following timing diagram describes the Timer0 works in pure Timer mode.

When the Timer0 prescaler (TM0PSC) is written, the internal 8-bit prescaler will be cleared to 0 to make the counting period correct at the first Timer0 count. TM0CLK is the internal signal that causes the Timer0 to increase by 1 at the end of TM0CLK. TM0WR is also the internal signal that indicates the Timer0 is directly written by instruction; meanwhile, the internal 8-bit prescaler will be cleared. When Timer0 counts from FFh to TM0RLD, TM0IF (Timer0 Interrupt Flag) will be set to 1 and generate interrupt if TM0IE (Timer0 Interrupt Enable) is set.



Timer0 works in Timer mode (TM0CKS=0)

The equation of TM0 interrupt time value is as following:

TM0 interrupt interval cycle time=Fsys/2/TM0PSC/ (256-TM0)

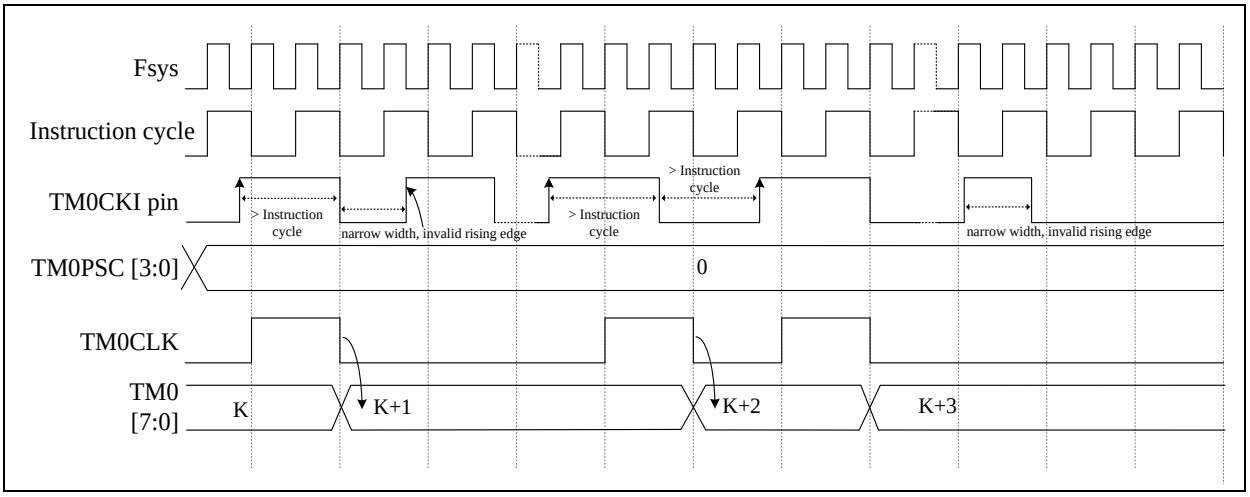
◇ Example: Setup TM0 work in Timer mode

```
; Setup TM0 clock source and divider
        MOVLW   0000 0101B      ; TM0CKS=0, Setup TM0 clock= Fsys/2
        MOVWX   TM0CTL          ; TM0PSC=5, TM0PSC= Fsys/64
; Set TM0 timer.
        BSX     TM0STP          ; Disable TM0 counting (Default "0").
        MOVLW   156
        MOVWX   TM0             ; Write 156 into TM0 register
        MOVLW   124
        MOVWX   TM0RLD          ; Write 156 into TM0RLD register

; Enable TM0 timer and interrupt function.
        MOVLW   1110 1111B      ; Clear TM0 request interrupt flag by byte operation
        MOVWX   INTIF           ; 0Ch
        MOVLW   0001 0000B      ; Enable TM0 interrupt function
        MOVWX   INTIE           ; 0Bh
        BCX     TM0STP          ; Enable TM0 counting (Default “0”).
```

The following timing diagram describes the Timer0 works in Counter mode.

If TM0CKS=1 then Timer0 counter source clock is from TM0CKI pin. TM0CKI signal is synchronized by instruction cycle (Fsys/2) that means the high/low time durations of TM0CKI must be longer than one instruction cycle time (Fsys/2) to guarantee each TM0CKI's change will be detected correctly by the synchronizer.



Timer0 works in Counter mode for TM0CKI (TM0EDG=0) , TM0CKS=1

◇ Example: Setup TM0 work in Counter mode and clock source from TM0CKI pin (PA2)

```
; Setup TM0 clock source from TM0CKI pin (PA2) and divider.
        MOVLW   00110000B
        MOVWX   TM0CTL      ; TM0EDG=1
                            ; Select TM0 prescaler counting edge=falling edge.
                            ; TM0CKS=1, Setup TM0 clock=TM0CKI pin (PA2)
                            ; TM0PSC=0
                            ; TM0 clock prescaler= TM0CKI divided by 1
; Set TM0 timer and stop TM0 counting.
        BSX     TM0STP      ; Disable TM0 counting (Default "0").
        MOVLW   00H
        MOVWX   TM0         ; Write 0 into TM0 register 01H.
; Start TM0 count and read TM0 counter.
        BCX     TM0STP      ; Enable TM0 counting.
        NOP
        NOP
        NOP
        BSX     TM0STP      ; Disable TM0 counting (Default "0")

        MOVXW   TM0
```

01h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0	TM0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

01h **TM0:** Timer0 content

0Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	ADCIE	T2IE	TM1IE	TM0IE	WKTIE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Bh.4 **TM0IE:** Timer0 interrupt enable
0: disable
1: enable

0Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	ADCIF	T2IF	TM1IF	TM0IF	WKTIF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Ch.4 **TM0IF:** Timer0 interrupt event pending flag
This bit is set by H/W while Timer0 overflows, write 0 to this bit will clear this flag

10h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0RLD	TM0RLD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

10h **TM0RLD:** Timer0 Reload Data

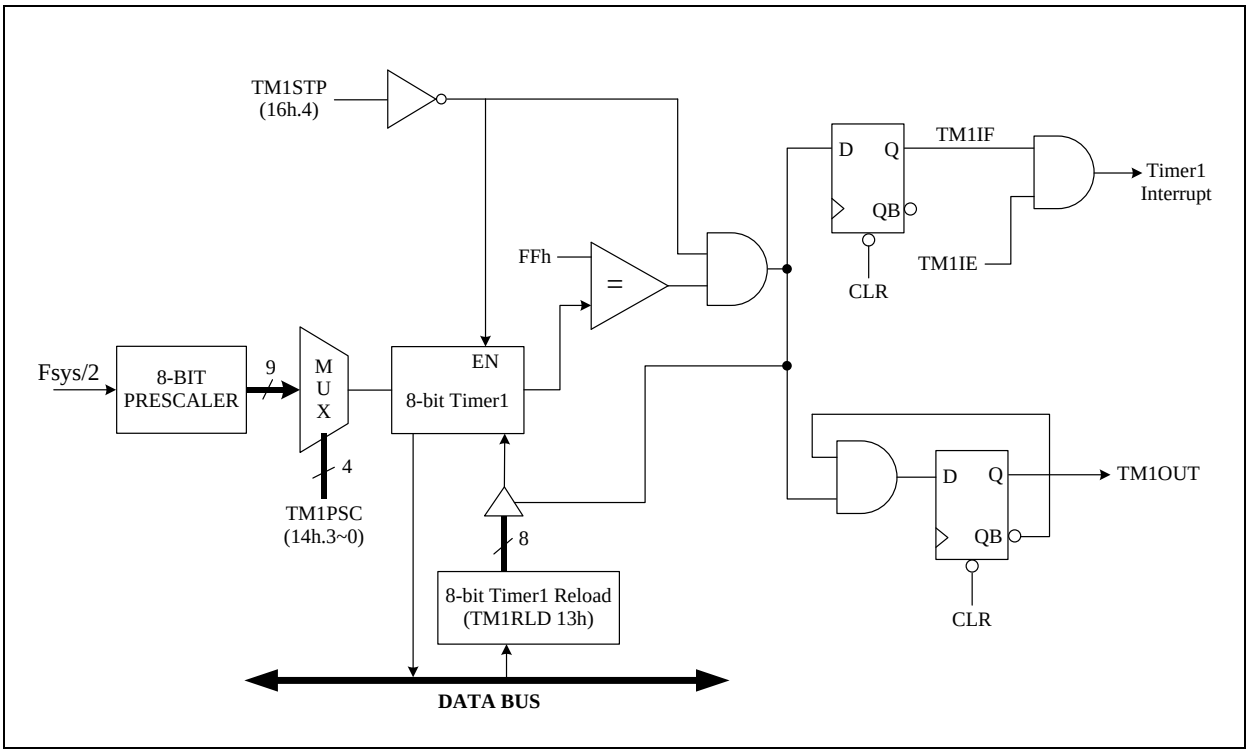
11h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0CTL	T0ISRC	TM0STP	TM0EDG	TM0CKS	TM0PSC			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

11h.7 **T0ISRC:** Timer0 Counter mode source
0: TM0CKI pin (PA2) 1: SXT/16
11h.6 **TM0STP:** Timer0 counter stop
0: Release 1: Stop counting
11h.5 **TM0EDG:** Timer0 prescaler counting edge for TM0CKI pin
0: rising edge 1: falling edge
11h.4 **TM0CKS**: Timer0 prescaler clock source
0:Fsys/2 1: TM0CKI pin (PA2 pin)
11h.3~0 **TM0PSC**: Timer0 prescaler. Timer0 prescaler clock source divided by

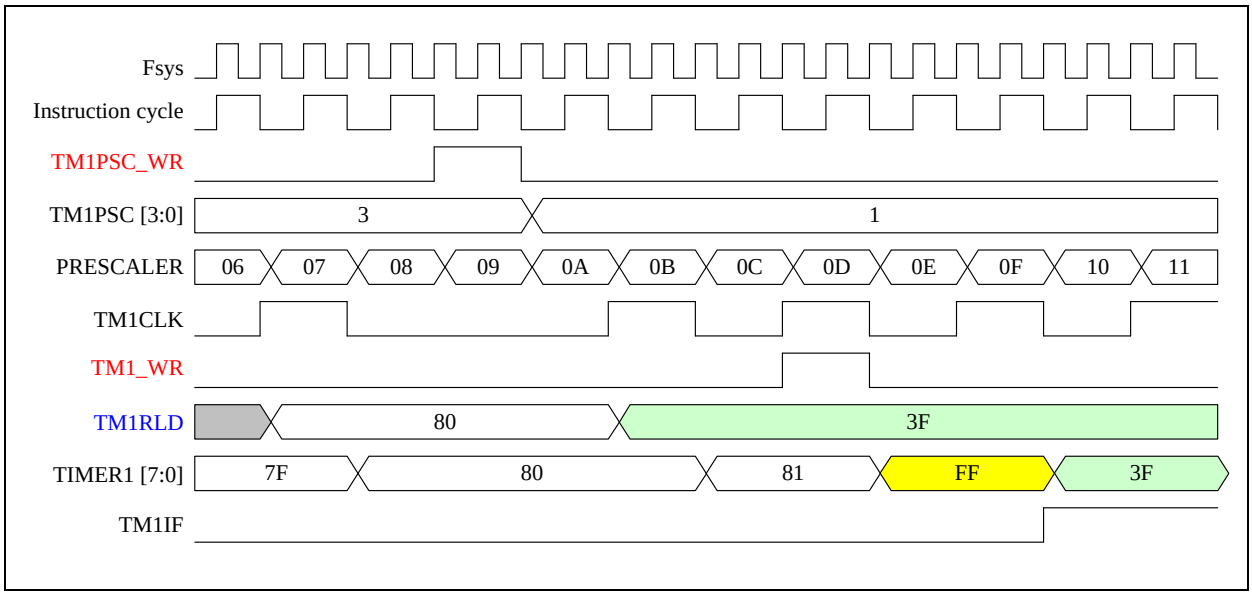
0000: /1	0001: /2	0010: /4	0011: /8
0100: /16	0101: /32	0110: /64	0111: /128
1000: /256	1001: /512	1010: /1024	1011: /2048
1100: /4096	1101: /8192	1110: /16384	1111: /32768

6.3 Timer1

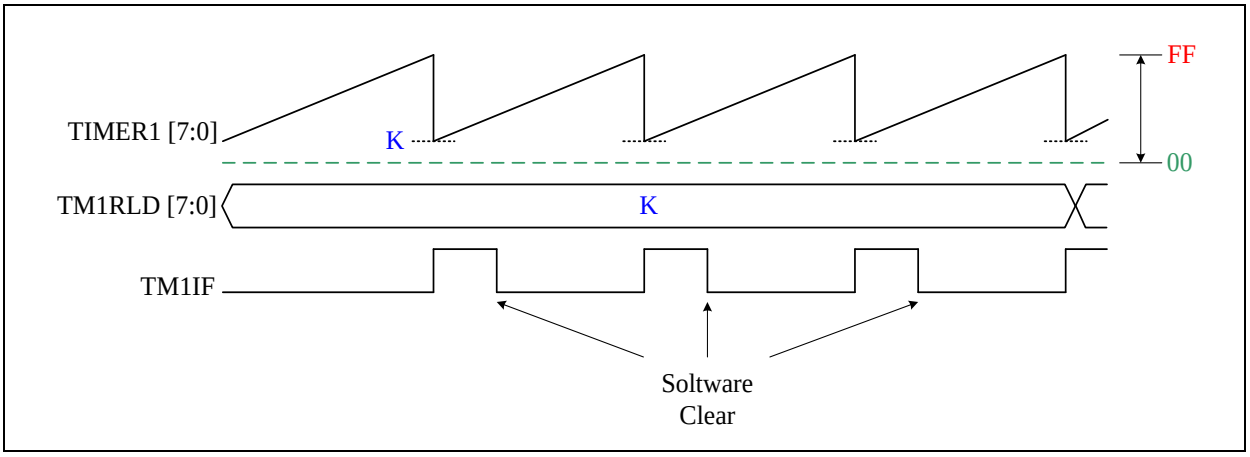
The Timer1 is an 8-bit wide register. It can be read or written as any other register. Besides, Timer1 increases itself periodically and automatically reloads a new "offset value" (TM1RLD) while it rolls over based on the pre-scaled instruction clock (Fsys/2). The Timer1 increase rate is determined by TM1PSC register. Set the TM1STP bit will stop Timer1 counting. TM1OUT is an output signal that toggles when Timer1 overflow.



Timer1 Block Diagram



Timer1 Timing Diagram



Timer1 Reload Diagram

◇ Example: Setup TM1 work in Timer mode and counting overflow toggle out to TM1OUT (PB0) configuration.

```
; Setup TM1 clock source, divider and enable TM1OUT
        MOVLW   0000 0101B
        MOVWX   TM1CTL      ; TM1PSC=5 , Select TM1 clock=Fsys/64.
        BSX     TM1OE       ; Enable TM1OUT function pin (PB0).

; Set TM1 timer offset and stops TM1 counting
        BSX     TM1STP      ; Stop TM1 counting (Default "0").
        MOVLW   F0H
        MOVWX   TM1         ; Write F0H into TM1 counter

; Enable TM1 timer and interrupt function.
        MOVLW   11011111B   ; Clear TM1 request interrupt flag by byte operation
        MOVWX   INTIF       ; 09H

        MOVLW   00100000B   ; Enable TM1 interrupt function.
        MOVWX   INTIE       ;

        BCX     TM1STP      ; Enable TM1 counting (Default “0”).
```

Example:

Fsys=4 MHz, TM1PSC=1, TM1 clock source=Fsys/4=1 MHz

TM1RLD=0xF0,

TM1 interrupt time= (1/1 MHz) * (0xFF – 0xF0) =1 us*16=16 us

TM1OUT output time period=16 us *2=32 us.

TM1OUT output frequency=1/32 us=31.250 KHz.

0Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	ADCIE	T2IE	TM1IE	TM0IE	WKTIE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Bh.5 **TM1IE:** Timer1 interrupt enable
0: disable
1: enable

0Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	ADCIF	T2IF	TM1IF	TM0IF	WKTIF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Ch.5 **TM1IF:** Timer1 interrupt event pending flag
This bit is set by H/W while Timer1 overflows, write 0 to this bit will clear this flag

12h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1	TM1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

12h **TM1:** Timer1 content

13h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1RLD	TM1RLD							
R/W	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

13h.7~0 **TM1RLD:** Timer1 reload offset value while it rolls over

14h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1CTL	–	–	–	TM1STP	TM1PSC			
R/W	–	–	–	R/W	W	W	W	W
Reset	–	–	–	0	0	0	0	0

14h.4 **TM1STP:** Timer1 counter stop
0: Release
1: Stop counting

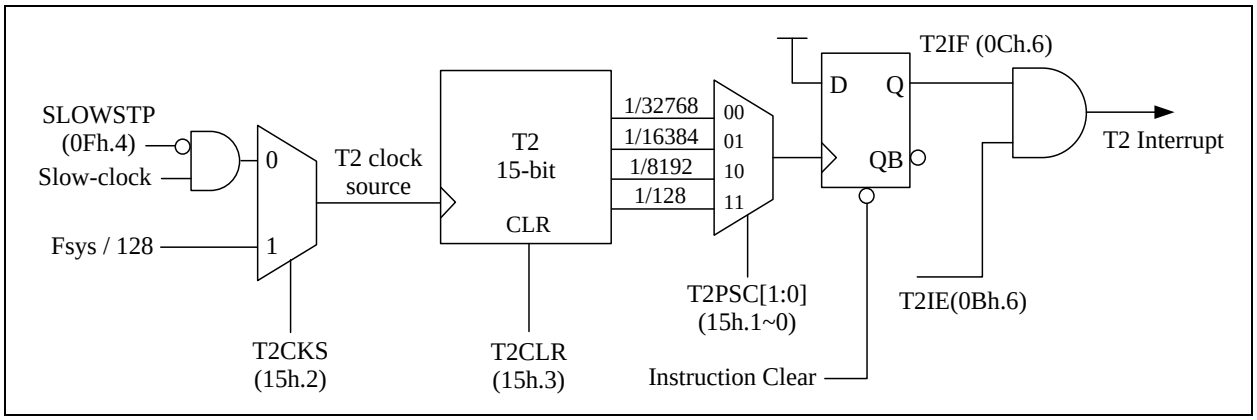
14h.3~0 **TM1PSC:** Timer1 prescaler. Timer1 clock source divided by
0000: Fsys/2 0001: Fsys/4 0010: Fsys/8 0011: Fsys/16
0100: Fsys/32 0101: Fsys/64 0110: Fsys/128 0111: Fsys/256
1xxx: Fsys/512

98h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF098	TCOE	TM1OE	PWM0OE	PWM2OE	PWM1AOE	PWM1BOE	PWM1COE	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset	0	0	0	0	0	0	0	-

F1B.5 **TM1OE:** Enable Timer1 overflow toggle output to PB0 pin (TM1OUT)

6.4 T2:15-bit Timer

The T2 is a 15-bit counter and the clock sources are from either Fsys/128 or Slow-clock. It is used to generate time base interrupt and T2 counter block clock. The T2 content cannot be read by instructions. It generates interrupt flag T2IF (0Ch.6) with the clock divided by 32768/16384/8192/128 depends on T2PSC[1:0] (15h.1~0) register bits. The following figure shows the block diagram of T2.



T2 Block Diagram

Example:

[CPU running at FAST mode, Fsys=Fast-clock= FIRC/4= 4.6 MHz]

◇ Example:

```
; Setup T2 clock source and divider .
        MOVLW   0000 1 101B     ;15h.3 (T2CLR)=1, Stop T2 counting
        MOVWX   T2CTL           ;15h.2 (T2CKS) = 1, T2 clock source = Fsys/128
  ✧                             ;15h.1~0 (T2PSC) =1, Divided by 16384

; Enable T2 timer and interrupt function.
        MOVLW   10111111B       ; Clear T2 request interrupt flag by byte operation
        MOVWX   INTIF           ;

        MOVLW   01000000B       ; Enable T2 interrupt function.
        MOVWX   INTIE           ;

        BCX     T2CLR           ; (T2CLR)=0, Enable T2 counting (Default “0”).
```

T2 clock source is Fsys/128 = 4.6 MHz/128 = 36000 Hz, T2PSC = /16384

T2 frequency = 36000 Hz / 16384 ≒ 2.197 Hz

◇Example:

[CPU running at SLOW mode, Fsys = Slow-clock = SIRC= 50KHz]

◇ Example:

```
; Setup T2 clock source and divider
        MOVLW   00001 000B     ; 15h.3 (T2CLR)=1, Stop T2 counting
        MOVWX   T2CTL          ; 15h.2 (T2CKS) = 0, T2 clock source = Slow-clock
                               ; 15.1~0 (T2PSC) =0, Divided by 32768

; Enable T2 timer and interrupt function.
        MOVLW   10111111B      ; Clear T2 request interrupt flag
        MOVWX   INTIF

        MOVLW   01000000B      ; Enable T2 interrupt function.
        MOVWX   INTIE

        BCX     T2CLR          ; (T2CLR)=0, Enable T2 counting (Default "0").
```

T2 clock source is Slow-clock = 50KHz, T2PSC = /32768,

T2 frequency = 50000Hz / 32768 ≒ 1.53Hz

0Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	ADCIE	T2IE	TM1IE	TM0IE	WKTIE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Bh.6 **T2IE:** T2 interrupt enable
0: disable
1: enable

0Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	ADCIF	T2IF	TM1IF	TM0IF	WKTIF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

0Ch.6 **T2IF:** T2 interrupt event pending flag
This bit is set by H/W while T2 overflows, write 0 to this bit will clear this flag

0Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCTL	SCKTYPE	FCKTYPE		SLOWSTP	FASTSTP	CPUCKS	CPUPSC	
R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	1	0	1	1

0Fh.4 **SLOWSTP:** Stop Slow-clock in Stop Mode
0: no Stop 1: Stop

15h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CTL					T2CLR	T2CKS	T2PSC	
R/W					R/W	R/W	R/W	R/W
Reset					1	0	0	0

15h.3 **T2CLR:** T2 counter clear
0: Release 1: Stop counting

15h.2 **T2CKS:** "T2 clock source" selection.
0: Slow-clock ; 1: Fsys/128

15h.1~0 **T2PSC:** T2 prescaler. "T2 clock source" divided by -
00: 32768 01: 16384 10: 8192 11: 128

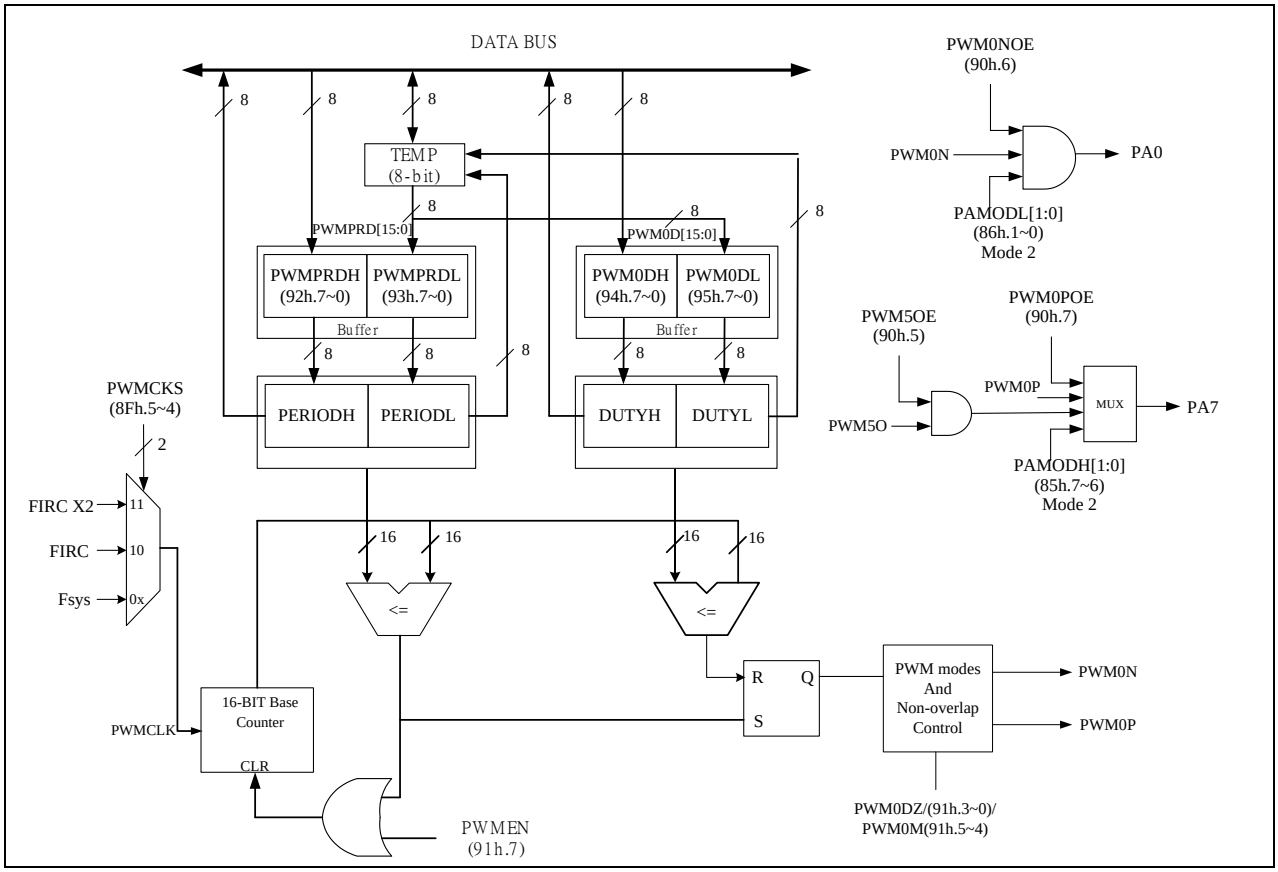
6.5 PWM: Six 16-bit PWM Module

This Chip has six 16-bit PWM modules, PWM0 to PWM5. PWM0~PWM5 have independent 16-bit duty control register, and share a set of 16-bit period register. The PWM can generate various frequency waveforms with 65536 duty resolution based on PWMCLK, which frequency can select Fsys or FIRC OR FIRC*2, decided by PWMCKS (8Fh.5~4).

The 16-bit PWM period PWMPRD and PWM duty PWM0D~PWM5D registers all have a low and high byte structure. **Writing to these register pairs must be carried out in a specific way. That is, write low byte register first and then writes high byte register**. For example, writing period value to PWMPRDL register (93h) and then PWMPRDH (92h). The PWMPRD will immediately change to the new values when high byte data has been written to the register. Writing PWM0D~PWM5D are the same as writing PWMPRD.

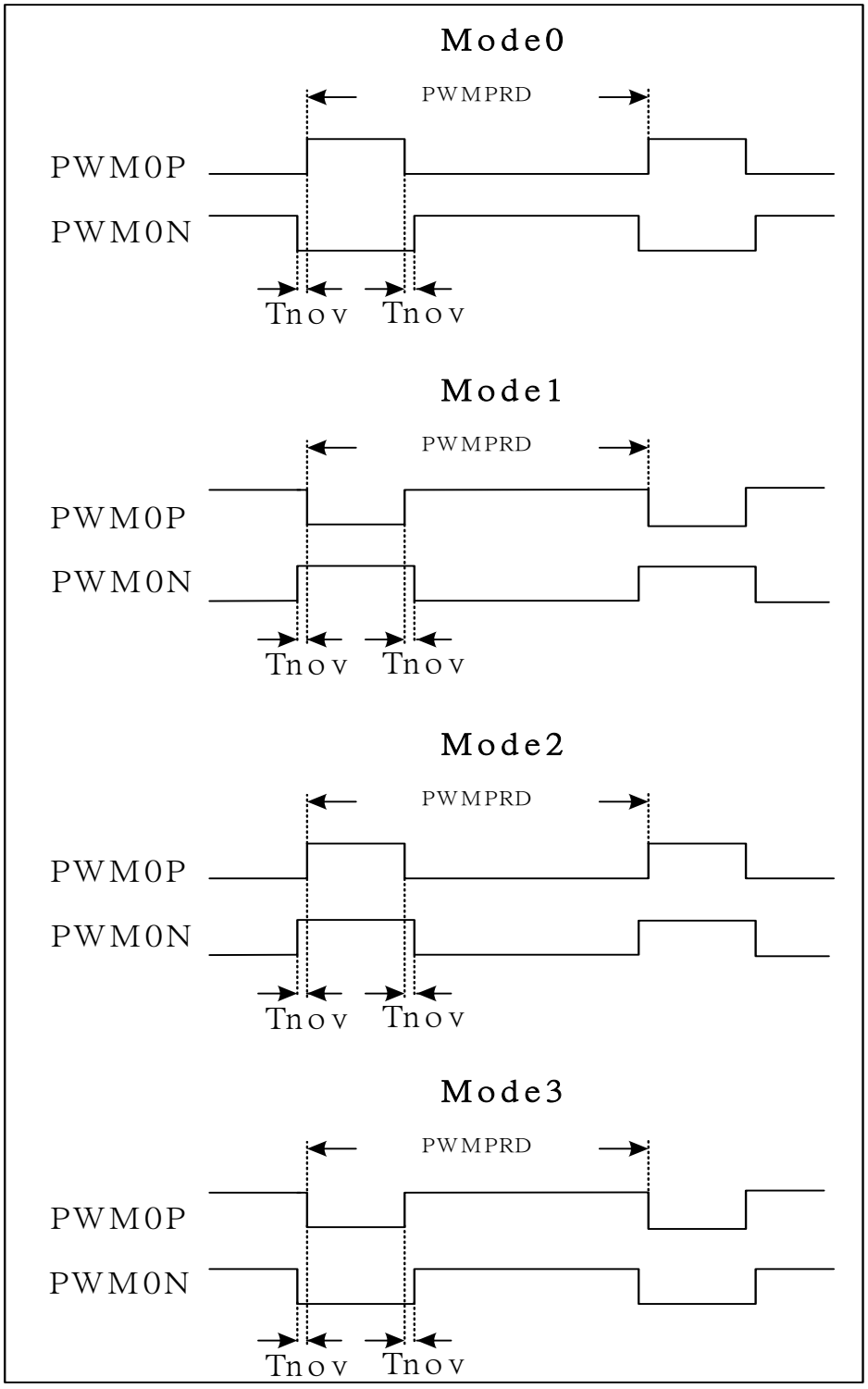
If PWMEN is cleared, the PWM0~5 will be cleared and stopped, otherwise the PWM0~5 remain running. The PWM0 structure is shown as follow. The PWM0 duty cycle can be changed by writing to PWM0DL and PWM0DH. The PWM0 period can be set by writing the period value to PWMPRDL and PWMPRDH register. There is a digital comparator that compares the PWM counter and PWMRD, if PWM counter is larger than PWMPRD the PWM counter will be cleared and PWM output signal will be set to high level. The PWM output signals PWM0~PWM5 reset to low level whenever the 16-bit base counter matches the PWM duty register PWM0D ~PWM5D individually.

Only PWM0 has dead-zone control (PWM0DZ), and is divided into PWM0P and PWM0N outputs with 4 modes (PWM0OM), and the remaining PWM1~5 have no non-overlap control. The PWM1~5 outputs are PWM1O~PWM5O.



PWM0 Block Diagram

Only PWM0 can be output via PWM0P and PWM0N with four different modes control by PWM0OM (91h.5~4). The edges of PWM pulse can be separated with 16 different time non-overlap clock intervals (Tnov). The width of Tnov can be selected by PWM0DZ (91h.3~0) within 0~15 pwm clock. The default output form is Mode0. The waveforms of the four output modes are shown below.



PWM0 Waveform Modes

◇ Example: [CPU running at Fast mode, Fsys=FIRC 18.432Mhz]

; Setup PWM0 clock prescaler

```
MOVLW     00000000B     ;
MOVWX     OPTION2       ; PWMCKS=00B, PWM clk source = Fsys=FIRC 18.432MHz
                        ; Tpwmclk=(1/18.432M)
MOVLW     20h
MOVWX     PWMPRDL       ; set PWM period Low byte =20h
                        ; low byte data is stored in TEMP, not in PWMPRD register
MOVLW     03h
MOVWX     PWMPRDH       ; set PWM period High byte =03h
                        ; PWMPRD = 0320h (TEMP data is also saved to PWMPRD)
MOVLW     90h
MOVWX     PWM0DL        ; set PWM0 Duty Low byte    =90h
                        ; low byte data is stored in TEMP, not in PWM0D register
MOVLW     01h           ;
MOVWX     PWM0DH        ; set PWM0 Duty High byte    =01h
                        ; PWM0D = 0190h (TEMP data is also saved to PWM0D)
MOVLW     10010100B
MOVWX     PWMCTL        ; set PWMEN=1, PWM0OM=10B=Mode 2,
                        ; PMW0DZ=0100B= non-overlap 4*Tpwmclk
MOVLW     10xxxx10B     ;
MOVWX     PAMODL        ; set PA7, PA0 as CMOS output
MOVLW     11000000B
MOVWX     PWMOE         ; enable PWM0P output to PA7, enable PWM0N output to PA0
```

90h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMOE	PWM0POE	PWM0NOE	PWM5OE	PWM4OE	PWM3OE	PWM2OE	PWM1OE	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset	0	0	0	0	0	0	0	-

90h.7 **PWM0POE:** PWM0P Output Enable
0: Disable
1:Enable, PWM0P output to PA7

90h.6 **PWM0NOE:** PWM0N Output Enable
0: Disable 1:Enable,
PWM0N output to PA0

90h.5 **PWM5OE:** PWM5 Output Enable
0: Disable
1:Enable, PWM5 output to PA7; PWM0POE has higher priority to output PA7

90 h.4 **PWM4OE:** PWM4 Output Enable
0: Disable
1:Enable, PWM4 output to PA4

90 h.3 **PWM3OE:** PWM3 Output Enable
0: Disable
1:Enable, PWM3 output to PA3

90 h.2 **PWM2OE:** PWM2 Output Enable
0: Disable
1:Enable, PWM2 output to PA2

90 h.1 **PWM1OE:** PWM1 Output Enable
0: Disable
1:Enable, PWM1 output to PA1

91h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCTL	PWMEN	-	PWM0OM		PWM0DZ			
R/W	R/W	-	R/W		R/W			
Reset	0	-	0	0	0	0	0	0

91h.7 **PWMEN:** PWM Clock Enable
0: Disable
1: Enable

91h.5~4 **PWM0OM:** PWM0 Output Mode
00: Mode 0
01: Mode 1
10: Mode 2
11: Mode 3

91h.3~0 **PWM0DZ:**PWM0 Dead Zone (non-overlap) control
0000: non-overlap 0*Tpwmclk; Original PWM0
0001: non-overlap 1*Tpwmclk
0010: non-overlap 2*Tpwmclk
……
1101: non-overlap 13*Tpwmclk
1110: non-overlap 14*Tpwmclk
1111: non-overlap 16*Tpwmclk

92h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMPRDH	PWMPRDH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

92h.7~0 **PWMPRDH:** PWM period data high byte

93h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMPRDL	PWMPRDL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

93h.7~0 **PWMPRDL:** PWM period data low byte

94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

94h.7~0 **PWM0DH:** PWM0 duty data high byte

95h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DL	PWM0DL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

95h.7~0 **PWM0DL:** PWM0 duty data low byte

96h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

96h.7~0 **PWM1DH:** PWM1 duty data high byte

97h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DL	PWM1DL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

97h.7~0 **PWM1DL:** PWM1 duty data low byte

98h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DH	PWM2DH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

98h.7~0 **PWM2DH:** PWM2 duty data high byte

99h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DL	PWM2DL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

99h.7~0 **PWM2DL:** PWM2 duty data low byte

9Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DH	PWM3DH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

9Ah.7~0 **PWM3DH:** PWM3 duty data high byte

9Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DL	PWM3DL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

9Bh.7~0 **PWM3DL:** PWM3 duty data low byte

9Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4DH	PWM4DH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

9Ch.7~0 **PWM4DH:** PWM4 duty data high byte

9Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM4DL	PWM4DL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

9Dh.7~0 **PWM4DL:** PWM4 duty data low byte

9Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM5DH	PWM5DH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

9Eh.7~0 **PWM5DH:** PWM5 duty data high byte

9Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM5DL	PWM5DL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

9Fh.7~0 **PWM5DL:** PWM5 duty data low byte

6.6 UART

TM56F1543 has built-in standard UART (Universal Asynchronous Receiver/Transmitter), which is responsible for performing serial communications among computers. Transmitting device changes the parallel data to serial data and sends the bit-stream data via TX line, the receiving device receives the data via RX line in serial form and converts to parallel data stored in register for MCU reading. The TX/RX module also handles data synchronization, parity bit generation and detection, frame error, overrun error, and interrupts generation. Figure 6.6.1 shows the data format of UART

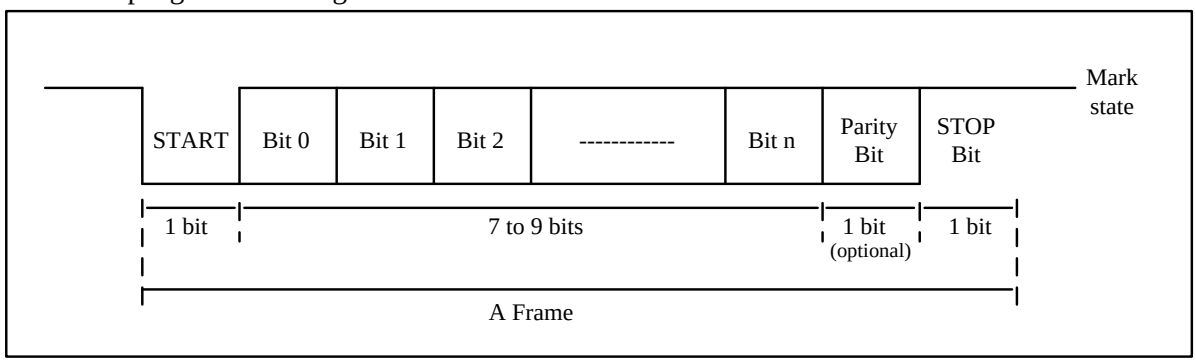


Figure 6.6.1 UART data format

The transmission line is normally kept in mark state (logic 1) until the transmission or reception start with a transition to space state (logic 0). The first bit transmitted is START bit and the length is 1 bit wide (1 bps second), followed by the transmitted bit stream of the data. The LSB (least Significant Bit) is sent first, the number or transmitted bit is defined by UMODE control bits that can have 7, 8 or 9 bits mode to be transmitted or received. The parity bit is followed by data bit and is selectable to be sent or not, but in 9-bit mode transmission, the parity bit is always not to be transmitted.

UART Modes

The UAT can operate in one of three modes, e.g. Mode 0 (7-bit data), Mode 1 (8-bit data) and Mode 2 (9-bit data). The data format of Mode 0 and Mode 1 can transmit/receive parity bit according to PRE bit. If PRE=1, the TX data format will add the parity bit after the data bits, otherwise, the TX only transmits the data bits. Mode 2 does not support parity bit transmit/receive. Note that the setting of UART between two communicating devices must be the same so that the RX part can check the data format and parity the same as TX part. The parity select bit is EVEN bit in UARTS control register. It uses even parity if EVEN=1, else it uses odd parity. Every UART transfer is ended with a STOP bit. If the STOP bit is not seen by RX part, the RX part will set the FMERR bit in UARTS control register to indicate the transfer may not be properly received/transmitted, it must be re-sent again or firmware handling. Figure 6.6.2 shows the data formats of three UART modes.

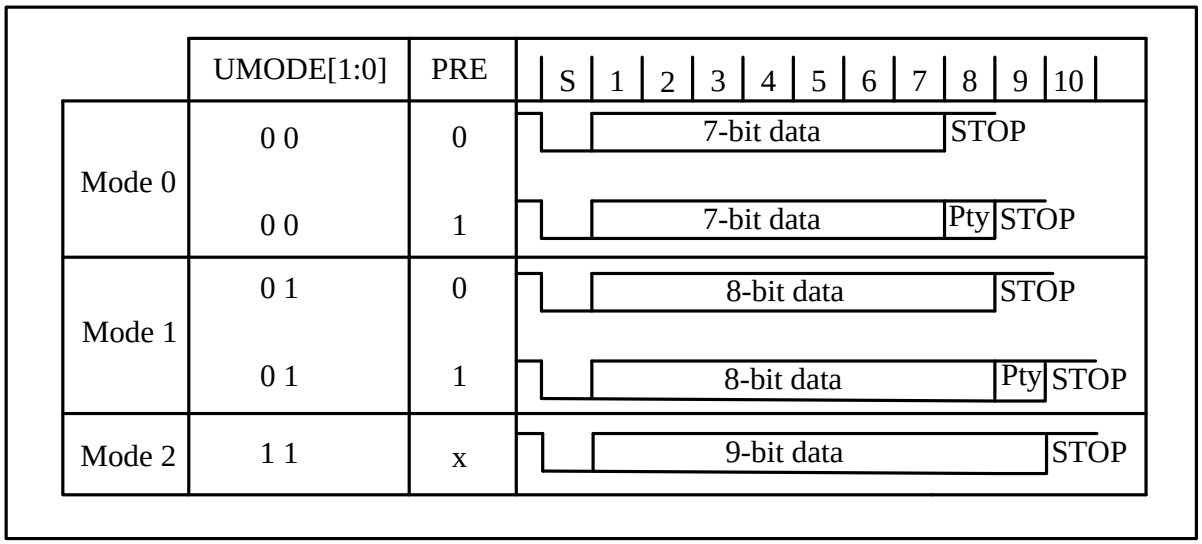


Figure 6.6.2 UART Modes

UART System Block

Figure 6.6.3 shows the system block of the UART built in TM56F1543. The Baud Clock Generator divides the Fsys to produce the proper frequency of the UART baud rate. The divisor is UBAUD register. Every bit of data stream is sampled by 16 Baud clocks which are generated from Baud Clock Generator. The desired Baud rate can be achieved by setting UBAUD with the following equation:

$$\text{Baud Rate} = \frac{\text{Fsys}}{\text{32*UBAUD}}$$

The divided clock (Baud clock) is then sent to TX and RX control logic and TX/RX shift buffers. The TX control logic start sending data out to TX pin (PA3) once the URDATA is written, URTD9 will be sent if the UART mode is Mode 2. When transmit completes, the “TX buffer Empty” signal is asserted, then interrupt will be generated if INTIE1.UARTIE is set. UINVEN will invert the output when it is set to 1, the RX will be inverted when UINVEN is set.

The UART RX signal is input from RX pin (PA2) and then it is inverted if UINVEN is set, passing through a synchronization circuit then clocked to RX shifter. Number of bits to be shifted into RX shifter depends on what UART Mode is operated, and then RX control logic handle them, including frame error detection (FMERR bit), parity detection (PRERR) and overrun error (OVERR) detection. Frame error means that the incoming frame STOP bit is not detected. Parity error means the incoming data parity bit does not equal to the parity of data bits that are evaluated by the RX control logic. Overrun error means the previous transfer that is stored in URDATA has not been read as a new incoming transfer is completed, the old URDATA will be lost when overrun error occurs.

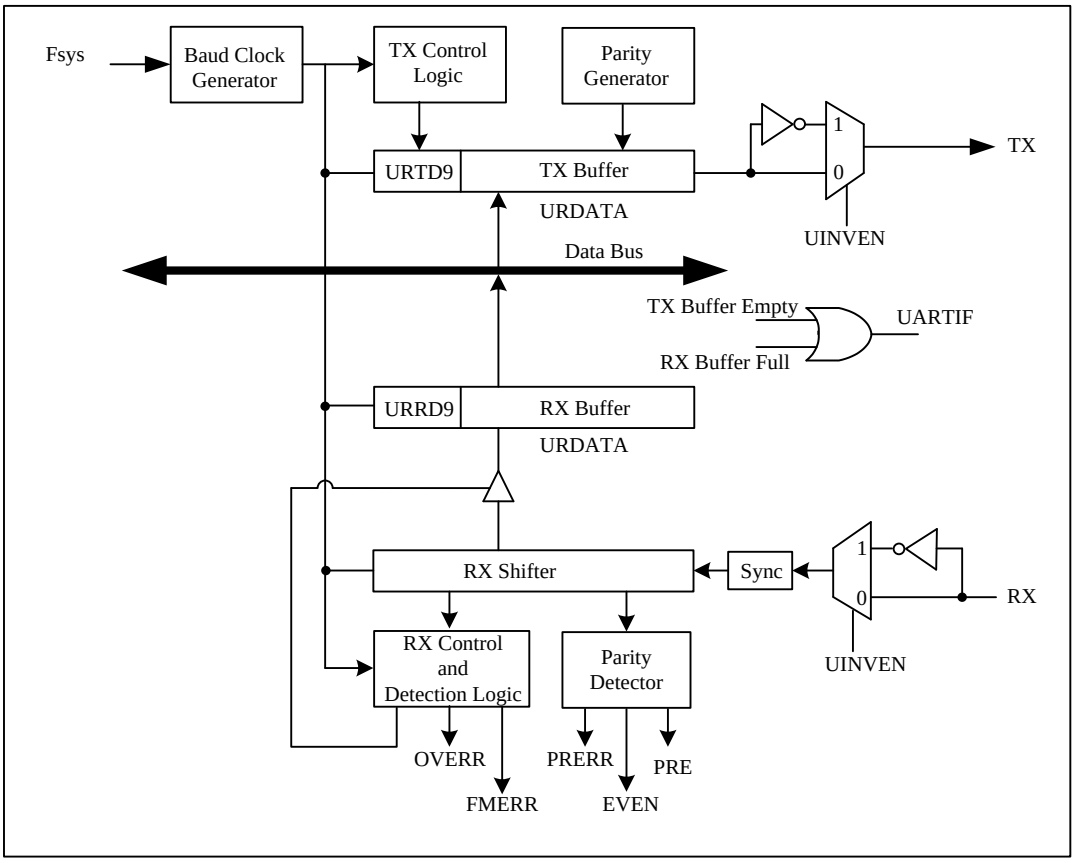


Figure 6.6.3 UART Block Diagram

Table 6.6. lists the common used operating frequency to generate common used Baud Rates under Fsys is 18.432MHz. Some Baud Rates cannot be achieved because frequency error is too large to use.

Fsys (Hz)	Desired Baud Rate (bps)	UBAUD	Actual Generate Baud Rate	Frequency Error(%)	
18432000	2400	240	2400	0	
18432000	4800	120	4800	0	
18432000	9600	60	9600	0	
18432000	14400	40	14400	0	
18432000	19200	30	19200	0	
18432000	28800	20	28800	0	
18432000	38400	15	38400	0	
18432000	57600	10	57600	0	
18432000	76800	8	72000	6.25%	Don’t use
18432000	76800	7	82285.7	7.14%	Don’t use
18432000	115200	5	115200	0	
18432000	192000	3	192000	0	

Table 6.6 UART Baud Rates setting

Example:

[CPU running at FAST mode , Fsys=FIRC 18.432 MHz]

UART Baud Rate = 115200 bps, RX pin (PA2), TX pin (PA3).
Transmit 91H data to TX (PA3)

◇ Example:

```
MOVLW   00000111B       ; Fsys=18.432 MHz
MOVWX   CLKCTL          ;

MOVLW   10010101B       ; RX (PA2) Pin Mode=1, TX (PA3) Pin Mode=2
MOVWX   PAMODL;

MOVLW   00000101B
MOVWX    UBAUD          ; 115200 bps (@Fsys=18.432MHz)

BSX     UARTIE          ; enable UART interrupt

MOVLW   00101010B       ;
MOVWX   UARTCTL         ; 8bit mode, UTXE=1, URXE=0, UARTE=1, UINVEN=0

MOVLW   10010001B       ;
MOVWX   URDATA          ; TX Buffer=91h, and then H/W send to TX pin via TX shifter

BTXSS   UTBE
LGOTO   $-1             ; check TX buffer until buffer is empty (transmit finished)
……
…...
```

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE1	LVDIE				TKIE	I2CIE	UARTIE	PXIE
R/W	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

INTIE1.1 **UARTIE:** UART TX/RX complete interrupt enable
0: disable
1: enable

1Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF1	LVDIF	TKM2IF	TKM1IF	TKM0IF	TKIF	I2CIF	UARTIF	PXIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1Ah.1 **UARTIF:** UART interrupt pending flag
This bit is set by H/W while TX/RX transfer is completed; write 0 to this bit will clear this flag.

10Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UBAUD	UBAUD							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

10Dh **UBAUD:** UART Baud Rate Divider

187h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UARTCTL	URTD9	UMODE			UTXE	URXE	UARTE	UINVEN
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset	0	0	0	–	0	0	0	0

187h.7 **URTD9:** UART Transmitted 9th bit
187h.6~5 **UMODE:** UART Mode Selection
00: 7-bit
01: 8-bit
10: 9-bit
11: Reserved
187h.3 **UTXE:** UART transmission enable:
0: Disable
1: Enable
187h.2 **URXE:** UART reception enable:
0: Disable
1: Enable
187h.1 **UARTE**: UART function enable:
0: Disable
1: Enable
187h.0 **UINVEN**: UART TX/RX output/input Inversion enable:
0: Disable
1: Enable

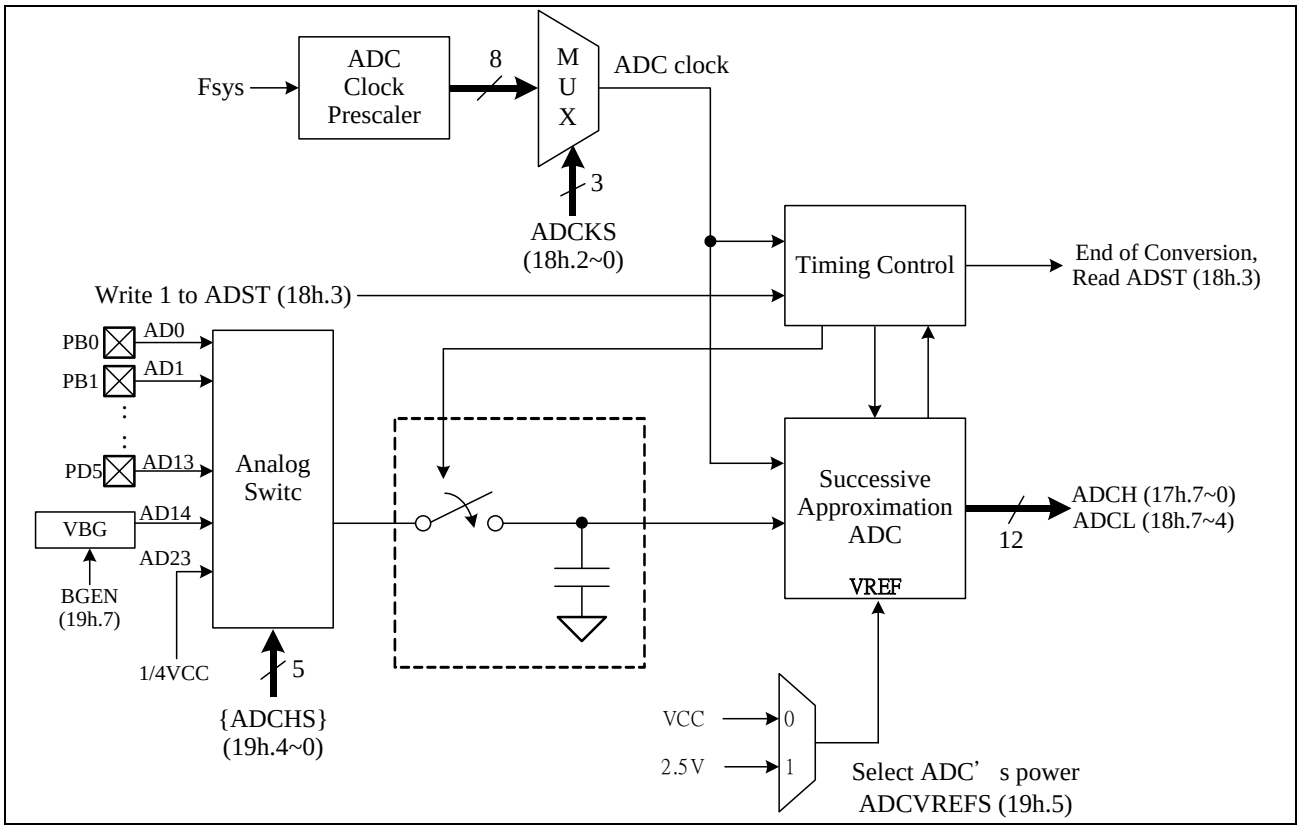
188h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UARTSTA	UTBE	URRD9	EVEN	PRE	PREERR	OVERR	FMERR	URBF
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

188h.7 **UTBE:** UART Transmitting status
0: TX is transmitting
1: TX buffer is empty
188h.6 **URRD9**: UART Received 9th bit
188h.5 **EVEN:** UART parity:
0: ENEN
1: ODD
188h.4 **PRE:**UART Parity Addition
0: Disable
1: Enable
188h.3 **PRERR**: UART Parity Error:
Set to 1 when parity error occurs, clear to 0 by F/W
188h.2 **OVERR**: UART Overrun Error
Set to 1 when overrun error occurs, clear to 0 by F/W
188h.1 **FMERR:** UART Frame Error
Set to 1 when frame error occurs, clear to 0 by F/W
188h.0 **URBF:** UART buffer status
Set to 1 when 1 byte (or 9 bits) is received
F/W read URDATA will clear to 0 automatically and then to receive the succeeding data without overrun error

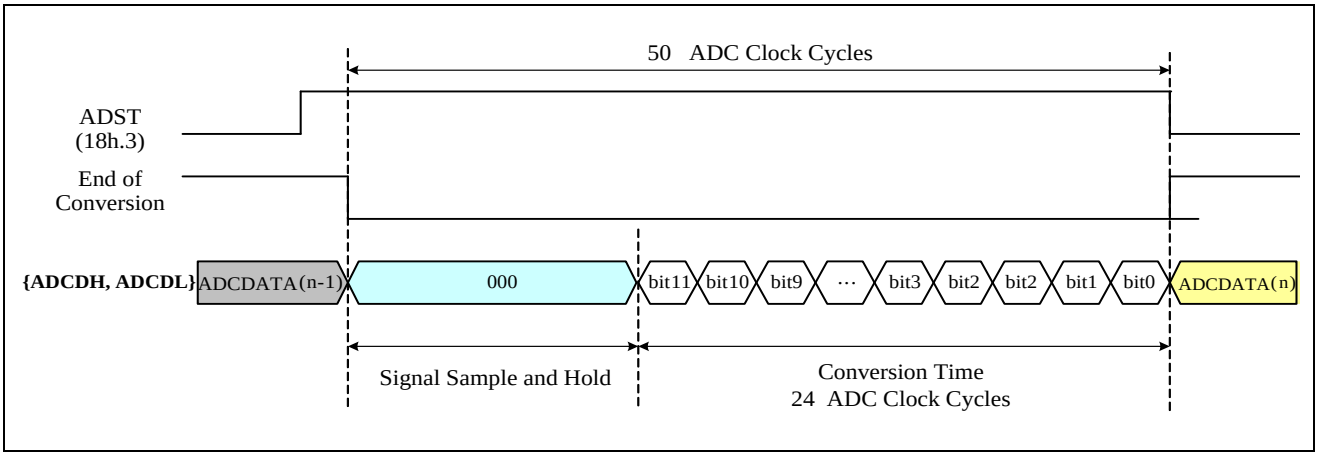
18Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
URDATA	URDATA							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

18Dh **URDATA:** UART Transmission/Reception Data Buffer
write: to transmit buffer
read: from receive buffer

6.7 Analog-to-Digital Converter



The 12-bit ADC (Analog to Digital Converter) consists of a 14-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, user needs to set ADCKS (18h.2~0) to choose a proper ADC clock frequency, which must be less than 1 MHz. User then launches the ADC conversion by setting the ADST (18h.3) control bit. After end of conversion, H/W automatic clears the ADST (18h.3) bit. User can poll this bit to know the conversion status. The PxMODx control registers are used for ADC pin configuration, user must set the Pin Mode=3 when the pin is used as an ADC input. The setting can disable the pin logical input path to save power consumption. User needs to set {ADCHS} (19h.4~0) to choose the input channel of ADC. Two of them, AD14 is VBG input for ADC and AD23 is 1/4VCC input for ADC. Besides, VBG is controlled by BGEN (19h.7). ADC reference voltage is selected by ADCVREFS (19h.5).



Example:

[CPU running at FAST mode , Fsys=FIRC 18.432 MHz]

ADC clock frequency=FIRC/32, ADC channel=ADC10 (PD2).

◇ Example:

```
MOVLW   00000111B     ; Fsys=18.432 MHz
MOVWX   CLKCTL        ;

MOVLW   01110101B     ; ADC10 (PD2) Pin Mode=3=ADC input
MOVWX   PDMODL;

MOVLW   00000011B     ; Fsys=18.432 MHz
MOVWX   ADCTL         ; 18h.2~0 (ADCKS) =ADC clock=Fsys/32=576KHz

MOVLW   1 00 01010B   ; 19h.7=1, enable VBG; 19h.6~5=0, VREF=VCC
MOVWX   ADCTL2        ; 19h.4~0 (ADCHS [4:0]) =10, ADC select ADC10 (PD2 pin).

BSX     ADST          ; 18h.3 (ADST) , ADC start conversion.

WAIT_ADC:
        BTXSC   ADST          ; Wait ADC conversion finish.
        LGOTO   WAIT_ADC

        MOVXW   ADH           ; 17h.7~0, Read ADC result [11:4] into W
        …
        MOVXW   ADCTL         ; 18h.7~4, Read ADC result [3:0] into W
        …
```

17h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R	R	R	R	R	R	R	R
Reset	–	–	–	–	–	–	–	–

17h.7~0 **ADCDH:** ADC output data MSB, ADQ [11:4]

18h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCTL	ADCDL				ADST	ADCKS		
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

18h.7~4 **ADCDL:** ADC output data LSB, ADQ [3:0]

18h.3 **ADST:** ADC start bit.
0: H/W clear after end of conversion
1: ADC start conversion

18h.2~0 **ADCKS:** ADC clock frequency selection:
000: Fsys/256 100: Fsys/16
001: Fsys/128 101: Fsys/8
010: Fsys/64 110: Fsys/4
011: Fsys/32 111: Fsys/2

19h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCTL2	BGEN	-	ADCVREFS	ADCHS				
R/W	R/W	-	R/W	R/W				
Reset	1	-	0		0	0	0	0

F19.7 **BGEN:** Band Gap BG1.2V enable
0: Disable
1: Enable and Auto disable in STOP/IDLE mode

F19.6~5 **ADCVREFS:** ADC reference voltage select,
0: VCC,
1: 2.5V,

F19.4~0 **ADCHS:** ADC channel select

00000: ADC0 (PB0)	00100: ADC4 (PC0)	01000: ADC8 (PD0)	01100: ADC12 (PD4)
00001: ADC1 (PB1)	00101: ADC5 (PC1)	01001: ADC9 (PD1)	01101: ADC13 (PD5)
00010: ADC2 (PB2)	00110: ADC6 (PC2)	01010: ADC10 (PD2)	01110: VBGO
00011: ADC3 (PB3)	00111: ADC7 (PC3)	01011: ADC11 (PD3)	10111: 1/4 VCC

6.8 Touch Key

The Touch Key offers an easy, simple and reliable method to implement finger touch detection. In most applications, it doesn't require any external component. The device support 3 modules, 24 channels touch key detection.

To use the Touch Key, user must setup the Pin Mode (***see Section 5***) correctly as below table. Setting Mode2 for an Idling Touch Key pin can CMOS output Low and reduce the mutual interference between the adjacent keys.

PxMODx setting for Touch Key	TK0~TK23
Pin is Touch Key, Idling	CMOS output Low (Mode2)
Pin is Touch Key, Scanning	

There are three Touch Key Modules (Module0, Module1 and Module2) in the TM56F1543. Each module can work independently. In the Touch Key Module, there are two oscillators: Reference Clock (RCKx) and Touch Clock (TCKx). They are connected to the Reference Counter and Data Counter respectively. The frequency of RCKx can be adjusted by setting TKMxREFC. Reference Counter is used to control conversion time. TKMxTCP is touch key clock frequency select (only available in TKMxJMP=0). When TKMxJMP =1, the touch key clock frequency is automatically change.

From starting touch key conversion to end, it will take 0 to 4096 RCK oscillation cycles by setting TKMxTMR. After end of conversion, user can get TK Data (TKMxDH, TKMxDL) from Data counter. TK Data is affected by finger touching. As finger touching TCK is getting slower, the value of TK Data is smaller than the no finger touching. According to the difference of TKMxDATA, user can check if it is touched of not. A suitable TKMxTMR and TKMxREFC setting can adjust TK Data to adapt the system board circumstances. To get the best TKMxREFC setting, user can try different TKMxREFC value, and then find the one which makes the TK Data and TKMxTMR as close as possible. In the other hand, user can adjust the overall operating frequency of the TK system (including TCKx & RCKx) by setting TKMxFSL (frequency select). For all Touch Key Module, there is a control signal TKMHSENSE (11Fh.7) can be set to enhance the Touch key performance.

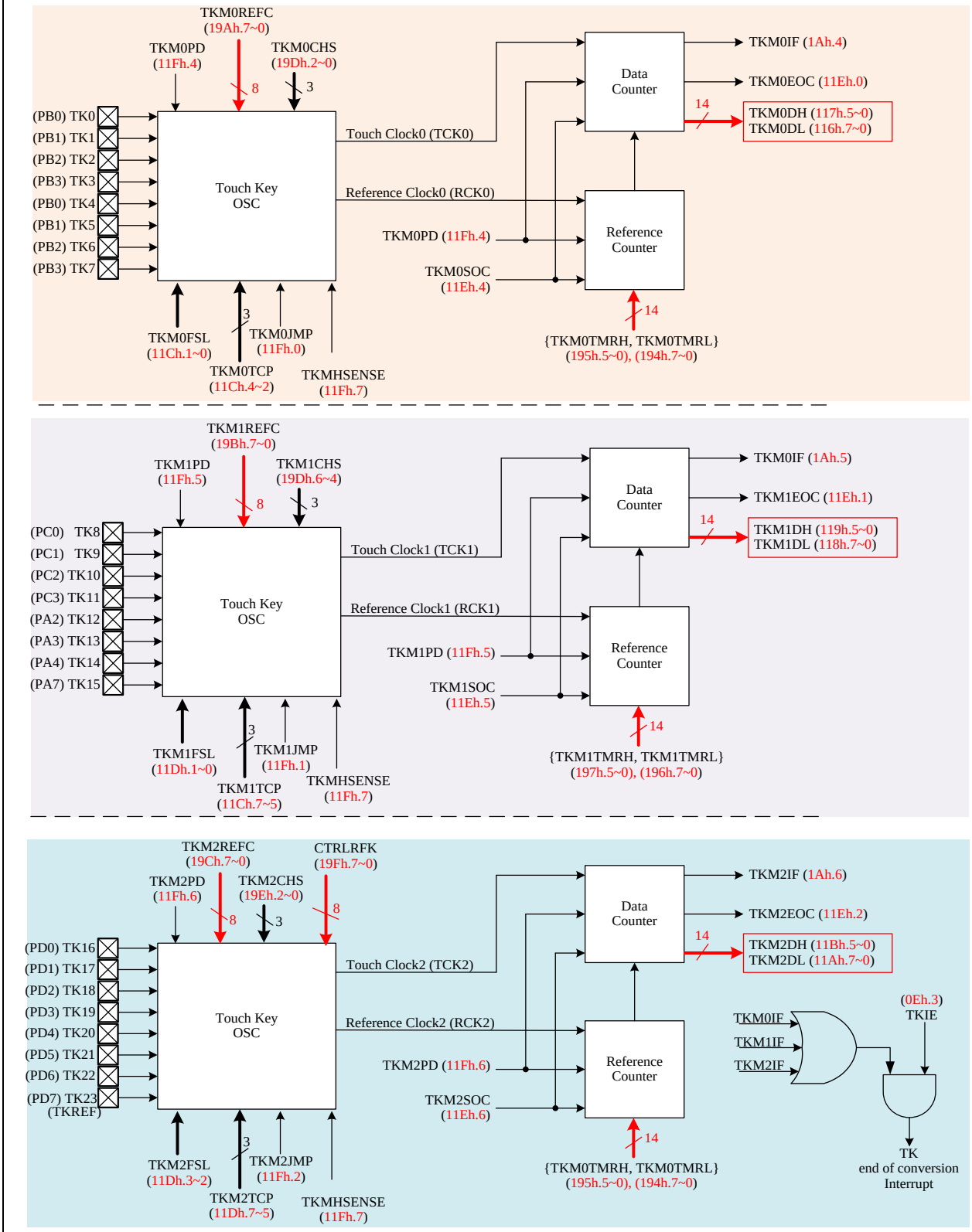
To start the Scanning, user assigns TKMxPD=0, then set the TKMxSOC bit to start touch key conversion, the TKMxSOC bit can be automatically cleared while end of conversion. However, if the SYSCLK is too slow, H/W might fail to clear TKMxSOC due to clock sampling rate. TKMxEOC=0 means conversion is in process. TKMxEOC=1 means the conversion is finish, and the touch key counting result is stored into the 12 bits TK Data Counter TKMxDH and TKMxDL.

TKIF (sum of TKM0IF, TKM1IF and TKM2IF) will active at the first time enable Touch Key function (TKMxPD=0), user should clear TKIF after TKMxPD cleared.

Touch Key Channel 23 (PD7) can set as reference key. The capacitor of the reference key is control by CTRLRFK (19F.7~0). (00: minimum capacitor on TK23, FF: maximum capacitor on TK23)

TKM0IF	TKM1IF	TKM2IF	TKIF	STATE
0	0	0	0	IDLE
1	0	0	1	TK Module0 is end of conversion
0	1	0	1	TK Module1 is end of conversion
1	1	0	1	TK Module0 and Module1 are both end of conversion
0	0	1	1	TK Module2 is end of conversion
1	0	1	1	TK Module0 and Module2 are both end of conversion
0	1	1	1	TK Module1 and Module2 are both end of conversion
1	1	1	1	All TK module are end of conversion

Touch Key Interrupt Flag Description



Touch Key Structure

◇ Example: Use TK module0, Module1 and Module2, Touch key channel = TK2 (PB2), TK8 (PC0), TK20 (PD4)

```
.ORG        00h
            LGOTO  START
.ORG        004h
INT:
            BTXSC       TKIF        ; check TKIF
            LCALL       INT_TK
            RETI
INT_TK:
            BTXSC       TKM0IF      ; check TKM0IF
            LCALL       INT_TKM0
            BTXSC       TKM1IF      ; check TKM1IF
            LCALL       INT_TKM1
            BTXSC       TKM2IF      ; check TKM2IF
            LCALL       INT_TKM2
            RET
INT_TKM0:
            MOVLW       11101111B   ; clear TKM0IF
            MOVWX       TKMFLG
            MOVXW       TKM0DH      ; read TK0 DATA[13:8] into W register
            …
            MOVXW       TKM0DL      ; read TK0 DATA[7:0] into W register
            …
            RET
INT_TKM1:
            MOVLW       11011111B   ; clear TKM1IF
            MOVWX       TKMFLG
            MOVXW       TKM0DH      ; read TK1 DATA[13:8] into W register
            …
            MOVXW       TKM1DL      ; read TK1 DATA[7:0] into W register
            …
            RET
INT_TKM2:
            MOVLW       11101111B   ; clear TKM2IF
            MOVWX       TKMFLG
            MOVXW       TKM2DH      ; read TK2 DATA[13:8] into W register
            …
            MOVXW       TKM2DL      ; read TK2 DATA[7:0] into W register
            …
            RET

START:
              …..
SET_MODE:
            MOVLW       xx10xxxxB   ; PBMODL[5:4] = 10b
            MOVWX       PBMODL      ; set PB2 as Mode 2 for touch key input
            BCX         PBD,2       ; clear PB2 as CMOS output low

            MOVLW       xxxxxx10B   ; PCMODL[1:0] = 10b
            MOVWX       PCMODL      ; set PC0 as Mode 2 for touch key input
            BCX         PCD,0       ; clear PC0 as CMOS output low
            MOVLW       xxxxxx10B   ; PDMODH[1:0] = 10b
```

```
            MOVWX     PDMODH      ; set PD4 as Mode 2 for touch key input
            BCX       PDD,4       ; clear PD4 as CMOS output low

TK_INIT:
            MOVLW     010 001 10B ;
            MOVWX     TKMCON0     ; set TKM1TCP=2, TKM0TCP=1, TKM0FSL=2
            MOVLW     110 x00 01B ;
            MOVWX     TKMCON1     ; set TKM2TCP=6, TKM2FSL=0, TKM1FSL=1

            MOVLW     00h
            MOVWX     TKM0TMRH
            MOVLW     64H
            MOVWX     TKM0TMRL    ; TKM0TMR=64H
            MOVLW     00h
            MOVWX     TKM1TMRH
            MOVLW     C8H
            MOVWX     TKM1TMRL    ; TKM1TMR=C8H
            MOVLW     01h
            MOVWX     TKM2TMRH
            MOVLW     26H
            MOVWX     TKM2TMRL    ; TKM12MR =126H

            MOVLW     4DH
            MOVWX     TKM0REFC    ; TKM0REFC=64H
            MOVLW     B3H
            MOVWX     TKM1REFC    ; TKM1REFC=B3H
            MOVLW     8AH
            MOVWX     TKM2REFC    ; TKM2REFC=8AH

            MOVLW     x100x010B   ; set TKM0CHS=2 (TK2)
            MOVWX     TKMCHS      ; set TKM1CHS=0 (TK8)
            MOVLW     00000100B
            MOVWX     TKM2CHS     ; set TKM2CHS=4 (TK20)

            MOVLW     1000x100B
            MOVWX     TKMCTL1     ; TKMHSEN=1, TK0/1/2 high sensitivity
                                  ; TMK2PD=TKM1PD=TKM0PD=0,
                                  ; enable TMM2/TKM1/TKM0 activity
                                  ; TKM2JMP=1, TKM2 clock mode auto-change
                                  ; TKM1JMP= TKM0JMP=0, TKM1/TKM0
                                  ;  clock mode fixed(refer to TKM1TCP/ TKM0TCP)
            MOVLW     11110111B
            MOVWX     INTIF1      ; clear TKIF
            BSX       TKIE        ; enable TKIE,  enable TK interrupt

TK_START:
             BSX      TKM0SOC     ; start TKM0 conversion
             BSX      TKM1SOC     ; start TKM1 conversion
             BSX      TKM2SOC     ; start TKM2 conversion
             …..
             …..
```

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE1	LVDIE				TKIE	I2CIE	UARTIE	PXIE
R/W	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

INTIE1.3 **TKIE:** Touch Key interrupt enable
0: disable
1: enable

1Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF1	LVDIF	TKM2IF	TKM1IF	TKM0IF	TKIF	I2CIF	UARTIF	PXIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1Ah.6 **TKM2IF:** Touch Key module2 interrupt pending flag
This is set by H/W after end of TK2 conversion, write 0 to clear this bit or write 1 to TKM2SOC will clear this flag

1Ah.5 **TKM1IF:** Touch Key module1 interrupt pending flag
This is set by H/W after end of TK1 conversion, write 0 to clear this bit or write 1 to TKM1SOC will clear this flag

1Ah.4 **TKM0IF:** Touch Key module0 interrupt pending flag
This is set by H/W after end of TK0 conversion, write 0 to clear this bit or write 1 to TKM0SOC will clear this flag

1Ah.3 **TKIF:** ouch Key interrupt pending flag,
set by H/W while TKM0 or TKM1 or TKM2 are end of conversion, write 0 to this bit will clear all of Touch Key interrupt flag

116h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM0DL	TKM0DL							
R/W	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

116h.7~0 **TKM0DL:** Touch Key Module0 data LSB[7:0]

117h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM0DH	-	-	TKM0DH					
R/W	-	-	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

117h.5~0 **TKM0DH:** Touch Key Module0 data MSB[13:8]

118h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM1DL	TKM1DL							
R/W	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

118h.7~0 **TKM1DL:** Touch Key Module1 data LSB[7:0]

119h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM1DH	-	-	TKM1DH					
R/W	-	-	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

119h.5~0 **TKM1DH:** Touch Key Module1 data MSB[13:8]

11Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM2DL	TKM2DL							
R/W	R	R	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

11Ah.7~0 **TKM2DL:** Touch Key Module2 data LSB[7:0]

11Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM2DH	-	-	TKM2DH					
R/W	-	-	R	R	R	R	R	R
Reset	-	-	-	-	-	-	-	-

11Bh.5~0 **TKM2DH:** Touch Key Module2 data MSB[13:8]

11Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCON0	TKM1TCP			TKM0TCP			TKM0FSL	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	1	0	0

11Ch.7~5 **TKM1TCP:** TK module1 touch key clock frequency select; (only available in TKM1JMP=0)

11Ch.4~2 **TKM0TCP:** TK module0 touch key clock frequency select; (only available in TKM0JMP=0)

11Ch.1~0 **TKM0FSL:** TK module0 clock(RCK0/TCK0) frequency selection;
00: slowest, …, 11: fastest

11Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCON1	TKM2TCP				TKM2FSL		TKM1FSL	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	0	0	0		0	0	0	0

11Dh.7~5 **TKM2TCP:** TK module2 touch key clock frequency select; (only available in TKM2JMP=0)

11Dh.3~2 **TKM2FSL:** TK module2 clock(RCK2/TCK2) frequency selection;
00: slowest, …, 11: fastest

11Dh.1~0 **TKM1FSL:** TK module1 clock(RCK1/TCK1) frequency selection;
00: slowest, …, 11: fastest

11Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCTL0	-	TKM2SOC	TKM1SOC	TKM0SOC	-	TKM2EOC	TKM1EOC	TKM0EOC
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset	-	0	0	0	-	-	-	-

11Eh.6 **TKM2SOC:** Start Touch Key Module2 conversion
Set 1 to start Touch Key Module2 conversion. If SYSCLK is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag

11Eh.5 **TKM1SOC:** Start Touch Key Module1 conversion
Set 1 to start Touch Key Module1 conversion. If SYSCLK is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag

11Eh.4 **TKM0SOC:** Start Touch Key Module0 conversion
Set 1 to start Touch Key Module0 conversion. If SYSCLK is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag

11Eh.2 **TKM2EOC:** Touch Key Module2 end of conversion flag, TKM2EOC may have 3uS delay after TKM2SOC=1, so F/W must wait enough time before polling this Flag.
0: Indicates conversion is in progress
1: Indicates conversion is finished

11Eh.1 **TKM1EOC:** Touch Key Module1 end of conversion flag, TKM1EOC may have 3uS delay after TKM1SOC=1, so F/W must wait enough time before polling this Flag.

0: Indicates conversion is in progress
1: Indicates conversion is finished

11Eh.0 **TKM0EOC:** Touch Key Module0 end of conversion flag, TKM0EOC may have 3uS delay after TKM0SOC=1, so F/W must wait enough time before polling this Flag.
0: Indicates conversion is in progress
1: Indicates conversion is finished

11Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCTL1	TKMHSEN	TKM2PD	TKM1PD	TKM0PD		TKM2JMP	TKM1JMP	TKM0JMP
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	1	1	1		0	0	0

11Fh.7 **TKMHSEN:** TK Module Sensitivity, 1=higher sensitivity; 0=normal.

11Fh.6 **TKM2PD:** Touch Key Module2 power down
0: Touch Key Module2 running
1: Touch Key Module2 power down

11Fh.5 **TKM1PD:** Touch Key Module1 power down
0: Touch Key Module1 running
1: Touch Key Module1 power down

11Fh.4 **TKM0PD:** Touch Key Module0 power down
0: Touch Key Module0 running
1: Touch Key Module0 power down

11Fh.2 **TKM2JMP:** Touch Key Module2 clock mode
0: Fix frequency (refer to TKM2TCP**)**
1: Auto-change

11Fh.1 **TKM1JMP:** Touch Key Module1 clock mode
0: Fix frequency (refer to TKM1TCP)
1: Auto-change

11Fh.0 **TKM0JMP:** Touch Key Module0 clock mode
0: Fix frequency (refer to TKM0TCP)
1: Auto-change

194h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM0TMRL	TKM0TMRL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

194h.7~0 **TKM0TMRL** Touch Key Module0 reference counter LSB[7~0]

195h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM0TMRH	-	-	TKM0TMRH					
R/W	-	-	R/W					
Reset	-	-	0	0	0	0	0	0

195h.3~0 **TKM0TMRH**: Touch Key Module0 reference counter MSB[13~8]

196h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM1TMRL	TKM1TMRL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

196h.7~0 **TKM1TMRL** Touch Key Module1 reference counter LSB[7~0]

197h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM1TMRH	-	-	TKM1TMRH					
R/W	-	-	R/W					
Reset	-	-	0	0	0	0	0	0

197h.3~0 **TKM1TMRH**: Touch Key Module1 reference counter MSB[13~8]

198h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM2TMRL	TKM2TMRL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

198h.7~0 **TKM2TMRL** Touch Key Module2 reference counter LSB[7~0]

199h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM2TMRH			TKM2TMRH					
R/W			R/W					
Reset			0	0	0	0	0	0

199h.3~0 **TKM2TMRH**: Touch Key Module2 reference counter MSB[13~8]

19Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM0REFC	TKM0REFC							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

19Ah.7~0 **TKM0REFC** TK module0 Reference clock capacitor select

19Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM1REFC	TKM1REFC							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

19Bh.7~0 **TKM1REFC** TK module1 Reference clock capacitor select

19Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKM2REFC	TKM2REFC							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

19Ch.7~0 **TKM2REFC** TK module2 Reference clock capacitor select

19Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCHS0		TKM1CHS				TKM0CHS		
R/W		R/W				R/W		
Reset		0	0	0		0	0	0

19Dh.6~4 **TKM1CHS**: TK module1 Channel Select

000: TK0 (PB0) 001: TK1 (PB1)
010: TK2 (PB2) 011: TK3 (PB3)
100: TK4 (PB4) 101: TK5 (PB5)
110: TK6 (PB6) 111: TK7 (PB7)

19Dh.2~0 **TKM0CHS**: TK module0 Channel Select

000: TK8 (PC0) 001: TK9 (PC1)
010: TK10 (PC2) 011: TK11 (PC3)
100: TK12 (PA2) 101: TK13 (PA3)
110: TK14 (PA4) 111: TK15 (PA7)

19Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKMCHS1						TKM2CHS		
R/W						R/W		
Reset						0	0	0

19Eh.2~0 **TKM2CHS**: TK module2 Channel Select

000: TK16 (PD0)　　001: TK17 (PD1)

010: TK18 (PD2)　　011: TK19 (PD3)

100: TK20 (PD4)　　101: TK21 (PD5)

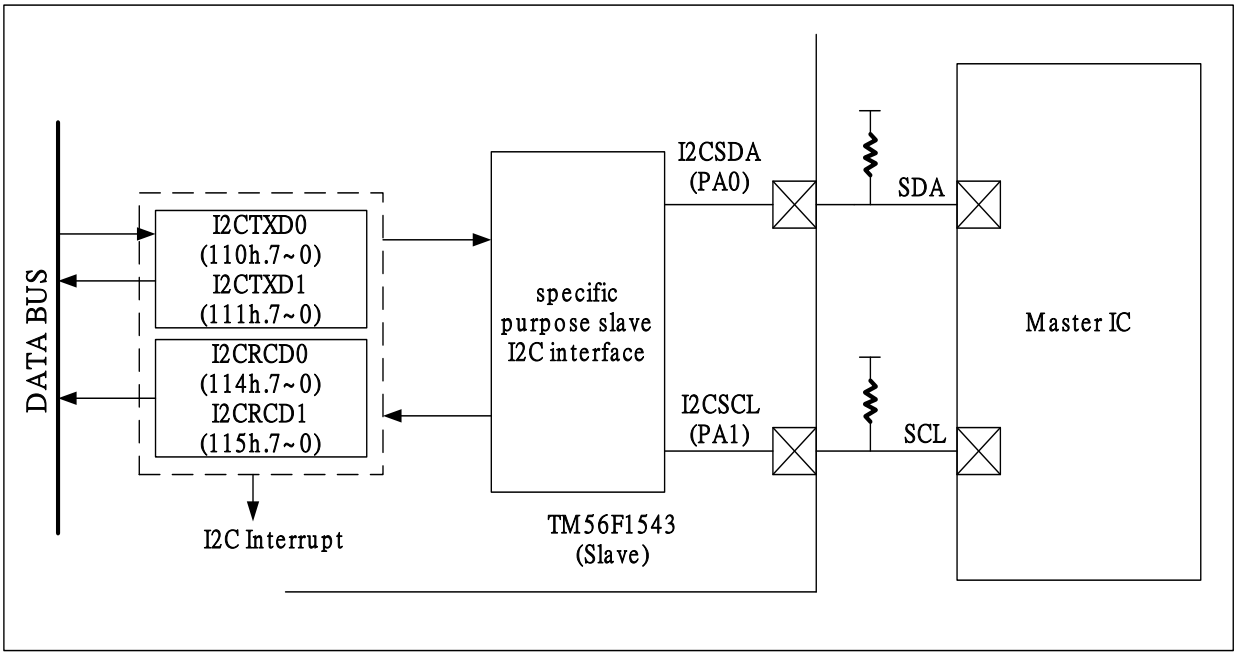
110: TK22 (PD6)　　111: TK23 (PD7)/(TKREF)

19Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTRLRFK	CTRLRFK							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

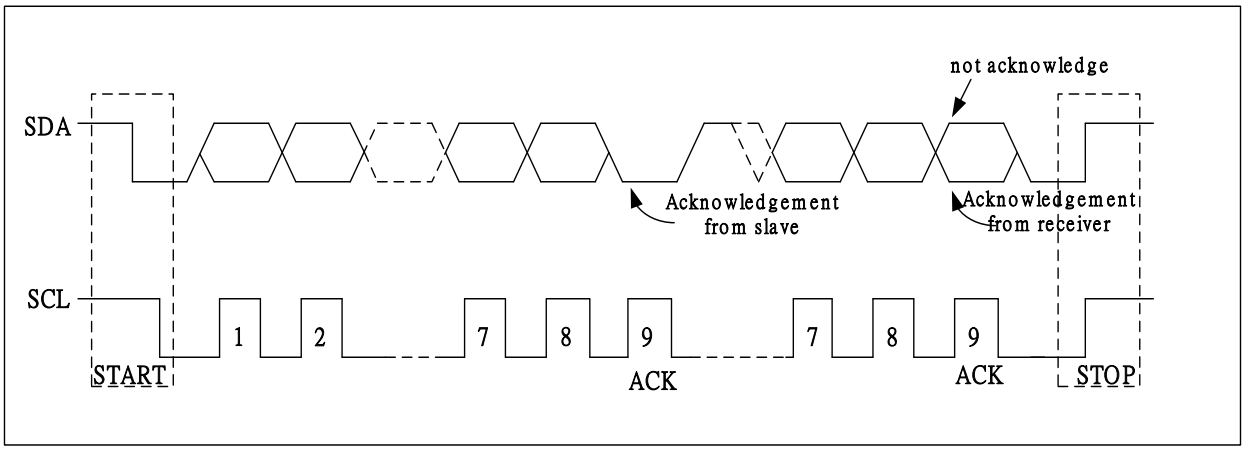
19Fh.7~0 **CTRLRFK**: TK module2 Reference Key(TK23) Capacitor Control

6.9 Specific Purpose Slave I2C Interface

Specific purpose slave I2C interface in TM56F1543 could be used for data transmission. This interface is based on a standard I2C (Inter-Integrated Circuit), and TM56F1543 is always as a slave mode. When the master node (another IC or device) sends the correct ID through I2C, it can read data from the register I2CTXD0 (110h.7~0) and I2CTXD1 (111h.7~0) of TM56F1543 or write data to the register I2CRCD0 (114h.7~0) and I2CRCD1 (115h.7~0) of TM56F1543.

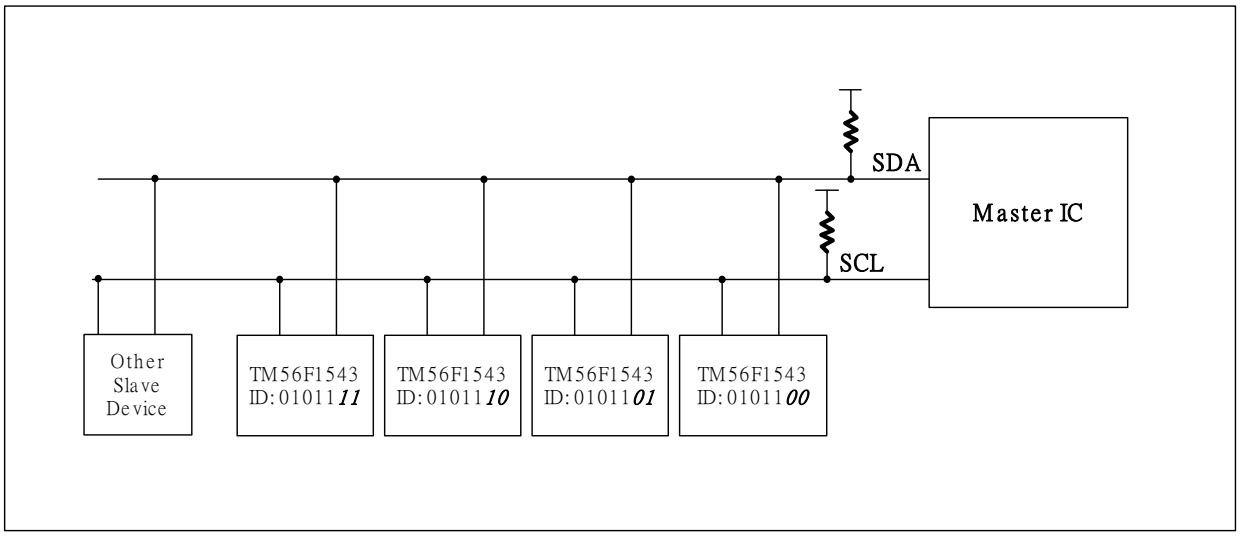


Slave I2C Interface Block Diagram

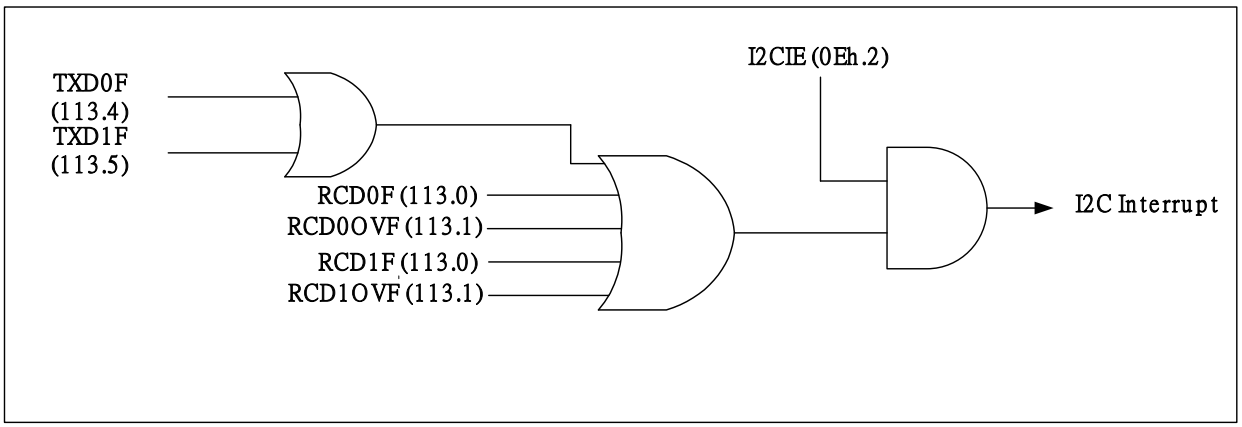


I2C Protocol

To use the slave I2C interface, the I2CEN (112h.3) bit has to be set. TM56F1543 supports 4 slave device IDs by setting I2CID (112.1~0). TM56F1543 can generate the transmitting flag TXD0F (113h.4) and TXD1F (113h.5) when data transmitting finished. It generates the receiving flag RCD0F (113h.0) and RCD1F (113h.2) when data receiving finished. It can also generates the receiving overflow flag RCD0OVF (113h.1) and RCD1OVF (113h.3) when data receiving finished but the receiving flag is not cleared. If one of those I2C flags is set, the I2C interrupt flag I2CIF (1Ah.2) will be generated. It generates I2C interrupt if the I2CIE (0Eh.2) bit is set. Refer to following table and figure.

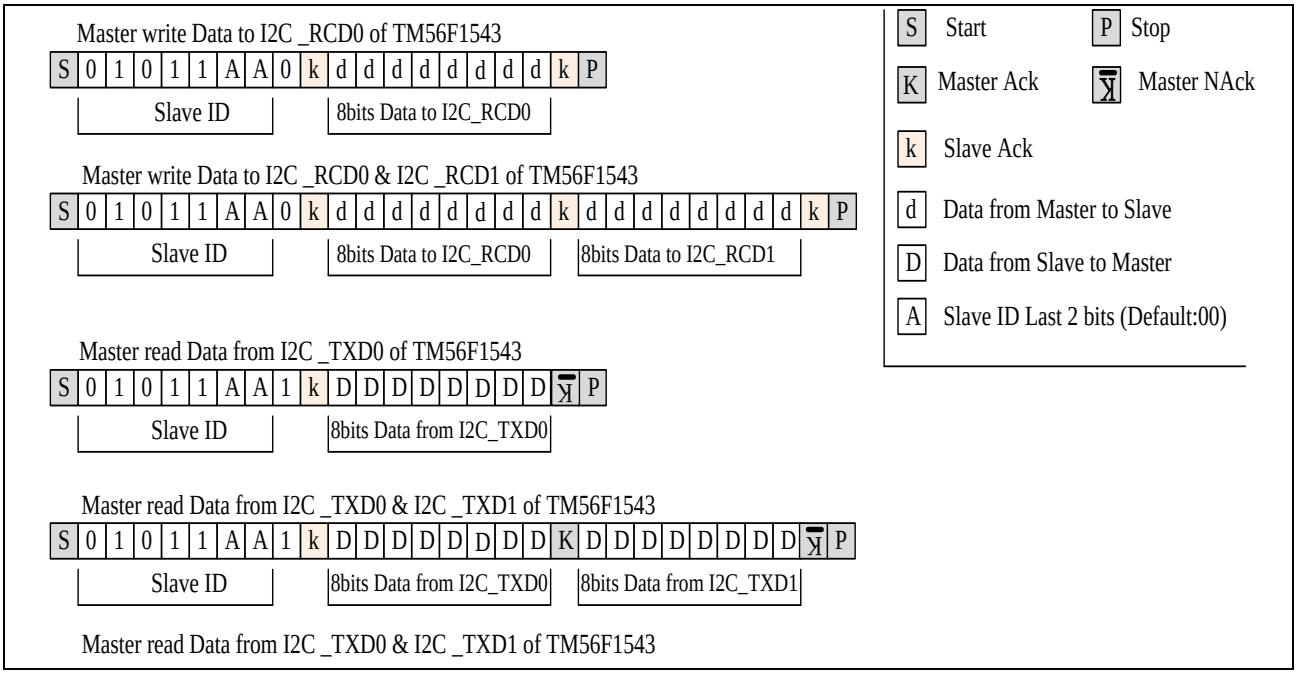


I2C Parallel Connection Application Circuit



Slave I2C Interrupt Block Diagram

RCDxOVF	RCDxF	I2CIF	STATE
0	0	0	IDLE
0	1	1	Date received to I2CRCDx register
1	1	1	Data overflow occurred at I2CRCDx register



TM56F1543 I2C Commands

0Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE1	LVDIE				TKIE	I2CIE	UARTIE	PXIE
R/W	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

INTIE1.2 **I2CIE:** Slave I2C interrupt enable
0: disable
1: enable

1Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF1	LVDIF	TKM2IF	TKM1IF	TKM0IF	TKIF	I2CIF	UARTIF	PXIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

1Ah.2 **I2CIF:** Slave I2C interrupt pending flag; refer to 113h (I2CFLG)
This bit is set by H/W while

- ✧ I2CRCD0 or I2CRCD1 receive data finished
- ✧ I2CRCD0 or I2CRCD1 data overflow occurred
- ✧ I2CTXD0 or I2CTXD1 data transmit finished

Write 0 to this bit will clear this flag and slave I2C related flags.

110h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CTXD0	I2CTXD0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

110h.7~0 **I2CTXD0:** The transmitting register 0 of slave I2C

111h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CTXD1	I2CTXD1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

111h.7~0 **I2CTXD1:** The transmitting register 1 of slave I2C

112h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CCTL	-	-	-	-	I2CEN	-	I2CID	
R/W	-	-	-	-	R/W	-	R/W	
Reset	-	-	-	-	0	-	0	0

112h.3 **I2CEN:** Slave I2C interface enable
0: disable
1: enable

112h.1~0 **I2CID:** Slave I2C ID last 2 bits

113h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CFLG	-	-	TXD1F	TXD0F	RCD1OVF	RCD1F	RCD1OVF	RCD0F
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	0	0	0	0	0	0

113h.5 **TXD1F:** Slave I2C transmitting data register 1 flag
This bit is set by H/W while I2CTXD1 data transmitting finished, write 0 to this bit will clear this flag

113h.4 **TXD0F:** Slave I2C transmitting data register 0 flag
This bit is set by H/W while I2CTXD0 data transmitting finished, write 0 to this bit will clear this flag

113h.3 **RCD1OVF:** Slave I2C receiving data register 1 overflow
This bit is set by H/W while receiving data to I2CRCD1 overflow, write 0 to this bit will clear this flag

113h.2 **RCD1F:** Slave I2C receiving data register 1 flag
This bit is set by H/W while data receiving to I2CRCD1 finished, write 0 to this bit will clear this flag

113h.1 **RCD0OVF:** Slave I2C receiving data register 0 overflow
This bit is set by H/W while receiving data to I2CRCD0 overflow, write 0 to this bit will clear this flag

113h.0 **RCD0F:** Slave I2C receiving data register 0 flag
This bit is set by H/W while data receiving to I2CRCD0 finished, write 0 to this bit will clear this flag

114h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CRCD0	I2CRCD0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

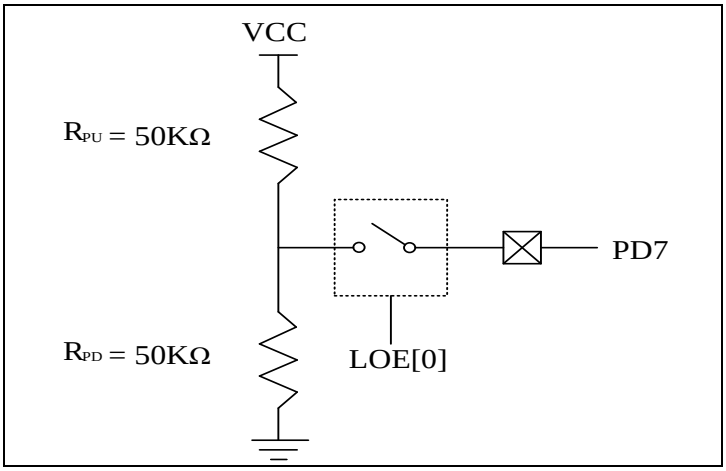
114h.7~0 **I2CRCD0:** The receiving register 0 of slave I2C

115h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I2CRCD1	I2CRCD1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

115h.7~0 **I2CRCD1:** The receiving register 1 of slave I2C

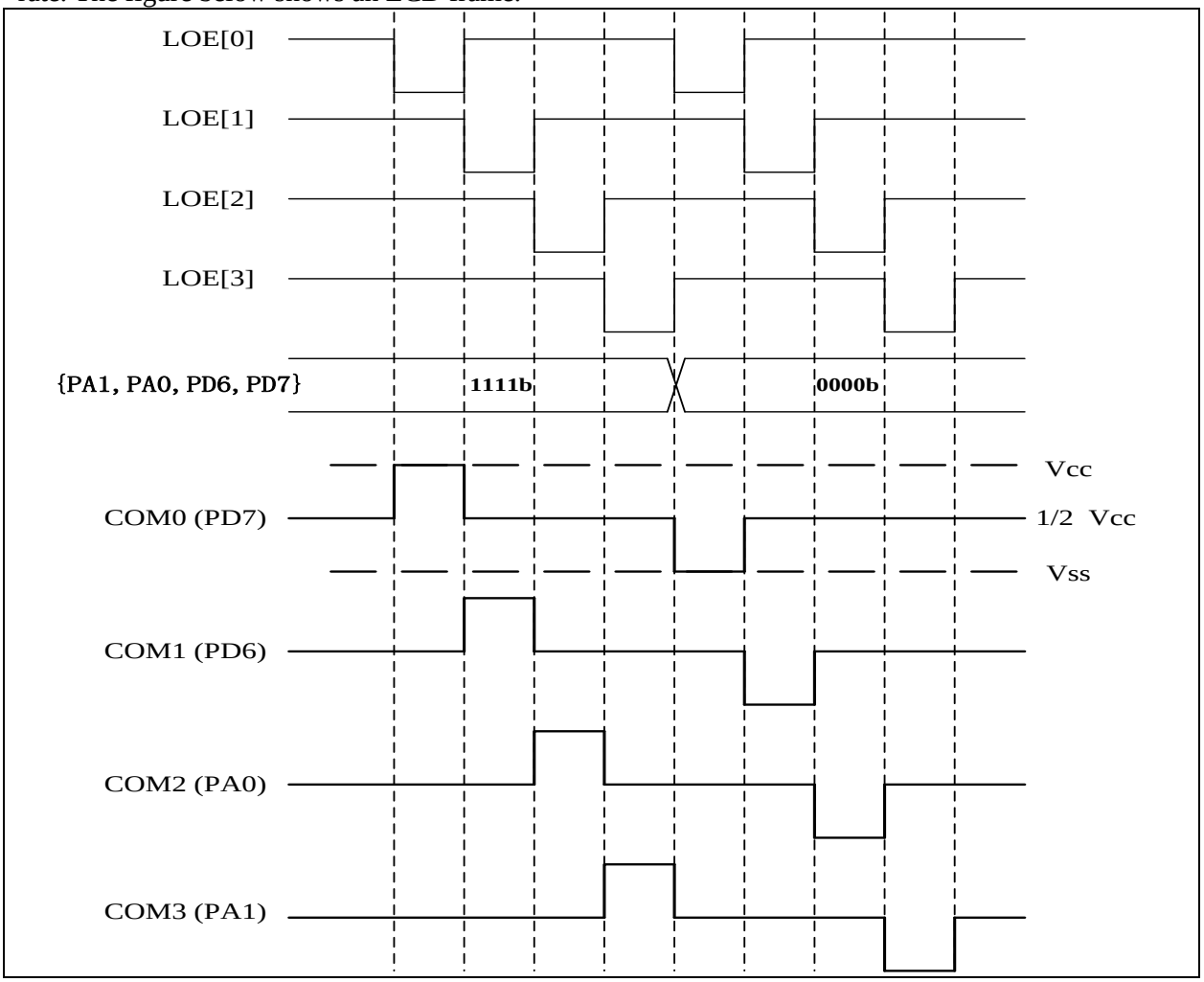
6.10 S/W Control LCD Driver

The chip support an S/W controlled method to driving LCD. Four IO pins can be the Common Pins. The four pin are PA0, PA1, PD6 and PD7. Common pins are capable of driving 1/2 bias by setting the register LOE. The COM0 circuit is shown below.

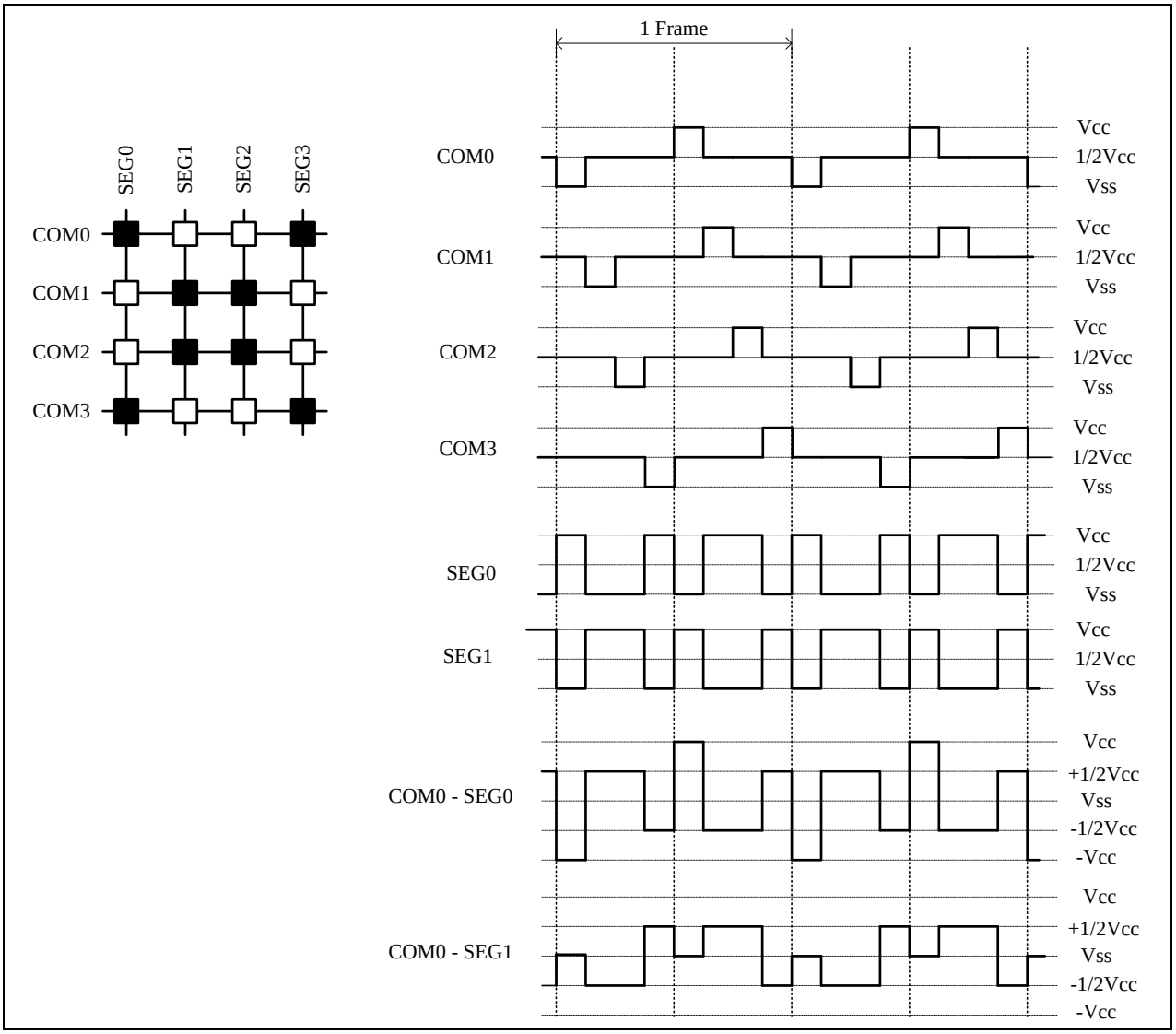


LCD COM0 Circuit

The frequency of any repeating waveform output on the COM pin can be used to represent the LCD frame rate. The figure below shows an LCD frame.



S/W Controlled LCD COM0 ~ COM3 Scanning

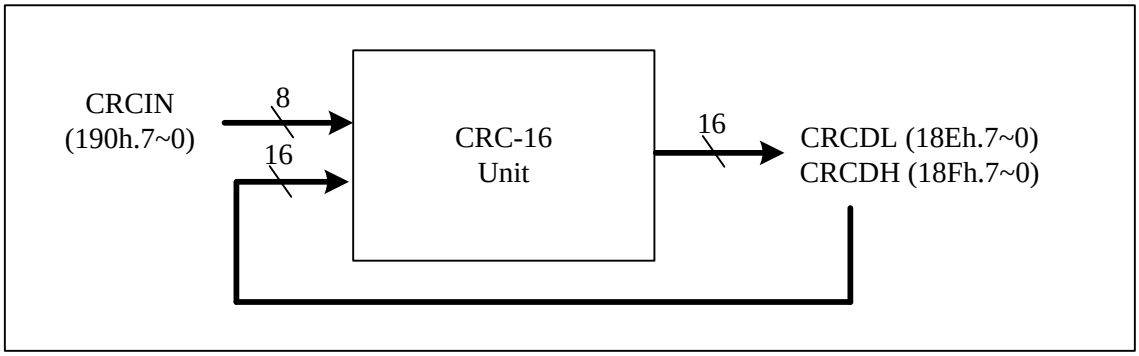


108h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LOE					LOE			
R/W					R/W			
Reset					0	0	0	0

108h.3~0 **LOE:** COM0~COM3 LCD 1/2 bias output enable control
0001: COM0 (PD7) Enable
0010: COM1 (PD6) Enable
0100: COM2 (PA0) Enable
1000: COM3 (PA1) Enable

6.11 Cyclic Redundancy Check (CRC)

The chip supports an integrated 16-bit Cyclic Redundancy Check function. The Cyclic Redundancy Check (CRC) calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. The CRC calculation takes an 8-bit data stream or a block of data as input and generates a 16-bit output remainder. The data stream is calculated by the same generator polynomial.



CRC16 Block Diagram

The CRC generator provides the 16-bit CRC result calculation based on the CRC-16-IBM polynomial. In this CRC generator, there is only one polynomial available for the numeric values calculation. It can't support the 16-bit CRC calculations based on any other polynomials. Each write operation to the CRCIN register creates a combination of the previous CRC value stored in the CRCDH and CRCDL registers. It will take one MCU instruction cycle to calculate.

CRC-16-IBM (Modbus) Polynomial representation: $X^{16} + X^{15} + X^2 + 1$

18Eh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDL	CRCDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

18Eh.7~0 **CRCDL**: 16-bit CRC checksum data bit 7~0

18Fh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDH	CRCDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

18Fh.7~0 **CRCDH**: 16-bit CRC checksum data bit 15~8

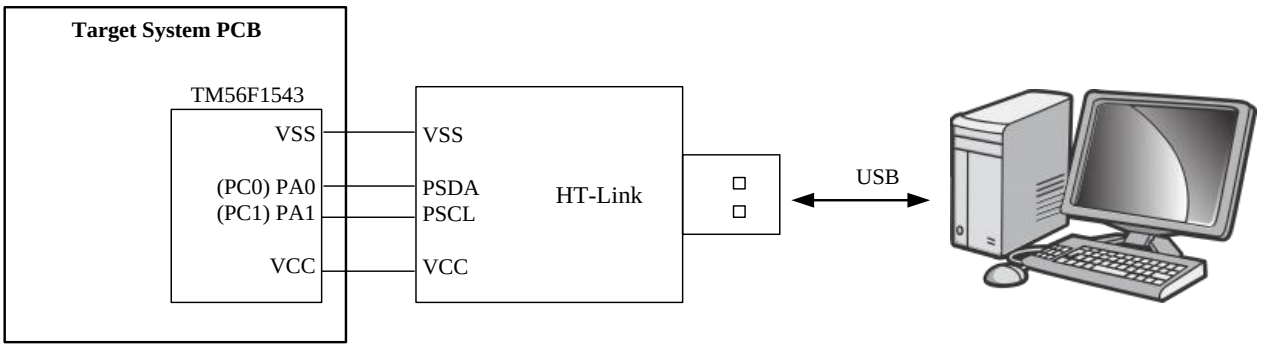
190h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCIN	CRCIN							
R/W	W							
Reset	-	-	-	-	-	-	-	-

190h.7~0 **CRCIN**: CRC data input, write this register to start CRC calculation

6.12 In Circuit Emulation (ICE) Mode

This device can support the In Circuit Emulation Mode. To use ICE Mode, user needs to connect PA0 and PA1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

- ✧ The device must be un-protect.
- ✧ The device's PA0 and PA1 pins must work in input Mode.
- ✧ The HT-Link communication Pin's function cannot be emulated.
- ✧ The PA0 and PA1 pins can be replaced by PC0 and PC1 (only in ICE Mode)
- ✧ The VCC level is controlled by HT-Link module.



MEMORY MAP

Name	Address	R/W	Rst	Description
INDF (00h/80h/100h/180h)				**Function related to: RAM W/R**
INDF	00.7~0	R/W	-	Not a physical register, addressing INDF actually point to the register whose address is contained in the FSR register
TM0 (01h/101h)				**Function related to: Timer0**
TM0	01.7~0	R/W	0	Timer0 content
PCL (02h/82h/105h/182h)				**Function related to: PROGRAM COUNT**
PCL	02.7~0	R/W	0	Programming Counter LSB [7~0]
STATUS (03h/83h/103h/183h)				**Function related to: STATUS**
IRP	03.7	R/W	0	Register Bank Select bit (used for indirect addressing)
RP1	03.6	R/W	0	Register Bank Select bit 1 (used for direct addressing)
RP0	03.5	R/W	0	Register Bank Select bit 0 (used for direct addressing)
TO	03.4	R	0	WDT timeout flag, cleared by PWRST, ‘SLEEP’ or ‘CLRWDT’ instruction
PD	03.3	R	0	Power down flag, set by ‘SLEEP’, cleared by ‘CLRWDT’ instruction
Z	03.2	R/W	0	Zero flag
DC	03.1	R/W	0	Decimal Carry flag
C	03.0	R/W	0	Carry flag
FSR (04h/84h/104h/184h)				**Function related to: RAM W/R**
FSR	04.7~0	R/W	-	File Select Register, indirect address mode pointer
PAD (05h)				**Function related to: Port A**
PAD	05.7~0	R	-	Port A pin or “data register” state
		W	FF	Port A output data register
PBD (06h)				**Function related to: Port B**
PBD	06.7~0	R	-	Port B pin or “data register” state
		W	FF	Port B output data register
PCD (07h)				**Function related to: Port C**
PCD	07.3~0	R	-	Port C pin or “data register” state
		W	FF	Port C output data register
PDD (08h)				**Function related to: Port D**
PDD	08.7~0	R	-	Port D pin or “data register” state
		W	FF	Port D output data register
INDF1 (09h/89h/109h/189h)				**Function related to: RAM (BANK4/5) W/R**
INDF1	09.7~0	R/W	0	Not a physical register, addressing INDF1 actually point to the register whose address is contained in the FSR1 register
PCLATH (0Ah/8Ah/10Ah/18Ah)				**Function related to: PROGRAM COUNT**
PCLATH	0A.4~0	R/W	0	Write Buffer for the upper 5 bits of the Program Counter

Name	Address	R/W	Rst	Description
INTIE (0Bh/8Bh/10Bh/18Bh)				**Function related to: Interrupt Enable**
ADCIE	0B.7	R/W	0	ADC interrupt enable, 1=enable, 0=disable
T2IE	0B.6	R/W	0	T2 interrupt enable, 1=enable, 0=disable
TM1IE	0B.5	R/W	0	Timer1 interrupt enable, 1=enable, 0=disable
TM0IE	0B.4	R/W	0	Timer0 interrupt enable, 1=enable, 0=disable
WKTIE	0B.3	R/W	0	Wakeup Timer interrupt enable, 1=enable, 0=disable Set 0 to clear & disable WKT timer
INT2IE	0B.2	R/W	0	INT2 pin (PA7) interrupt enable, 1=enable, 0=disable
INT1IE	0B.1	R/W	0	INT1 pin (PA4) interrupt enable, 1=enable, 0=disable
INT0IE	0B.0	R/W	0	INT0 pin (PA0) interrupt enable, 1=enable, 0=disable
INTIF (0Ch)				**Function related to: Interrupt Flag**
ADCIF	0C.7	R	-	ADC interrupt flag, set by H/W after end of ADC conversion
		W	0	write 0: clear this flag; write 1: no action
T2IF	0C.6	R	-	T2 interrupt event pending flag, set by H/W while T2 overflows
		W	0	write 0: clear this flag; write 1: no action
TM1IF	0C.5	R	-	Timer1 interrupt event pending flag, set by H/W while Timer1 overflows
		W	0	write 0: clear this flag; write 1: no action
TM0IF	0C.4	R	-	Timer0 interrupt event pending flag, set by H/W while Timer0 overflows
		W	0	write 0: clear this flag; write 1: no action
WKTIF	0C.3	R	-	WKT interrupt event pending flag, set by H/W while WKT time out
		W	0	write 0: clear this flag; write 1: no action
INT2IF	0C.2	R	-	INT2 (PA7) interrupt event pending flag, set by H/W at INT2 pin's falling edge
		W	0	write 0: clear this flag; write 1: no action
INT1IF	0C.1	R	-	INT1 (PA4) interrupt event pending flag, set by H/W at INT1 pin's falling/rising edge
		W	0	write 0: clear this flag; write 1: no action
INT0IF	0C.0	R	-	INT0 (PA0) interrupt event pending flag, set by H/W at INT0 pin's falling/rising edge
		W	0	write 0: clear this flag; write 1: no action
FSR1 (0Dh)				**Function related to: RAM (BANK4/5) W/R**
FSR1	0D.7~0	R/W	-	File Select 1 Register, indirect address mode pointer
INTIE1 (0Eh)				**Function related to: Interrupt Enable Group 1**
LVDIE	0E.7	R/W	0	LVD interrupt enable, 0=disable , 1=enable
TKIE	0E.3	R/W	0	TK interrupt enable, 0=disable , 1=enable
I2CIE	0E.2	R/W	0	I2C interrupt enable, 0=disable , 1=enable
UARTIE	0E.1	R/W	0	UART TX/RX interrupt enable, 0=disable , 1=enable
PXIE	0E.0	R/W	0	Pin change interrupt enable, 0=disable , 1=enable

Name	Address	R/W	Rst	Description
CLKCTL (0Fh)				**Function related to: Fsys**
SCKTYPE	0F.7	R/W	0	Slow-clock type 0: SIRC 1: SXT
FCKTYPE	0F.6	R/W	0	Fast-clock type 0: FIRC 1: FXT
SLOWSTP	0F.4	R/W	0	Stop Slow-clock in Stop Mode 0: no Stop 1: Stop
FASTSTP	0F.3	R/W	1	Stop Fast-clock 0:no Stop 1:Stop
CPUCKS	0F.2	R/W	0	Select Fast-clock 0: Fsys=Slow-clock 1: Fsys=Fast-clock
CPUPSC	0F.1~0	R/W	11	Fsys Prescaler, 0: div 8, 1: div 4, 2: div 2, 3: div 1
TM0RLD (10h)				**Function related to: TM0**
TM0RLD	10.7~0	R/W	0	Timer0 reload Data
TM0CTL (11h)				**Function related to: TM0**
T0ISRC	11.7	R/W	0	Timer0 Counter mode source 0: TM0CKI pin (PA2) 1: SXT divided 16
TM0STP	11.6	R/W	0	Timer0 counter stop 0: Release 1: Stop counting
TM0EDG	11.5	R/W	0	Timer0 prescaler counting edge for TM0CKI pin 0: rising edge 1: falling edge
TM0CKS	11.4	R/W	0	Timer0 prescaler clock source 0: Fsys/2 1: TM0CKI pin (PA2 pin)
TM0PSC	11.3~0	R/W	0	Timer0 prescaler. Timer0 prescaler clock source divided by 0000: /1 0101: /32 1010: /1024 1111: /32768 0001: /2 0110: /64 1011: /2048 0010: /4 0111: /128 1100: /4096 0011: /8 1000: /256 1101: /8192 0100: /16 1001: /512 1110: /16384
TM1 (12h)				**Function related to: Timer1**
TM1	12.7~0	R/W	0	Timer1 content
TM1RLD (13h)				**Function related to: Timer1**
TM1RLD	13.7~0	R/W	0	Timer1 reload Data
TM1CTL (14h)				**Function related to: Timer1**
TM1STP	14.4	R/W	0	Timer1 counter stop 0: Release 1: Stop counting
TM1PSC	14.3~0	R/W	0	Timer1 prescaler. Timer1 clock source 0000: Fsys/2 0001: Fsys/4 0010: Fsys/8 0011: Fsys/16 0100: Fsys/32 0101: Fsys/64 0110: Fsys/128 0111: Fsys/256 1xxx: Fsys/512
T2CTL (15h)				**Function related to: T2**
T2CLR	15.3	R/W	1	T2 counter clear 0: Release 1: Stop counting
T2CKS	15.2	R/W	0	T2 clock source selection. 1: Fsys/128 0: Slow-clock
T2PSC	15.1~0	R/W	0	T2 prescaler. T2 clock source divided by - 00: 32768 01: 16384 10: 8192 11: 128

Name	Address	R/W	Rst	Description
LVCTL (16h)				**Function related to: LVR/LVD**
LVDF	16.7	R	-	Low voltage detection flag, set by H/W while Vcc ≦ LVD
LVRSAV	16.5	R/W	1	LVR/LVD power save 1: LVR/LVD auto power off in STOP/IDLE mode 0: LVR/LVD enable in STOP/IDLE mode
LVDSAV	16.4	R/W	1	LVD auto power off in STOP/IDLE mode 0= LVD enable 1= LVD enable in slow/Fast mode; disable in STOP/IDLE mode
LVDS	16.3~0	R/W	01	LVD select; 0000: Disable, 0001: 2.19V, …. 1111: 4.15V
ADCDH (17h)				**Function related to: ADC**
ADCDH	17.7~0	R	-	ADC output data MSB, ADQ [11:4]
ADCTL (18h)				**Function related to: ADC**
ADCDL	18.7~4	R	-	ADC output data LSB, ADQ [3:0]
ADST	18.3	R/W	0	ADC start bit. 0: H/W clear after end of conversion 1: ADC start conversion
ADCKS	18.2~0	R/W	0	ADC clock frequency selection: 000: Fsys/256 100: Fsys/16 001: Fsys/128 101: Fsys/8 010: Fsys/64 110: Fsys/4 011: Fsys/32 111: Fsys/2 (TC)
ADCTL2 (19h)				**Function related to: ADC**
BGEN	19.7	R/W	1	Band Gap BG1.25V enable 0: Disable 1: Enable and Auto disable in STOP/IDLE mode
ADCVREFS	19.5	R/W	0	ADC VREF select, 00: VCC, 01: 2.5V
ADCHS	19.4~0	R/W	0	ADC channel select ADC channel select 00000: ADC0 (PB0) 00001: ADC1 (PB1) 00010: ADC2 (PB2) 00011: ADC3 (PB1) 00100: ADC4 (PC0) 00101: ADC5 (PC1) 00110: ADC6 (PC2) 00111: ADC7 (PC3) 01000: ADC8 (PD0) 01001: ADC9 (PD1) 01010: ADC10(PD2) 01011: ADC11(PD3) 01100: ADC12(PD4) 01101: ADC13(PD5) 01110: VBGO 10111: 1/4 VCC others: reserved

Name	Address	R/W	Rst	Description
INTIF1 (1Ah)				**Function related to: Interrupt Flag**
LVDIF	1A.7	R/W	0	LVD interrupt event pending flag, set by H/W while LV Detected write 0: clear this flag; write 1: no action
TKM2IF	1A.6	R/W	0	STK Module2 Interrupt event pending flag set by H/W at the STK module2 end of conversion S/W writes 0 to TKM2IF or sets the TKM2SOC bit to clear this flag.
TKM1IF	1A.5	R/W	0	STK Module1 Interrupt event pending flag set by H/W at the STK module1 end of conversion S/W writes 0 to TKM1IF or sets the TKM1SOC bit to clear this flag.
TKM0IF	1A.4	R/W	0	STK Module0 Interrupt event pending flag set by H/W at the STK module0 end of conversion S/W writes 0 to TKM0IF or sets the TKM0SOC bit to clear this flag.
TKIF	1A.3	R/W	0	Touch Key interrupt event pending flag, set by H/W at the end of All Touch Key conversion S/W writes 0 to TKIF or sets the TKMxSOC bit to clear this flag.
I2CIF	1A.2	R/W	0	Slave I2C interrupt pending flag This bit is set by H/W while ✧ I2CRCD0 or I2CRCD1 receive data finished ✧ I2CRCD0 or I2CRCD1 data overflow occurred ✧ I2CTXD0 or I2CTXD1 data transmit finished. Write 0 to clear this flag
UARTIF	1A.1	R/W	0	UART Interrupt Flag, set by H/W while TX/RX transfers complete; F/W write 0 to clear this flag
PXIF	1A.0	R/W	0	Port A/B/C/D Pin Change Interrupt Flag F/W write 0 to clear this flag;
IOCCTRL (1Bh)				**Function related to: IO Port**
LED	1B.7~4	R/W	0	IO current Control for LED usage enable LED[3]: PD port LED[2]: PC port LED[1]: PB port LED[0]: PA port 1: enable, 0 disable
HSNK	1B.3~0	R/W	0	IO current Control for High Sink usage enable HSNK[3]: PD port HSNK[2]: PC port HSNK[1]: PB port HSNK[0]: PA port 1: enable, 0: disable
PAWKE (1Ch)				**Function related to: Port A**
PAWKE	1C.7~0	R/W	0	PA pin Individual Wake up Enable 0: disable 1: enable
PBWKE (1Dh)				**Function related to: Port B**
PBWKE	1D.7~0	R/W	0	PB pin Individual Wake up Enable 0: disable 1: enable
PCWKE (1Eh)				**Function related to: Port C**
PCWKE	1E.7~0	R/W	0	PC pin Individual Wake up Enable 0: disable 1: enable

Name	Address	R/W	Rst	Description
PDWKE (1Fh)				**Function related to: Port D**
PDWKE	1F.7~0	R/W	0	PD pin Individual Wake up Enable 0: disable 1: enable
User Data Memory				
RAM	20~6F	R/W	-	RAM Bank0 area (80 Bytes)
RAM	70~7F	R/W	-	RAM common area (16 Bytes)

Name	Address	R/W	Rst	Description
OPTION (81h/181h)				**Function related to: STATUS/INT0/INT1/WDT/WKT**
HWAUTO	81.7	R/W	0	Enter interrupt vector, HW auto save/restore WREG and STATUS w/o TO, PD 0:disable 1: Enable ; (work for ASM not for C)
INT0EDG	81.6	R/W	0	INT0 pin edge interrupt event 0: falling edge to trigger 1: rising edge to trigger
INT1EDG	81.5	R/W	0	INT1 pin edge interrupt event 0: falling edge to trigger 1: rising edge to trigger
FREQL	81.4	R/W	1	SIRC Frequency selection 0: 60KHz 1: 50KHz
WDTPSC	81.3~2	R/W	11	WDT pre-scale selections: 00: 164mS 01: 328mS 10: 655mS 11: 1311mS
WKTPSC	81.1~0	R/W	11	WKT pre-scale selections: 00: 21mS 01: 41mS 10: 82mS 11: 164mS
PAMODH (85h)				**Function related to: Port A**
PA7MOD	85.7~6	R/W	01	PA7, PA4 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PA4MOD	85.1~0	R/W	01	
PAMODL (86h)				**Function related to: Port A**
PA3MOD	86.7~6	R/W	01	PA3~PA0 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PA2MOD	86.5~4	R/W	01	
PA1MOD	86.3~2	R/W	01	
PA0MOD	86.1~0	R/W	01	
PBMODH (87h)				**Function related to: Port B**
PB7MOD	87.7~6	R/W	01	PB7~PB4 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PB6MOD	87.5~4	R/W	01	
PB5MOD	87.3~2	R/W	01	
PB4MOD	87.1~0	R/W	01	
PBMODL (88h)				**Function related to: Port B**
PB3MOD	88.7~6	R/W	01	PB3~PB0 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PB2MOD	88.5~4	R/W	01	
PB1MOD	88.3~2	R/W	01	
PB0MOD	88.1~0	R/W	01	
PCMODL (8Ch)				**Function related to: Port C**
PC3MOD	8C.7~6	R/W	01	PC3~PC0 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PC2MOD	8C.5~4	R/W	01	
PC1MOD	8C.3~2	R/W	01	
PC0MOD	8C.1~0	R/W	01	

Name	Address	R/W	Rst	Description
PDMODH (8Dh)				**Function related to: Port D**
PD7MOD	8D.7~6	R/W	01	PD7~PD4 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PD6MOD	8D.5~4	R/W	01	
PD5MOD	8D.3~2	R/W	01	
PD4MOD	8D.1~0	R/W	01	
PDMODL (8Eh)				**Function related to: Port D**
PD3MOD	8E.7~6	R/W	01	Pd3~PD0 I/O mode control 00: Mode0 01: Mode1 10: Mode2 11: Mode3
PD2MOD	8E.5~4	R/W	01	
PD1MOD	8E.3~2	R/W	01	
PD0MOD	8E.1~0	R/W	01	
OPTION2 (8Fh)				**Function related to: PWM0/PWM1**
TCOE	8F.7	R/W	0	TCOUT Output Enable 0: Disable 1: Enable, output to PB1
TM1OE	8F.6	R/W	0	Timer1 overflow toggle Output Enable 0: Disable 1:Enable, output to PB0
PWMCKS	8F.5~4	R/W	0	PWM0 Clock Source 0x: Fsys 10:FIRC 11:FIRC*2
INT2SEL	8F.2	R/W	0	INT2 Pin Select 0: PA7 1: PB7
INT1SEL	8F.1	R/W	0	INT1 Pin Select 0: PA4 1: PB4
INT0SEL	8F.0	R/W	0	INT0 Pin Select 0: PA0 1: PB0
PWMOE (90h)				**Function related to: PWM0/PWM1**
PWM0POE	90.7	R/W	0	PWM0P Output Enable to PA7 0: disable 1: enable
PWM0NOE	90.6	R/W	1	PWM0N Output Enable to PA0 0: disable 1: enable
PWM5OE	90.5	R/W	1	PWM5 Output Enable to PA7 0: disable 1: enable (PWM0POE has higher priority)
PWM4OE	90.4	R/W	1	PWM4 Output Enable to PA4 0: disable 1: enable
PWM3OE	90.3	R/W	1	PWM3 Output Enable to PA3 0: disable 1: enable
PWM2OE	90.2	R/W	0	PWM2 Output Enable to PA2 0: disable 1: enable
PWM1OE	90.1	R/W	0	PWM1 Output Enable to PA1 0: disable 1: enable

Name	Address	R/W	Rst	Description
PWMCTL (91h)				**Function related to: PWM**
PWMEN	91.7	R/W	0	PWM Clock Enable 0: Disable 1: Enable
PWM0OM	91.5~4	R/W	0	PWM0 output mode 00~11: Mode0 ~Mode3
PWM0DZ	91.3~0	R/W	0	PWM0 dead zone (non-overlap) 0000~1111: 0~14, 16 *Tpwmclk
PWMPRDH (92h)				**Function related to: PWM**
PWMPRDH	92.7~0	R/W	0	PWM Period MSB data
PWMPRDL (93h)				**Function related to: PWM**
PWMPRDL	93.7~0	R/W	0	PWM Period LSB data
PWM0DH (94h)				**Function related to: PWM**
PWM0DH	94.7~0	R/W	0	PWM0 DutyMSB data
PWM0DL (95h)				**Function related to: PWM**
PWM0DL	95.7~0	R/W	0	PWM0 Duty LSB data
PWM1DH (96h)				**Function related to: PWM**
PWM1DH	96.7~0	R/W	0	PWM1 Duty MSB data
PWM1DL (97h)				**Function related to: PWM**
PWM1DL	97.7~0	R/W	0	PWM1 Duty LSB data
PWM2DH (98h)				**Function related to: PWM**
PWM2DH	98.7~0	R/W	0	PWM2 Duty MSB data
PWM2DL (99h)				**Function related to: PWM**
PWM2DL	99.7~0	R/W	0	PWM2 Duty LSB data
PWM3DH (9Ah)				**Function related to: PWM**
PWM3DH	9A.7~0	R/W	0	PWM3 Duty MSB data
PWM3DL (9Bh)				**Function related to: PWM**
PWM3DL	9B.7~0	R/W	0	PWM3 Duty LSB data
PWM4DH (9Ch)				**Function related to: PWM**
PWM4DH	9C.7~0	R/W	0	PWM4 Duty MSB data
PWM4DL (9Dh)				**Function related to: PWM**
PWM4DL	9D.7~0	R/W	0	PWM4 Duty LSB data
PWM5DH (9Eh)				**Function related to: PWM**
PWM5DH	9E.7~0	R/W	0	PWM5 Duty MSB data
PWM5DL (9Fh)				**Function related to: PWM**
PWM5DL	9F.7~0	R/W	0	PWM5 Duty LSB data
User Data Memory				
RAM	A0~EF	R/W	-	RAM Bank1area (80 Bytes)

Name	Address	R/W	Rst	Description
TSTREG (105h)				**Function related to: TEST**
TSTREG	105.7~0	R/W	03	Test bits, Keep 03
ChgRdMode (106h)				**Function related to: TEST**
ChgRdMode	105.7~0	W	0	Test bits, Keep 00
LVRPD (107h)				**Function related to: LVR**
LVRPD	107	W	0	LVR power down control Write 0x37 to force LVR+POR disable Write 0x38 to force LVR disable, POR still enable Write 0x39 to force POR disable, LVR still enable Write other value to enable LVR/POR
PORPDF	107.1	R	0	1: when Reg. 107h write 0x37 or 0x39; 0: when Reg. 107h write other value
LVRPDF	107.0	R	0	1: when Reg. 107h write 0x37 or 0x38; 0: when Reg. 107h write other value
LOE (108h)				**Function related to: Software LCD COM**
LOE	108	R/W	0	Software COM3~0 LCD 1/2 bias Output Enable
	108.3	R/W	0	1: PA1 as LCD COM3 1/2 bias Output Enable
	108.2	R/W	0	1: PA0 as LCD COM2 1/2 bias Output Enable
	108.1	R/W	0	1: PD6 as LCD COM1 1/2 bias Output Enable
	108.0	R/W	0	1: PD7 as LCD COM0 1/2 bias Output Enable
PCH (10Ch)				**Function related to: PC**
PCH	10C.4~0	R	0	Program Counter [12:8]
		W	0	Write 1Ch to this register, then it's not necessary to write PCLATCH for table read lookup
UBAUD (10Dh)				**Function related to: UART**
UBAUD	10D	R/W	0	UART Baud Rate divider
BGTRIM (10Eh)				**Function related to: VBG**
BGTRIM	10E.3~0	R/W		VBG voltage adjustment 00h: Lowest voltage Fh: Highest voltage
I2CTXD0 (110h)				**Function related to: Slave I2C**
I2CTXD0	110.7~0	R/W	0	The transmitting register0 of slave I2C
I2CTXD1 (111h)				**Function related to: Slave I2C**
I2CTXD1	111.7~0	R/W	0	The transmitting register1 of slave I2C
I2CCTL (112h)				**Function related to: Slave I2C**
I2CEN	112.3	R/W	0	Slave I2C interface enable 0: Disable 1: Enable
I2CID	112.1~0	R/W	0	Slave I2C ID last 2 bits

Name	Address	R/W	Rst	Description
I2CFLG (113h)				**Function related to: Touch Key Module0**
TXD1F	113.5	R/W	0	Slave I2C transmitting data register 1 flag, set by H/W while I2CTXD1 data transmitting finished Write 0 to clear this flag
TXD0F	113.4	R/W	0	Slave I2C transmitting data register 0 flag, set by H/W while I2CTXD0 data transmitting finished Write 0 to clear this flag
RCD1OVF	113.3	R/W	0	Slave I2C receiving data register 1 overflow, set by H/W while receiving data to I2CRCD1 overflow. Write 0 to clear this flag
RCD1F	113.2	R/W	0	Slave I2C receiving data register 1 flag, set by H/W while I2CRCD1 data receiving finished Write 0 to clear this flag
RCD0OVF	113.1	R/W	0	Slave I2C receiving data register 0 overflows, set by H/W while receiving data to I2CRCD0 overflow. Write 0 to clear this flag
RCD0F	113.0	R/W	0	Slave I2C receiving data register 0 flag, set by H/W while I2CRCD0 data receiving finished Write 0 to clear this flag
I2CRCD0 (114h)				**Function related to: Slave I2C**
I2CRCD0	114.7~0	R	0	The receiving register0 of slave I2C
I2CRCD1 (115h)				**Function related to: Slave I2C**
I2CRCD1	115.7~0	R	0	The receiving register1 of slave I2C
TKM0DL (116h)				**Function related to: Touch Key Module0**
TKM0DL	116.7~0	R	-	STK Module0 Data LSB [7~0]
TKM0DH (117h)				**Function related to: Touch Key Module0**
TKM0DH	117.5~0	R	-	STK Module0 Data MSB [13~8]
TKM1DL (118h)				**Function related to: Touch Key Module1**
TKM1DL	118.7~0	R	-	STK Module1 Data LSB [7~0]
TKM1DH (119h)				**Function related to: Touch Key Module1**
TKM1DH	119.5~0	R	-	STK Module1 Data MSB [13~8]
TKM2DL (11Ah)				**Function related to: Touch Key Module2**
TKM2DL	11A.7~0	R	-	STK Module2 Data LSB [7~0]
TKM2DH (11Bh)				**Function related to: Touch Key Module2**
TKM2DH	11B.5~0	R	-	STK Module2 Data MSB [13~8]
TKMCON0 (11Ch)				**Function related to: Touch Key Module**
TKM1TCP	11C.7~5	R/W	1	TK module1 touch key clock frequency select; 000:slowest, …, 111:fastest
TKM0TCP	11C.4~2	R/W	1	TK module0 touch key clock frequency select; 000:slowest, …, 111:fastest
TKM0FSL	11C.1~0	R/W	0	TK module0 clock(RCK0/TCK0) frequency selection; 00: slowest, …, 11: fastest

Name	Address	R/W	Rst	Description
TKMCON1 (11Dh)				**Function related to: Touch Key Module**
TKM2TCP	11D.7~5	R/W	1	TK module2 touch key clock frequency select; 000:slowest, …, 111:fastest
TKM2FSL	11D.3~2	R/W	0	TK module2 clock(RCK2/TCK2) frequency selection; 00: slowest, …, 11: fastest
TKM1FSL	11D.1~0	R/W	0	TK module1 clock(RCK1/TCK1) frequency selection; 00: slowest, …, 11: fastest
TKMCTL0 (11Eh)				**Function related to: Touch Key Module**
TKM2SOC	11E.6	R/W	0	STK Module2 Start of Conversion, HW clear it while end of conversion
TKM1SOC	11E.5	R/W	0	STK Module1 Start of Conversion, HW clear it while end of conversion
TKM0SOC	11E.4	R/W	0	STK Module0 Start of Conversion, HW clear it while end of conversion
TKM2EOC	11E.2	R	-	STK Module2 End of Conversion
TKM1EOC	11E.1	R	-	STK Module1 End of Conversion
TKM0EOC	11E.0	R	-	STK Module0 End of Conversion
TKMCTL1 (11Fh)				**Function related to: Touch Key Module**
TKMHSEN	11F.7	R/W	0	All STK Module Sensitivity 0: lower sensitivity 1: higher sensitivity
TKM2PD	11F.6	R/W	1	STK Module2 Power Down 0: Touch Key disable Power Down 1: Touch Key enable Power Down
TKM1PD	11F.5	R/W	1	STK Module1 Power Down 0: Touch Key disable Power Down 1: Touch Key enable Power Down
TKM0PD	11F.4	R/W	1	STK Module0 Power Down 0: Touch Key disable Power Down 1: Touch Key enable Power Down
TKM2JMP	11F.2	R/W	0	STK Module2 touch key clock mode 0: fixed frequency 1: auto-change frequency
TKM1JMP	11F.1	R/W	0	STK Module1 touch key clock mode 0: fixed frequency 1: auto-change frequency
TKM0JMP	11F.0	R/W	0	STK Module1 touch key clock mode 0: fixed frequency 1: auto-change frequency
User Data Memory				
RAM	120~16F	R/W	-	RAM Bank2 area (80 Bytes)

Name	Address	R/W	Rst	Description
DPL (185h)				**Function related to: Table Read**
DPL	185.7~0	R/W	0	Table read low address, data ROM pointer (DPTR) low byte
DPH (186h)				**Function related to: Table Read**
DPH	186.4~0	R/W	0	Table read high address, data ROM pointer (DPTR) high byte
UARTCTL (187h)				**Function related to: UART Control**
URTD9	187.7	R/W	0	UART Transmitted 9th bit
UMODE	187.6~5	R/W	0	UART Mode Selection 0: 7-bit, 1: 8-bit, 2: 9-bit, 3: Reserved
UTXE	187.3	R/W	0	UART Transmit Enable 0: Disable 1: Enable
URXE	187.2	R/W	0	UART Receive Enable 0: Disable 1: Enable
UARTE	187.1	R/W	0	UART Function Enable 0: Disable 1: Enable
UINVEN	187.0	R/W	0	UART TX/RX output/input Inversion Enable 0: Disable 1: Enable
UARTSTA (188h)				**Function related to: UART Status and Control**
UTBE	188.7	R	0	0: TX is transmitting 1: TX buffer is empty;
URRD9	188.6	R	0	Received 9th bit
EVEN	188.5	R/W	0	UART Parity ; 0: ODD 1: EVEN,
PRE	188.4	R/W	0	UART Parity addition; 0: Disable 1: Enable,
PRERR	188.3	R/W	0	set to 1 when parity error occurs, F/W write 0 to clear it
OVERR	188.2	R/W	0	set to 1 when overrun error occurs, F/W write 0 to clear it
FMERR	188.1	R/W	0	set to 1 when frame error occurs, F/W write 0 to clear it
URBF	188.0	R/W	0	set to 1 when 1 byte (or 9-bit) is received Read UARTDAT register will clear it to 0
TABR (18Ch)				**Function related to: Table Read**
TABR	18C.7~0	R/W	0	1: TABR write 1 = opcode TABRL 2: TABR write 2 = opcode TABRH 3: after step1 or step2, read TABR to get main ROM table read value after step1, read TABR to get EEPROM value (when EEPEN=E2h) *Table Read for ASM: TABRL/TABRH or TABR* *Table Read for C: using register TABR* ***and it is forbidden to us in interrupt***

Name	Address	R/W	Rst	Description
URDATA (18Dh)				**Function related to: UART DATA**
URDATA	18D.7~0	R/W	0	UART TX/RX Data Buffer
		R	0	from Receive Buffer
		W	0	to Transmit shifter
CRCDL (18Eh)				**Function related to: CRC16**
CRCDL	18E.7~0	R/W	0	CRC16 Data 7~0
CRCDH(18Fh)				**Function related to: CRC16**
CRCDH	18F.7~0	R/W	0	CRC16 Data 15~8
CRCIN(190h)				**Function related to: CRC16**
CRCIN	190.7~0	W	0	CRC input data
EEPCTL (191h)				**Function related to: EEPROM**
EEPTO	191.7	R	0	EEPROM Write Time-out flag
EEPTE	191.1~0	R/W	11	EEPROM Write Time-out enable; 00: Disable; 01:2.5ms; 10:10ms; 11:20.5ms
EEPEN (192h)				**Function related to: EEPROM**
EEPEN	192.7~0	W	0	EEPROM Enable 0xE2: Enable Others: Disable
EEPDT (193h)				**Function related to: EEPROM**
EEPDT	193.7~0	W	0	EEPROM Data to write in
TKM0TMRL (194h)				**Function related to: Touch Key Module0**
TKM0TMRL	194.7~0	R/W	FF	STK Module0 reference counter LSB [7~0]
TKM0TMRH (195h)				**Function related to: Touch Key Module0**
TKM0TMRH	195.5~0	R/W	0	STK Module0 reference counter MSB [13~8]
TKM1TMRL (196h)				**Function related to: Touch Key Module1**
TKM1TMRL	196.7~0	R/W	FF	STK Module1 reference counter LSB [7~0]
TKM1TMRH (197h)				**Function related to: Touch Key Module1**
TKM1TMRH	197.5~0	R/W	0	STK Module1 reference counter MSB [11~8]
TKM2TMRL (198h)				**Function related to: Touch Key Module2**
TKM2TMRL	198.7~0	R/W	FF	STK Module2 reference counter LSB [7~0]
TKM2TMRH (199h)				**Function related to: Touch Key Module2**
TKM2TMRH	199.5~0	R/W	0	STK Module2 reference counter MSB [11~8]
TKM0REFC (19Ah)				**Function related to: Touch Key Module0**
TKM0REFC	19A.7~0	R/W	-	STK Module0 Reference clock capacitor select
TKM1REFC (19Bh)				**Function related to: Touch Key Module1**
TKM1REFC	19B.7~0	R/W	-	STK Module1 Reference clock capacitor select
TKM2REFC (19Ch)				**Function related to: Touch Key Module2**
TKM2REFC	19C.7~0	R/W	-	STK Module2 Reference clock capacitor select

Name	Address	R/W	Rst	Description
TKMCHS0 (19Dh)				**Function related to: Touch Key Module0/1**
TKM1CHS	19D.6~4	R/W	0	STK Module1 Channel Select: 0:TK8 1:TK9 2:TK10 3:TK11 4:TK12 5:TK13 6:TK14 7:TK15
TKM0CHS	19D.2~0	R/W	0	STK Module0 Channel Select: 0:TK0 1:TK1 2:TK2 3:TK3 4:TK4 5:TK5 6:TK6 7:TK7
TKMCHS1 (19Eh)				**Function related to: Touch Key Module2**
TKM2CHS	19E.2~0	R/W	0	STK Module2 Channel Select: 0:TK16 1:TK17 2:TK18 3:TK19 4:TK20 5:TK21 6:TK22 7:TK23
CTRLRFK (19Fh)				**Function related to: Touch Key Module2**
CTRLRFK	19F.7~0	R/W	0	STK module2 Reference Key(TK23) Capacitor Control 0 : minimum capacitor on TK23 FF: maximum capacitor on TK23
User Data Memory				
RAM	1A0~1EF	R/W	-	RAM Bank3 area (80 Bytes)
Indirect Addressing User Data Memory				**Use INDF1/FSR1 to access RAM Bank 4/5**
RAM	20~ 6F	R/W	-	Indirect Addressing RAM Bank4 area (80 Bytes); use **INDF1/FSR1**
RAM	A0~EF	R/W	-	Indirect Addressing RAM Bank5 area (80 Bytes); use **INDF1/FSR1**

INSTRUCTION SET

Each instruction is a 16-bit word divided into an Op Code, which specifies the instruction type, and one or more operands, which further specify the operation of the instruction. The instructions can be categorized as byte-oriented, bit-oriented and literal operations list in the following table.

For byte-oriented instructions, “f” represents the address designator and “d” represents the destination designator. The address designator is used to specify which address in Program memory is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If “d” is “0”, the result is placed in the W register. If “d” is “1”, the result is placed in the address specified in the instruction.

For bit-oriented instructions, “b” represents a bit field designator, which selects the number of the bit affected by the operation, while “f” represents the address designator. For literal operations, “k” represents the literal or constant value.

Field/Legend	Description
f	Register File Address
b	Bit address
k	Literal. Constant data or label
d	Destination selection field, 0: Working register, 1: Register file
W	Working Register
Z	Zero Flag
C	Carry Flag or/Borrow Flag
DC	Decimal Carry Flag or Decimal/Borrow Flag
PC	Program Counter
TOS	Top Of Stack
GIE	Global Interrupt Enable Flag (i-Flag)
[]	Option Field
( )	Contents
.	Bit Field
B	Before
A	After
←	Assign direction

Mnemonic		Op Code	Cycle	Flag Affect	Description
Byte-Oriented File Register Instruction					
ADDWX	f, d	ff00 0111 dfff ffff	1	C, DC, Z	Add W and "f"
ANDWX	f, d	ff00 0101 dfff ffff	1	Z	AND W with "f"
CLRX	f	ff00 0001 1fff ffff	1	Z	Clear "f"
CLRW		0000 0001 0100 0000	1	Z	Clear W
COMX	f, d	ff00 1001 dfff ffff	1	Z	Complement "f"
DECX	f, d	ff00 0011 dfff ffff	1	Z	Decrement "f"
DECXSZ	f, d	ff00 1011 dfff ffff	1 or 2	-	Decrement "f", skip if zero
INCX	f, d	ff00 1010 dfff ffff	1	Z	Increment "f"
INCXSZ	f, d	ff00 1111 dfff ffff	1 or 2	-	Increment "f", skip if zero
IORWX	f, d	ff00 0100 dfff ffff	1	Z	OR W with "f"
MOVX	f,d	ff00 1000 dfff ffff	1	Z	Move "f"
MOVXW	f	ff00 1000 0fff ffff	1	Z	Move "f" to W
MOVWX	f	ff00 0000 1fff ffff	1	-	Move W to "f"
RLX	f, d	ff00 1101 dfff ffff	1	C	Rotate left "f" through carry
RRX	f, d	ff00 1100 dfff ffff	1	C	Rotate right "f" through carry
SUBWX	f, d	ff00 0010 dfff ffff	1	C, DC, Z	Subtract W from "f"
SWAPX	f, d	ff00 1110 dfff ffff	1	-	Swap nibbles in "f"
TSTX	f	ff00 1000 1fff ffff	1	Z	Test if "f" is zero
XORWX	f, d	ff00 0110 dfff ffff	1	Z	XOR W with "f"
Bit-Oriented File Register Instruction					
BCX	f, b	ff11 00bb bfff ffff	1	-	Clear "b" bit of "f"
BSX	f, b	ff11 01bb bfff ffff	1	-	Set "b" bit of "f"
BTXSC	f, b	ff11 10bb bfff ffff	1 or 2	-	Test "b" bit of "f", skip if clear
BTXSS	f, b	ff11 11bb bfff ffff	1 or 2	-	Test "b" bit of "f", skip if set
Literal and Control Instruction					
ADDLW	k	0001 1100 kkkk kkkk	1	C, DC, Z	Add Literal "k" and W
ANDLW	k	0001 1011 kkkk kkkk	1	Z	AND Literal "k" with W
LCALL	k	kk10 0kkk kkkk kkkk	2	-	Call subroutine "k"
CLRWDT		0001 1110 0000 0100	1	TO, PD	Clear Watch Dog Timer
LGOTO	k	kk10 1kkk kkkk kkkk	2	-	Jump to branch "k"
IORLW	k	0001 1010 kkkk kkkk	1	Z	OR Literal "k" with W
MOVLW	k	0001 1001 kkkk kkkK	1	-	Move Literal "k" to W
NOP		0000 0000 0000 0000	1	-	No operation
RET		0000 0000 0100 0000	2	-	Return from subroutine
RETI		0000 0000 0110 0000	2	-	Return from interrupt
RETLW	k	0001 1000 kkkk kkkk	2	-	Return with Literal in W
SLEEP		0001 1110 0000 0011	1	TO, PD	Go into Power-down mode, Clock oscillation stops
SUBLW	k	0001 1111 kkkk kkkk	1	C, DC, Z	Subtract W from literal
TABRH		0000 0000 0101 1000	2	-	Lookup ROM high data to W
TABRL		0000 0000 0101 0000	2	-	Lookup ROM low data to W
XORLW	k	0001 1101 kkkk kkkk	1	Z	XOR Literal "k" with W

ADDLW	**Add Literal "k" and W**	
Syntax	ADDLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← (W) + k	
Status Affected	C, DC, Z	
OP-Code	0001 1100 kkkk kkkk	
Description	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.	
Cycle	1	
Example	ADDLW 0x15	B : W =0x10 A : W =0x25

ADDWX	**Add W and "f"**	
Syntax	ADDWX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (W) + (f)	
Status Affected	C, DC, Z	
OP-Code	ff00 0111 dfff ffff	
Description	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	ADDWX FSR, 0	B : W =0x17, FSR =0xC2 A : W =0xD9, FSR =0xC2

ANDLW	**Logical AND Literal "k" with W**	
Syntax	ANDLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← (W) AND k	
Status Affected	Z	
OP-Code	0001 1011 kkkk kkkk	
Description	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.	
Cycle	1	
Example	ANDLW 0x5F	B : W =0xA3 A : W =0x03

ANDWX	**AND W with "f"**	
Syntax	ANDWX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (W) AND (f)	
Status Affected	Z	
OP-Code	ff00 0101 dfff ffff	
Description	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	ANDWX FSR, 1	B : W =0x17, FSR =0xC2 A : W =0x17, FSR =0x02

BCX	**Clear "b" bit of "f"**	
Syntax	BCX f [,b]	
Operands	f : 00h ~ 1FFh, b : 0 ~ 7	
Operation	(f.b) ← 0	
Status Affected	-	
OP-Code	ff11 00bb bfff ffff	
Description	Bit 'b' in register 'f' is cleared.	
Cycle	1	
Example	BCX FLAG_REG, 7	B : FLAG_REG =0xC7 A : FLAG_REG =0x47

BSX	**Set "b" bit of "f"**	
Syntax	BSX f [,b]	
Operands	f : 00h ~ 1FFh, b : 0 ~ 7	
Operation	(f.b) ← 1	
Status Affected	-	
OP-Code	ff11 01bb bfff ffff	
Description	Bit 'b' in register 'f' is set.	
Cycle	1	
Example	BSX FLAG_REG, 7	B : FLAG_REG =0x0A A : FLAG_REG =0x8A

BTXSC	**Test "b" bit of "f", skip if clear(0)**	
Syntax	BTXSC f [,b]	
Operands	f : 00h ~ 1FFh, b : 0 ~ 7	
Operation	Skip next instruction if (f.b) =0	
Status Affected	-	
OP-Code	ff11 10bb bfff ffff	
Description	If bit 'b' in register 'f' is 1, then the next instruction is executed. If bit 'b' in register 'f' is 0, then the next instruction is discarded, and a NOP is executed instead, making this a 2nd cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 BTXSC FLAG, 1 TRUE GOTO SUB1 FALSE ...	B : PC =LABEL1 A : if FLAG.1 =0, PC =FALSE if FLAG.1 =1, PC =TRUE

BTXSS	**Test "b" bit of "f", skip if set(1)**	
Syntax	BTXSS f [,b]	
Operands	f : 00h ~ 1FFh, b : 0 ~ 7	
Operation	Skip next instruction if (f.b) =1	
Status Affected	-	
OP-Code	ff11 11bb bfff ffff	
Description	If bit 'b' in register 'f' is 0, then the next instruction is executed. If bit 'b' in register 'f' is 1, then the next instruction is discarded, and a NOP is executed instead, making this a 2nd cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 BTXSS FLAG, 1 TRUE GOTO SUB1 FALSE ...	B : PC =LABEL1 A : if FLAG.1 =0, PC =TRUE if FLAG.1 =1, PC =FALSE

LCALL	Call subroutine "k"	
Syntax	LCALL k	
Operands	k : 000h ~ 1FFFh	
Operation	Operation: TOS ← (PC) + 1, PC.10~0 ← k	
Status Affected	-	
OP-Code	kk10 0kkk kkkk kkkk	
Description	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The 13-bit immediate address is loaded into PC bits <12:0>. The upper bits of PC are loaded from PCLATH. CALL is a two-cycle instruction.	
Cycle	2	
Example	LABEL1 LCALL SUB1	B : PC =LABEL1 A : PC =SUB1, TOS =LABEL1 + 1

CLRX	Clear "f"	
Syntax	CLRX f	
Operands	f : 00h ~ 1FFh	
Operation	(f) ← 00h, Z ← 1	
Status Affected	Z	
OP-Code	ff00 0001 1fff ffff	
Description	The contents of register 'f' are cleared and the Z bit is set.	
Cycle	1	
Example	CLRX FLAG_REG	B : FLAG_REG =0x5A A : FLAG_REG =0x00, Z =1

CLRW	Clear W	
Syntax	CLRW	
Operands	-	
Operation	(W) ← 00h, Z ← 1	
Status Affected	Z	
OP-Code	0000 0001 0100 0000	
Description	W register is cleared and Z bit is set.	
Cycle	1	
Example	CLRW	B : W =0x5A A : W =0x00, Z =1

CLRWDT	Clear Watchdog Timer	
Syntax	CLRWDT	
Operands	-	
Operation	WDT Timer ← 00h	
Status Affected	TO, PD	
OP-Code	0001 1110 0000 0100	
Description	CLRWDT instruction clears the Watchdog Timer	
Cycle	1	
Example	CLRWDT	B : WDT counter =? A : WDT counter =0x00

COMX	**Complement "f"**	
Syntax	COMX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← ($\bar{f}$)	
Status Affected	Z	
OP-Code	ff00 1001 dfff ffff	
Description	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	COMX REG1, 0	B : REG1 =0x13 A : REG1 =0x13, W =0xEC

DECX	**Decrement "f"**	
Syntax	DECX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (f) - 1	
Status Affected	Z	
OP-Code	ff00 0011 dfff ffff	
Description	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	DECX CNT, 1	B : CNT =0x01, Z =0 A : CNT =0x00, Z =1

DECXSZ	**Decrement "f", Skip if 0**	
Syntax	DECXSZ f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (f) - 1, skip next instruction if result is 0	
Status Affected	-	
OP-Code	ff00 1011 dfff ffff	
Description	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2 cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 DECXSZ CNT, 1 GOTO LOOP CONTINUE	B : PC =LABEL1 A : CNT =CNT – 1 if CNT =0, PC =CONTINUE if CNT ≠0, PC =LABEL1 + 1

LGOTO	**Unconditional Branch**	
Syntax	LGOTO k	
Operands	k : 000h ~ 1FFFh	
Operation	PC.10~0 ← k	
Status Affected	-	
OP-Code	kk10 1kkk kkkk kkkk	
Description	GOTO is an unconditional branch. The 13-bit immediate value is loaded into PC bits <12:0>.The upper bits of PC are loaded from PCLATH. GOTO is a two-cycle instruction.	
Cycle	2	
Example	LABEL1 LGOTO SUB1	B : PC =LABEL1 A : PC =SUB1

INCX	**Increment "f"**	
Syntax	INCX f [,d]	
Operands	f : 00h ~ 1FFh	
Operation	(destination) ← (f) + 1	
Status Affected	Z	
OP-Code	ff00 1010 dfff ffff	
Description	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	
Cycle	1	
Example	INCX CNT, 1	B : CNT =0xFF, Z =0 A : CNT =0x00, Z =1

INCXSZ	**Increment "f", Skip if 0**	
Syntax	INCXSZ f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (f) + 1, skip next instruction if result is 0	
Status Affected	-	
OP-Code	ff00 1111 dfff ffff	
Description	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2 cycle instruction.	
Cycle	1 or 2	
Example	LABEL1 INCXSZ CNT, 1 GOTO LOOP CONTINUE	B : PC =LABEL1 A : CNT =CNT + 1 if CNT =0, PC =CONTINUE if CNT ≠0, PC =LABEL1 + 1

IORLW	**Inclusive OR Literal with W**	
Syntax	IORLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← (W) OR k	
Status Affected	Z	
OP-Code	0001 1010 kkkk kkkk	
Description	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.	
Cycle	1	
Example	IORLW 0x35	B : W =0x9A A : W =0xBF, Z =0

IORWX	**Inclusive OR W with "f"**	
Syntax	IORWF f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (W) OR k	
Status Affected	Z	
OP-Code	ff00 0100 dfff ffff	
Description	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	
Cycle	1	
Example	IORWX RESULT, 0	B : RESULT =0x13, W =0x91 A : RESULT =0x13, W =0x93, Z =0

MOVX	**Move f**	
Syntax	MOVX f,d	
Operands	f : 00h ~ 1FFh	
Operation	(destination) ← (f)	
Status Affected	Z	
OP-Code	ff00 1000 dfff ffff	
Description	The contents of register 'f' are moved to a destination dependent upon the status of d. If d=0, destination is W register. If d =1, the destination is file register f itself. d=1 is useful to test a file register, since status flag Z is affected.	
Cycle	1	
Example	MOVX FSR,0	B : FSR =0xC2, W =? A : FSR =0xC2, W 0xC2

MOVXW	**Move "f" to W**	
Syntax	MOVXW f	
Operands	f : 00h ~ 1FFh	
Operation	(W) ← (f)	
Status Affected	Z	
OP-Code	ff00 1000 0fff ffff	
Description	The contents of register 'f' are moved to W register.	
Cycle	1	
Example	MOVXW FSR	B : FSR =0xC2, W =? A : FSR =0xC2, W 0xC2

MOVLW	**Move Literal to W**	
Syntax	MOVLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← k	
Status Affected	-	
OP-Code	0001 1001 kkkk kkkk	
Description	The eight-bit literal 'k' is loaded into W register. The don’t cares will assemble as 0’s.	
Cycle	1	
Example	MOVLW 0x5A	B : W =? A : W =0x5A

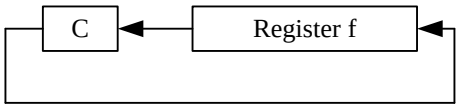
MOVWX	**Move W to "f"**	
Syntax	MOVWX f	
Operands	f : 00h ~ 1FFh	
Operation	(f) ← (W)	
Status Affected	-	
OP-Code	ff00 0000 1fff ffff	
Description	Move data from W register to register 'f'.	
Cycle	1	
Example	MOVWX REG1	B : REG1 =0xFF, W =0x4F A : REG1 =0x4F, W =0x4F

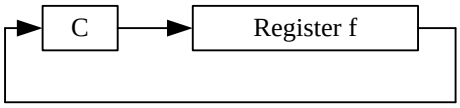
NOP	No Operation	
Syntax	NOP	
Operands	-	
Operation	No Operation	
Status Affected	-	
OP-Code	0000 0000 0000 0000	
Description	No Operation	
Cycle	1	
Example	NOP	-

RET	Return from Subroutine	
Syntax	RET	
Operands	-	
Operation	PC ← TOS	
Status Affected	-	
OP-Code	0000 0000 0100 0000	
Description	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.	
Cycle	2	
Example	RET	A : PC =TOS

RETI	Return from Interrupt	
Syntax	RETI	
Operands	-	
Operation	PC ← TOS, GIE ← 1	
Status Affected	-	
OP-Code	0000 0000 0110 0000	
Description	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in to the PC. Interrupts are enabled. This is a two-cycle instruction.	
Cycle	2	
Example	RETI	A : PC =TOS, GIE =1

RETLW	Return with Literal in W	
Syntax	RETLW k	
Operands	k : 00h ~ FFh	
Operation	PC ← TOS, (W) ← k	
Status Affected	-	
OP-Code	0001 1000 kkkk kkkk	
Description	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.	
Cycle	2	
Example	LCALL TABLE	B : W =0x07
	:	A : W =value of k8
	TABLE ADDWX PCL, 1	
	RETLW k1	
	RETLW k2	
	:	
	RETLW kn	

RLX	**Rotate Left "f" through Carry**	
Syntax	RLX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation		
Status Affected	C	
OP-Code	ff00 1101 dfff ffff	
Description	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	RLX REG1, 0	B : REG1 =1110 0110, C =0 A : REG1 =1110 0110 W =1100 1100, C =1

RRX	**Rotate Right "f" through Carry**	
Syntax	RRX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation		
Status Affected	C	
OP-Code	ff00 1100 dfff ffff	
Description	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	
Cycle	1	
Example	RRX REG1, 0	B : REG1 =1110 0110, C =0 A : REG1 =1110 0110 W =0111 0011, C =0

SLEEP	**Go into Power-down mode, Clock oscillation stops**	
Syntax	SLEEP	
Operands	-	
Operation	-	
Status Affected	TO, PD	
OP-Code	001 1110 0000 0011	
Description	Go into Power-down mode with the oscillator stops.	
Cycle	1	
Example	SLEEP	-

SUBLW	Subtract W from Literal	
Syntax	SUBLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← k – (W)	
Status Affected	C, DC, Z	
OP-Code	0001 1111 kkkk kkkk	
Description	The W register is subtracted (2's complement method) from the eight-bit literal "k". The result is placed in the W register.	
Cycle	1	
Example	SUBLW 0x25	B : W =0x15 A : W =0x10

SUBWX	Subtract W from "f"	
Syntax	SUBWX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (f) – (W)	
Status Affected	C, DC, Z	
OP-Code	ff00 0010 dfff ffff	
Description	Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	SUBWX REG1, 1	B : REG1 =0x03, W =0x02, C =?, Z =? A : REG1 =0x01, W =0x02, C =1, Z =0
	SUBWX REG1, 1	B : REG1 =0x02, W =0x02, C =?, Z =? A : REG1 =0x00, W =0x02, C =1, Z =1
	SUBWX REG1, 1	B : REG1 =0x01, W =0x02, C =?, Z =? A : REG1 =0xFF, W =0x02, C =0, Z =0

SWAPX	Swap Nibbles in "f"	
Syntax	SWAPX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination,7~4) ← (f.3~0), (destination.3~0) ← (f.7~4)	
Status Affected	-	
OP-Code	ff00 1110 dfff ffff	
Description	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.	
Cycle	1	
Example	SWAPX REG, 0	B : REG1 =0xA5 A : REG1 =0xA5, W =0x5A

TABRH	**Return DPTR high byte to W**
Syntax	TABRH
Operands	-
Operation	(W) ← ROM[DPTR] high byte content, Where DPTR = {DPH[max:8], FSR[7:0]}
Status Affected	-
OP-Code	0000 0000 0101 1000
Description	The W and TABR register is loaded with high byte of ROM[DPTR]. This is a two-cycle instruction.
Cycle	2
Example	MOVLW (TAB1&0xFF) MOVWX DPL ;Where DPL is register MOVLW (TBA1>>8)&0xFF MOVWX DPH ;Where DPH is register TABRL ;W =0x89, TABR=0x89 TABRH ;W =0x37, TABR=0x37 ORG 0234H TAB1: DT 0x3789, 0x2277 ;ROM data 16 bits

TABRL	**Return DPTR low byte to W**
Syntax	TABRL
Operands	-
Operation	(W) ← ROM[DPTR] low byte content, Where DPTR = {DPH[max:8], FSR[7:0]}
Status Affected	-
OP-Code	0000 0000 0101 0000
Description	The W and TABR register is loaded with low byte of ROM[DPTR]. This is a two-cycle instruction.
Cycle	2
Example	MOVLW (TAB1&0xFF) MOVWX DPL ;Where DPL register MOVLW (TBA1>>8)&0xFF MOVWX DPH ;Where DPH register TABRL ;W =0x89, TABR=0x89 TABRH ;W =0x37, TABR=0x37 ORG 0234H TAB1: DT 0x3789, 0x2277 ;ROM data 16 bits

TSTX	**Test if "f" is zero**	
Syntax	TSTX f	
Operands	f : 00h ~ 1FFh	
Operation	Set Z flag if (f) is 0	
Status Affected	Z	
OP-Code	ff00 1000 1fff ffff	
Description	If the content of register 'f' is 0, Zero flag is set to 1.	
Cycle	1	
Example	TSTX REG1	B : REG1 =0, Z =? A : REG1 =0, Z =1

XORLW	**Exclusive OR Literal with W**	
Syntax	XORLW k	
Operands	k : 00h ~ FFh	
Operation	(W) ← (W) XOR k	
Status Affected	Z	
OP-Code	0001 1101 kkkk kkkk	
Description	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.	
Cycle	1	
Example	XORLW 0xAF	B : W =0xB5 A : W =0x1A

XORWX	**Exclusive OR W with "f"**	
Syntax	XORWX f [,d]	
Operands	f : 00h ~ 1FFh, d : 0, 1	
Operation	(destination) ← (W) XOR (f)	
Status Affected	Z	
OP-Code	ff00 0110 dfff ffff	
Description	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.	
Cycle	1	
Example	XORWX REG, 1	B : REG =0xAF, W =0xB5 A : REG =0x1A, W =0xB5

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A =25℃)

Parameter	Rating	Unit
Supply voltage	V_{SS} -0.3 to V_{SS} +5.5	V
Input voltage	V_{SS} -0.3 to V_{CC} +0.3	
Output voltage	V_{SS} -0.3 to V_{CC} +0.3	
Output current high per 1 PIN	-25	mA
Output current high per all PIN	-80	
Output current low per 1 PIN	+30	
Output current low per all PIN	+150	
Maximum operating voltage	5.5	V
Operating temperature	-40 to +105	℃
Storage temperature	-65 to +150	

2. DC Characteristics (T_A =25℃, V_{DD} =5.0V, unless otherwise specified)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{cc}	Fsys=18.432Mhz		2.8		5.5	
		Fsys= 9.2Mhz		LVR		5.5	
Input High Voltage	V_{IH}	All Input	V_{CC} = 3~5V	0.6Vcc	–	Vcc	V
Input Low Voltage	V_{IL}	All Input	V_{CC} = 3~5V	Vss	–	0.2Vcc	V
Output High Current	I_{OH}	All Output	V_{CC} = 5V,V_{OH} = 4.5V LED[x]=0	10	12	–	mA
			V_{CC} = 5V,V_{OH} = 3.5V LED[x]=1	15	19		
			V_{CC} = 3V,V_{OH} = 2.7V LED[x]=0	4	5	–	
			V_{CC} = 3V,V_{OH} = 2.1V LED[x]=1	6	8		
Output Low Current	I_{OL}	All Output	V_{CC} = 5V,V_{OL} = 0.5V HSNK[x]=0	33	42	–	mA
			V_{CC} = 5V,V_{OL} = 0.5V HSNK[x]=1	60	70		
			V_{CC} = 3V,V_{OL} = 0.3V HSNK[x]=0	15	19	–	
			V_{CC} = 3V,V_{OL} = 0.3V HSNK[x]=1	27	34		
Input Leakage Current (pin high)	I_{ILH}	All Input	V_{IN} = V_{CC}	–	–	1	uA
Input Leakage Current (pin low)	I_{ILL}	All Input	V_{IN} = 0V	–	–	–1	uA

Parameter	Sym	Conditions		Min	Typ	Max	Unit
Power Supply Current (No Load)	I_{CC}	FAST mode FXT 20MHz	V_{CC} = 5V	–	7.3	–	mA
			V_{CC} = 3V		4.1		
		FAST mod FIRC 18.4 MHz	V_{CC} = 5V		7		
			V_{CC} = 3V		4		
		FAST mode FIRC 9.2 MHz	V_{CC} = 5V		5.1		
			V_{CC} = 3V		3.1		
		FAST mode FIRC 4.6 MHz	V_{CC} = 5V	–	4.2	–	
			V_{CC} = 3V		2.6		
		FAST mode FIRC 2.3 MHz	V_{CC} = 5V	–	3.7	–	
			V_{CC} = 3V	–	2.3	–	
		SLOW mode SIRC 50KHz FIRC STOP	V_{CC} = 5.0V	–	2.2	–	mA
			V_{CC} = 3.0V	–	1.6	–	
		IDLE mode SIRC 50 KHz	V_{CC} = 5.0V	–	6.5	–	uA
			V_{CC} = 3.0V	–	2.1	–	
		STOP mode POR/LVR Off	V_{CC} = 5.0V	–	-	1	uA
			V_{CC} = 3.0V	–	-	1	
Pull-up Resistor	R_{UP}	V_{IN} = 0 V Ports A/B/C/D	V_{CC} = 5.0V	–	32	–	KΩ
			V_{CC} = 3.0V	–	56	–	

3. Clock Timing (T_A = -40°C to +85°C)

Parameter	Condition	Min	Typ	Max	Unit
FIRC Frequency (*)	25℃, V_{CC} =5.0 V	-1%	18.432	+1%	MHz
	-40℃ ~ 105℃, V_{CC} = 5.0 V	-1.5%	18.432	+1.5%	
	-40℃ ~ 105℃, V_{CC} = 3.0 ~ 5.0V	-2.5%	18.432	+2.5%	

(*) FIRC frequency can be divided by 1/2/4/8.

4. Reset Timing Characteristics (T_A = -40°C to +85°C)

Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input V_{CC} = 5 V ±10 %	-	30	–	μs
WDT time	V_{CC} = 3 V, WDTPSC = 11	–	1520	–	ms
	V_{CC} = 5 V, WDTPSC = 11		1360		
WKT time	V_{CC} = 3 V, WKTPSC = 11	–	190	–	ms
	V_{CC} = 5 V, WKTPSC = 11		170		
CPU start up time	V_{CC} = 5 V	–	38	–	ms

5. EEPROM Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Write Voltage, Vcc	-20℃ ~ 105℃	3.0	5	5.5	V
	-40℃ ~ 105℃	3.5	5	5.5	V
Write Endurance(1)	Vcc=3.0~5.5V, -40~105℃	30K			cycles
	Vcc=3.0~5.5V, -20 ~105℃	40K			cycles
	Vcc=3.0~5.5V, -10~ 105℃	50K			cycles

Note:1 The value of this parameter is based on the characteristics of tested samples

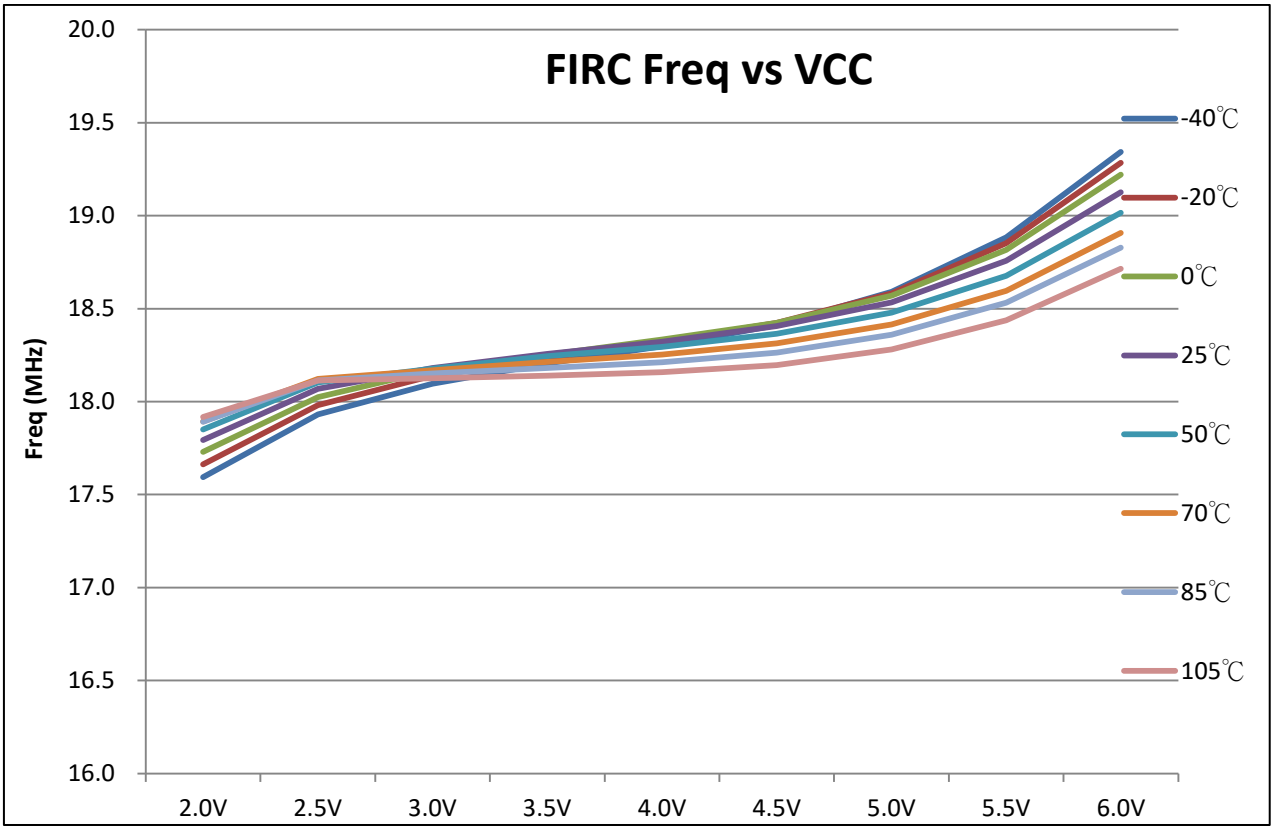
6. LVR Circuit Characteristics (T_A = 25℃)

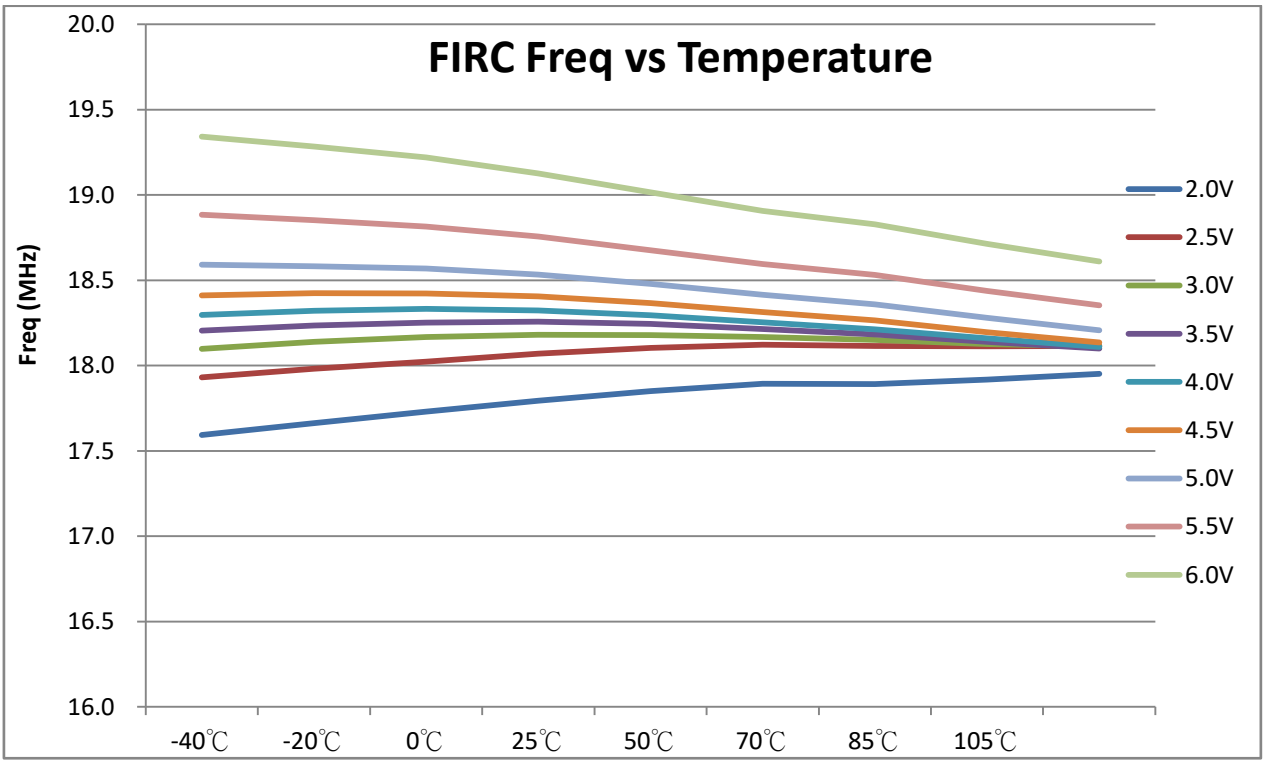
Parameter	Sym	Conditions	Min	Typ	Max	Unit
LVR Reference Voltage	V_{LVR}	T_A = 25℃	–	4.15	–	V
			–	4.01	–	
			–	3.87	–	
			–	3.73	–	
			–	3.59	–	
			–	3.45	–	
			–	3.31	–	
			–	3.17	–	
			–	3.03	–	
			–	2.89	–	
			–	2.75	–	
			–	2.62	–	
			–	2.47	–	
			–	2.33	–	
			–	2.19	–	
			–	2.05	–	
LVD Reference Voltage	V_{LVd}	T_A = 25℃	–	4.15	–	V
			–	4.01	–	
			–	3.87	–	
			–	3.73	–	
			–	3.59	–	
			–	3.45	–	
			–	3.31	–	
			–	3.17	–	
			–	3.03	–	
			–	2.89	–	
			–	2.75	–	
			–	2.62	–	
			–	2.47	–	
			–	2.33	–	
			–	2.19	–	
			–	2.05	–	
LVR Hysteresis Voltage	V_{HYST}	T_A = 25℃	–	±0.1	–	V
Low Voltage Detection time	t_{LVR}	T_A = 25℃	100	–	–	μs

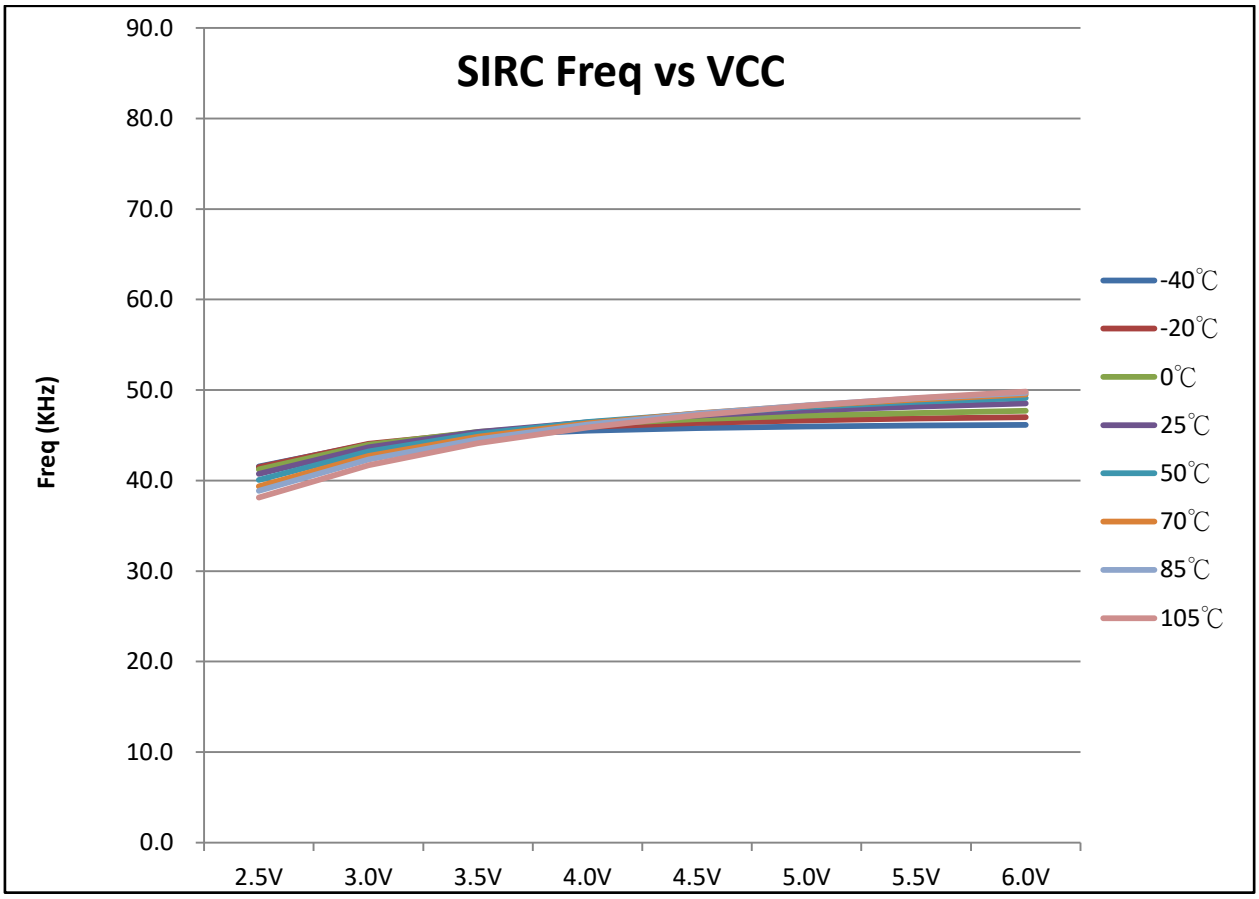
7. ADC Electrical Characteristics (T_A = 25℃, VCC = 3.0V to 5.5V, VSS = 0V)

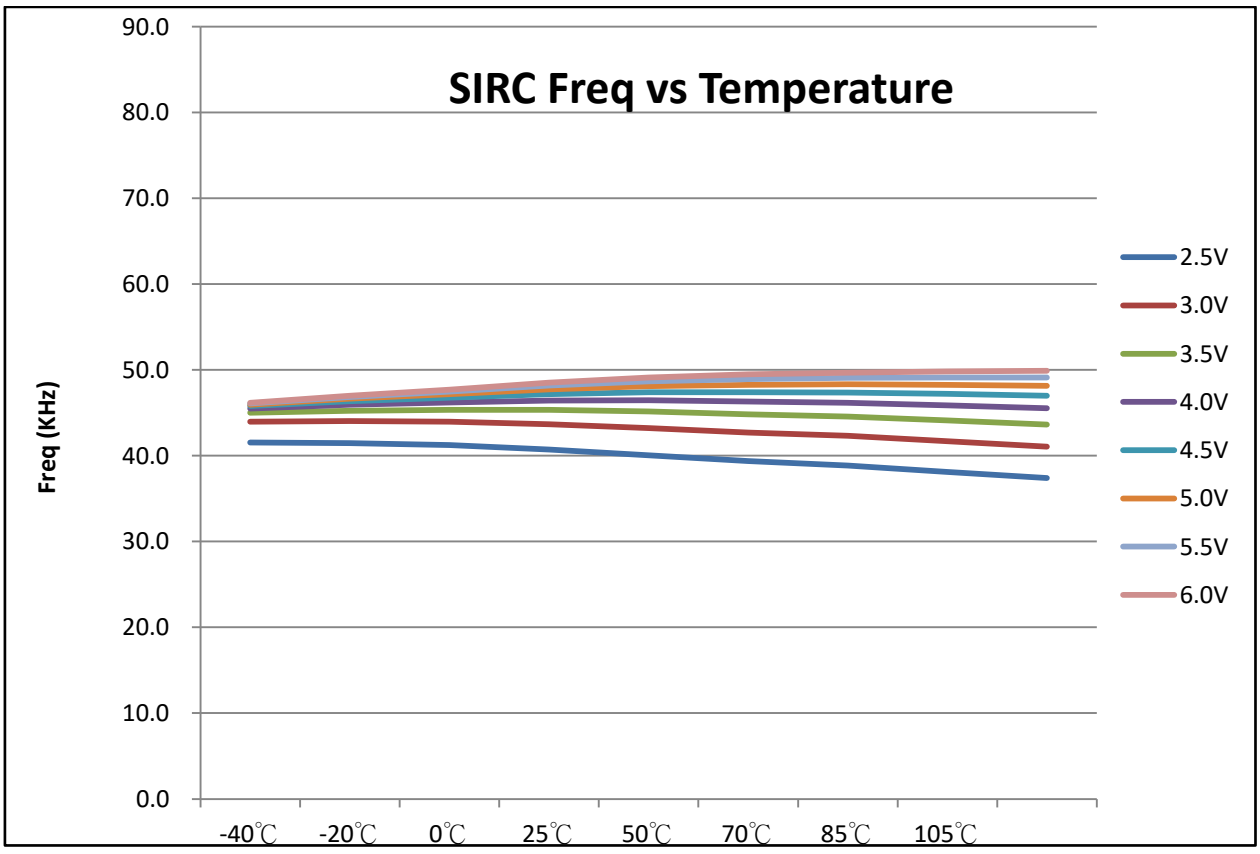
Parameter	Conditions	Min	Typ	Max	Units
Total Accuracy	V_{CC} = 5V, V_{SS} = 0V, F_{ADC} = 1 MHz	–	±3	±13	LSB
Integral Non-Linearity		–	±3.2	±15	
Differential Non-linearity		–	±1	±4	
Max Input Clock freq. (F_{ADC})	Source impedance (Rs<10K omh)	–	–	2	MHz
	Source impedance (Rs<20K omh)	–	–	1	
	Source impedance (Rs<50K omh)	–	–	0.5	
	Source is VBG (ADCHS=01110)	–	–	2	
Conversion Time	F_{ADC} = 1 MHz	–	50	–	μs
BandGap Voltage Reference (VBG)	-20℃~105℃, V_{CC} = 3.0~5.0V	-2%	1.2	+1.5%	V
ADC reference voltage(V_{REF}) (ADCVREFS=1)	-20℃~105℃, V_{CC} = 3.0~5.0V	-2.5%	2.5	+2%	
Vcc/4 reference voltage	25℃, V_{CC} = 3.0~5.0V	-1%	0.25*Vcc	1%	
Input Voltage	–	V_{SS}	–	Vcc	

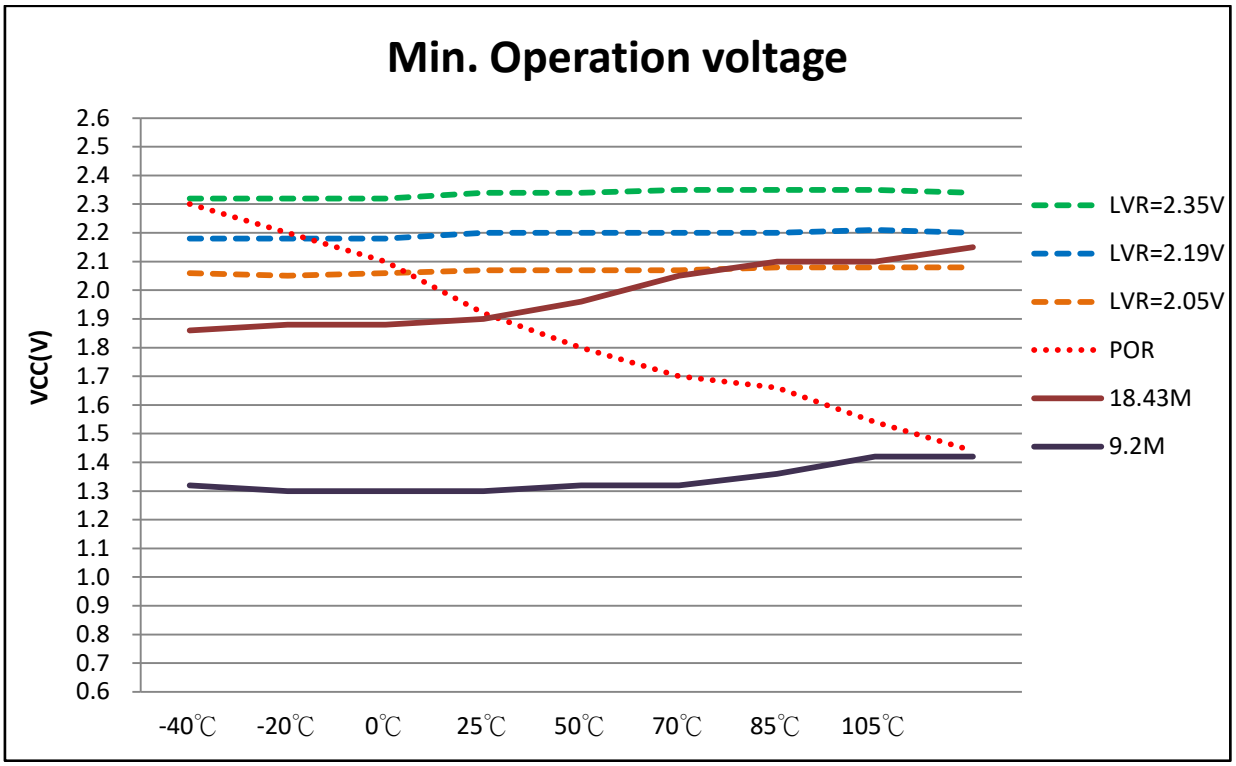
8. Characteristic Graphs

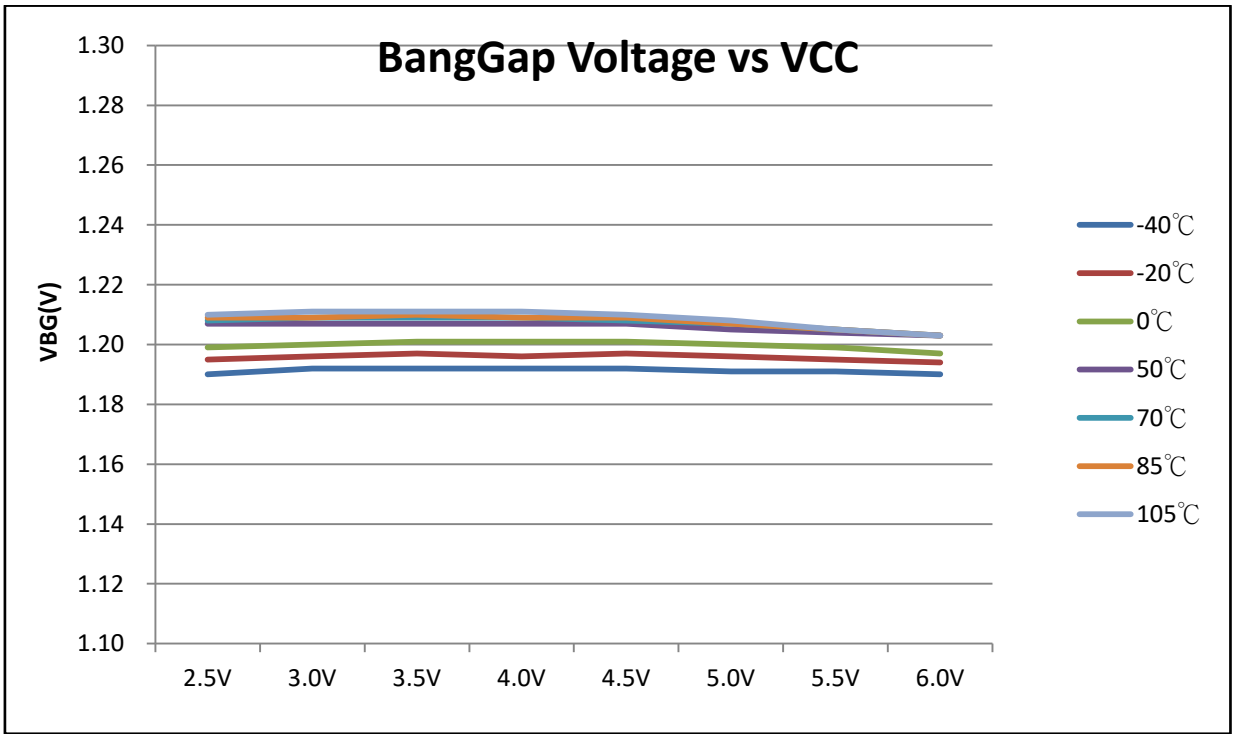





SIRC Freq vs VCC
Freq (KHz)
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
6.0V
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
105℃


SIRC Freq vs Temperature
Freq (KHz)
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
105℃
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
6.0V


Min. Operation voltage
VCC(V)
2.6
2.5
2.4
2.3
2.2
2.1
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
105℃
LVR=2.35V
LVR=2.19V
LVR=2.05V
POR
18.43M
9.2M


BangGap Voltage vs VCC
VBG(V)
1.30
1.28
1.26
1.24
1.22
1.20
1.18
1.16
1.14
1.12
1.10
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
6.0V
-40℃
-20℃
0℃
50℃
70℃
85℃
105℃

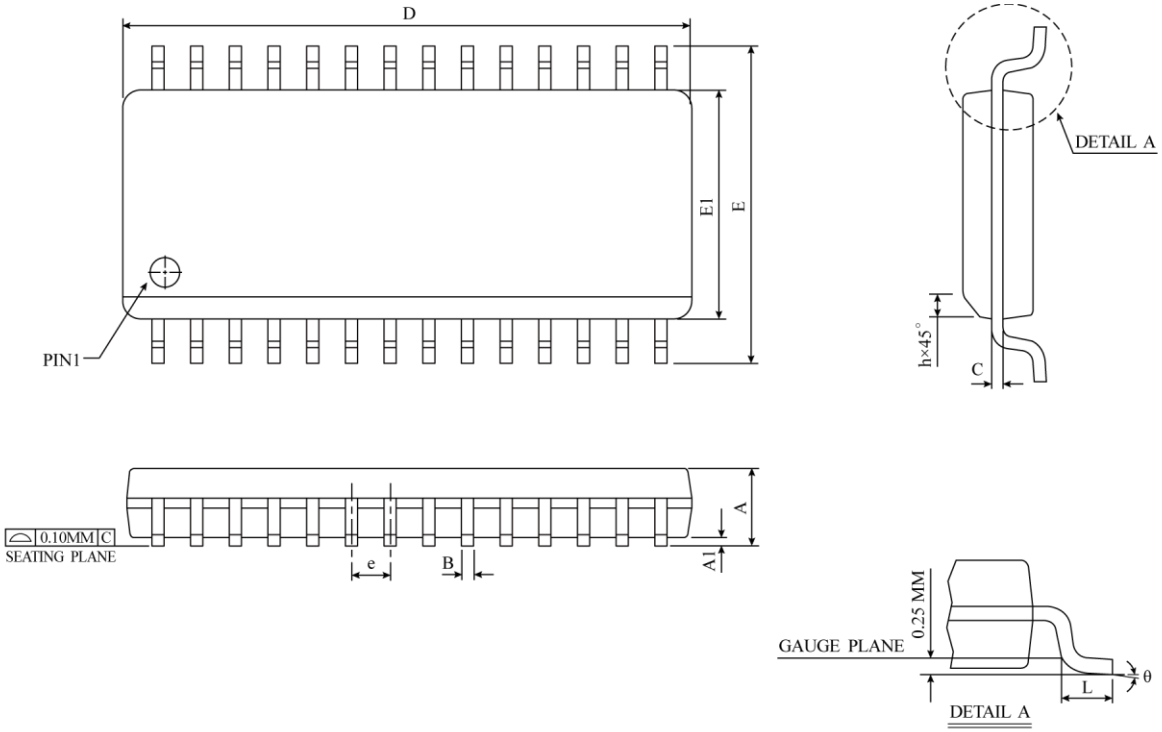
PACKAGING INFORMATION

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

The ordering information:

Ordering number	Package
TM56F1543-MTP	Wafer/Dice blank chip
TM56F1543-COD	Wafer/Dice with code
TM56F1543-MTP-23	SOP 28-pin (300 mil)
TM56F1543-MTP-21	SOP 20-pin (300 mil)
TM56F1543-MTP-46	TSSOP 20-pin (173 mil)
TM56F1543-MTP-16	SOP 16-pin (150 mil)
TM56F1543-MTP-14	SOP 8-pin (150 mil)

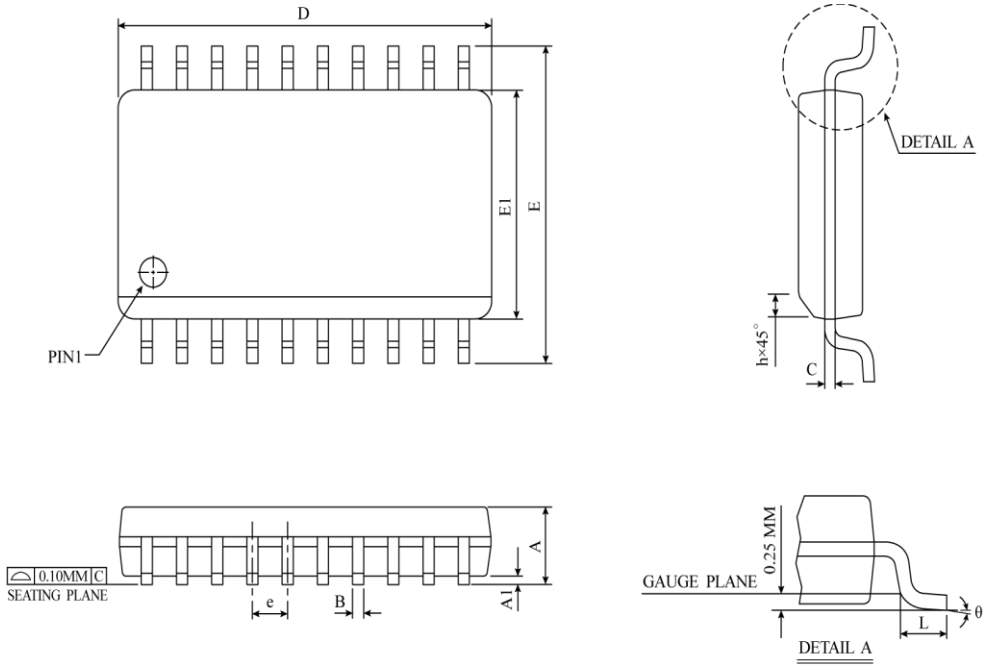
✧ SOP-28 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	17.70	17.90	18.10	0.6969	0.7047	0.7125
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AE)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

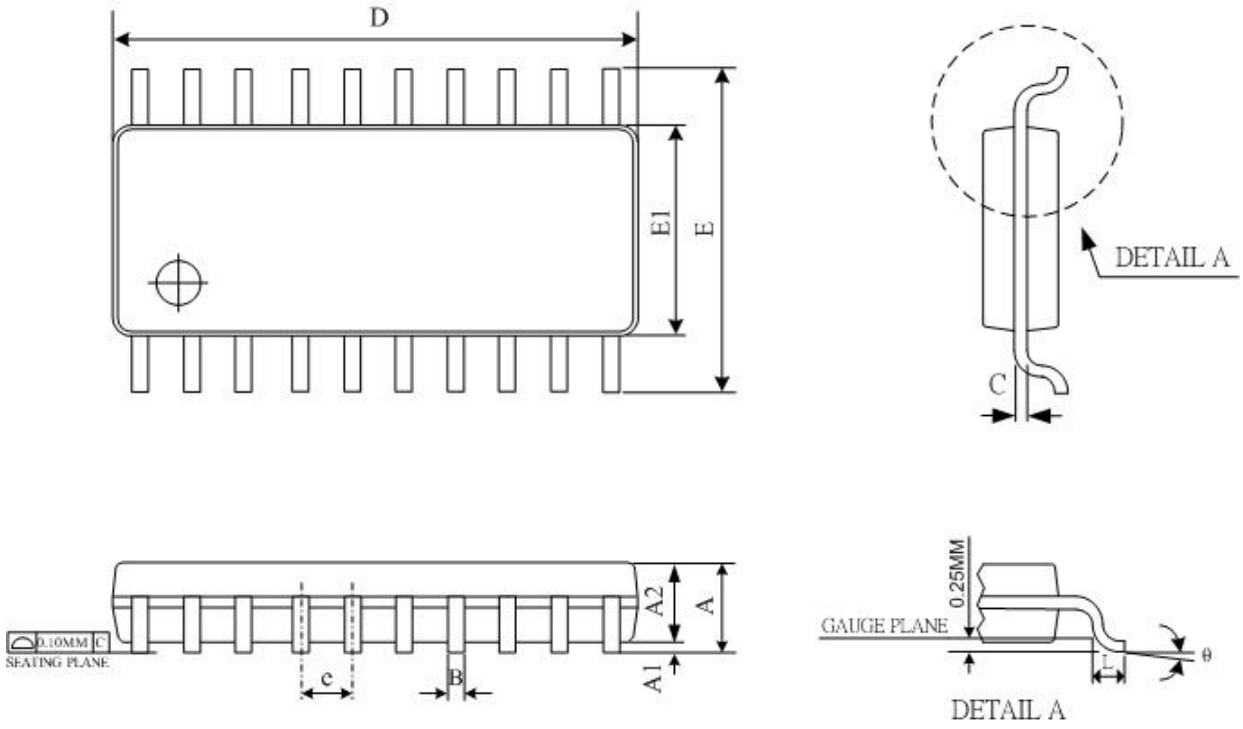
✧ SOP-20 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

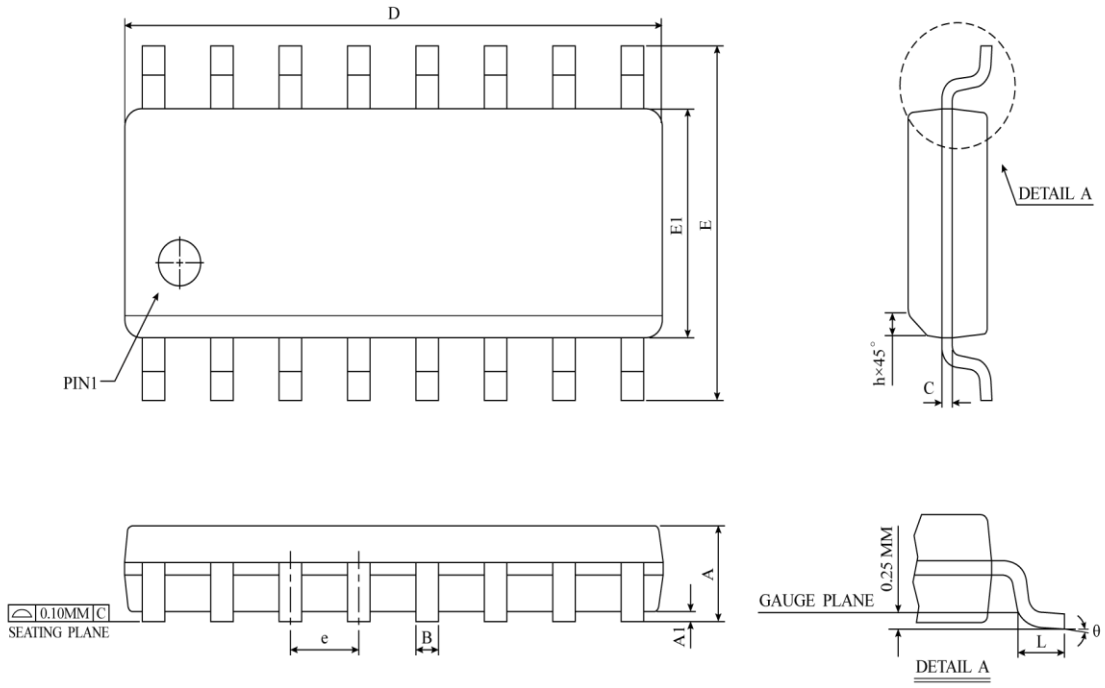
✧ TSSOP-20 (173mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.8	0.93	1.05	0.031	0.036	0.041
B	0.19	-	0.3	0.007	-	0.012
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.55	0.246	0.252	0.258
E1	4.3	4.4	4.5	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0 °		8 °	0 °		8 °
JEDEC	MO-153 AC REV.F					

Notes：
1.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
2.DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
3.DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE "B" DIMENSION AT MAXIMUM METERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07MM.

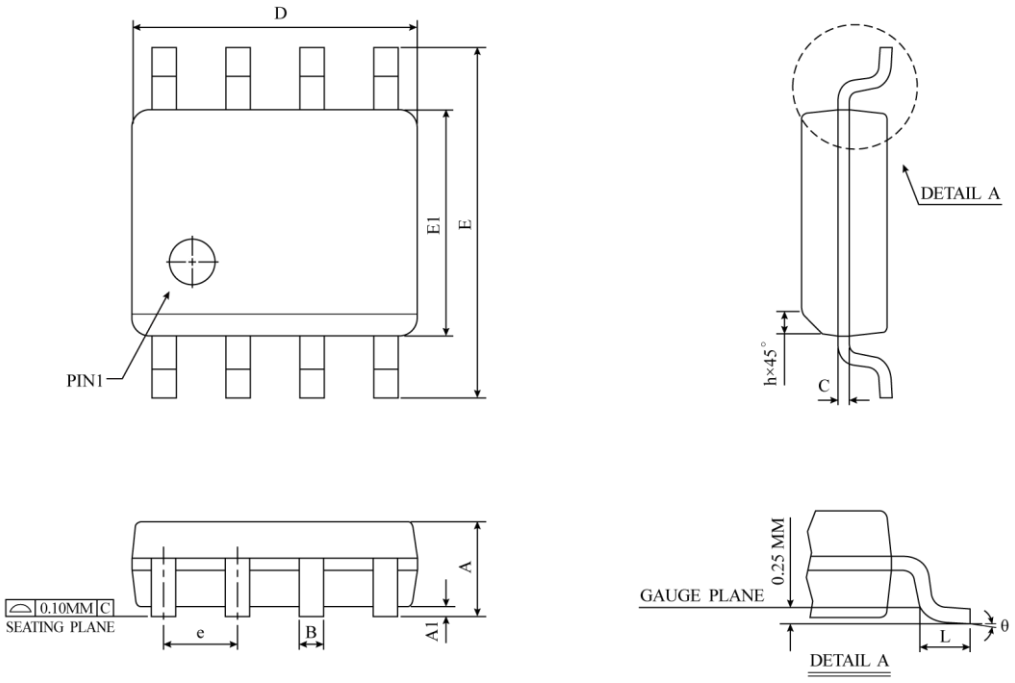
✧ SOP-16 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

✧ SOP-8 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	4.80	4.90	5.00	0.1890	0.1939	0.1988
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AA)					

⚠ * NOTES：DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.