



十速

TM52M5254/58

DATA SHEET

Rev 0.95

tenx reserves the right to change or discontinue the manual and online documentation to this product herein to improve reliability, function or design without further notice. **tenx** does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. **tenx** products are not designed, intended, or authorized for use in life support appliances, devices, or systems. If Buyer purchases or uses **tenx** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **tenx** and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, cost, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use even if such claim alleges that **tenx** was negligent regarding the design or manufacture of the part.

AMENDMENT HISTORY

Version	Date	Description
V0.90	Nov, 2013	New release.
V0.91	Oct, 2014	註:本文從 V0.91 版起由 DV0.90 版改為 V0.91 版 1. Ordering information 增加 SOP/DIP 16、刪除 TM52M5254-MTP-21 的 X 及 NOTE (P69) 2. Package Information 增加 SOP/DIP 16 (P70.71)
V0.92	Jun, 2015	page5: family member feature update page7: FRC/2 page21: LVR table & AP-TM52XXXXX_02S page22: FRC/2 page23: AP-TM52XXXXX_01S & AP-TM52XXXXX_02S
V0.93	Sep, 2015	1. Page49: TKEOC may have 3uS delay after TKSOC=1 2. Page64: add Vbg error range
V0.94	Aug, 2017	1. Remove CFGW.WDTE 2. Stop mode description 3. FRC accuracy & Temp. curve 4. Modify TK CLD dis-charge Time 5. Other detail
V0.95	Jun, 2018	Add Package type Other detail

CONTENTS

AMENDMENT HISTORY	2
TM52 F52xx FAMILY	5
GENERAL DESCRIPTION	6
BLOCK DIAGRAM	6
FEATURES	7
PIN ASSIGNMENT	9
PIN DESCRIPTION	11
PIN SUMMERY	12
FUNCTIONAL DESCRIPTION	13
1. CPU Core	13
1.1 Accumulator (ACC)	13
1.2 B Register (B)	13
1.3 Stack Pointer (SP)	13
1.4 Dual Data Pointer (DPTRs)	14
1.5 Program Status Word (PSW)	14
2. Memory	16
2.1 Program Memory	16
2.2 Data Memory	17
3. Power	19
4. Reset	20
4.1 Power on Reset	20
4.2 Low Voltage Reset	20
4.3 External Pin Reset	21
4.4 Watch Dog Timer Reset	21
5. Clock Circuitry & Operation Mode	23
5.1 System Clock	23
5.2 Operation Modes	25
6. Interrupt & Wake-up	26
6.1 Interrupt Enable and Priority Control	26
6.2 Pin Interrupt	29
6.3 Idle mode Wake up and Interrupt	30
6.4 Stop mode Wake up and Interrupt	30
7. I/O Ports	32
8. Timers	38
8.1 Timer0 / Timer1	38
8.2 Timer2	39

8.3 Timer3	40
9. UART	42
10. PWMs.....	44
11. ADC	47
12. Touch Key (M5258 only).....	49
SFR & CFGW MAP	52
SFR & CFGW DESCRIPTION.....	53
INSTRUCTION SET	60
ELECTRICAL CHARACTERISTICS	63
1. Absolute Maximum Ratings.....	63
2. DC Characteristics.....	64
3. Clock Timing.....	66
4. Reset Timing Characteristics	66
5. ADC Electrical Characteristics	66
6. Characteristic Graphs	67
Package and Dice Information.....	70

TM52 F52xx FAMILY

Common Feature

CPU	MTP/Flash Program memory	RAM bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LVD	LVR
Fast 8051 (2T)	4K~16K with IAP, ISP, ICP	256 ~ 512	SXT SRC FXT FRC	Fast Slow Idle Stop	8051 Standard		15-bit	2.3V	1.9V 2.3V 2.9V

Note: IAP, ISP only for Flash type program memory

Family Members Features

P/N	Program Memory	RAM Bytes	IO Pin	PWM	SAR ADC	Touch Key	LCD	LED	SPI	Status
TM52-M5254	MTP 4K Bytes	256	18	(8+2)-bit x2	12-bit 12-ch	—	—	—	—	Product
TM52-M5258						14-ch				
TM52-F5264B	Flash 8K Bytes	256	22	(8+2)-bit x2	12-bit 12-ch	—	—	—	Yes	Product
TM52-F5268B						14-ch				
TM52-F5274B	Flash 8K Bytes	512	30	(8+2)-bit x2	12-bit 12-ch	—	4x18	4x18	Yes	Product
TM52-F5278B						14-ch				
TM52-F5288B	Flash 16K Bytes	512	42	(8+2)-bit x2	12-bit 12-ch	—	8x20	8x20	Yes	Product
TM52-F5284B						12-ch				

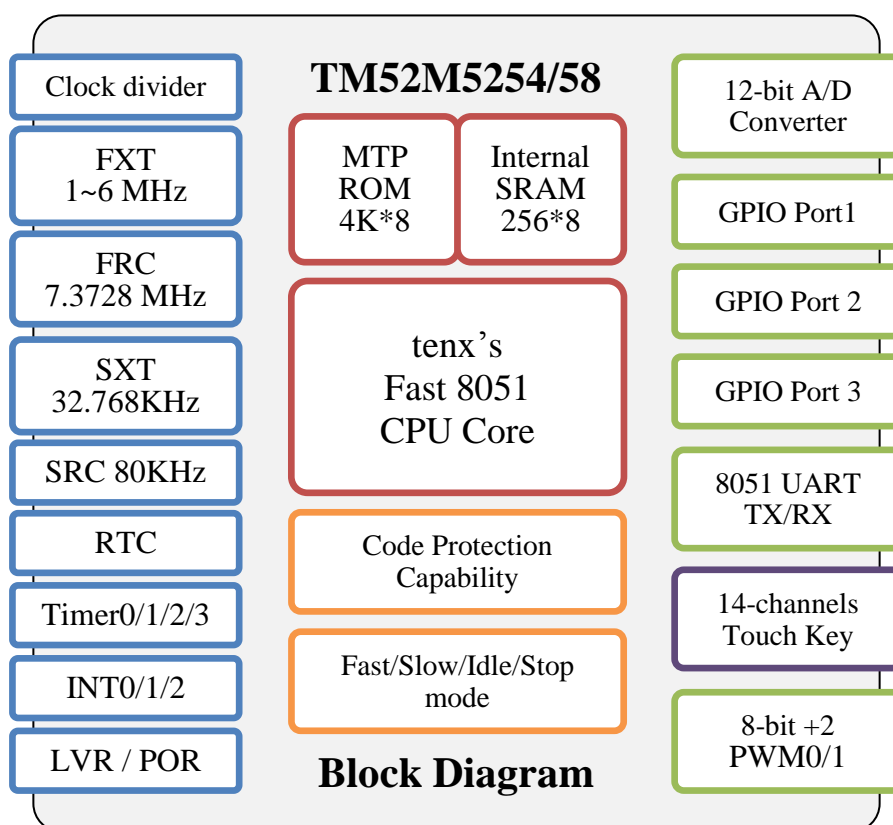
P/N	Operation Voltage	Operation Current (V _{CC} =3V) Mode3V=1, PWRSAV=1, LVR Disable				Max. System Clock (Hz)			
		Fast FRC	Slow SRC	Idle SRC	Stop	SXT	SRC	FXT	FRC
TM52-M5254	1.9~5.5V	2.0mA	21μA	5.2μA	< 0.1μA	32K	80K	6M	7.37M/2
TM52-M5258									
TM52-F5264B	1.9~5.5V	2.5mA	8μA	2.0μA	< 0.1μA	32K	24K	8M	7.37M
TM52-F5268B									
TM52-F5274B	1.9~5.5V	2.5mA	8μA	2.5μA	< 0.1μA	32K	24K	8M	7.37M
TM52-F5278B									
TM52-F5288B	1.9~5.5V	2.3mA	22μA	4.5μA	< 0.1μA	32K	80K	8M	7.37M
TM52-F5284B									

GENERAL DESCRIPTION

TM52_{series} M5254 and M5258 are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, and retains most 8051 peripheral's functional block. Typically, the **TM52-M5254/58** executes instructions six times faster than the standard 8051 architecture.

The **TM52-M5254/58** provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 4K Bytes MTP program memory, 256 Bytes SRAM, Low Voltage Reset (LVR), Low Voltage Detector (LVD), dual clock power saving operation mode, 8051 standard UART and Timer0/1/2, real time clock Timer3, 2 set (8+2)-bit PWMs, 10 channels 12-bit A/D Converter, 14 channels Touch Key (M5258 only) and Watch Dog Timer. Its high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

BLOCK DIAGRAM



FEATURES

- 1. Standard 8051 Instruction set, fast machine cycle**
 - Executes instructions six times faster than the standard 8051.
- 2. 4K Bytes MTP Program Memory**
 - Support "In Circuit Programming" (ICP) for the MTP code
 - Code Protection Capability
- 3. 256 Bytes SRAM in the 8051 internal data memory area (IRAM)**
- 4. Four System Clock type selections**
 - Fast clock from 1~6 MHz Crystal (FXT)
 - Fast clock from Internal RC (FRC/2, 7.3728 MHz / 2)
 - Slow clock from 32768Hz Crystal (SXT)
 - Slow clock from Internal RC (SRC, 80 KHz)
 - System Clock can be divided by 1/2/4/16 option
- 5. 8051 Standard Timer – Timer0/1/2**
 - 16-bit Timer0, also supports T0O clock output for Buzzer application
 - 16-bit Timer1
 - 16-bit Timer2, also supports T2O clock output for Buzzer application
- 6. 15-bit Timer3**
 - Clock source is Slow clock
 - Interrupt period can be clock divided by 32768/16384/8192/128 option
- 7. 8051 Standard UART**
 - Support One Wire UART mode
- 8. Two independent "8+2" bits PWMs with prescaler/ period-adjustment**
- 9. 14-Channel Touch Key (M5258 only)**
- 10. 12-bit ADC with 10 channels External Pin Input and 2 channels Internal Reference Voltage**
- 11. Max. 18 Programmable I/O pins**
 - CMOS Output
 - Pseudo-Open-Drain, or Open-Drain Output
 - Schmitt Trigger Input
 - Pin Pull-up can be Enabled or Disabled
- 12. Pin Interrupt can Wake up CPU from Power-Down (Stop) mode**
 - P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
 - P3.7 (INT2) Interrupt & Wake-up
 - Each Port1 pin can be defined as Interrupt & Wake-up pin (by pin change)

13. 10 Sources, 4-level priority Interrupt

- Timer0/Timer1/Timer2/Timer3 Interrupt
- INT0/INT1 pin Falling-Edge/Low-Level Interrupt
- P3.7 (INT2) pin Interrupt
- Port1 Pin Change Interrupt
- UART TX/RX Interrupt
- ADC/Touch Key Interrupt

14. Four types Reset

- Power on Reset
- Selectable External Pin Reset
- Selectable Watch Dog Reset
- Selectable Low Voltage Reset (1.9V/2.3V/2.9V/Disable)

15. Low Voltage Detector Flag (LVD=2.3V)**16. Independent RC Oscillating Watch Dog Timer**

- 400ms/200ms/100ms/50ms selectable WDT timeout options

17. Four Power Operation Modes

- Fast/Slow/Idle/Stop mode

18. Operating Voltage and Current

- $V_{CC}=2.9V(LVR) \sim 5.5V$ @ $F_{SYSCLK}=6$ MHz (FXT)
- $V_{CC}=2.3V(LVR) \sim 5.5V$ @ $F_{SYSCLK}=3.7$ MHz (FRC/2)
- $V_{CC}=1.9V(LVR) \sim 5.5V$ @ $F_{SYSCLK} < 2$ MHz
- $I_{CC} < 0.1\mu A$ @Stop mode, all function turn off

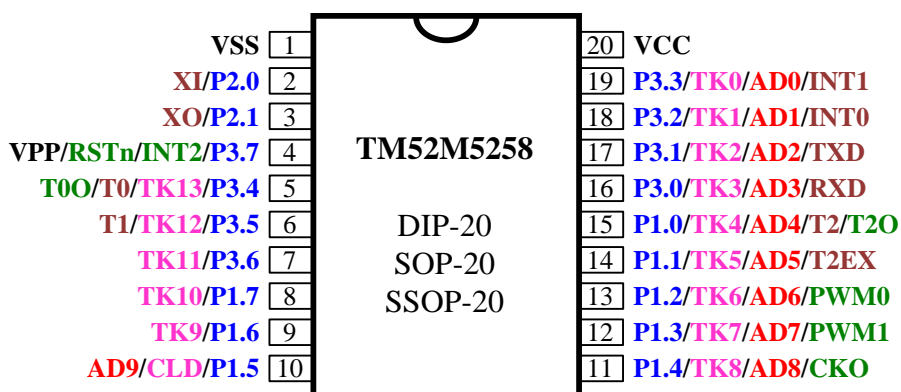
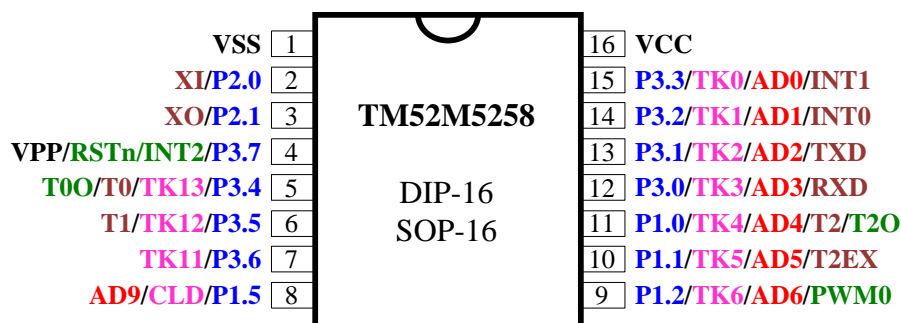
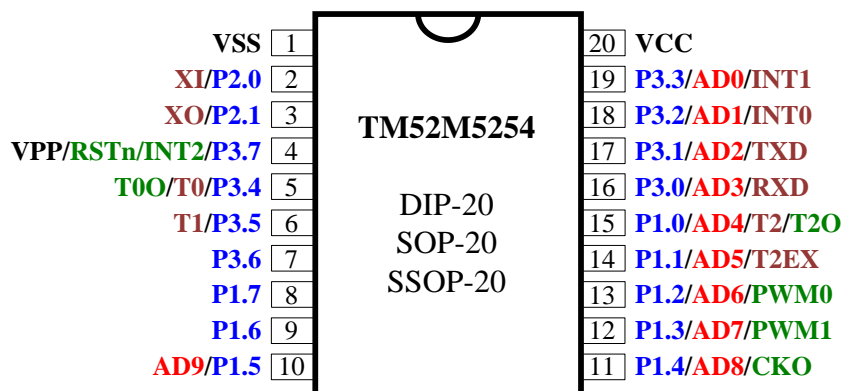
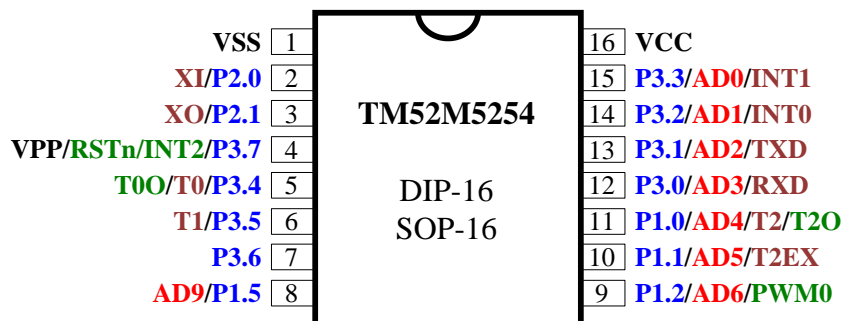
19. Operating Temperature Range

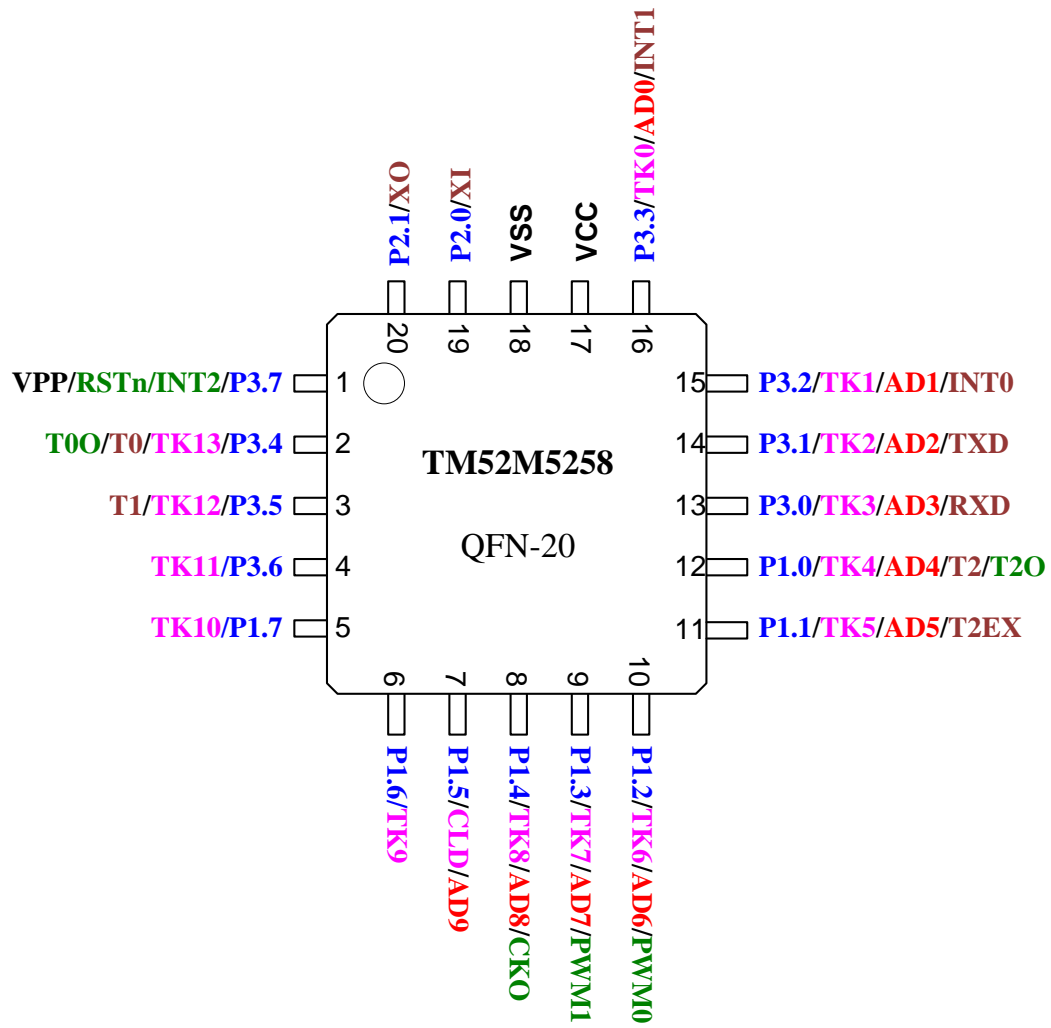
- $-40^{\circ}C \sim +85^{\circ}C$

20. Package Types

- 20 pin DIP / SOP / SSOP / QFN
- 16 pin DIP / SOP

PIN ASSIGNMENT





PIN DESCRIPTION

Name	In/Out	Pin Description
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can interrupt/wake up CPU from Idle/Stop mode.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or " pseudo open drain " output. Pull-up resistors are assignable by software.
P3.3~P3.6 P2.0~P2.1	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or "open-drain" output. Pull-up resistor is fix enable.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Stop mode wake up input.
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input.
T2EX	I	Timer2 external trigger input.
T0O	O	Timer0 overflow divided by 64 output
T2O	O	Timer2 overflow divided by 2 output
CKO	O	System Clock divided by 2 output
PWM0, PWM1	O	8+2 bit PWM output
AD0~AD9	I	ADC input
TK0~TK13	I	Touch Key input (M5258 only)
CLD	I/O	Touch Key charge collection capacitor connection pin (M5258 only)
RSTn	I	External active low reset input, Pull-up resistor is fixed enable.
XI, XO	–	Crystal/Resonator oscillator connection for System clock (FXT or SXT)
VPP	I	MTP memory programming high voltage input
VCC, VSS	P	Power input pin and ground

PIN SUMMERY

Pin #		Pin Name	Type	Reset State	Input			Output			Alternative Function					
DIP/SOP-20	DIP/SOP-16				Pull-up Control	Wake up	Ext. Interrupt	CMOS P.P.	P.O.D.	O.D.	ADC	Touch Key	PWM	Clock Output	Timer Input	Others
1	1	VSS	P	–												
2	2	XI/P2.0	I/O	Hi-Z	●			●		●						Crystal
3	3	XO/P2.1	I/O	Hi-Z	●			●		●						Crystal
4	4	VPP/RSTn/INT2/P3.7	I/O	PU	⊙	●	●			●						Reset, VPP
5	5	T0O/T0/TK13/P3.4	I/O	PU	●			●		●		●		●	●	
6	6	T1/TK12/P3.5	I/O	PU	●			●		●		●			●	
7	7	TK11/P3.6	I/O	PU	●			●		●		●				
8	–	TK10/P1.7	I/O	PU	●	●	●	●		●		●				
9	–	TK9/P1.6	I/O	PU	●	●	●	●		●		●				
10	8	AD9/CLD/P1.5	I/O	PU	●	●	●	●		●	●	●				
11	–	CKO/AD8/TK8/P1.4	I/O	PU	●	●	●	●		●	●	●		●		
12	–	PWM1/AD7/TK7/P1.3	I/O	PU	●	●	●	●		●	●	●	●			
13	9	PWM0/AD6/TK6/P1.2	I/O	PU	●	●	●	●		●	●	●	●			
14	10	T2EX/AD5/TK5/P1.1	I/O	PU	●	●	●	●		●	●	●			●	
15	11	T2O/T2/AD4/TK4/P1.0	I/O	PU	●	●	●	●		●	●	●		●	●	
16	12	RXD/AD3/TK3/P3.0	I/O	Hi-Z	●			●	●		●	●				UART
17	13	TXD/AD2/TK2/P3.1	I/O	Hi-Z	●			●	●		●	●				UART
18	14	INT0/AD1/TK1/P3.2	I/O	Hi-Z	●	●	●	●	●		●	●				
19	15	INT1/AD0/TK0/P3.3	I/O	Hi-Z	●	●	●	●		●	●	●				
20	16	VCC	P	–												

Symbol:

P.P. = Push-Pull

O.D. = Open Drain

P.O.D. = Pseudo Open Drain

PU = Pull-up

Hi-Z = High-Z

⊙ = P3.7 Pull-up resistor is fix enable

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The **M5254/58** features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR E0h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC**: Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands be in A and B.

SFR F0h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B**: B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer. The Stack Pointer points to the top location of the stack.

SFR 81h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP**: Stack Point

1.4 Dual Data Pointer (DPTRs)

M5254/58 has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR 82h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL**: Data Point low byte

SFR 83h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH**: Data Point high byte

SFR F8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	—	—	—	DPSEL
R/W	R/W	R/W	R/W	R/W	—	—	—	R/W
Reset	0	0	0	0	—	—	—	0

F8h.0 **DPSEL**: Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR D0h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY**: ALU carry flag

D0h.6 **AC**: ALU auxiliary carry flag

D0h.5 **F0**: General purpose user-definable flag

D0h.4~3 **RS1, RS0**: The contents of (RS1, RS0) enable the working register banks as:

00: Bank 0 (00h~07h)

01: Bank 1 (08h~0Fh)

10: Bank 2 (10h~17h)

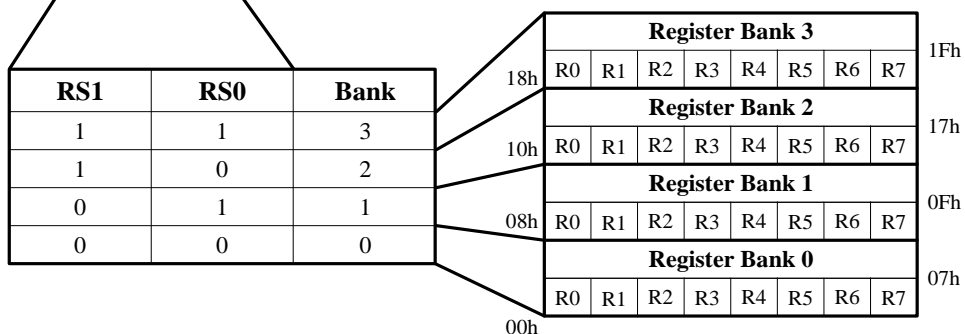
11: Bank 3 (18h~1Fh)

D0h.2 **OV**: ALU overflow flag

D0h.1 **F1**: General purpose user-definable flag

D0h.0 **P**: Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.

PSW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CY	AC	FO	RS1	RS0	OV	F1	P



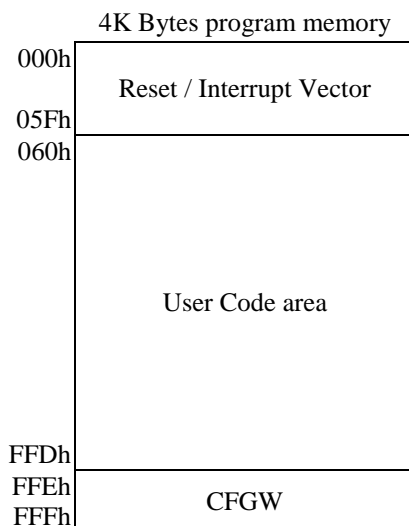
2. Memory

2.1 Program Memory

The **M5254/58** has a 4K Bytes MTP program memory, which can support In Circuit Programming (ICP) mode. The MTP program memory address continuous space (000h~FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The address space 000h~05Fh of program memory is occupied by Reset/Interrupt vectors as standard 8051. The last 2 bytes (FFEh~FFFh) is defined as chip Configuration Word (CFGWH, CFGWL), which is loaded into the device control registers upon power on reset (POR). CFGWL is copied to the SFR F7h after power on reset, software then take over CFGWL's control capability by modifying the SFR F7h.



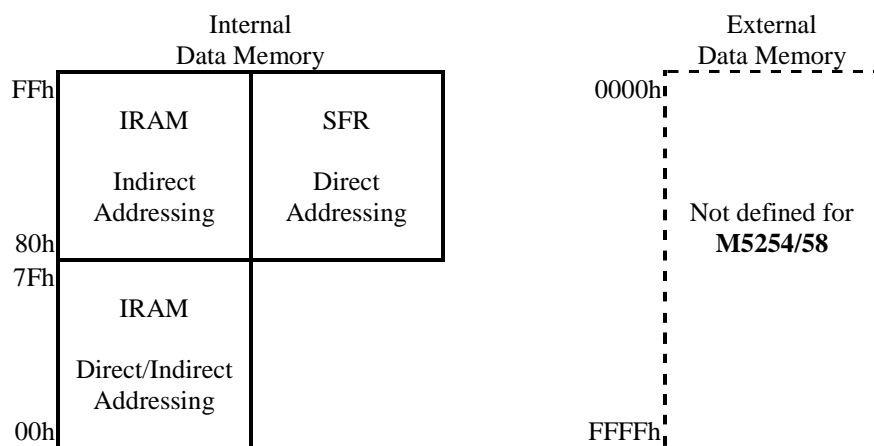
2.1.2 MTP ICP Mode

The MTP memory can be programmed by the tenx proprietary writer (**TWR98/TWR99**), which needs at least five wires (VCC, VSS, VPP, P3.0 and P3.1) to connect to this chip. If user wants to program the MTP memory on the target circuit board (In Circuit Program, ICP), these pins must be reserved sufficient freedom to be connected to the Writer. Beside 5-Wire mode, the Writer also provide 7-Wire mode for programming efficiency and speed.

Writer wire number	Pin connection
5-Wire	VCC, VSS, VPP, P3.0, P3.1
7-Wire	VCC, VSS, VPP, P3.0, P3.1, P3.3, P1.2 <i>Note:</i> P3.2 and P3.5 always output in this mode

2.2 Data Memory

The **M5254/58** only has the 8051's Internal Data Memory space, which consists of 256 Bytes IRAM and 51 SFRs. The space can be accessed through a rich instruction set. Comparing to the TM52 members, the 8051's External Data Memory space is not defined for **M5254/58**.

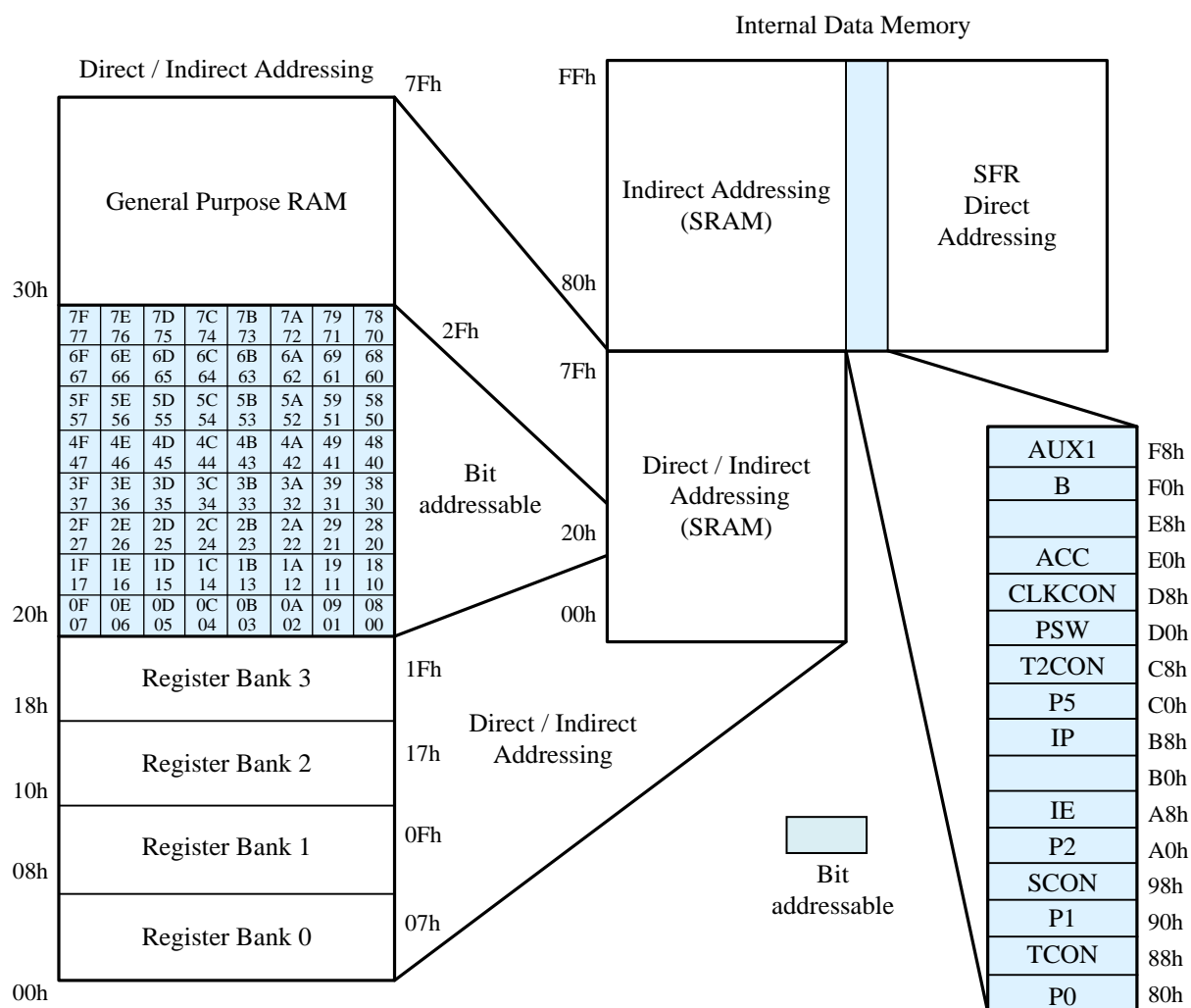


2.2.1 IRAM

IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.2.2 SFRs

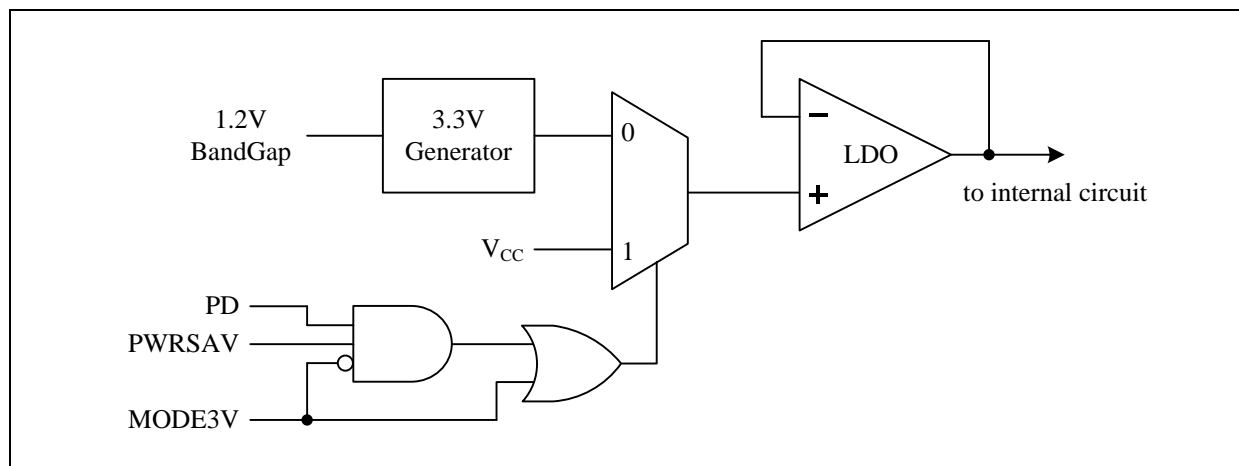
All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the **M5254/58**. Beside the standard 8051 SFRs, the device implements additional SFRs used to configure and access subsystems such as the ADC/PWM, which are unique to the **M5254/58**.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B							CFGWL
E8h								
E0h	ACC							
D8h	CLKCON							
D0h	PSW							
C8h	T2CON		RCP2L	RCP2H	TL2	TH2		
C0h								
B8h	IP	IPH	IP1	IP1H				
B0h	P3							
A8h	IE	INTE1	ADTKDT	ADCDH	TKDL	TKCON	CHSEL	
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PINMOD	
98h	SCON	SBUF	PWM0PRD	PWM0DH	PWM1PRD	PWM1DH		
90h	P1				OPTION	INTFLG	P1WKUP	
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH				PCON

3. Power

The **M5254/58** has a built-in internal low dropout regulator. When $\text{MODE3V}=0$, the voltage regulator outputs 3.3V power to the internal chip circuit. When $\text{MODE3V}=1$, the LDO is turned off, and the internal circuit receives a power supply directly from the V_{CC} pin. Because the LDO consumes $150\mu\text{A}$ for operation, turning off LDO by setting $\text{MODE3V}=1$ can reduce the chip current consumption. However, setting $\text{MODE3V}=1$ is only valid for an operating condition of $V_{CC} < 3.6\text{V}$. The PWRSV bit also control the LDO function. When $\text{MODE3V}=0$ and $\text{PWRSV}=1$, the LDO is turned off in Stop mode for saving power consumption. In addition, set PWRSV will affect the LVR/LVD setting.



LDO Regulator

MTP FFFh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		MODE3V	PWRSV	–	–

FFFh.3 **MODE3V**: 3V mode selection control bit

If this bit is set, the chip can be only operated in the condition of $V_{CC} < 3.6\text{V}$, and LDO is turned off to save current.

FFFh.2 **PWRSV**: Set 1 to reduce the chip's power consumption.

SFR 94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	VCCFLT	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **VCCFLT**: Set 1 to enhance the chip's power noise immunity

4. Reset

The **M5254/58** has four types of reset methods. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 24ms as chip warm up time, then downloads the CFGW register from MTP's last two bytes (Other Reset will not reload the CFGW). The Power on Reset needs VCC pin's voltage first discharge to near V_{SS} level, then rise beyond 1.9V.

4.2 Low Voltage Reset

The **M5254/58** offers LVR and Low Voltage Detection (LVD) functions. The LVR can be selected by CFGW as 2.9V, 2.3V, 1.9V or disable. The 2.3V LVD flag is available when LVR is 1.9V or disable. The MODE3V and PWRSAV CFGW bits also affect LVR/LVD function as tables below.

MODE3V=0 (5V mode)	CFGW		LDO	LVR	LVD	Function
	PWRSAV	LVRE				
Fast Slow Idle	X	00	ON	ON	–	LV Reset 2.9V
	X	01	ON	ON	–	LV Reset 2.3V
	X	10	ON	OFF	ON	LV Reset Disable
	X	11	ON	ON	ON	LV Reset 1.9V
Stop	0	00	ON	ON	–	LV Reset 2.9V
	0	01	ON	ON	–	LV Reset 2.3V
	0	10	ON	OFF	–	LV Reset Disable
	0	11	ON	ON	–	LV Reset 1.9V
	1	00	OFF	ON	–	LV Reset 1.9V
	1	01	OFF	ON	–	LV Reset 1.9V
	1	10	OFF	OFF	–	LV Reset Disable
	1	11	OFF	ON	–	LV Reset 1.9V

LDO, LVR and LVD function when MODE3V=0 (5V mode)

MODE3V=1 (3V mode)	CFGW		LDO	LVR	LVD	Function
	PWRSAV	LVRE				
Fast Slow Idle	0	00	OFF	ON	–	LV Reset 2.9V
	0	01	OFF	ON	–	LV Reset 2.3V
	0	10	OFF	OFF	ON	LV Reset Disable
	0	11	OFF	ON	ON	LV Reset 1.9V
	1	00	OFF	ON	–	LV Reset 1.9V
	1	01	OFF	ON	–	LV Reset 1.9V
	1	10	OFF	OFF	–	LV Reset Disable
	1	11	OFF	ON	–	LV Reset 1.9V
Stop	0	00	OFF	ON	–	LV Reset 2.9V
	0	01	OFF	ON	–	LV Reset 2.3V
	0	10	OFF	OFF	–	LV Reset Disable
	0	11	OFF	ON	–	LV Reset 1.9V
	1	00	OFF	ON	–	LV Reset 1.9V
	1	01	OFF	ON	–	LV Reset 1.9V
	1	10	OFF	OFF	–	LV Reset Disable
	1	11	OFF	ON	–	LV Reset 1.9V

LDO, LVR and LVD function when MODE3V=1 (3V mode)

4.3 External Pin Reset

External Pin Reset is active low. The RSTn pin needs to keep at least 2 SRC clock cycle long to be sampled by the chip. Pin Reset can be disabled or enabled by CFGW.

4.4 Watch Dog Timer Reset

WDT overflow Reset is disabled or enable SFR F7h. The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Stop mode. WDT overflow speed can be defined by WDTOSC SFR. WDT is cleared by chip Reset or CLRWDT SFR bit.

MTP FFFh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		MODE3V	PWRSV	—	—

FFFh.6 **XRSTE:** External Pin Reset control

0: Disable External Pin Reset

1: Enable External Pin Reset

FFFh.5~4 **LVRE:** Low Voltage Reset function select

00: Set LVR at 2.9V; LVD disable

01: Set LVR at 2.3V; LVD disable

10: LVR disable; LVD enable if not in Stop mode and MODE3V*PWRSV=0

11: Set LVR at 1.9V; LVD enable if not in Stop mode and MODE3V*PWRSV=0

SFR F7h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	WDTE		—	FRCF				
R/W	R/W		—	R/W				
Reset	—	—	—	—	—	—	—	—

F7h.7~6 **WDTE:** Watchdog Timer Reset control

0x: Watchdog Timer Reset disable

10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode

11: Watchdog Timer Reset always enable

Note: FW should not change FRCF while writing WDTE

Note3: The SFR F7h (CFGWL) is automatically loaded with MTP's 0xFFE data at power on reset and can be read/written as any other SFR register in normal mode. So the WDT functionality & FRC clock speed can be changed on CPU run time by S/W.

SFR 94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	VCCFLT	WDTOSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.5~4 **WDTOSC:** Watchdog Timer pre-scalar time select

00: 400ms WDT overflow rate

01: 200ms WDT overflow rate

10: 100ms WDT overflow rate

11: 50ms WDT overflow rate

SFR F8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	—	—	—	DPSEL
R/W	R/W	R/W	R/W	R/W	—	—	—	R/W
Reset	0	0	0	0	—	—	—	0

F8h.7 **CLRWDT:** Set 1 to clear WDT, H/W auto clear it at next clock cycle

SFR 95h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	—	TKIF	ADIF	—	IE2	P1IF	TF3
R/W	R	—	R/W	R/W	—	R/W	R/W	R/W
Reset	—	—	0	0	—	0	0	0

95h.7 **LVD:** Low Voltage Detect flag (2.3V)

Set by H/W when a low voltage occurs. The flag is valid when LVR is 1.9V or disabled. This flag is disabled in Stop mode or MODE3V=PWRSAV=1.

Note: also refer to AP-TM52XXXXX_02S about LVR Application Note.

System Clock frequency	6MHz (FXT)	3.7MHz (FRC/2)	< 2MHz
Minimum LVR level	LVR=2.9V	LVR=2.3V	LVR=1.9V

LVR setting table

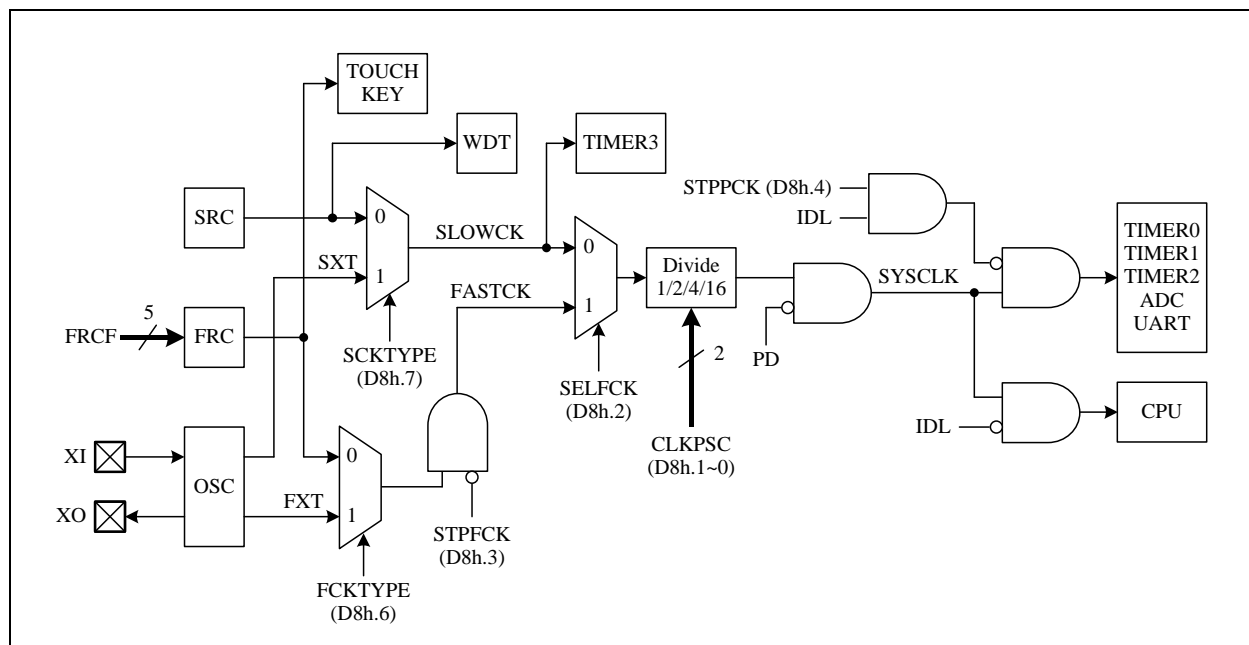
5. Clock Circuitry & Operation Mode

5.1 System Clock

The **M5254/58** is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock can be selected as **FXT** (Fast Crystal, 1~6 MHz) or **FRC/2** (Fast Internal RC, 7.3728 MHz /2). The Slow clock can be selected as **SXT** (Slow Crystal, 32 KHz) or **SRC** (Slow Internal RC, 80 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with SRC. Before switching to the Fast clock, S/W must select the Fast clock type in advance. S/W also has to select a proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In typical condition, 6 MHz System clock rate requires $V_{CC} > 2.5V$.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both **STPFCK=1** & **SELFCK=1**. It is recommended to write this SFR bit by bit.



Clock Structure

MTP FFEh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	—	—	—	FRCF				

FFEh.4~0 **FRCF**: FRC frequency adjustment.

FRC is trimmed to 7.3728 MHz in chip manufacturing. FRCF records the adjustment data.

SFR F7h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	WDTE		—	FRCF				
R/W	R/W		—	R/W				
Reset	—	—	—	—	—	—	—	—

F7h.4~0 **FRCF**: FRC frequency adjustment (*see Note3*)

00h=central frequency, 0Fh=highest frequency, 10h=lowest frequency.

SFR D8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	—	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	—	R/W	R/W	R/W	R/W	
Reset	0	0	—	0	0	0	1	1

- D8h.7 **SCKTYPE**: Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT, P2.0 and P2.1 are crystal pins
- D8h.6 **FCKTYPE**: Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT
- D8h.4 **STPPCK**: Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.
- D8h.3 **STPFCK**: Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
- D8h.2 **SELFCK**: System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock
- D8h.1~0 **CLKPSC**: System clock prescaler.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

SYSCLK	CLKCON (D8h)			
	bit7 SCKTYPE	bit6 FCKTYPE	bit3 STPFCK	bit2 SELFCK
Fast FXT	0/1	1	0	1
Fast FRC	0/1	0	0	1
Slow SXT	1	0/1	0/1	0
Slow SRC	0	0/1	0/1	0
Fast type change	0/1	0 \leftarrow \rightarrow 1	0/1	0
Slow type change	0 \leftarrow \rightarrow 1	0/1	0	1
Stop FRC/FXT	0/1	0/1	0 \rightarrow 1	0
Switch to FRC/FXT	0/1	0/1	0	0 \rightarrow 1
Switch to SRC/SXT	0/1	0/1	0	1 \rightarrow 0

Note: also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.

The chip can also output the "System clock divided by 2" signal (CKO) to P1.4 pin. CKO pin's output setting is controlled by TCOE SFR (*see section 7*).

5.2 Operation Modes

There are four operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The “STPPCK” bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK is set, only Timer3 and pin interrupts are alive in Idle Mode, others peripherals such as Timer0/1/2, UART and ADC are stop. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR. This mode is the so-called “Power Down” mode in standard 8051. In Stop mode, all clocks stop except the WDT could be alive if it is enabled. Stop Mode is terminated by Reset or pin wake up.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enable. (INTn=0 and EXn=1, n=0,1,2)

Note: FW must turn off Bandgap to obtain Tiny Current (ADCHS≠0b1011)

SFR 87h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	—	—	—	GF1	GF0	PD	IDL
R/W	R/W	—	—	—	R/W	R/W	R/W	R/W
Reset	0	—	—	—	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

6. Interrupt & Wake-up

The **M5254/58** has a 10-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	—	Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	P1IF	Port1 external pin change Interrupt (can wake up Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Stop mode)
0053	ADIF+TKIF	ADC/Touch Key Interrupt

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The P1WKUP SFR controls the individual Port1 pin's wake-up and interrupt capability. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR 96h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP**: P1.7~P1.0 pin individual Wake-up / Interrupt enable control

0: Disable

1: Enable

SFR A8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

- A8h.7 **EA**: Global interrupt enable control.
 0: Disable all Interrupts.
 1: Each interrupt is enabled or disabled by its individual interrupt control bit
- A8h.5 **ET2**: Timer2 interrupt enable
 0: Disable Timer2 interrupt
 1: Enable Timer2 interrupt
- A8h.4 **ES**: Serial Port (UART) interrupt enable
 0: Disable Serial Port (UART) interrupt
 1: Enable Serial Port (UART) interrupt
- A8h.3 **ET1**: Timer1 interrupt enable
 0: Disable Timer1 interrupt
 1: Enable Timer1 interrupt
- A8h.2 **EX1**: External INT1 pin Interrupt enable and Stop mode wake up enable
 0: Disable INT1 pin Interrupt and Stop mode wake up
 1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
- A8h.1 **ET0**: Timer0 interrupt enable
 0: Disable Timer0 interrupt
 1: Enable Timer0 interrupt
- A8h.0 **EX0**: External INT0 pin Interrupt enable and Stop mode wake up enable
 0: Disable INT0 pin Interrupt and Stop mode wake up
 1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR A9h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	–	–	–	–	ADTKIE	EX2	P1IE	TM3IE
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

- A9h.3 **ADTKIE**: ADC/Touch Key interrupt enable
 0: Disable ADC/Touch Key interrupt
 1: Enable ADC/Touch Key interrupt
- A9h.2 **EX2**: External INT2 pin Interrupt enable and Stop mode wake up enable
 0: Disable INT2 pin Interrupt and Stop mode wake up
 1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
- A9h.1 **P1IE**: Port1 pin change interrupt enable. This bit does not affect the Port1 pin's Stop mode wake up capability.
 0: Disable Port1 pin change interrupt
 1: Enable Port1 pin change interrupt
- A9h.0 **TM3IE**: Timer3 interrupt enable
 0: Disable Timer3 interrupt
 1: Enable Timer3 interrupt

SFR B9h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	—	—	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	—	—	0	0	0	0	0	0

SFR B8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	—	—	PT2	PS	PT1	PX1	PT0	PX0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
Reset	—	—	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2** : Timer2 Interrupt Priority control. (PT2H, PT2) =

11: Level 3 (highest priority)

10: Level 2

01: Level 1

00: Level 0 (lowest priority)

B9h.4, B8h.4 **PSH, PS** : Serial Port (UART) Interrupt Priority control. Definition as above.

B9h.3, B8h.3 **PT1H, PT1** : Timer1 Interrupt Priority control. Definition as above.

B9h.2, B8h.2 **PX1H, PX1** : External INT1 pin Interrupt Priority control. Definition as above.

B9h.1, B8h.1 **PT0H, PT0** : Timer0 Interrupt Priority control. Definition as above.

B9h.0, B8h.0 **PX0H, PX0** : External INT0 pin Interrupt Priority control. Definition as above.

SFR BBh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	—	—	—	—	PADTKIH	PX2H	PP1H	PT3H
R/W	—	—	—	—	R/W	R/W	R/W	R/W
Reset	—	—	—	—	0	0	0	0

SFR BAh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	—	—	—	—	PADTKI	PX2	PP1	PT3
R/W	—	—	—	—	R/W	R/W	R/W	R/W
Reset	—	—	—	—	0	0	0	0

BBh.3, BAh.3 **PADTKIH, PADTKI** : ADC/Touch Key Interrupt Priority control. Definition as above.

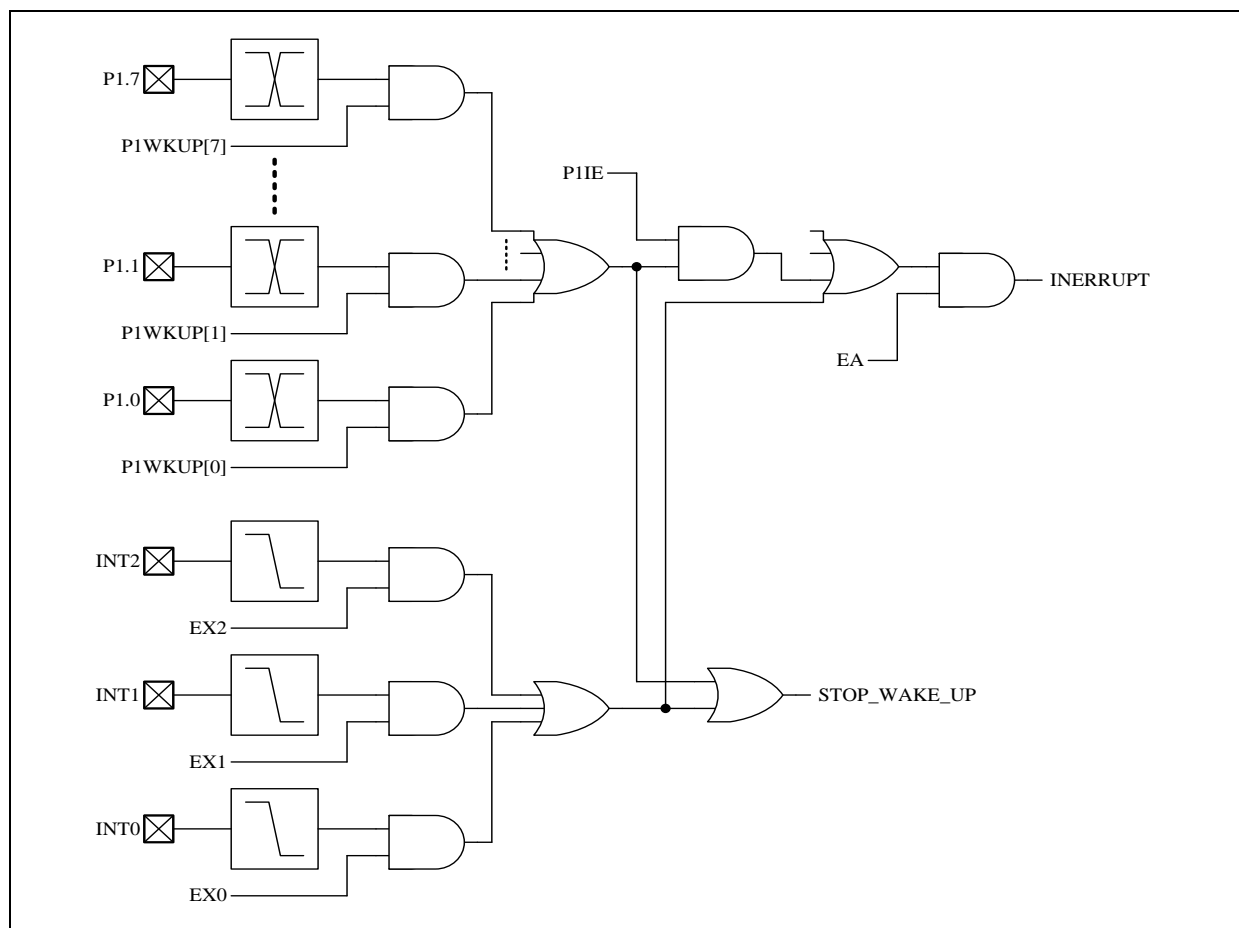
BBh.2, BAh.2 **PX2H, PX2** : External INT2 pin Interrupt Priority control. Definition as above.

BBh.1, BAh.1 **PP1H, PP1** : Port1 Pin Change Interrupt Priority control. Definition as above.

BBh.0, BAh.0 **PT3H, PT3** : Timer3 Interrupt Priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P3.7) and Port1 Change Interrupt. These pins also have the Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

SFR 88h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- 88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag.
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
- 88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin
- 88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
- 88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR 95h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	—	TKIF	ADIF	—	IE2	P1IF	TF3
R/W	R	—	R/W	R/W	—	R/W	R/W	R/W
Reset	—	—	0	0	—	0	0	0

95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag

Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1.

It is cleared automatically when the program performs the interrupt service routine.

S/W can write FBh to INTFLG to clear this bit.

95h.1 **P1IF:** Port1 pin change interrupt flag

Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P1WKUP).

P1IE does not affect this flag's setting.

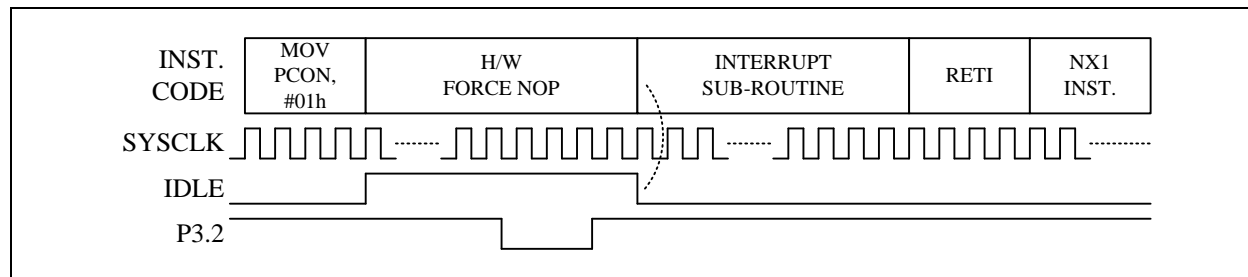
It is cleared automatically when the program performs the interrupt service routine.

S/W can write FDh to INTFLG to clear this bit.

Note5: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

6.3 Idle mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers, TK and UART) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR 87h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	—	—	—	GF1	GF0	PD	IDL
R/W	R/W	—	—	—	R/W	R/W	R/W	R/W
Reset	0	—	—	—	0	0	0	0

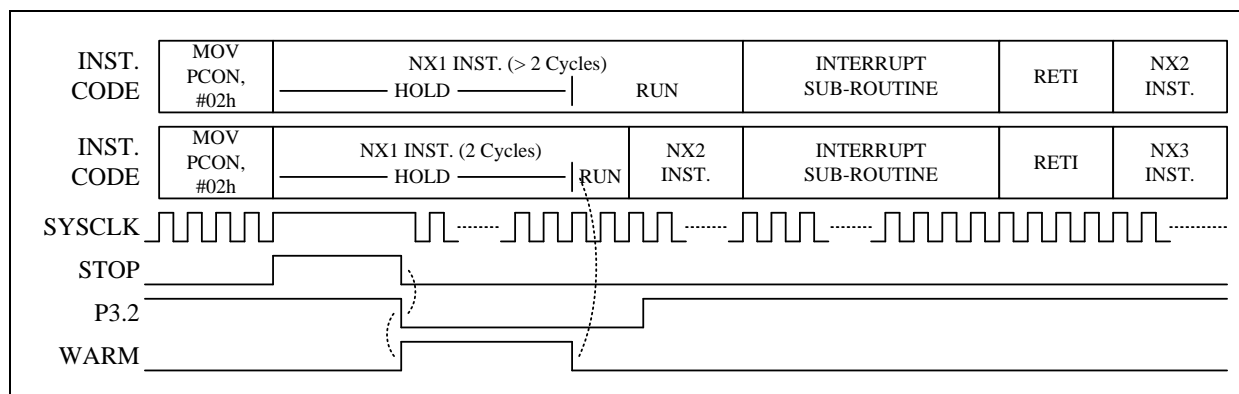
87h.1 **PD:** Power down control bit, set 1 to enter STOP mode.

87h.0 **IDL:** Idle mode control bit, set 1 to enter IDLE mode.

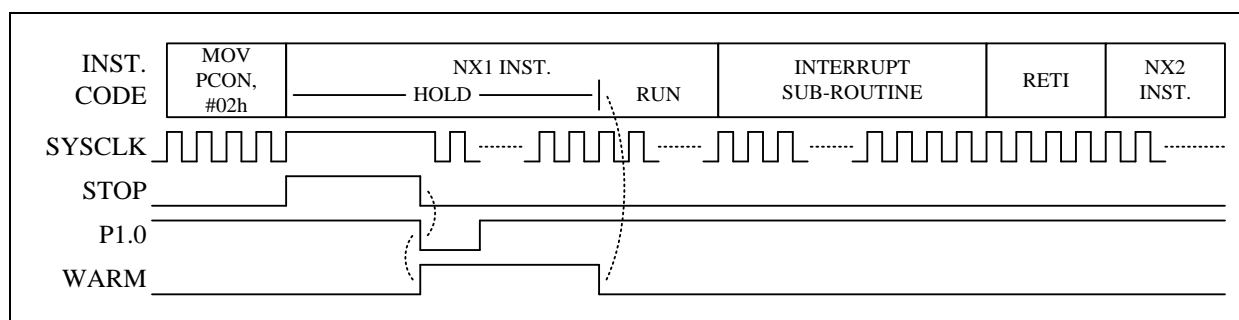
6.4 Stop mode Wake up and Interrupt

Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Stop mode wake up capability. Set P1WKUP bit 7~0 can enable P1.7~P1.0's Stop mode wake up capability. Upon Stop wake up, "the first instruction behind PD setting (PCON.1)" is executed immediately before Interrupt service. Interrupt entry requires EA=1 (P1WKUP also needs P1IE=1) and trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Stop mode wake up.

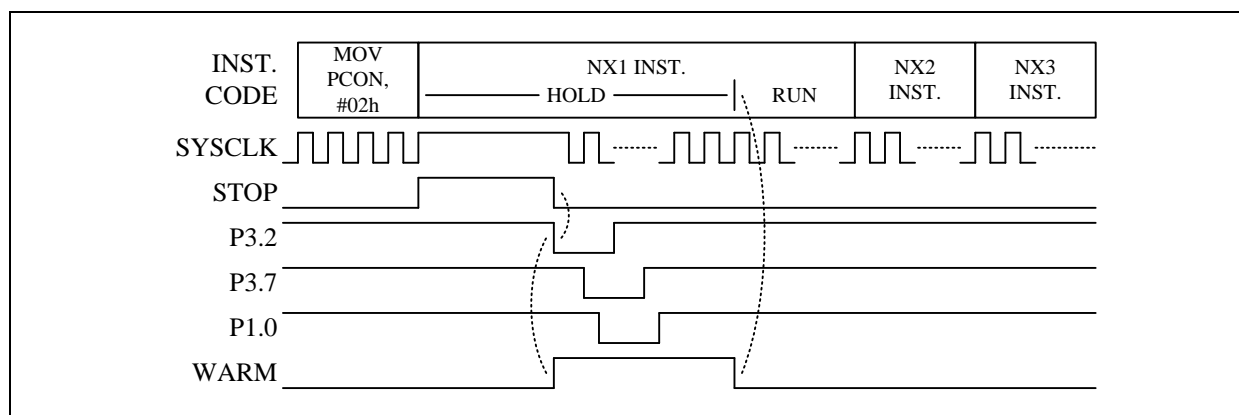
Note: It is recommended to place the NX1/NX2 with NOP Instruction in figures below.



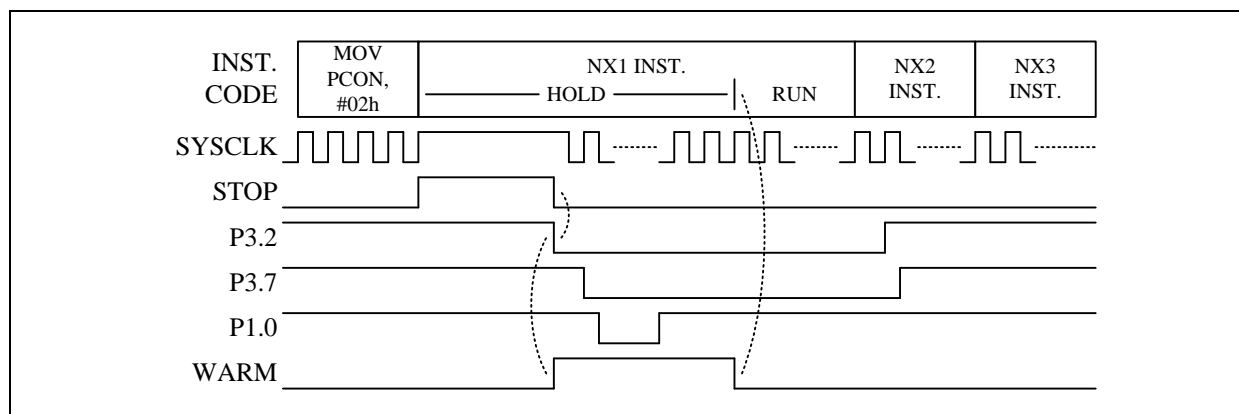
EA=EX0=1, P3.2 (INT0) is sampled after warm-up, Stop mode wake-up and Interrupt



EA=P1IE=P1WKUP=1, P1.0 change (not need clock sample), Stop mode wake-up and Interrupt



EA=EX0=EX2=P1WKUP=1, P1IE=0, Stop mode wake-up but not Interrupt. P3.2/P3.7 pulse too narrow



EX0=EX2=P1WKUP=P1IE=1, EA=0, Stop mode wake-up but not Interrupt

7. I/O Ports

The M5254/58 has total 18 multi-function I/O pins. All I/O pins follow the standard 8051 “Read-Modify-Write” feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR (ex: ANL P1, A; INC P2; CPL P3.0). Each I/O pins except P3.7 can operate in four different modes as the table below. P3.7 can be only used as Schmitt-trigger input or open-drain output, with pull-up resistor always enable. P3.7 pin is also shared with RSTn, INT2 and MTP VPP function.

Mode	Pin function (except P3.7)		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input	
	P3.0~P3.2	Others					
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N	
			1	Pull-up	Y	Y	
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N	
			1	Hi-Z	N	Y	
Mode 2	CMOS Output		0	Drive Low	N	N	
			1	Drive High	N	N	
Mode 3	Analog input for ADC or Touch Key, digital input buffer is disabled		X (don't care)	—	N	N	

I/O Pin Function Table

If an I/O pin (except P3.7) is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry. Beside I/O port function, each pin has one or more alternative functions, such as Touch Key, ADC and PWM. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins also have standard 8051 auxiliary definition (INT0/1, T0/1/2, T2EX, RXD/TXD) as table below.

Pin Name	8051	Wake-up	ADC	TK	Mode3	others
P1.0	T2	Y	AD4	TK4	AD4/TK4	T2O
P1.1	T2EX	Y	AD5	TK5	AD5/TK5	
P1.2		Y	AD6	TK6	AD6/TK6	PWM0
P1.3		Y	AD7	TK7	AD7/TK7	PWM1
P1.4		Y	AD8	TK8	AD8/TK8	CKO
P1.5		Y	AD9	CLD	AD9/CLD	
P1.6		Y		TK9	TK9	
P1.7		Y		TK10	TK10	
P2.0						XI
P2.1						XO
P3.0	RXD		AD3	TK3	AD3/TK3	
P3.1	TXD		AD2	TK2	AD2/TK2	
P3.2	INT0	Y	AD1	TK1	AD1/TK1	
P3.3	INT1	Y	AD0	TK0	AD0/TK0	
P3.4	T0			TK13	TK13	T0O
P3.5	T1			TK12	TK12	
P3.6				TK11	TK11	
P3.7		Y				INT2, RSTn, VPP

Pin multi-function Table

To use the 8051 auxiliary function of Port1/Port3 pins (INT0/1, T0/1/2, T2EX, RXD/TXD), S/W needs to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n / P3.n SFR at 1. In the PWM and Clock output pin usage, the Pin Mode control is still effective. For example, while P1.2 is switched to PWM0 by setting PWM0OE=1, Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS output. When P2.0/P2.1 is used for Crystal OSC circuitry, user should select the pins as Mode0 and set the P2.n SFR to 1. The necessary SFR setting for pin's alternative functions is list below.

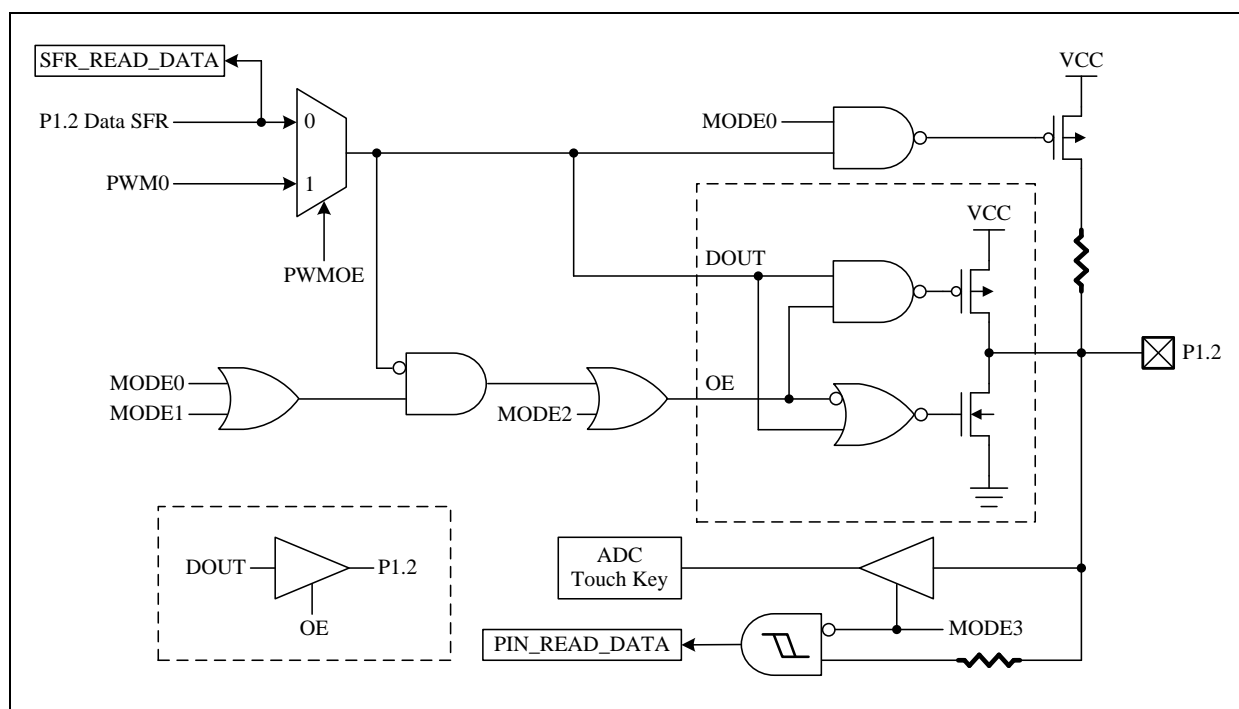
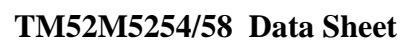
Alternative Function	Mode	Px.n SFR data	Pin State	other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1	0	1	Input with Pull-up	—
	1	1	Input	
RXD, TXD	0	1	Input with Pull-up/Pseudo Open Drain Output	—
	1	1	Input/Pseudo Open Drain Output	
CKO, T00, T20, PWM0, PWM1	0	X	Open Drain Output with Pull-up	PINMOD, T0OE
	1	X	Open Drain Output	
	2	X	CMOS Push-Pull output	
TK0~TK13	0	1	Touch Key Idling, Pull-up	—
	3	X	Touch Key Scanning	
CLD	3	X	Touch Key Capacitor Connection	—
ADC0~ADC9	3	X	ADC Voltage Input	—
XI, XO	0	1	FXT/SXT Crystal Oscillation	CLKCON
INT2, RSTn	—	1	Input with Pull-up	—

Mode Setting for Pin Alternative Function

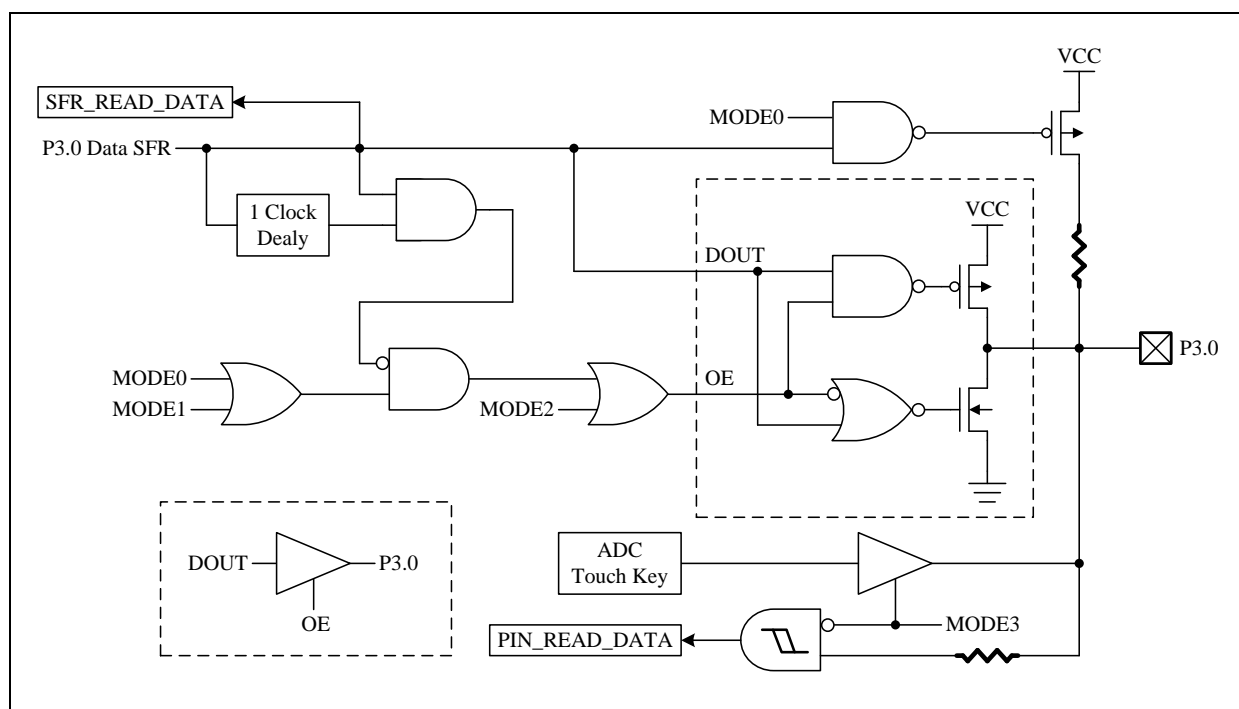
For tables above, a “**CMOS Output**” pin means it can sink and drive at least 4 mA current. It is not recommended to use such pin as input function.

An “**Open Drain**” pin means it can sink at least 4 mA current but only drive a small current (<20 μ A). It can be used as input or output function and typically needs an external pull up resistor.

An 8051 standard pin is a “**Pseudo Open Drain**” pin. It can sink at least 4 mA current when output is at low level, and drives at least 4 mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20 μ A) to maintain the pin at high level. It can be used as input or output function.



P1.2 Pin Structure



P3.0 Pin Structure

SFR 90h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR A0h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.1~0 **P2.1~P2.0:** P2.1~P2.0 data

SFR B0h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7 **P3.7:** P3.7 data, also controls the pin's I/O mode. If the P3.7 SFR data is "1", the P3.7 is assigned as Schmitt-trigger input mode; otherwise, it is assigned as open-drain output mode.

B0h.6~0 **P3.6~P3.0:** P3.6~P3.0 data

SFR D8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	—	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	—	R/W	R/W	R/W	R/W	
Reset	0	0	—	0	0	0	1	1

D8h.7 **SCKTYPE:** Set 1 to enable P2.0 and P2.1 pin's crystal oscillation mode

D8h.6 **FCKTYPE:** Set 1 to enable P2.0 and P2.1 pin's crystal oscillation mode

SFR A2h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A2h.7~6 **P1MOD3:** P1.3 pin control.

00: Mode0

01: Mode1

10: Mode2

11: Mode3, P1.3 is ADC or Touch Key input.

A2h.5~4 **P1MOD2:** P1.2 pin control.

00: Mode0

01: Mode1

10: Mode2

11: Mode3, P1.2 is ADC or Touch Key input.

A2h.3~2 **P1MOD1:** P1.1 pin control.

00: Mode0

01: Mode1

10: Mode2

11: Mode3, P1.1 is ADC or Touch Key input.

A2h.1~0 **P1MOD0:** P1.0 pin control.

00: Mode0

01: Mode1

10: Mode2

11: Mode3, P1.0 is ADC or Touch Key input.

SFR A3h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A3h.7~6 **P1MOD7**: P1.7 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P1.7 is Touch Key input.

A3h.5~4 **P1MOD6**: P1.6 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P1.6 is Touch Key input.

A3h.3~2 **P1MOD5**: P1.5 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P1.5 is ADC input or Touch Key CLD.

A3h.1~0 **P1MOD4**: P1.4 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P1.4 is ADC or Touch Key input.

SFR A4h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3**: P3.3 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.3 is ADC or Touch Key input.

A4h.5~4 **P3MOD2**: P3.2 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.2 is ADC or Touch Key input.

A4h.3~2 **P3MOD1**: P3.1 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.1 is ADC or Touch Key input.

A4h.1~0 **P3MOD0**: P3.0 pin control.

- 00: Mode0
- 01: Mode1
- 10: Mode2
- 11: Mode3, P3.0 is ADC or Touch Key input.

SFR A5h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	T0OE	—	P3MOD6		P3MOD5		P3MOD4	
R/W	R/W	—	R/W		R/W		R/W	
Reset	0	—	0	0	0	0	0	0

- A5h.7 **T0OE**: Timer0 signal output (T0O) control
 0: Disable "Timer0 overflow divided by 64" output to P3.4 pin
 1: Enable "Timer0 overflow divided by 64" output to P3.4 pin

- A5h.5~4 **P3MOD6**: P3.6 pin control.
 00: Mode0
 01: Mode1
 10: Mode2
 11: Mode3, P3.6 is Touch Key input.

- A5h.3~2 **P3MOD5**: P3.5 pin control.
 00: Mode0
 01: Mode1
 10: Mode2
 11: Mode3, P3.5 is Touch Key input.

- A5h.1~0 **P3MOD4**: P3.4 pin control.
 00: Mode0
 01: Mode1
 10: Mode2
 11: Mode3, P3.4 is Touch Key input.

SFR A6h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0OE	TCOE	T2OE	P2MOD1		P2MOD0	
R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	1	0	1

- A6h.7 **PWM1OE**: PWM1 control
 0: PWM1 disable
 1: PWM1 enable and signal output to P1.3 pin
- A6h.6 **PWM0OE**: PWM0 control
 0: PWM0 disable
 1: PWM0 enable and signal output to P1.2 pin
- A6h.5 **TCOE**: System clock signal output (CKO) control
 0: Disable "System clock divided by 2" output to P1.4 pin
 1: Enable "System clock divided by 2" output to P1.4 pin
- A6h.4 **T2OE**: Timer2 signal output (T2O) control
 0: Disable "Timer2 overflow divided by 2" output to P1.0 pin
 1: Enable "Timer2 overflow divided by 2" output to P1.0 pin

- A6h.3~2 **P2MOD1**: P2.1 pin control.
 00: Mode0
 01: Mode1
 10: Mode2
 11: not defined

- A6h.1~0 **P2MOD0**: P2.0 pin control.
 00: Mode0
 01: Mode1
 10: Mode2
 11: not defined

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Timer3 is used for a real-time clock count with SXT or SRC timing source. Compare to the traditional 12T 8051, the chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every “2 System clock” rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device.

In addition to the standard 8051 timers function. The T0O pin can output the “Timer0 overflow divided by 64” signal, and the T2O pin can output the “Timer2 overflow divided by 2” signal. The T0O and T2O are useful for Buzzer or IR application. (*see Section7*, output setting for T0O, T2O).

8.1 Timer0 / Timer1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

SFR 88h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- 88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.
- 88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs
- 88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.
- 88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR 89h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

- 89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
- 89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge
- 89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops
- 89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

- 89h.2 **CT0N:** Timer0 Counter/Timer select bit
 0: Timer mode, Timer0 data increases at 2 System clock cycle rate
 1: Counter mode, Timer0 data increases at T0 pin's negative edge

- 89h.1~0 **TMOD0:** Timer0 mode select
 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
 01: 16-bit timer/counter
 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR 8Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR 8Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR 8Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR 8Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.

SFR C8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

- C8h.7 **TF2:** Timer2 overflow flag
 Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
- C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
 Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
- C8h.5 **RCLK:** UART receive clock control bit
 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

- C8h.4 **TCLK:** UART transmit clock control bit
 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
- C8h.3 **EXEN2:** T2EX pin enable
 0: T2EX pin disable
 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
- C8h.2 **TR2:** Timer2 run control
 0: Timer2 stops
 1: Timer2 runs
- C8h.1 **CT2N:** Timer2 Counter/Timer select bit
 0: Timer mode, Timer2 data increases at 2 System clock cycle rate
 1: Counter mode, Timer2 data increases at T2 pin's negative edge
- C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1.
 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1.
 If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.

SFR CAh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR CBh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR CCh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

SFR CDh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

8.3 Timer3

Timer3 works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 32768, 16384, 8192, or 128 depending on the TM3PSC SFR. The Timer3 clock source is Slow clock (SRC or SXT). This is ideal for real-time-clock (RTC) functionality when the clock source is SXT.

SFR F8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	—	—	—	DPSEL
R/W	R/W	R/W	R/W	R/W	—	—	—	R/W
Reset	0	0	0	0	—	—	—	0

F8h.6 **CLRTM3**: Set 1 to clear Timer3, H/W auto clear it at next clock cycle.

SFR 94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	VCCFLT	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.1~0 **TM3PSC**: Timer3 Interrupt rate

00: Timer3 Interrupt rate is 32768 Slow clock cycle

01: Timer3 Interrupt rate is 16384 Slow clock cycle

10: Timer3 Interrupt rate is 8192 Slow clock cycle

11: Timer3 Interrupt rate is 128 Slow clock cycle

SFR 95h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	—	TKIF	ADIF	—	IE2	P1IF	TF3
R/W	R	—	R/W	R/W	—	R/W	R/W	R/W
Reset	—	—	0	0	—	0	0	0

95h.0 **TF3**: Timer3 Interrupt Flag

Set by H/W when Timer3 reaches TM3PSC setting cycles. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (*Note5*)

Note6: also refer to Section 6 for more information about Timer0/1/2/3 Interrupt enable and priority.

9. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR 87h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	—	—	—	GF1	GF0	PD	IDL
R/W	R/W	—	—	—	R/W	R/W	R/W	R/W
Reset	0	—	—	—	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit

0: Disable UART double baud rate

1: Enable UART double baud rate

SFR 94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	VCCFLT	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.7 **UART1W:** One wire UART mode enable, both TXD/RXD use P3.1 pin

0: Disable one wire UART mode

1: Enable one wire UART mode

SFR 98h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1

00: Mode0: 8 bit shift register, Baud Rate= $F_{SYSCLK}/2$

01: Mode1: 8 bit UART, Baud Rate is variable

10: Mode2: 9 bit UART, Baud Rate= $F_{SYSCLK}/32$ or/64

11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2

SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable

0: Disable reception

1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag

Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag

Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR 99h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	—	—	—	—	—	—	—	—

99h.7~0 **SBUF**: UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency, the UART baud rate is calculated as below.

- **Mode 0:**
Baud Rate = $F_{\text{SYSCLK}}/2$
- **Mode 1, 3:** if using Timer1 auto reload mode
Baud Rate = $(\text{SMOD} + 1) \times F_{\text{SYSCLK}} / (32 \times 2 \times (256 - \text{TH1}))$
- **Mode 1, 3:** if using Timer2
Baud Rate = $\text{Timer2 overflow rate} / 16 = F_{\text{SYSCLK}} / (32 \times (65536 - \text{RCP2H}, \text{RCP2L}))$
- **Mode 2:**
Baud Rate = $(\text{SMOD} + 1) \times F_{\text{SYSCLK}} / 64$

Note6: also refer to Section 6 for more information about UART Interrupt enable and priority.

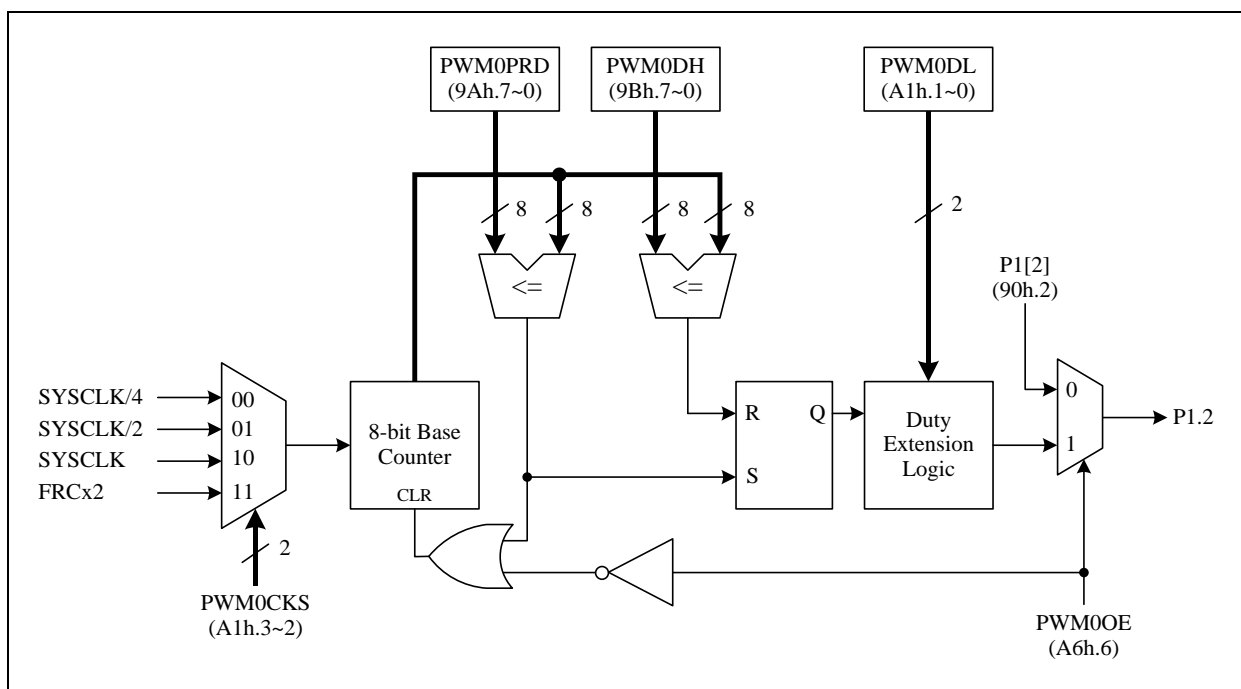
Note: also refer to Section 8 for more information about how Timer2 controls UART clock.

10. PWMs

The **M5254/58** has two independent PWM modules, PWM0 and PWM1. The PWM can generate a fixed frequency waveform with 1024 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRCx2) or F_{SYSCLK} divided by 1, 2, or 4 as its clock source. A spread LSB technique allows PWM to run its frequency at the “PWM clock divided by 256” instead of at the “PWM clock divided by 1024”, which means the PWM is four times faster than normal. The advantage of a higher PWM frequency is that the post RC filter can transform the PWM signal to a more stable DC voltage level.

The PWM output signal resets to a low level whenever the 8-bit base counter matches the 8-bit MSB of the PWM duty register. When the base counter rolls over, the 2-bit LSB of the PWM duty register decides whether to set the PWM output signal high immediately or set it high after one clock cycle delay. The PWM period can be set by writing the period value to the 8-bit PWM period register.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (*see section 7*)



PWM Structure

SFR 9Ah	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRD	PWM0PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ah.7~0 **PWM0PRD**: PWM0 8-bit period register

SFR 9Bh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Bh.7~0 **PWM0DH**: bits 9~2 of the PWM0 10-bit duty register

SFR 9Ch	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRD	PWM1PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ch.7~0 **PWM1PRD**: PWM1 8-bit period register

SFR 9Dh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Dh.7~0 **PWM1DH**: bits 9~2 of the PWM1 10-bit duty register

SFR A1h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
R/W	R/W		R/W		R/W		R/W	
Reset	1	0	0	0	1	0	0	0

A1h.7~6 **PWM1CKS**: PWM1 clock source

- 00: $F_{SYSCLK}/4$
- 01: $F_{SYSCLK}/2$
- 10: F_{SYSCLK}
- 11: $FRCx2$

A1h.5~4 **PWM1DL**: bits 1~0 of the PWM1 10-bit duty register

A1h.3~2 **PWM0CKS**: PWM0 clock source

- 00: $F_{SYSCLK}/4$
- 01: $F_{SYSCLK}/2$
- 10: F_{SYSCLK}
- 11: $FRCx2$

A1h.1~0 **PWM0DL**: bits 1~0 of the PWM0 10-bit duty register

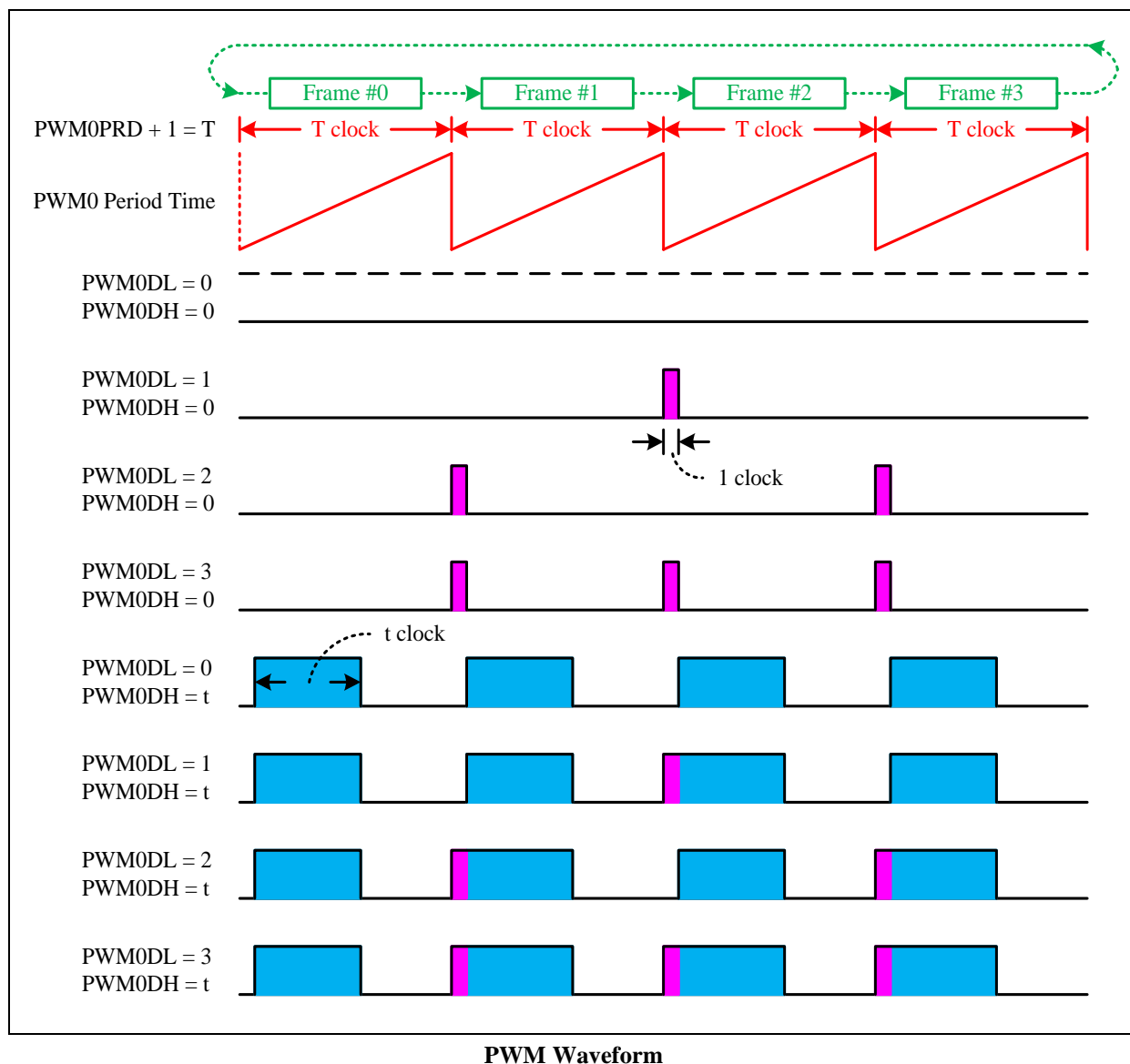
SFR A6h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1OE	PWM0OE	TCOE	T2OE	P2MOD1		P2MOD0	
R/W	R/W	R/W	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	1	0	1

A6h.7 **PWM1OE**: PWM1 control

- 0: PWM1 disable
- 1: PWM1 enable and signal output to P1.3 pin

A6h.6 **PWM0OE**: PWM0 control

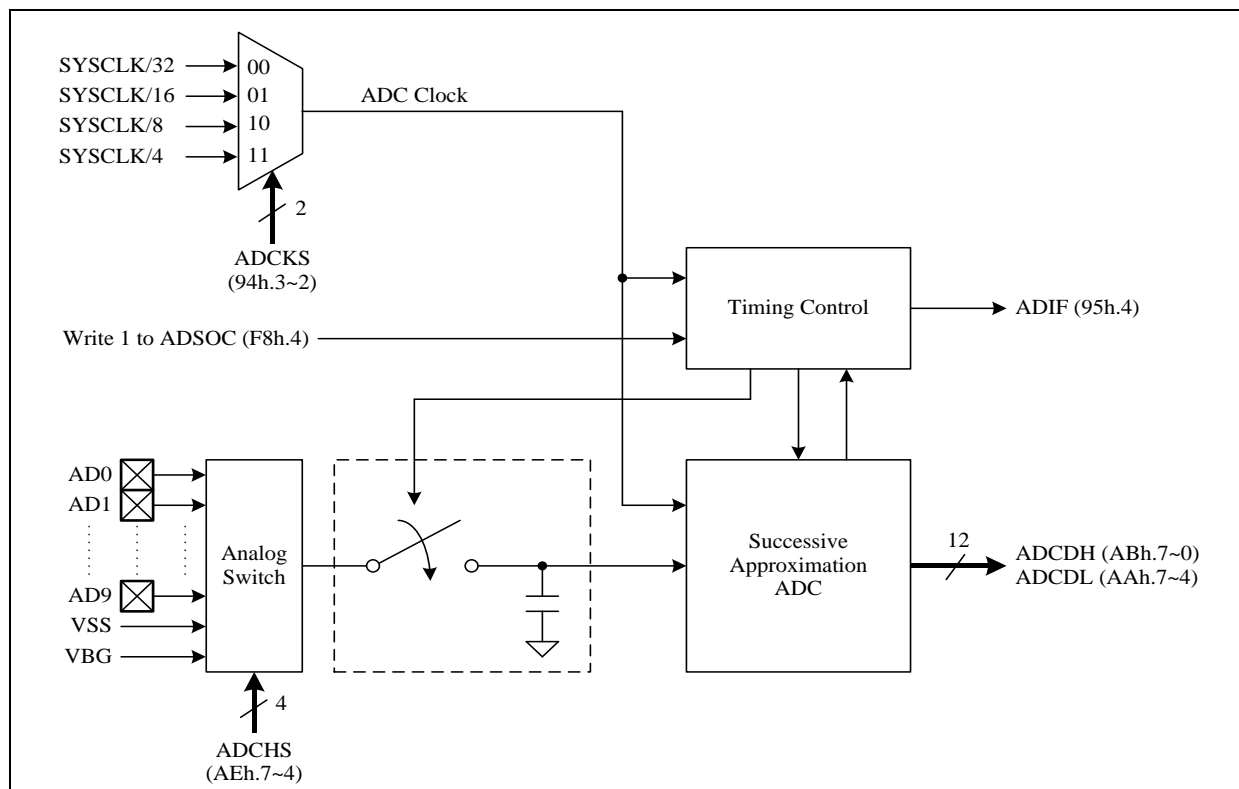
- 0: PWM0 disable
- 1: PWM0 enable and signal output to P1.2 pin



11. ADC

The 12-bit ADC supports 12-channel analog inputs, which include AD0~AD9 pins, V_{SS} and $1.2V V_{BG}$. To use the ADC, S/W needs to select ADC clock frequency less than 1MHz by setting the ADCKS. The ADC channel's pin mode must be set to Mode3 (see section7) to disable the pin digital input path.

S/W launches the ADC conversion by setting the ADSOC bit. The ADC unit requires 50 ADC clock cycles to complete a conversion. After the end of conversion, H/W clears ADSOC bit and set the ADIF interrupt flag. The ADIF flag can be cleared by writing EFh to INTFLG or writing "1" to ADSOC bit.



SFR F8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	—	—	—	DPSEL
R/W	R/W	R/W	R/W	R/W	—	—	—	R/W
Reset	0	0	0	0	—	—	—	0

F8h.4 **ADSOC**: ADC Start of Conversion

Set 1 to start ADC conversion. It is cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

SFR 94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	VCCFLT	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.3~2 **ADCKS**: ADC clock rate select

- 00: $F_{SYSCLK}/32$
- 01: $F_{SYSCLK}/16$
- 10: $F_{SYSCLK}/8$
- 11: $F_{SYSCLK}/4$

SFR 95h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	PIIF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag

Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag. (**Note5**)

SFR AAh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADCDL				TKEOC	TKOVF	TKDH	
R/W	R				R	R	R	
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR ABh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR AEh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				TKCHS			
R/W	R/W				R/W			
Reset	1	1	1	1	1	1	1	1

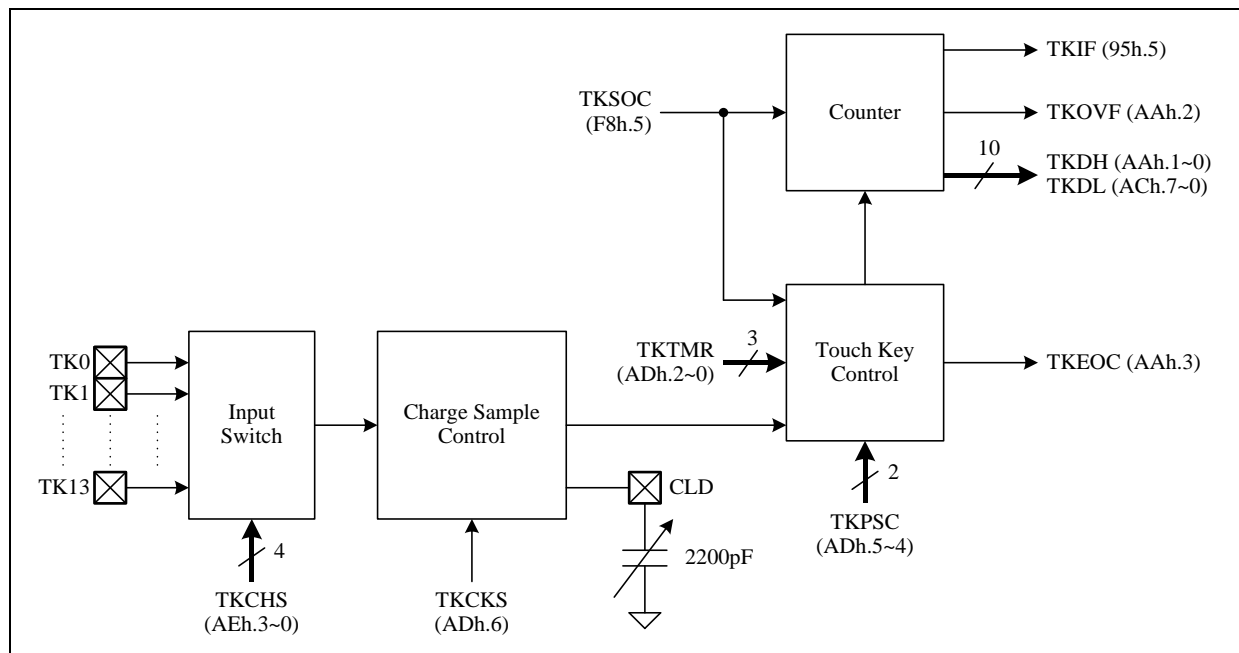
AEh.7~4 **ADCHS:** ADC channel select

0000: AD0 (P3.3)
0001: AD1 (P3.2)
0010: AD2 (P3.1)
0011: AD3 (P3.0)
0100: AD4 (P1.0)
0101: AD5 (P1.1)
0110: AD6 (P1.2)
0111: AD7 (P1.3)
1000: AD8 (P1.4)
1001: AD9 (P1.5)
1010: V_{SS}
1011: V_{BG} (Internal Bandgap Reference Voltage)
11xx: Undefined

Note: FW must turn off Bandgap to obtain Tiny Current (ADCHS ≠ 0b1011)

12. Touch Key (M5258 only)

The Touch Key unit offers an easy, simple and reliable method to implement finger touch detection. During the key scan operation, it only requires an external capacitor component on CLD pin. The device support 14 channels touch key detection.



Touch Key Structure

To use the Touch Key, user must setup the Pin Mode (*see Section 7*) correctly as below table. Setting Mode0 for an Idling Touch Key pin can pull up the pin and reduce the mutual interference between the adjacent keys. While a TK pin is under scanning, user must set the pin to Mode3 to disable the pull up resistor.

P1MODx / P3MODx setting for Touch Key	TK0~TK13	CLD
Pin is Touch Key, Idling	Mode0/3	Mode3
Pin is Touch Key, Scanning	Mode3	Mode3

S/W set the **TKSOC** bit to start Touch Key conversion. After the end of conversion, H/W clears **TKSOC** and set the **TKIF** interrupt flag. However, if the **SYSCLK** is too slow, H/W might fail to clear **TKSOC** and to set **TKIF** because of clock sampling rate. The **TKIF** bit can be cleared by writing DFh to **INTFLG** or writing 1 to the **TKSOC**. **TKEOC**=0 means conversion is in process. **TKEOC**=1 means the conversion is finished and the touch key counting result is stored into the 10-bits TK data counter **TKDH** and **TKDL**. The larger TK pin capacitance is, the smaller TK data counter is. After **TKEOC**=1, user must wait at least 50us for next conversion. (CLD discharge time is in proportion to CLD capacitance, also refer to [AP-TM52_57XX_Touch_02S](#)). If **TKOVF**=1, means conversion overflow. S/W can reduce/increase **TKTMR** to reduce/increase the TK counting result.

SFR F8h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	—	—	—	DPSEL
R/W	R/W	R/W	R/W	R/W	—	—	—	R/W
Reset	0	0	0	0	—	—	—	0

F8h.5 TKSOC: Touch Key Start of Conversion

Set 1 to start Touch Key conversion. If **SYSCLK** is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

SFR 95h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	PIIF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.5 **TKIF:** Touch Key Interrupt Flag

Set by H/W at the end of Touch Key conversion if SYSCLK is fast enough. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag. (*Note5*)

SFR AAh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADC DL				TKEOC	TKOVF	TKDH	
R/W	R				R	R	R	
Reset	–	–	–	–	–	–	–	–

AAh.3 **TKEOC:** Touch Key end of conversion flag, TKEOC may have 3μs delay after TKSOC=1, so F/W must wait enough time before polling this Flag.

0: Indicates conversion is in progress

1: Indicates conversion is finished

AAh.2 **TKOVF:** Touch Key counter overflow

0: Indicates that the counter has not overflow

1: Indicates that the counter has overflow

AAh.1~0 **TKDH:** Touch Key counter data bit 9~8

SFR Ach	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKDL	TKDL							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ACh.7~0 **TKDL:** Touch Key counter data bit 7~0

SFR ADh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON	TKPD	TKCKS	TKPSC		–	TKTMR		
R/W	R/W	R/W	R/W		–	R/W		
Reset	1	1	0	0	–	1	0	0

ADh.7 **TKPD:** Touch Key power down

0: Touch Key enable

1: Touch Key disable

ADh.6 **TKCKS:** Touch Key counter clock select

0: FRC/4

1: FRC/2

ADh.5~4 **TKPSC:** Touch Key data prescaler select

00: Touch Key data divided by 1

01: Touch Key data divided by 2

10: Touch Key data divided by 4

11: Touch Key data divided by 8

ADh.2~0 **TKTMR:** Touch Key conversion time select

TKTMR adjusts the value of Touch Key reference voltage. A larger value of TKTMR requires a longer charging time, which can affect the sensitivity of touch sensing.

000: Conversion time shortest

...

111: Conversion time longest

SFR AEh	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				TKCHS			
R/W	R/W				R/W			
Reset	1	1	1	1	1	1	1	1

AEh.3~0 **TKCHS:** Touch Key channel select

0000: TK0 (P3.3)
 0001: TK1 (P3.2)
 0010: TK2 (P3.1)
 0011: TK3 (P3.0)
 0100: TK4 (P1.0)
 0101: TK5 (P1.1)
 0110: TK6 (P1.2)
 0111: TK7 (P1.3)
 1000: TK8 (P1.4)
 1001: TK9 (P1.6)
 1010: TK10 (P1.7)
 1011: TK11 (P3.6)
 1100: TK12 (P3.5)
 1101: TK13 (P3.4)
 111x: Undefined

Note6: also refer to Section 6 for more information about Touch Key Interrupt enable and priority.

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	SP	SP							
82h	0000-0000	DPL	DPL							
83h	0000-0000	DPH	DPH							
87h	0xxx-0000	PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	TL0	TL0							
8Bh	0000-0000	TL1	TL1							
8Ch	0000-0000	TH0	TH0							
8Dh	0000-0000	TH1	TH1							
90h	1111-1111	P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
94h	0000-0000	OPTION	UART1W	VCCFLT	WDTPSC		ADCKS		TM3PSC	
95h	xx00-x000	INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
96h	0000-0000	P1WKUP	P1WKUP							
98h	0000-0000	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	SBUF	SBUF							
9Ah	1111-1111	PWM0PRD	PWM0PRD							
9Bh	1000-0000	PWM0DH	PWM0DH							
9Ch	1111-1111	PWM1PRD	PWM1PRD							
9Dh	1000-0000	PWM1DH	PWM1DH							
A0h	1111-1111	P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	1000-1000	PWMCON	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
A2h	0000-0000	P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0000-0000	P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0x00-0000	P3MODH	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
A6h	0000-0101	PINMOD	PWM1OE	PWM0OE	TCOE	T2OE	P2MOD1		P2MOD0	
A8h	0x00-0000	IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	xxxx-0000	INTE1	–	–	–	–	ADTKIE	EX2	P1IE	TM3IE
AAh	xxxx-xxxx	ADTKDT	ADCDL				TKEOC	TKOVF	TKDH	
ABh	xxxx-xxxx	ADCDH	ADCDH							
ACH	xxxx-xxxx	TKDL	TKDL							
ADh	1100-x100	TKCON	TKPD	TKCKS	TKPSC		–	TKTMR		
Aeh	1111-1111	CHSEL	ADCHS				TKCHS			
B0h	1111-1111	P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B8h	xx00-0000	IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	xxxx-0000	IP1	–	–	–	–	PADTKI	PX2	PP1	PT3
BBh	xxxx-0000	IP1H	–	–	–	–	PADTKIH	PX2H	PP1H	PT3H
C8h	0000-0000	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
CAh	0000-0000	RCP2L	RCP2L							
CBh	0000-0000	RCP2H	RCP2H							
CCh	0000-0000	TL2	TL2							
CDh	0000-0000	TH2	TH2							
D0h	0000-0000	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
D8h	00x0-0011	CLKCON	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
E0h	0000-0000	ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
F0h	0000-0000	B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F7h	xxxx-xxxx	CFGWL	WDTE		–	FRCF				
F8h	0000-xxx0	AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	–	–	–	DPSEL

MTP Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FFeH	CFGWL	–		–	FRCF				
FFFh	CFGWH	PROT	XRSTE	LVRE		MODE3V	PWRSVAV	–	–

SFR & CFGW DESCRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
80h	P0	7~0	P0	R/W	FFh	Port0 has no pin out, so P0 is used as general purpose register
81h	SP	7~0	SP	R/W	07h	Stack Point
82h	DPL	7~0	DPL	R/W	00h	Data Point low byte
83h	DPH	7~0	DPH	R/W	00h	Data Point high byte
87h	PCON	7	SMOD	R/W	0	Set 1 to enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter STOP mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter IDLE mode
88h	TCON	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	TMOD	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	TL0	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	TL1	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	TH0	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	TH1	7~0	TH1	R/W	00h	Timer1 data high byte

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
90h	P1	7~0	P1	R/W	FFh	Port1 data
94h	OPTION	7	UART1W	R/W	0	Set 1 to enable one wire UART mode, both TXD/RXD use P3.1 pin.
		6	VCCFLT	R/W	0	Set 1 to enhance the chip's power noise immunity
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 400ms WDT overflow rate 01: 200ms WDT overflow rate 10: 100ms WDT overflow rate 11: 50ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: F _{SYSCLK} /32; 01: F _{SYSCLK} /16; 10: F _{SYSCLK} /8; 11: F _{SYSCLK} /4
		1~0	TM3PSC	R/W	00	Timer3 Interrupt rate 00: Timer3 Interrupt rate is 32768 Slow clock cycle 01: Timer3 Interrupt rate is 16384 Slow clock cycle 10: Timer3 Interrupt rate is 8192 Slow clock cycle 11: Timer3 Interrupt rate is 128 Slow clock cycle
95h	INTFLG	7	LVD	R	–	Low Voltage Detect flag (2.3V) Set by H/W when a low voltage occurs. The flag is valid when LVR is 1.9V or disabled. This flag is disabled in Stop mode or MODE3V=PWRSAV=1.
		5	TKIF	R/W	0	Touch Key Interrupt Flag Set by H/W at the end of TK conversion if SYSCLK is fast enough. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag.
		4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	Port1 pin change Interrupt flag Set by H/W when a Port1 pin state change is detected and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer3 Interrupt Flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
96h	P1WKUP	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake-up/Interrupt enable control 0: Disable; 1: Enable.
98h	SCON	7	SM0	R/W	0	Serial port mode select bit 0, 1 (SM0, SM1) = 00: Mode0: 8 bit shift register, Baud Rate=F _{SYSCLK} /2 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate=F _{SYSCLK} /32 or /64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
99h	SBUF	7~0	SBUF	R/W	—	UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	PWM0PRD	7~0	PWM0PRD	R/W	FFh	PWM0 8-bit period register
9Bh	PWM0DH	7~0	PWM0DH	R/W	80h	bits 9~2 of the PWM0 10-bit duty register
9Ch	PWM1PRD	7~0	PWM1PRD	R/W	FFh	PWM1 8-bit period register
9Dh	PWM1DH	7~0	PWM1DH	R/W	80h	bits 9~2 of the PWM1 10-bit duty register
A0h	P2	7~2	P2.7~P2.2	R/W	3Fh	P2.7~P2.2 have no pin out, so these bits are used as general purpose register
		1~0	P2.1~P2.0	R/W	11	P2.1~P2.0 data
A1h	PWMCON	7~6	PWM1CKS	R/W	10	PWM1 clock source 00: F _{SYSCLK} /4 01: F _{SYSCLK} /2 10: F _{SYSCLK} 11: FRCx2
		5~4	PWM1DL	R/W	00	bits 1~0 of the PWM1 10-bit duty register
		3~2	PWM0CKS	R/W	10	PWM0 clock source 00: F _{SYSCLK} /4 01: F _{SYSCLK} /2 10: F _{SYSCLK} 11: FRCx2
		1~0	PWM0DL	R/W	00	bits 1~0 of the PWM0 10-bit duty register
A2h	P1MODL	7~6	P1MOD3	R/W	00	P1.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.3 is ADC or Touch Key input
		5~4	P1MOD2	R/W	00	P1.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.2 is ADC or Touch Key input
		3~2	P1MOD1	R/W	00	P1.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.1 is ADC or Touch Key input
		1~0	P1MOD0	R/W	00	P1.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.0 is ADC or Touch Key input
A3h	P1MODH	7~6	P1MOD7	R/W	00	P1.7 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.7 is Touch Key input
		5~4	P1MOD6	R/W	00	P1.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.6 is Touch Key input
		3~2	P1MOD5	R/W	00	P1.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.5 is ADC or Touch Key CLD
		1~0	P1MOD4	R/W	00	P1.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P1.4 is ADC or Touch Key input
A4h	P3MODL	7~6	P3MOD3	R/W	01	P3.3 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.3 is ADC or Touch Key input
		5~4	P3MOD2	R/W	01	P3.2 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.2 is ADC or Touch Key input
		3~2	P3MOD1	R/W	01	P3.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.1 is ADC or Touch Key input
		1~0	P3MOD0	R/W	01	P3.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.0 is ADC or Touch Key input

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
A5h	P3MODH	7	T0OE	R/W	0	Set 1 to enable "Timer0 overflow divided by 64" (T0O) output to P3.4 pin
		5~4	P3MOD6	R/W	00	P3.6 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.6 is Touch Key input
		3~2	P3MOD5	R/W	00	P3.5 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.5 is Touch Key input
		1~0	P3MOD4	R/W	00	P3.4 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: Mode3, P3.4 is Touch Key input
A6h	PINMOD	7	PWM1OE	R/W	0	PWM1 control 0: PWM1 disable 1: PWM1 enable and signal output to P1.3 pin
		6	PWM0OE	R/W	0	PWM0 control 0: PWM0 disable 1: PWM0 enable and signal output to P1.2 pin
		5	TCOE	R/W	0	Set 1 to enable "System clock divided by 2" (CKO) output to P1.4 pin
		4	T2OE	R/W	0	Set 1 to enable "Timer2 overflow divided by 2" (T2O) output to P1.0 pin
		3~2	P2MOD1	R/W	01	P2.1 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: not defined
		1~0	P2MOD0	R/W	01	P2.0 Pin Control 00: Mode0; 01: Mode1; 10: Mode2 11: not defined
A8h	IE	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		5	ET2	R/W	0	Set 1 to enable Timer2 interrupt
		4	ES	R/W	0	Set 1 to enable Serial Port (UART) Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Stop mode wake up capability
A9h	INTE1	3	ADTKIE	R/W	0	Set 1 to enable ADC/Touch Key Interrupt
		2	EX2	R/W	0	Set 1 to enable external INT2 pin Interrupt & Stop mode wake up capability
		1	PIIE	R/W	0	Set 1 to enable Port1 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
AAh	ADTKDT	7~4	ADCDL	R	–	ADC data bit 3~0
		3	TKEOC	R	–	Touch Key End of Conversion, 1=EOC
		2	TKOVF	R	–	Touch Key counter overflow, 1=overflow
		1~0	TKDH	R	–	Touch Key counter data bit 9~8
ABh	ADCDH	7~0	ADCDH	R	–	ADC data bit 11~4
ACh	TKDL	7~0	TKDL	R	–	Touch Key counter data bit 7~0
ADh	TKCON	7	TKPD	R/W	1	Touch Key Power Down 0: Touch Key enable; 1: Touch Key disable
		6	TKCKS	R/W	1	Touch Key counter clock select 0: FRC/4; 1: FRC/2
		5~4	TKPSC	R/W	00	Touch Key data pre-scale select 00: Touch Key data divided by 1 01: Touch Key data divided by 2 10: Touch Key data divided by 4 11: Touch Key data divided by 8
		2~0	TKTMR	R/W	100	Touch Key Conversion Time 000: Conversion time shortest ... 111: Conversion time longest

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
AEh	CHSEL	7~4	ADCHS	R/W	1111	ADC channel select 0000: AD0 (P3.3) 0001: AD1 (P3.2) 0010: AD2 (P3.1) 0011: AD3 (P3.0) 0100: AD4 (P1.0) 0101: AD5 (P1.1) 0110: AD6 (P1.2) 0111: AD7 (P1.3) 1000: AD8 (P1.4) 1001: AD9 (P1.5) 1010: V _{SS} 1011: V _{BG} (Internal Bandgap Reference Voltage) 11xx: Undefined
		3~0	TKCHS	R/W	1111	Touch Key channel select 0000: TK0 (P3.3) 0001: TK1 (P3.2) 0010: TK2 (P3.1) 0011: TK3 (P3.0) 0100: TK4 (P1.0) 0101: TK5 (P1.1) 0110: TK6 (P1.2) 0111: TK7 (P1.3) 1000: TK8 (P1.4) 1001: TK9 (P1.6) 1010: TK10 (P1.7) 1011: TK11 (P3.6) 1100: TK12 (P3.5) 1101: TK13 (P3.4) 111x: Undefined
B0h	P3	7	P3.7	R/W	1	P3.7 data, also controls the pin's I/O mode. If the P3.7 SFR data is "1", the P3.7 is assigned as Schmitt-trigger input mode; otherwise, it is assigned as open-drain output mode.
		6~0	P3.6~P3.0	R/W	7Fh	P3.6~P3.0 data
B8h	IP	5	PT2	R/W	0	Timer2 Interrupt Priority Low bit
		4	PS	R/W	0	Serial Port (UART) Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	IPH	5	PT2H	R/W	0	Timer2 Interrupt Priority High bit
		4	PSH	R/W	0	Serial Port (UART) Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	IP1	3	PADTKI	R/W	0	ADC/Touch Key Interrupt Priority Low bit
		2	PX2	R/W	0	External INT2 Pin Interrupt Priority Low bit
		1	PP1	R/W	0	Port1 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit
BBh	IP1H	3	PADTKIH	R/W	0	ADC/Touch Key Interrupt Priority High bit
		2	PX2H	R/W	0	External INT2 Pin Interrupt Priority High bit
		1	PP1H	R/W	0	Port1 Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
C8h	T2CON	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0
		2	TR2	R/W	0	Timer2 run control. 1:timer runs; 0:timer stops
		1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1. 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1. If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow.
CAh	RCP2L	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	RCP2H	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	TL2	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	TH2	7~0	TH2	R/W	00h	Timer2 data high byte
D0h	PSW	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag
D8h	CLKCON	7	SCKTYPE	R/W	0	Slow clock Type. This bit can be changed only in Fast mode (SELFCK=1). 0: SRC 1: SXT, P2.0 and P2.1 are crystal pins
		6	FCKTYPE	R/W	0	Fast clock type. This bit can be changed only in Slow mode (SELFCK=0). 0: FRC 1: FXT, P2.0 and P2.1 are crystal pins, oscillator gain is high for FXT
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock select. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
E0h	ACC	7~0	ACC	R/W	00h	Accumulator
F0h	B	7~0	B	R/W	00h	B register
F7h	CFGWL	7~6	WDTE	R/W	–	Watchdog Timer Reset control 0x: WDT disable 10: WDT enable in Fast/Slow mode, disable in Idle/Stop mode 11: WDT always enable
		4~0	FRCF	R/W	–	FRC frequency adjustment 00h: central frequency ... 0Fh: highest frequency ... 10h: lowest frequency
F8h	AUX1	7	CLRWDT	R/W	0	Set 1 to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set 1 to clear Timer3, HW auto clear it at next clock cycle.
		5	TKSOC	R/W	0	Touch Key Start of Conversion Set 1 to start Touch Key conversion. If SYSCLK is fast enough, this bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		4	ADSOC	R/W	0	ADC Start of Conversion Set 1 to start ADC conversion. Cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		0	DPSEL	R/W	0	Active DPTR Select

Adr	MTP	Bit#	Bit Name	Description
FFEh	CFGWL	4~0	FRCF	FRC frequency adjustment. FRC is trimmed to 7.3728 MHz in chip manufacturing. FRCF records the adjustment data.
FFFh	CFGWH	7	PROT	MTP Code Protect, 1=Protect
		6	XRSTE	External Pin Reset enable, 1=enable.
		5~4	LVRE	Low Voltage Reset function select 00: Set LVR at 2.9V; LVD disable 01: Set LVR at 2.3V; LVD disable 10: LVR disable; LVD enable if not in Stop mode and MODE3V*PWRSAV=0 11: Set LVR at 1.9V; LVD enable if not in Stop mode and MODE3V*PWRSAV=0
		3	MODE3V	3V mode selection control bit If this bit is set, the chip can be only operated in the condition of V _{CC} < 3.6V, and LDO is turned off to save current.
		2	PWRSAV	Set 1 to reduce the chip's power consumption.

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 1~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	Description	byte	cycle	opcode
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	2	25
ADD A,@Ri	Add indirect memory to A	1	2	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	2	35
ADDC A,@Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	2	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	Description	byte	cycle	opcode
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	2	55
ANL A,@Ri	AND indirect memory to A	1	2	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	2	52
ANL dir,#data	AND immediate to direct byte	3	4	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	2	45
ORL A,@Ri	OR indirect memory to A	1	2	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	2	42
ORL dir,#data	OR immediate to direct byte	3	4	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	2	65
XRL A,@Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	2	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4

LOGICAL				
Mnemonic	Description	byte	cycle	opcode
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	Description	byte	cycle	opcode
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	2	E5
MOV A,@Ri	Move indirect memory to A	1	2	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	4	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	4	88-8F
MOV dir,dir	Move direct byte to direct byte	3	4	85
MOV dir,@Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir,#data	Move immediate to direct byte	3	4	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	2	76-77
MOV DPTR,#data	Move immediate to data pointer	3	4	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4	93
MOVC A,@A+PC	Move code byte relative PC to A	1	4	83
MOVB A,@Ri	Move external data(A8) to A	1	4	E2-E3
MOVB A,@DPTR	Move external data(A16) to A	1	4	E0
MOVB @Ri,A	Move A to external data(A8)	1	4	F2-F3
MOVB @DPTR,A	Move A to external data(A16)	1	4	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	2	C5
XCH A,@Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	Description	byte	cycle	opcode
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C,bit	AND direct bit to carry	2	4	82
ANL C,/bit	AND direct bit inverse to carry	2	4	B0
ORL C,bit	OR direct bit to carry	2	4	72
ORL C,/bit	OR direct bit inverse to carry	2	4	A0
MOV C,bit	Move direct bit to carry	2	2	A2
MOV bit,C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	Description	byte	cycle	opcode
ACALL addr 11	Absolute jump to subroutine	2	4	11-F1
LCALL addr 16	Long jump to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	4	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	4	80
JC rel	Jump on carry = 1	2	4	40
JNC rel	Jump on carry = 0	2	4	50
JB bit,rel	Jump on direct bit = 1	3	4	20
JNB bit,rel	Jump on direct bit = 0	3	4	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4	73
JZ rel	Jump on accumulator = 0	2	4	60
JNZ rel	Jump on accumulator ... 0	2	4	70
CJNE A,dir,rel	Compare A,direct, jump not equal relative	3	4	B5
CJNE A,#data,rel	Compare A,immediate, jump not equal relative	3	4	B4
CJNE Rn,#data,rel	Compare register,immediate, jump not equal relative	3	4	B8-BF
CJNE @Ri,#data,rel	Compare indirect,immediate, jump not equal relative	3	4	B6-B7
DJNZ Rn,rel	Decrement register, jump not zero relative	2	4	D8-DF
DJNZ dir,rel	Decrement direct byte, jump not zero relative	3	4	D5

MISCELLANEOUS				
Mnemonic	Description	byte	cycle	opcode
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

Parameter	Rating	Unit
Supply voltage	$V_{SS}-0.3 \sim V_{SS}+5.5$	V
Input voltage	$V_{SS}-0.3 \sim V_{CC}+0.3$	
Output voltage	$V_{SS}-0.3 \sim V_{CC}+0.3$	
Output current high per 1 PIN	-25	mA
Output current high per all PIN	-80	
Output current low per 1 PIN	+30	
Output current low per all PIN	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	$-40 \sim +85$	$^{\circ}\text{C}$
Storage temperature	$-65 \sim +150$	

2. DC Characteristics ($T_A=25\text{ }^{\circ}\text{C}$, $V_{CC}=2.0\text{V} \sim 5.5\text{V}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage (Ignore LVR)	V_{CC}	FAST mode, 25°C , $F_{SYSCLK}=6\text{ MHz}$ (FXT)	2.8	—	5.5	V
		FAST mode, 25°C , $F_{SYSCLK}=3.7\text{ MHz}$ (FRC/2)	2.1	—	5.5	
		All mode, 25°C , $F_{SYSCLK} < 2\text{ MHz}$	1.8	—	5.5	
Input High Voltage	V_{IH}	All Input, except P3.7, P2.1	$V_{CC}=5\text{V}$	$0.6V_{CC}$	—	V
			$V_{CC}=3\text{V}$	$0.6V_{CC}$	—	V
		P3.7, P2.1	$V_{CC}=5\text{V}$	$0.8V_{CC}$	—	V
			$V_{CC}=3\text{V}$	$0.8V_{CC}$	—	V
Input Low Voltage	V_{IL}	All Input	$V_{CC}=5\text{V}$	—	$0.2V_{CC}$	V
			$V_{CC}=3\text{V}$	—	$0.2V_{CC}$	V
I/O Port Source Current	I_{OH}	All Output except P3.7	$V_{CC}=5\text{V}$, $V_{OH}=0.9V_{CC}$	4	8	mA
			$V_{CC}=3\text{V}$, $V_{OH}=0.9V_{CC}$	2	4	mA
I/O Port Sink Current	I_{OL}	All Output,	$V_{CC}=5\text{V}$, $V_{OL}=0.1V_{CC}$	8	16	mA
			$V_{CC}=3\text{V}$, $V_{OL}=0.1V_{CC}$	4	8	
Supply Current	I_{DD}	FAST mode $V_{CC}=5\text{V}$ MODE3V=0	FXT=4 MHz	—	1.8	mA
			FRC=7.3728 MHz	—	2.3	
		FAST mode $V_{CC}=3\text{V}$ MODE3V=1	FXT=4 MHz	—	1.1	
			FRC=7.3728 MHz	—	2	
		SLOW mode $V_{CC}=5\text{V}$ MODE3V=0	SXT=32 KHz	—	185	μA
			SRC, CLKPSC=11	—	188	
		SLOW mode $V_{CC}=3\text{V}$ MODE3V=1 PWRSAV=1	SXT=32 KHz	—	11	
			SRC, CLKPSC=11	—	21	
		SLOW mode $V_{CC}=3\text{V}$ MODE3V=1 PWRSAV=0	SXT=32 KHz	—	46	
			SRC, CLKPSC=11	—	57	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply Current	I_{DD}	IDLE mode, $V_{CC}=5V$, $MODE3V=0$	SXT=32 KHz	–	178	–	μA
			SRC, CLKPSC=11	–	173	–	
		IDLE mode, $V_{CC}=3V$, $MODE3V=1$ $PWRSV=1$	SXT=32 KHz	–	4	–	
			SRC, CLKPSC=11	–	5.2	–	
		IDLE mode, $V_{CC}=3V$, $MODE3V=1$ $PWRSV=0$	SXT=32 KHz	–	40	–	
			SRC, CLKPSC=11	–	41	–	
		STOP mode $V_{CC}=5V$ $MODE3V=0$	$PWRSV=1$	–	0.1	–	
			$PWRSV=0$ LVR disable	–	137	–	
			$PWRSV=0$ LVR enable	–	168	–	
		STOP mode, $V_{CC}=3V$ $MODE3V=1$	$PWRSV=1$	–	–	0.1	
System Clock Frequency	F_{SYSCLK}	$V_{CC} > LVR_{TH}$	$V_{CC}=2.9V$	–	–	6	MHz
			$V_{CC}=2.3V$	–	–	4	
			$V_{CC}=1.9V$	–	–	3	
LVR Reference Voltage	V_{LVR}	$T_A=25^{\circ}C$		–	2.9	–	V
				–	2.3	–	V
				–	1.9	–	V
LVR Hysteresis Voltage	V_{HYST}	$T_A=25^{\circ}C$		–	± 0.1	–	V
LVD Reference Voltage	V_{LVD}	$T_A=25^{\circ}C$		–	2.3	–	V
Low Voltage Detection time	t_{LVR}	$T_A=25^{\circ}C$		100	–	–	μs
Pull-Up Resistor	R_P	$V_{IN}=0V$, all except P3.7	$V_{CC}=5V$	–	120	–	$K\Omega$
			$V_{CC}=3V$		240		
		$V_{IN}=0V$, P3.7	$V_{CC}=5V$	–	180	–	$K\Omega$
			$V_{CC}=3V$		180		

3. Clock Timing ($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$)

Parameter	Condition	Min	Typ	Max	Unit
FRC Frequency	25°C, $V_{CC}=5.0\text{V}$	-1.6%	7.3728	+1.6%	MHz
	0°C ~ 85°C, $V_{CC}=3.0 \sim 5.5\text{V}$	-4.0%	7.3728	+3.0%	
	-40°C ~ 85°C, $V_{CC}=3.0 \sim 5.5\text{V}$	-8.0%	7.3728	+3.0%	

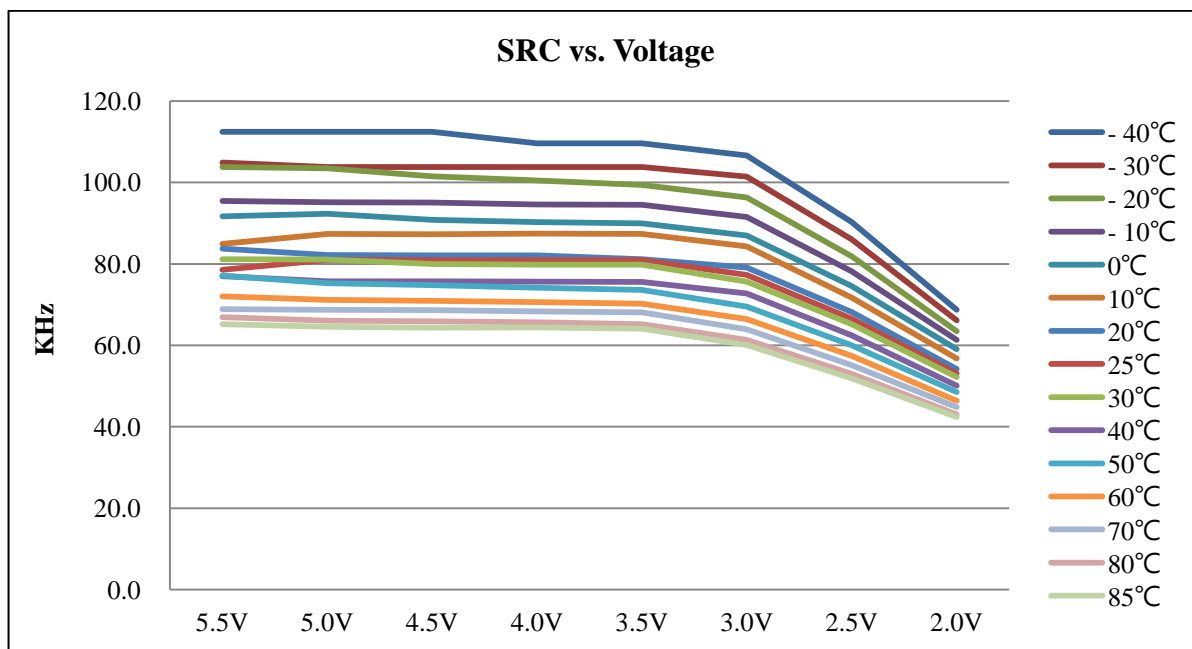
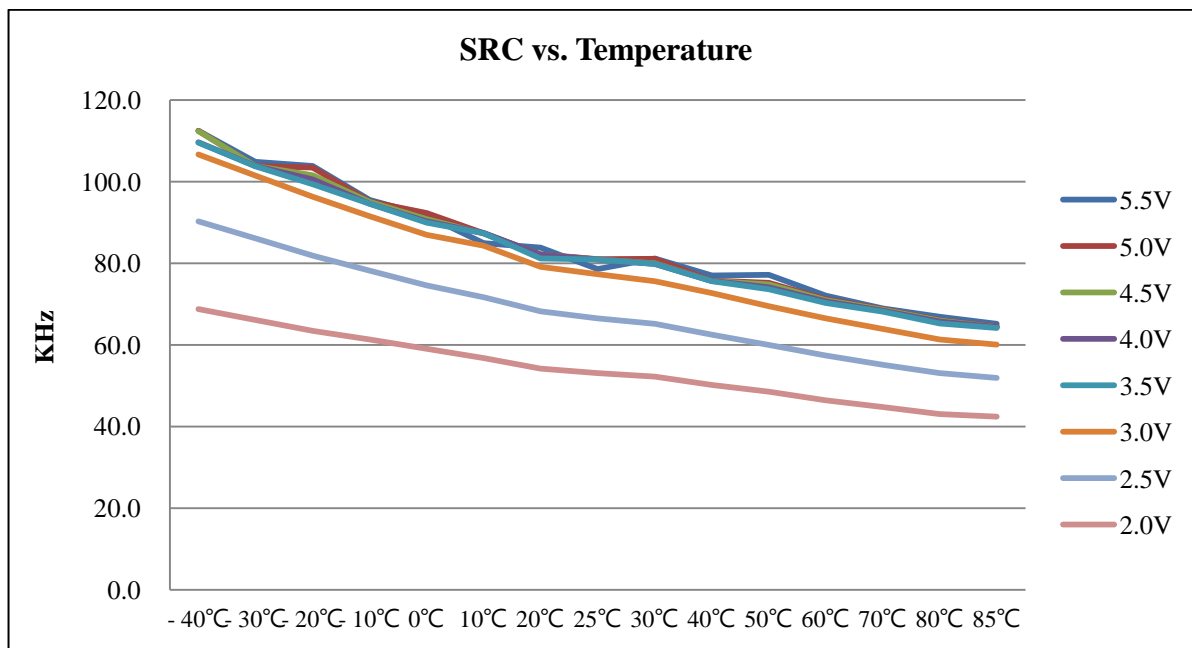
4. Reset Timing Characteristics ($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$)

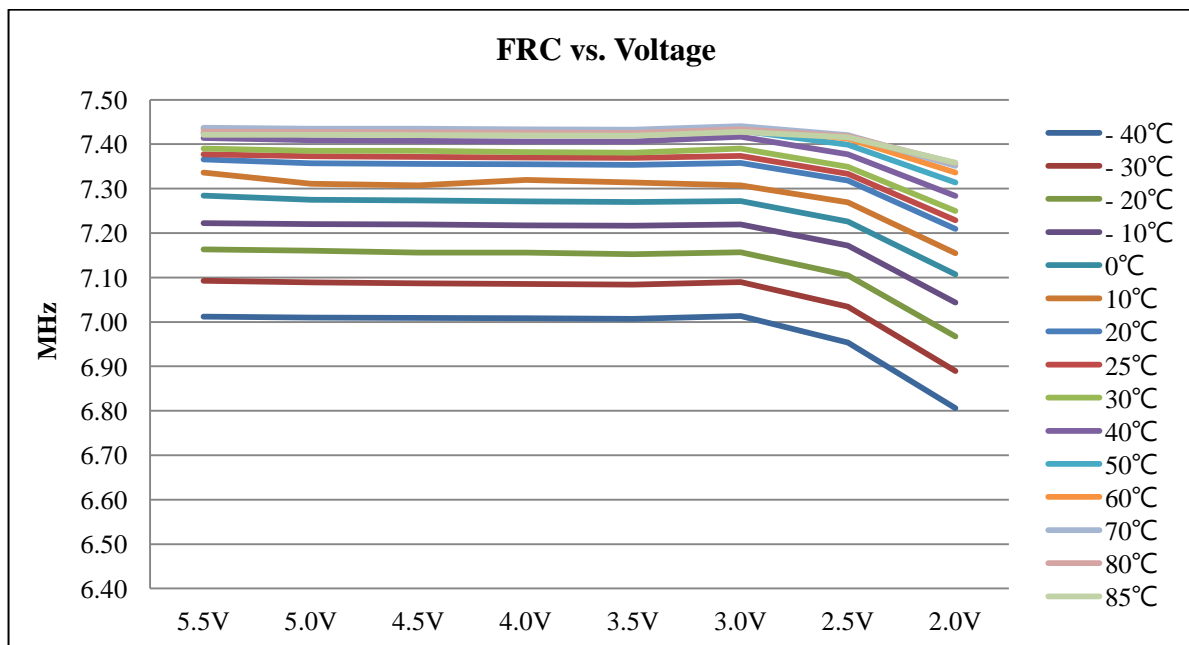
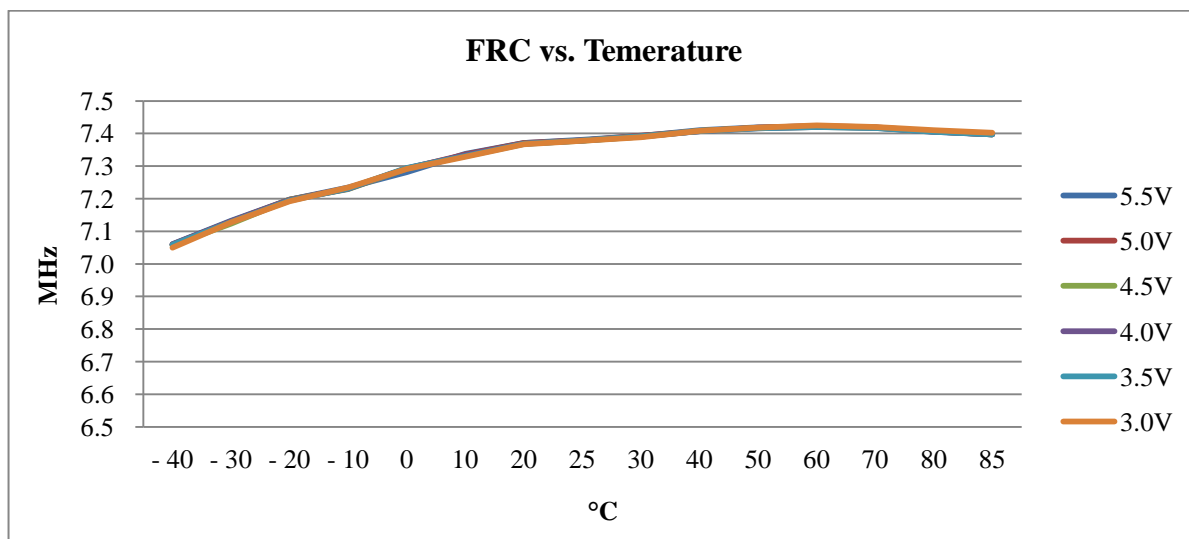
Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input $V_{CC}=5\text{V} \pm 10\%$	30	—	—	μs
WDT wakeup time	$V_{CC}=5\text{V}$, WDTPSC=11	—	52	—	ms
	$V_{CC}=3\text{V}$, WDTPSC=11	—	52	—	

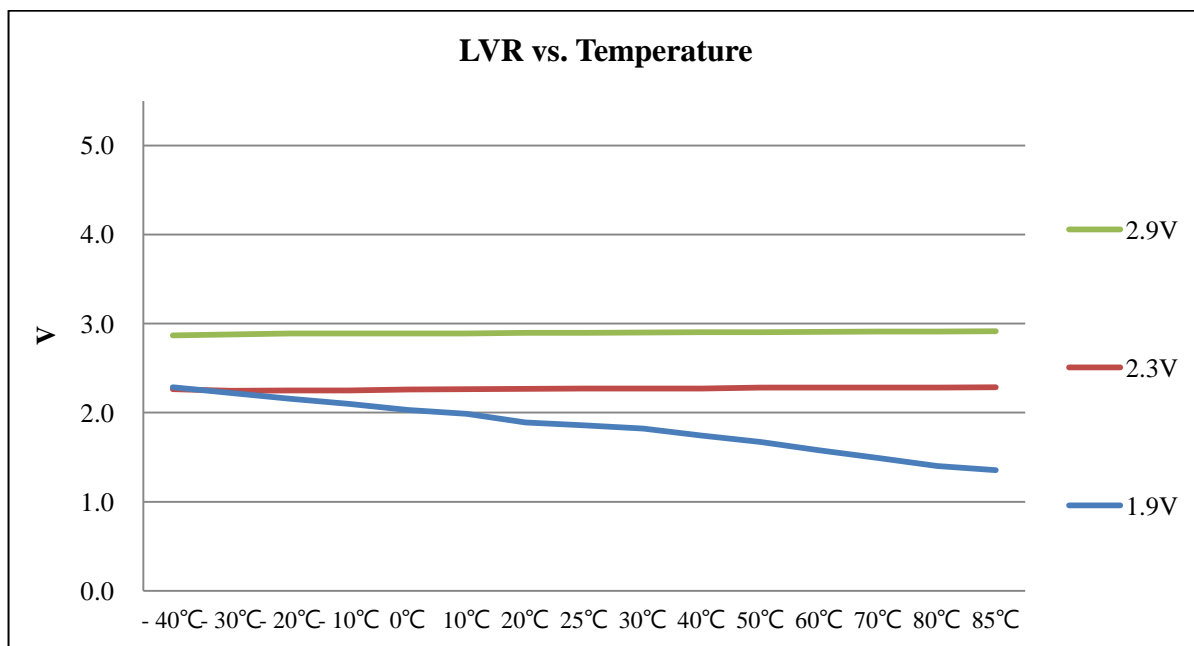
5. ADC Electrical Characteristics ($T_A = 25^{\circ}\text{C}$, $V_{CC} = 3.0\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

Parameter	Conditions	Min	Typ	Max	Unit
Total Accuracy	$V_{CC}=5.12\text{V}$, $V_{SS}=0\text{V}$	—	± 2.5	± 4	LSB
Integral Non-Linearity		—	± 3.2	± 5	
Max Input Clock (f_{ADC})	—	—	—	1	MHz
Conversion Time	$F_{\text{ADC}} = 1\text{MHz}$	—	50	—	μs
BandGap Voltage Reference	$V_{CC} = 5\text{V}$	-8%	1.2	+8%	V
Input Voltage	—	V_{SS}	—	V_{CC}	V

6. Characteristic Graphs







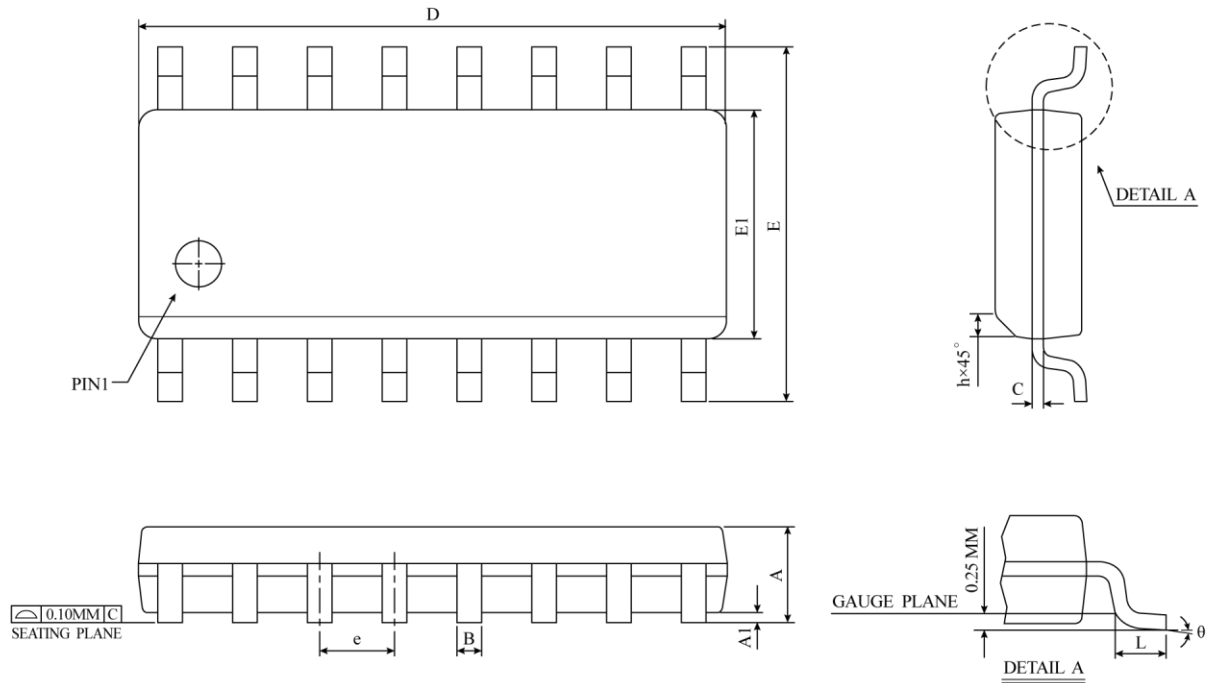
Package and Dice Information

Ordering information

Ordering number	Package
TM52M5254-MTP	Wafer/Dice blank chip
TM52M5254-COD	Wafer/Dice with code
TM52M5254-MTP-16	SOP 16-pin (150 mil)
TM52M5254-MTP-03	DIP 16-pin (300 mil)
TM52M5254-MTP-21	SOP 20-pin (300 mil)
TM52M5254-MTP-05	DIP 20-pin (300 mil)
TM52M5254-MTP-31	SSOP 20-pin (209 mil)
TM52M5254BQ-MTP-97	QFN 20-pin (4x4x0.75-0.5 mm)
TM52M5258-MTP	Wafer/Dice blank chip
TM52M5258-COD	Wafer/Dice with code
TM52M5258-MTP-16	SOP 16-pin (150 mil)
TM52M5258-MTP-03	DIP 16-pin (300 mil)
TM52M5258-MTP-21	SOP 20-pin (300 mil)
TM52M5258-MTP-05	DIP 20-pin (300 mil)
TM52M5258-MTP-31	SSOP 20-pin (209 mil)
TM52M5258BQ-MTP-97	QFN 20-pin (4x4x0.75-0.5 mm)

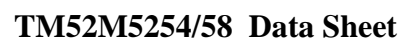
Package Information

SOP-16 (150mil) Package Dimension



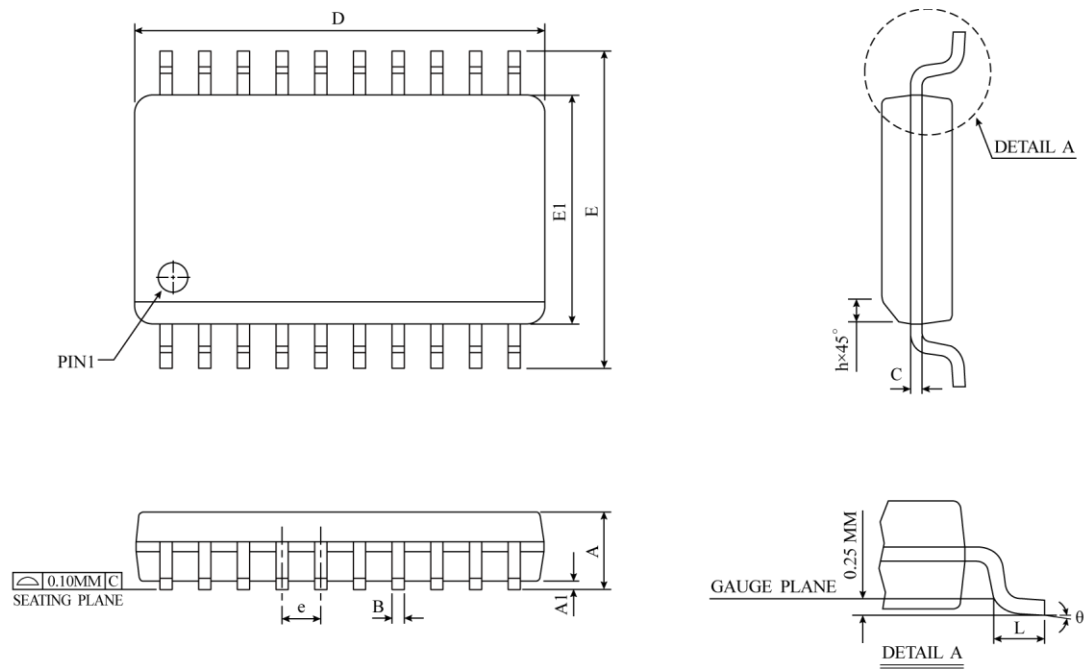
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

△ * NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.



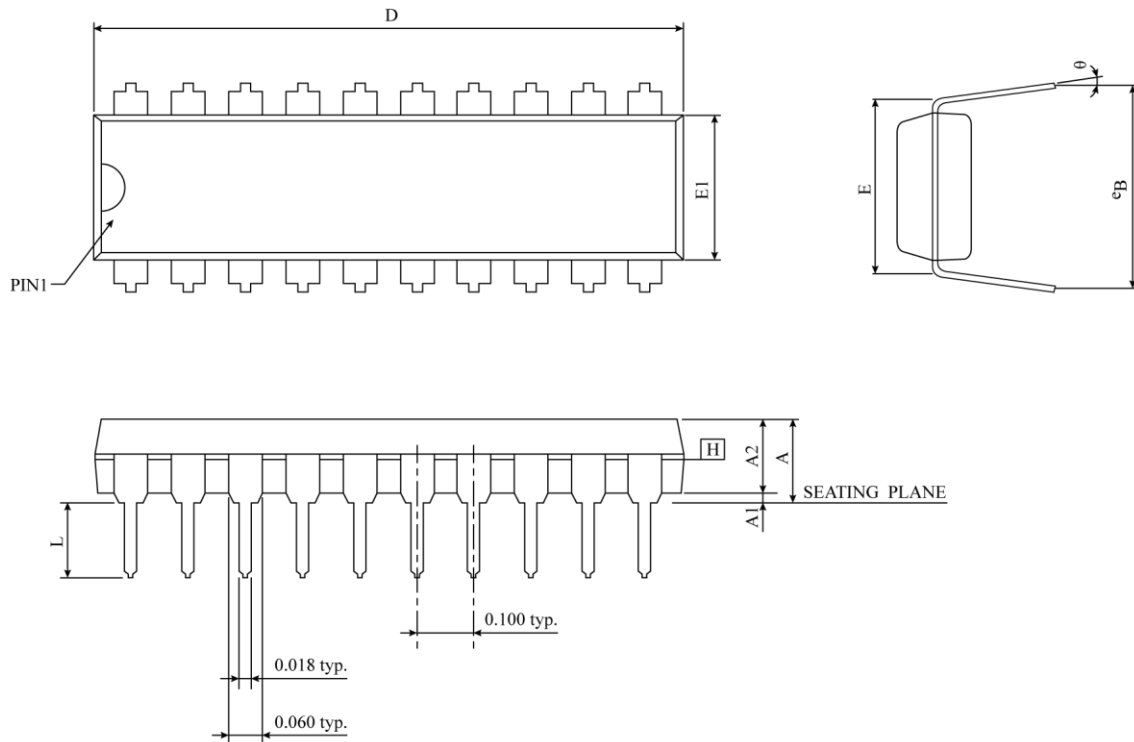
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.369	-	-	0.172
A1	0.381	0.673	0.965	0.015	0.027	0.038
A2	3.175	3.302	3.429	0.125	0.130	0.135
D	18.669	19.177	19.685	0.735	0.755	0.775
E	7.620 BSC			0.300 BSC		
E1	6.223	6.350	6.477	0.245	0.250	0.255
L	2.921	3.366	3.810	0.115	0.133	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ	0°	7.5°	15°	0°	7.5°	15°
JEDEC	MS-001 (BB)					

1. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
2. CB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
3. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
4. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
5. DATUM PLANE III COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

SOP-20 (300mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	12.60	12.80	13.00	0.4961	0.5040	0.5118
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AC)					

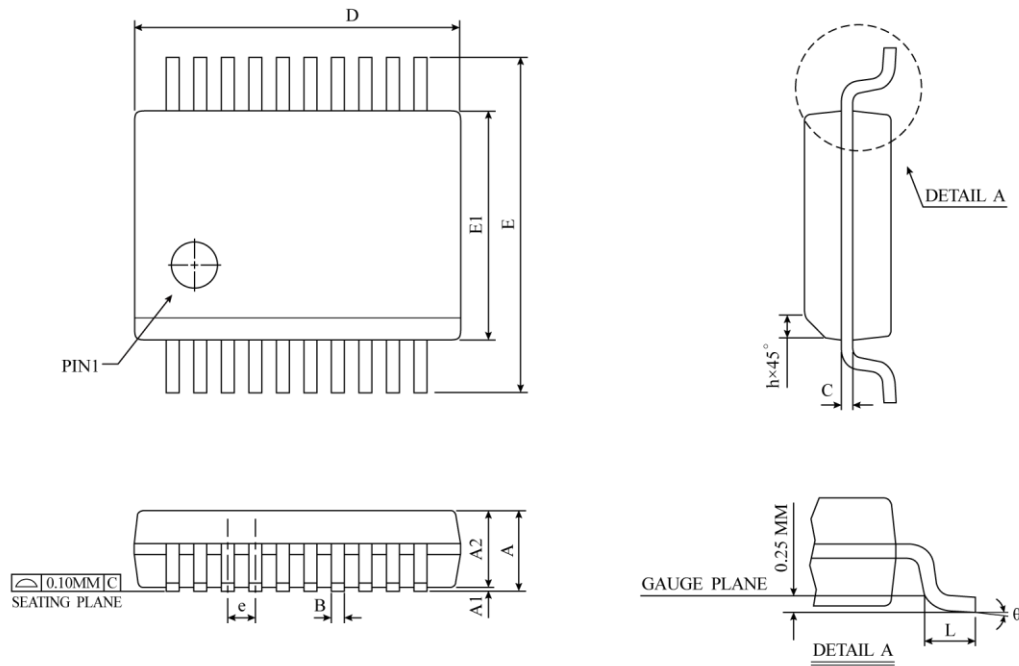
△ *NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

DIP-20 (300mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.445	-	-	0.175
A1	0.381	-	-	0.015	-	-
A2	3.175	3.302	3.429	0.125	0.130	0.135
D	25.705	26.061	26.416	1.012	1.026	1.040
E	7.620	7.747	7.874	0.300	0.305	0.310
E1	6.223	6.350	6.477	0.245	0.250	0.255
L	3.048	3.302	3.556	0.120	0.130	0.140
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ	0°	7.5°	15°	0°	7.5°	15°
JEDEC	MS-001 (AD)					

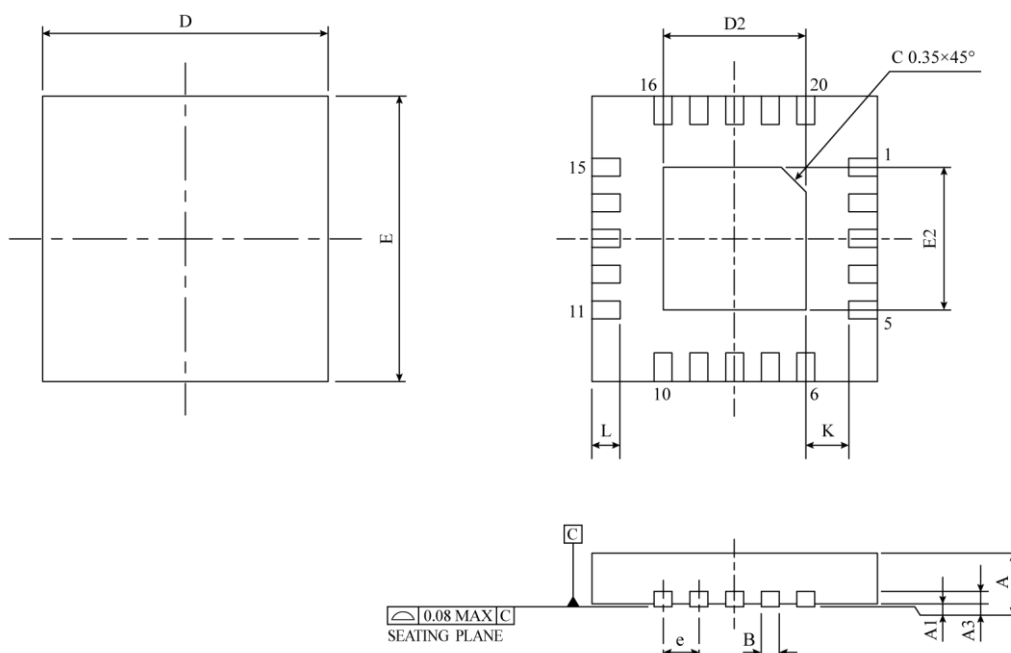
NOTES :

1. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
2. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
3. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
4. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
5. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

SSOP-20 (209mil) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	2.0	-	-	0.079
A1	0.05	-	-	0.002	-	-
A2	1.65	1.75	1.85	0.065	0.069	0.073
B	0.22	0.28	0.33	0.009	0.011	0.013
C	0.09	0.15	0.21	0.004	0.006	0.008
D	6.90	7.20	7.50	0.272	0.284	0.295
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BSC			0.026 BSC		
L	0.55	0.75	0.95	0.022	0.030	0.038
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-150 (AE)					

△ * NOTES : DIMENSION " D " DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS,
BUT DO INCLUDE MOLD MISMATCH MOLD FLASH OR PROTRUSION SHALL NOT EXCEED
0.20 MM (0.008 INCH) PER SIDE.

QFN 20 (4*4*0.75-0.5mm) Package Dimension


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.03	0.05	0.000	0.001	0.002
A3	0.20 REF.			0.008 REF.		
B	0.20	0.25	0.30	0.008	0.001	0.012
D	4.00 BSC			0.157 BSC		
E	4.00 BSC			0.157 BSC		
e	0.50 BSC			0.020 BSC		
K	0.20	-	-	0.008	-	-
E2	2.40	2.48	2.55	0.094	0.097	0.100
D2	2.40	2.48	2.55	0.094	0.097	0.100
L	0.35	0.45	0.55	0.014	0.018	0.022
JEDEC	W(V) GGD-11					

△ * NOTES : DIMENSION B APPLIES TO METALLIZED TERMINAL AND IS MEASURED
 BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS
 THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
 BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK
 SLUG AS WELL AS THE TERMINALS.